TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Integrated Master's in Aerospace Engineering, Técnico, University of Lisbon

Laboratory 3 Report

Francisco Alves 95787, Tomás Nunes 95855, Rodrigo Sequeira 96480

May 8th, 2021

Contents

1 Introduction

The objective of this laboratory assignment is to design an AC/DC converter circuit using an Envelope Detector circuit, a Voltage Regulator circuit and components such as resistors, capacitors and diodes. A representation of the circuit can be seen in Figure 1. The main goal of this project is to balance the cost of the circuit and its effectiveness given the characteristics required ($V_{out} = 12V$ with DC signal). This is given by the Merit Figure.

Since we know the value of V_1 and we are considering the ideal model for a transformer, we can replace the transformer used by a dependent current source (on the left) and a dependent voltage source (on the right), as seen in Figure 1. The value of the variable n is 1.0(45); we

used this value because we verified that it gave us the best voltage ripple value for this circuit. The equations for these dependent sources are, respectively:

$$i_1 = \frac{1}{n} i_2 \tag{1}$$

$$v_2 = \frac{1}{n} v_1 \tag{2}$$

By trial and error, we concluded that the best design for the circuit in order to have the best quality/cost ratio was:

using a Full-Wave Rectifier, a 560μF capacitor and a 600kΩ resistor for the Envelope Detector;

using a 512.99kΩ resistor and 19 diodes for the Voltage Regulator.

In Section 2, a theoretical analysis of the circuit using Octave is presented. In Section 3, the circuit is analysed by simulation with Ngspice software and the results are compared to the theoretical results in Section 5. Conclusions of this study can be found in Section 4.

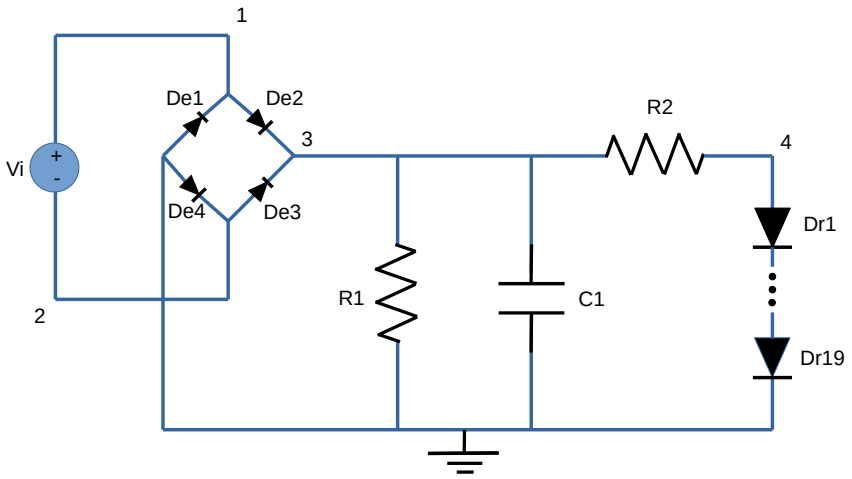


Figure 1: Circuit in study.

2 Theoretical Analysis

We used the ideal diode model for the theoretical predictions, with a voltage $V_{on} = 0.6316V$. The reference values for I_S, η and V_T were taken from Ngspice's data from the Default Diode Model used by us.

2.1 Envelope Detector Output Prediction

The theoretical calculations for the Envelope Detector circuit were based on the following model, considering that the beggining of each period is when v_S (the Envelope Detector's input voltage) is at its maximum.

While $t < t_{off}$,

$$v_O = v_S \tag{3}$$

t_{off} is given as

$$\frac{1}{\omega} arctan(\frac{1}{\omega RC}) + t_0 \tag{4}$$

At $t > t_{off}$,

$$v_O = Acos(\omega t_{off}) e^{-\frac{t - t_{off}}{RC}} \tag{5}$$

Until $t = t_{on}$, which is given by,

$$Acos(\omega t_{on}) = Acos(\omega t_{off}) e^{-\frac{t_{on} - t_{off}}{RC}} \tag{6}$$

and t_{off} becomes,

$$t_{off} = t_{off} + T/2 \tag{7}$$

And the cycle repeats.

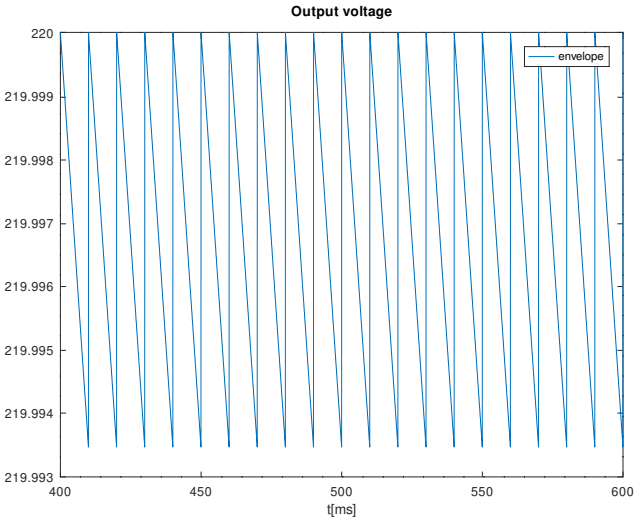


Figure 2: vO Envelope Detector

Name	Value [V]
V_I	220.000
V_{max}	220.000
V_{min}	219.993
V_{ripple}	6.531405e-03
V_{avg}	219.997

Table 1: Envelope Detector

2.2 Voltage Regulator Output Prediction

The theoretical calculations for the Voltage Regulator circuit were based on an incremental model defined by the following equations.

$$v_S = V_S + v_s, v_O = V_O + v_o, V_O = nV_{on}, V_S > nV_{on} \tag{8}$$

$$v_o = \frac{nr_d}{nr_d + R} v_s \tag{9}$$

The incremental diode resistance is given by

$$\frac{\eta V_T}{I_S e^{\frac{V_D}{\eta V_T}}} \tag{10}$$

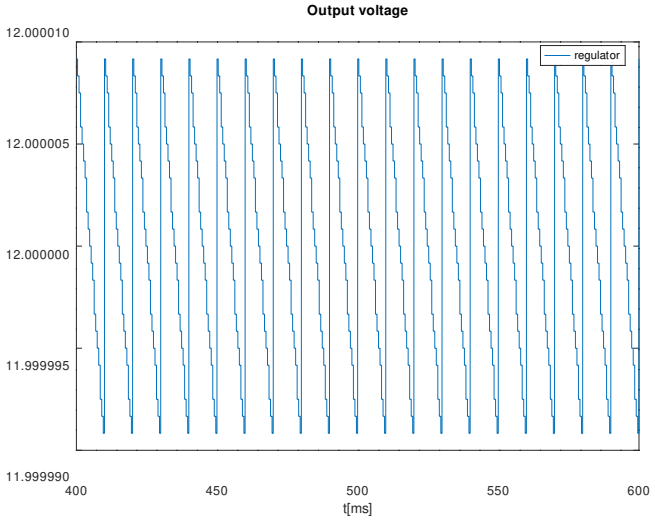


Figure 3: vO Voltage Regulator

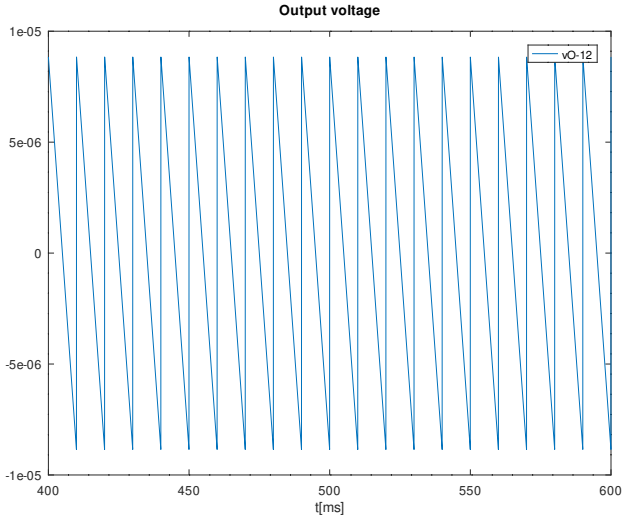


Figure 4: vO Voltage Regulator - 12

Name	Value [V]
V_{max}	12.00001
V_{min}	11.99999
V_{ripple}	1.769225e-05
V_{avg}	12.00000
V_{avg}-12	0.00000

Table 2: Voltage Regulator

3 Simulation Analysis

In this section we present the results obtained for a 10 period simulation of the circuit.

3.1 Envelope Detector Output

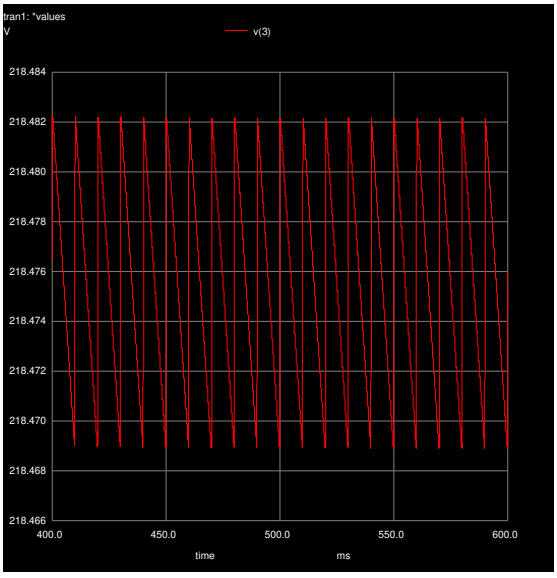


Figure 5: vO Envelope Detector

Name	Value [V]
vi	2.200000e+02
voenvmax	2.184823e+02
voenvmin	2.184689e+02
vrippleenv	1.340000e-02
voenvavg	2.184756e+02

Table 3: Envelope Detector

3.2 Voltage Regulator Output

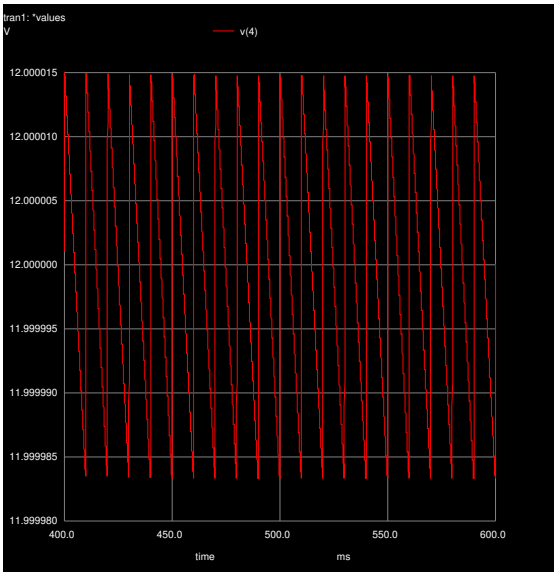


Figure 6: vO Voltage Regulator

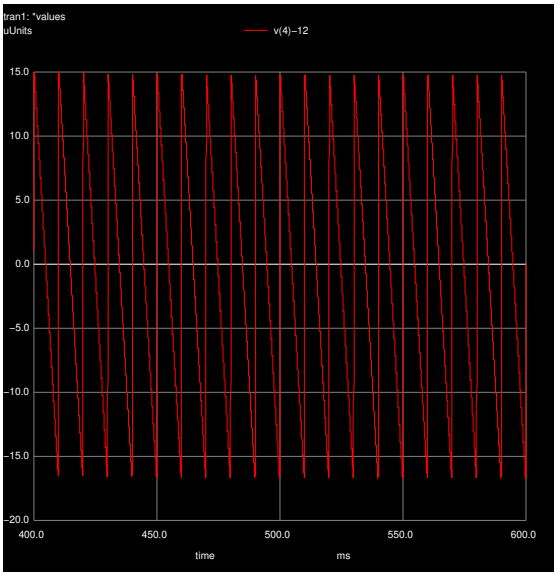


Figure 7: vO Voltage Regulator - 12

Name	**Value [V]**
vomax	1.200001e+01
vomin	1.199998e+01
vripplereg	3.000000e-05
voavg	1.200000e+01
voavg-12	0.000000e+00

Table 4: Voltage Regulator

3.3 Cost and Merit

Name	Value [V]
cost	1.675290e+03
merit	1.925521e+01

Table 5: Cost and Merit

4 Conclusion

We analysed the simulation values, since they are more accurate than the theoretical analysis. However, the theoretical analysis was useful to guide us on what values to use in Ngspice. In spite of the relatively high cost, we achieved a voltage ripple of $3 * 10^{-5}V$ and an output voltage of 12V, which gave us a Merit Figure of 19.26. This value shows that the goal of the lab assignment was achieved successfully. All in all, this lab assignment showed us the challenges of a real project, because we were introduced to the concept of keeping a budget in mind while working on a solution to a problem. Once again, the outputs given by the predictions and the simulations differed considerably, and that can be seen as a consequence of the non-linear behavior of some of the components used (diodes). Also, the theoretical model used was the ideal one, which has some approximations in spite of giving consistent results.

5 Side-by-side

5.1 Envelope detector

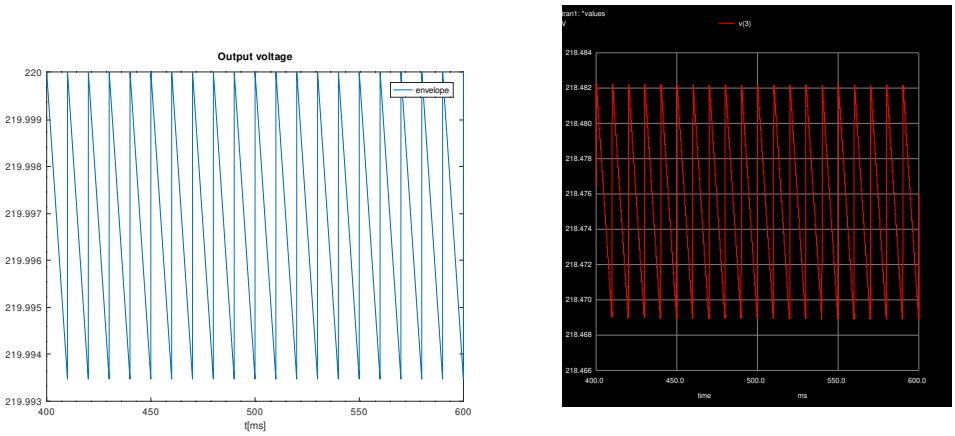


Figure 8: Envelope detector

5.2 Voltage Regulator Output

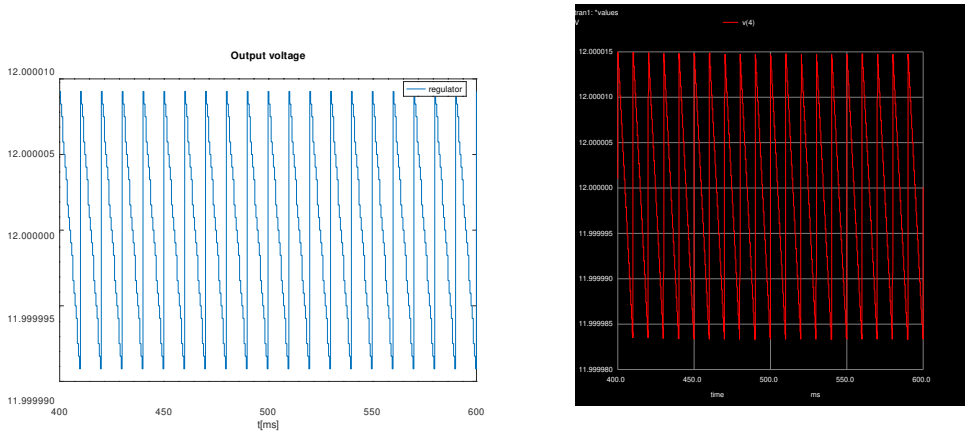
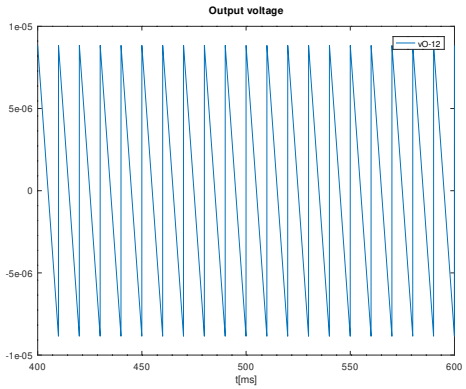


Figure 9: Output voltage/Voltage Regulator Output

5.3 vO Voltage Regulator - 12



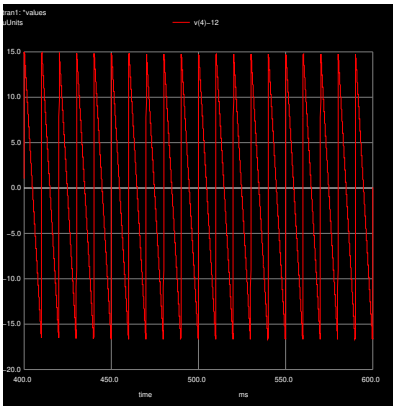


Figure 10: vO Voltage Regulator - 12