TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Integrated Master's in Aerospace Engineering, Técnico, University of Lisbon

Laboratory 4 Report

Francisco Alves 95787, Tomás Nunes 95855, Rodrigo Sequeira 96480

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1 Introduction

In this laboratory assignment, we are asked to create an Audio Amplififer Circuit, in which we are supposed to design the architecture of the Gain and Output stages of the circuit. The goal is to achieve the best ratio between the cost of the circuit and its quality in terms of the specifications asked (Merit Figure): the gain's frequency response and the input and output impedances.

To build the circuit, we used 7 resistors, 3 capacitors and 2 transistors (one PNP type and one NPN type). A representative image of the circuit can be seen in 1.

As stated, the circuit has 2 different stages (gain and output), where the first one amplifies the input signal and the last one increases the output current. The gain stage is characterized by a high gain but the output impedance is also high, whereas the output stage has a near 1 gain with a low output impedance.

In Section 2, a theoretical analysis of the circuit using Octave is presented. In Section 3, the circuit is analysed by simulation with Ngspice software and the results are compared to the theoretical results in Section 4. Conclusions of this study can be found in Section 5.

The components used have the following values:

Table 1: Values in SI units.

R_{in}	100
R_1	100000
R_2	20000
R_c	500
R_e	100
R_{out}	100
C_i	0.001000
C_b	0.005000
C_o	0.001995

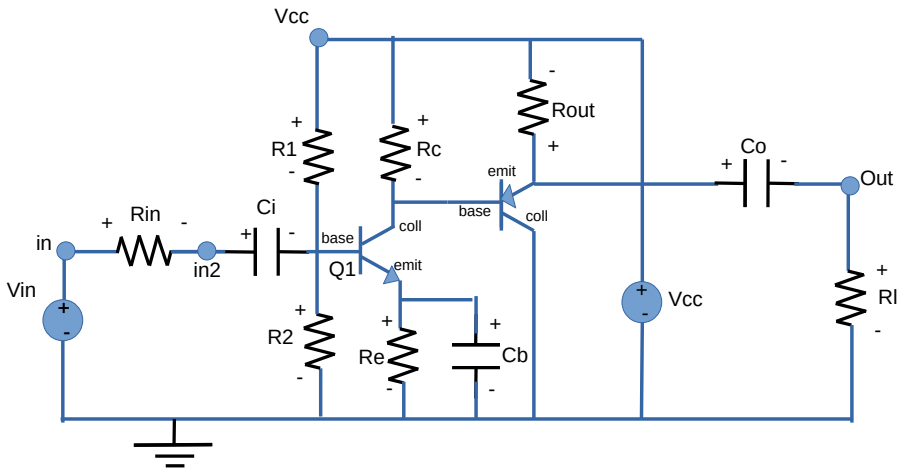

Figure 1: Circuit in study.

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically.

For the gain stage, we assigned the values $R_S = 100\Omega$, $V_T = 25 \times 10^3 V$, $\beta_{FN} = 178.7$, $V_{AFN} = 69.7V$, $R_{E1} = 100\Omega$, $R_{C1} = 500\Omega$, $R_{B1} = 100000\Omega$, $R_{B2} = 20000\Omega$, $V_{BEON} = 0.7V$, $V_{CC} = 12V$ and defined R_{SB} as

$$R_{SB} = \frac{R_B \times R_S}{R_B + R_S}$$

g_{m1} as

$$g_{m1} = I_{C1}/V_T$$

$r_{\pi 1}$ as

$$r_{\pi 1} = \frac{\beta_{FN}}{g_{m1}}$$

and r_{o1} as

$$r_{o1} = \frac{V_{AFN}}{I_{C1}}$$

For the output stage, we assigned the values $\beta_{FP} = 227.3$, $V_{AFP} = 37.2V$, $R_{E2} = 100\Omega$, $V_{EBON} = 0.7V$, $V_{I2} = V_{O1}$, $I_{E2} = \frac{V_{CC} - V_{EBON} - V_{I2}}{R_{E2}}$, $I_{C2} = \frac{\beta_{FP}}{(\beta_{FP}+1)I_{E2}}$, $V_{O2} = V_{CC} - R_{E2} \times I_{E2}$ and defined g_{m2} as

$$g_{m2} = \frac{I_{C2}}{V_T}$$

g_{o2} as

$$g_{o2} = \frac{I_{C2}}{V_A FP}$$

$g_{\pi 2}$ as

$$g_{\pi 2} = \frac{g_{m2}}{\beta_{FP}}$$

and g_{e2} as

$$g_{e2} = \frac{1}{R_{E2}}$$

2.1 Operating point

In this analysis, the circuit used is the one presented in Figure 1. The operating points were computed for both the gain and output stages to verify that the transistors had the acceptable voltages to be functioning.

The NPN transistor used in the gain stage had to obey $V_{CE} > V_{BEON} = 0.7V$.

The PNP transistor used in the output stage had to obey $V_{EC} = V_{O2} > V_{EBON} = 0.7V$.

In the following table, we present the operating point values.

Gain stage: Firstly, we have

$$R_B = \frac{1}{\frac{1}{R_{B1}} + \frac{1}{R_{B2}}}$$

$$V_{EQ} = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC}$$

$$I_{B1} = \frac{V_{EQ} - V_{BEON}}{R_B + (1 + \beta_{FN}) * R_{E1}}$$

$$I_{C1} = \beta_{FN} \times I_{B1}$$

$$I_{E1} = (1 + \beta_{FN}) I_{B1}$$

$$V_{E1} = R_{E1} \times I_{E1}$$

$$V_{O1} = V_{CC} - R_{C1} \times I_{C1}$$

$$V_{CE} = V_{O1} - V_{E1}$$

Output stage:

$$V_{I2} = V_{O1}$$

$$I_{E2} = \frac{V_{CC} - V_{EBON} - V_{I2}}{R_{E2}}$$

$$I_{C2} = \frac{\beta_{FP}}{\beta_{FP} + 1} \times I_{E2}$$

$$V_{O2} = V_{CC} - R_{E2} \times I_{E2}$$

Name	Value [V]
V_{CE}	7.972014
V_{BE}	0.7000000
V_{O1}	8.646473
V_{EC}	9.346473
V_{EB}	0.7000000
V_{O2}	9.346473

Table 2: Operating point

Note that both transistors are working in the Forward Active Region.

2.2 Gain, input and output impedances

To obtain the following values we need to analyse the incremental circuit version of the original circuit.

Gain stage: We can write the following equations: -To compute the gain stage's gain,

$$R_{E1} = 0, AV_1 = \frac{R_{SB}}{R_S} \times \frac{R_{C1}(R_{E1} - g_{m1} \times r_{\pi 1} \times r_{o1})}{(r_{o1} + R_{C1} + R_{E1}) \times (R_{SB} + r_{\pi 1} + R_{E1}) + g_{m1} * R_{E1} * r_{o1} * r_{\pi 1} - R_{E1}^2)} \quad (1)$$

-To compute the gain stage's input impedance

$$R_{E1} = 0, Z_{I1} = \frac{1}{\frac{1}{R_B} + \frac{1}{\frac{(r_{o1}+R_{C1}+R_{E1}) \times (r_{\pi 1}+R_{E1}) + g_{m1} \times R_{E1} \times r_{o1} \times r_{\pi 1} - R_{E1}^2}{r_{o1}+R_{C1}+R_{E1}}}} \quad (2)$$

-To compute the gain stage's output impedance

$$Z_{O1} = \frac{1}{\frac{1}{r_{o1}} + \frac{1}{R_{C1}}} \quad (3)$$

Output stage:
We can write the following equations:
-To compute the output stage's gain,

$$AV_2 = \frac{g_{m2}}{g_{m2} + g_{\pi 2} + g_{o2} + g_{e2}} \quad (4)$$

-To compute the output stage's input impedance,

$$Z_{I2} = \frac{g_{m2} + g_{\pi 2} + g_{o2} + g_{e2}}{g_{\pi 2}(g_{\pi 2} + g_{o2} + g_{e2})} \tag{5}$$

-To compute the output stage's output impedance,

$$Z_{O2} = \frac{1}{g_{m2} + g_{\pi 2} + g_{o2} + g_{e2}} \tag{6}$$

The following table presents the values for the gain, input impedance and output impedance of both stages.

Name	**Value [Ω]**
Z_{I1}	640.4922
Z_{O1}	477.0475
AV_1	110.6998
Z_{I2}	15013.86
Z_{O2}	0.9327305
AV_2	0.9856738

Table 3: Gain, input impedance and output impedance

Total:

In order to make a comparison with the simulation's gain, and input and output impedances, we computed the theoretical values for these variables.

$$g_B = \frac{1}{\frac{1}{g_{\pi 2}} + Z_{O1}} \tag{7}$$

$$AV = AV_1 \frac{\frac{g_B + g_{m2}}{g_{\pi 2} \times g_B}}{g_B + g_{e2} + g_{o2} + \frac{g_{m2}}{g_{\pi 2}} \times g_B} \tag{8}$$

$$Z_I = Z_{I1} \tag{9}$$

$$Z_O = \frac{1}{g_{o2} + \frac{g_{m2}}{g_{\pi}2} \times g_B + g_{e2} + g_B} \tag{10}$$

Name	**Value [Ω]**
Z_I	640.4922
Z_O	2.936362
AV	107.21838

Table 4: Gain, input impedance and output impedance

2.3 Frequency response

In order to obtain the Merit Figure of our circuit, we tried to compute the theoretical value of the bandwidth. However, we were only able to obtain the value of the lower cut off frequency as seen in 2, so we used Ngspice's value for the upper cut off frequency. This is due to the fact that for this frequency we need to take parasite capacitors into account which would lead to complex calculations.

Name	Value [Hz]
uco	3106930.0
lco	11.75169
$bandwith$	3106918.25

Table 5: Bandwidth

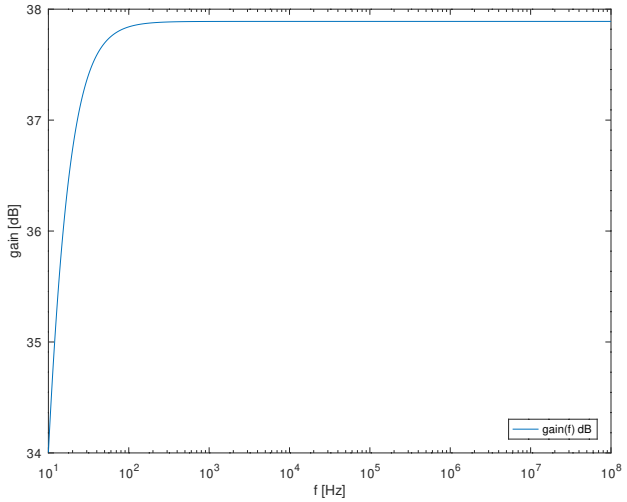

Figure 2: Output voltage gain in order to frequency

Here we present the merit figure of our circuit.

Name	Value [Mu]
$cost$	8116.008
$merit$	3492.661

Table 6: Merit figure

3 Simulation Analysis

3.1 Operating Point Analysis

Once again, the simulated operating points were computed to check if the transistors were working in the correct regions.

Table shows the simulated operating point results for the circuit under analysis.

Name	Value [V]
vce	7.969251e+00
vbe	6.986238e-01
vo1	8.654746e+00
vec	9.397377e+00
veb	7.426318e-01
vo2	9.397377e+00

Table 7: Operating point

Here the transistors are working in the Forward Active Region. The values are compared with the theoretical predictions in Section 4.

3.2 Frequency Analysis

The frequency analysis was done in order to obtain the gain of the circuit as a function of the frequency.

The following plot shows the function we obtained for V_{out}.

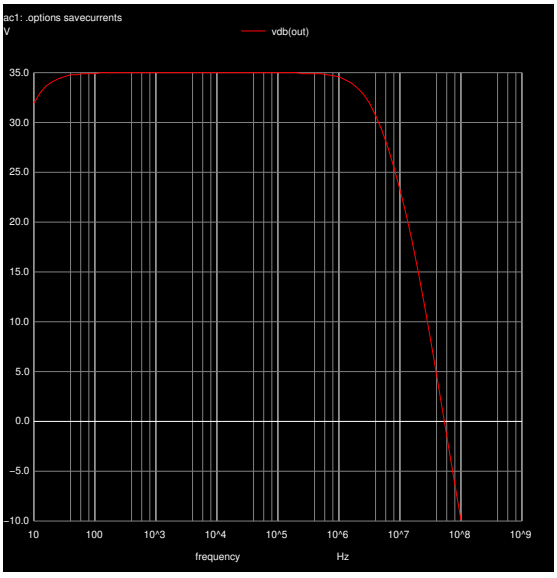

Figure 3: vOUT (dB)

From this analysis, we can also obtain the values for the upper and lower cut off frequencies, which allows us to compute the bandwidth. the input impedance and the output impedance, where we used a different circuit with V_{IN} and R_{IN} disconnected and an output voltage source.

The values obtained for the impedances and for the gain are presented in the following table. They are compared with the theoretical calculations in Section 4.

Name	Value [Ω]
abs(zin1)	7.664021e+02
zout	4.496054e+00
abs(gain)	5.604104e+01

Table 8: Gain, input impedance and output impedance

Here we present the values of the cutt off frequencies and the value of the bandwidth. Once again, these are compared with the theoretical results in Section 4.

Name	Value [Hz]
uco	3.106930e+06
lco	7.923603e+00
bandwith	3.106922e+06

Table 9: Bandwidth

3.3 Merit Figure

In this section, we present the costs of the components and the total cost of the circuit, as well as the merit figure.

Name	Value [Mu]
cost	8.116008e+03
merit	2.707518e+03

Table 10: Merit figure

4 Side-by-side

As a viewer's reference note, the theoretical values are presented on the left and the simulation values on the right.

Name	Value [V]	Name	Value [V]
V_{CE}	7.972014	vce	7.969251e+00
V_{BE}	0.7000000	vbe	6.986238e-01
V_{O1}	8.646473	vo1	8.654746e+00
V_{EC}	9.346473	vec	9.397377e+00
V_{EB}	0.7000000	veb	7.426318e-01
V_{O2}	9.346473	vo2	9.397377e+00

Table 11: Comparison 1

We can see that the values are similar. Also, we can observe that the transistors are working in the Forward Active Region.

Name	Value [Ω]	Name	Value [Ω]
Z_I	640.4922	abs(zin1)	7.664021e+02
Z_O	2.936362	zout	4.496054e+00
AV	107.21838	abs(gain)	5.604104e+01

Table 12: Comparison 2

There are some noticeable differences but both values are in the same order of magnitude.

Name	Value [Hz]	Name	Value [Hz]
uco	3106930.0	uco	3.106930e+06
lco	11.75169	lco	7.923603e+00
$bandwith$	3106918.25	bandwith	3.106922e+06

Table 13: Comparison 3

Here we can see that the values are very similar to eachother.

Name	Value [Mu]	Name	Value [Mu]
$cost$	8116.008	cost	8.116008e+03
$merit$	3492.661	merit	2.707518e+03

Table 14: Comparison 4

We can see that the cost is the same but the merit figure is higher using Ngspice's values, probably due to a higher bandwidth.

5 Conclusion

All in all, this laboratory assignment showed that the difference between the theoretical models and the simulation is minimal, never differing more than one order of magnitude as seen in Section 4.

This lab assignment showed us that the main purpose of the bypass capacitor C_E in the gain stage is to avoid a gain loss through resistor R_E and the main purpose of resistor R_E is to stabilize the temperature effect. In the DC component the temperature effect is most important while in AC the gain is. Therefore there needs to be an equilibrium, which is achieved by placing these components in parallel.

Also, for lower frequencies (DC) capacitor C_E behaves like an open circuit, so the current goes through resistor R_E, stabilizing the temperature effect. For higher frequencies (AC) the capacitor behaves like a short circuit and therefore it is used to bypass the resistor R_E , avoiding a reduction of the gain (gain is stable in the desired passband).

As for R_C, it increases the gain, so by playing with its value it is possible to achieve a better merit figure.