Sequential Circuits

Topics

- Latches and flip-flops
- Clocked synchronous state-machine analysis
- Implementation and simulation with Quartus Prime

Problems

1. *[Paper and pencil].* Complete the following timing diagram (Fig. 1) to illustrate the difference between a D latch and a positive-edge-triggered D flip-flop (illustrate only the functional behavior assuming that all delays are 0).

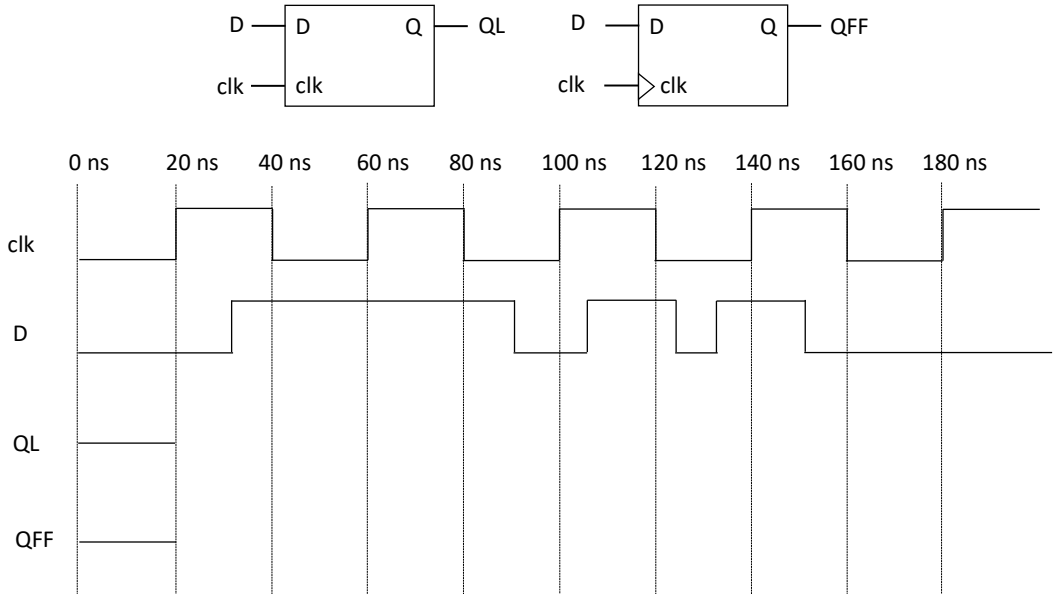

Fig. 1 – Functional behavior of a D latch and a positive-edge-triggered D flip-flop.

Determine the period, frequency, and duty cycle of the `clk` signal. Do not forget to indicate the correct units.

2. *[Paper and pencil].* Analyze the circuits in Fig. 2 and indicate the location of a D latch, a positive-edge-triggered D flip-flop, and a negative-edge-triggered D flip-flop.

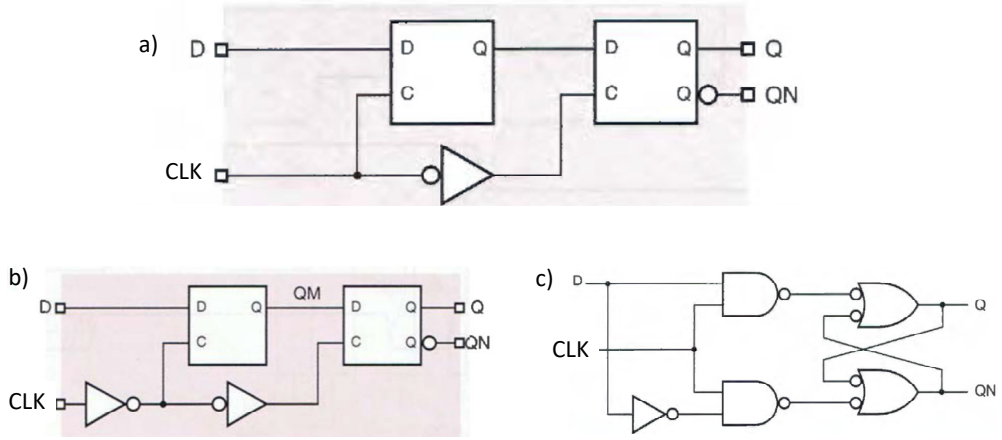

Fig. 2 – This figure contains a D latch, a positive-edge-triggered D flip-flop, and a negative-edge-triggered D flip-flop. Identify their locations.

3. *[Paper and pencil].* Complete the timing diagram of a positive edge-triggered flip-flop, illustrated in Fig. 3, with the following timing specifications: t_{setup} = 5 ns, t_{hold} = 3 ns, t_{pHL} = 10 ns, t_{pLH} = 5 ns.

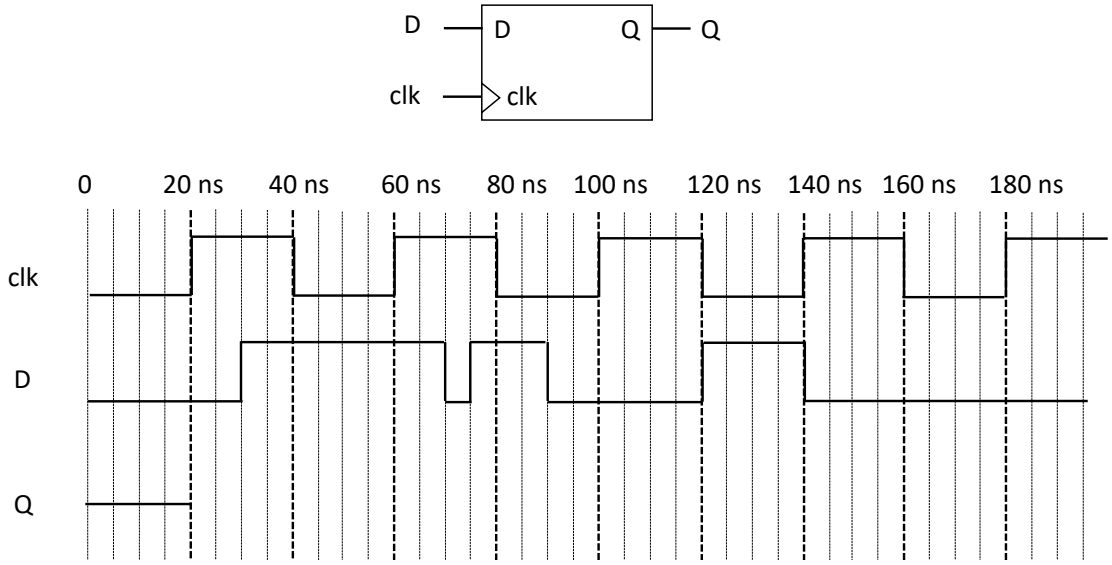

Fig. 3 – A timing diagram of a positive edge-triggered flip-flop to complete.

4. *[Paper and pencil].* Analyze the circuit in Fig. 4 and complete the following timing diagram (for now, assume that all delays are 0). What is the function of this circuit? Determine the period, frequency, and duty cycle of both the `clk` signal and `Q` output. Do not forget to indicate the correct units.
Assuming that the flip-flop has the following timing specifications: t_{setup} = 5 ns, t_{hold} = 3 ns, t_{pHL} = 15 ns, t_{pLH} = 10 ns, determine the maximum operating frequency of the circuit.

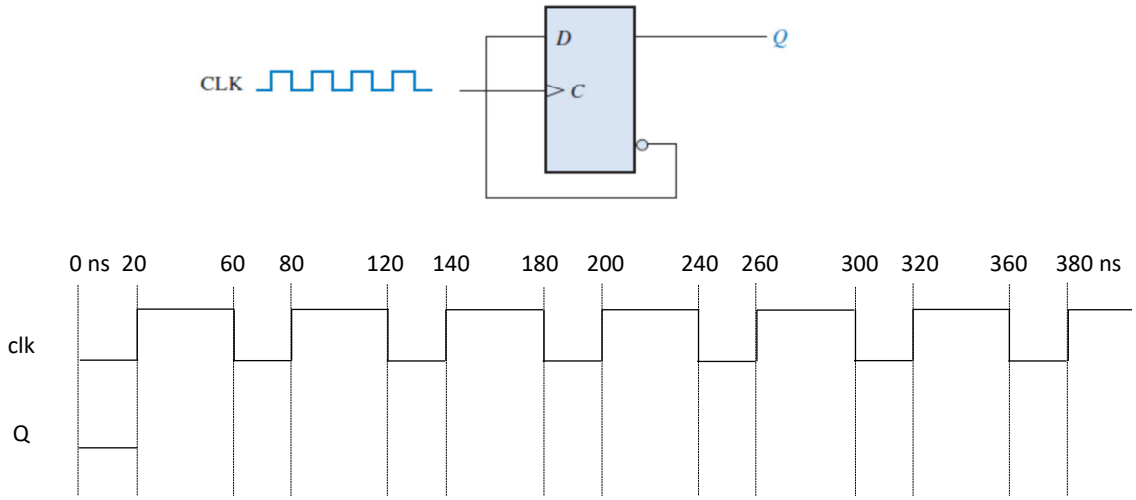

Fig. 4 – A circuit based on a D flip-flop and its timing diagram.

5. *[Paper and pencil].* Analyze the circuit in Fig. 5 and respond the following questions:

a. What are the circuit inputs and outputs?
b. What is the output function?
c. What is the next state function?
d. What is the type of this finite state machine: Mealy or Moore?
e. Construct the transition/output table.
f. Draw the state diagram.
g. What is the function performed by the circuit?
h. Assume that the flip-flops in Fig. 5 have the following timing specifications: t_{setup} = 15 ns, t_{hold} = 5 ns, t_{pHL} = 25 ns, t_{pLH} = 20 ns. What is the maximum delay that an elementary logic gate t_{gate} could have so that the circuit would function correctly at 20 MHz?

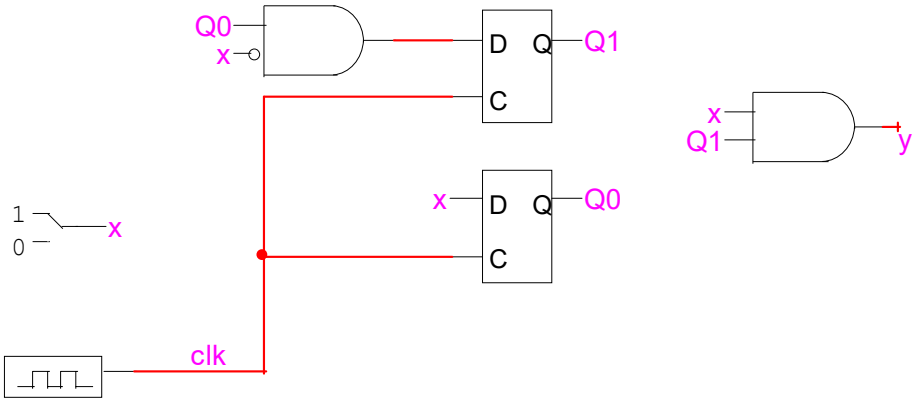

Fig. 5 – A circuit to analyze in the problem 5. The used sequential components are D flip-flops.

6. *[Paper and pencil + Quartus Prime]*. Draw and check the state diagram for the circuit in Fig. 6. Indicate whether this is a Mealy machine or a Moore machine.

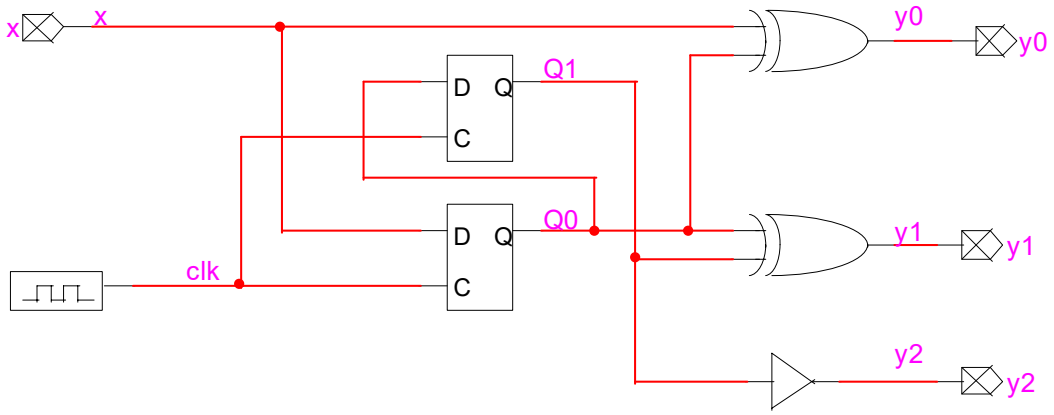

Fig. 6 – A binary to Gray code converter to analyze in the problem 6.

Assuming that the flip-flops in Fig. 6 have the following timing specifications: t_{setup} = 15 ns, t_{hold} = 5 ns, t_{pHL} = 25 ns, t_{pLH} = 20 ns and that the delay of any elementary logic gate is t_{gate} = 10 ns, determine the maximum operating frequency of the circuit.

Modify the circuit so that it has an active-low synchronous reset input.

Using the *Quartus Prime* software, create a new project named "Bin2Gray". Create a new file for a schematic diagram and implement the circuit from Fig. 6 (let `clk` be an input port). Simulate the circuit and show that it is a serial to parallel converter from binary to Gray code for words of length 3.