2.a) Referring to the system S, complete the memory map with the three vectors A, B and C.

Fill in the orange fields with your answers	
Nome	
Cognome	
Matricola	

2

2.a.i) Complete the map with the three vectors A, B and C.

BA[31..0]	Byte3	Byte2	Byte1	Byte0	BA[31..0]
0x8000_5FFF	C[1023]	C[1023]	C[1023]	C[1023]	0x8000_5FFC
0x8000_5003	C[0]	C[0]	C[0]	C[0]	0x8000_5000
0x8000_3FFF	B[1023]	B[1023]	B[1023]	B[1023]	0x8000_3FFC
0x8000_3003	B[0]	B[0]	B[0]	B[0]	0x8000_3000
0x8000_1FFF	A[1023]	A[1023]	A[1023]	A[1023]	0x8000_1FFC
0x8000_1003	A[0]	A[0]	A[0]	A[0]	0x8000_1000
	MSB			LSB	

NOTE:

2.a.ii) How many bits are needed to represent the TAG and Set ID of vectors A, B and C? Specify the address and bits of TAG and Set ID of the first and last elements of each of vectors A, B and C.

Proprieta'	A	B	C
# Elementi	1024	1024	1024
# Bytes	4096	4096	4096
# bit TAG	21	21	21
# bit Set ID	7	7	7
TAG [0]	0x100002	0x100006	0x10000A
Set ID [0]	0x0	0x0	0x0
TAG [1023]	0x100003	0x100007	0x10000B
Set ID [1023]	0x7F	0x7F	0x7F

NOTE:

2.a.iii) How much memory do the three vectors A, B, and C occupy in total? Is it possible that all three vectors are simultaneously and entirely in cache at the same time?

NOTE: No, the cache is 4KiB and the required memory would be 12KiB.

2.b) Analyze the dynamics of the data cache by assuming that task T1 executes one iteration of the loop body after two iterations of the loop body of task T0. Assume that all cache lines of the two cores are initially invalid. Answer the following questions precisely, schematically, concisely, and tabularly:

2.b.i) Show the cache contents, MESI state, and LRU bit value for the first iteration of task T0 (i=0).

Task T0	Iterazione:	0	Miss	1		Hit	0
	Istruzione:			flw f15, 0(x10)			
	Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]	E	1	-	-	-

Task T0	Iterazione:	0	Miss	2		Hit	0
	Istruzione:			fsw f15, -4(x11)			
	Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]	E	0	0x100006	B[0]	M

2

2.b.iii) Calculate the number of accesses, MISS and WB cycles at the end of execution of each repetition of tasks T0 and T1.

Ripetizione		Core 0 #accessi	Core 0 #hit	Core 0 #miss	Core 1 #accessi	Core 1 #hit	Core 1 #miss
1	T0	2	0	2	-	-	-
2	T0	2	2	0	-	-	-
3	T1	-	-	-	2	0	2
4	T0	2	2	0	-	-	-
5	T0	2	2	0	-	-	-
6	T1	-	-	-	2	2	0

Any task executes 128 cycles of WB when the second half of B and C arrays is written.

2.b.iv) Calculate the overall hit and miss rate at the end of the executions of the two tasks. How would the hit and miss rates change if the L1 caches were directly mapped?

Task T0 has 2 cache misses every 8 accesses (1 miss every 4 load, 1 miss every 4 store), while task T1 has 2 cache misses every 4 accesses (1 miss every 2 loads, 1 miss every 2 store).

T0 miss rate is 25% and T1 miss rate is 50%

Assuming a directly mapped cache with the same size, the miss rate would have been 100% for both tasks, since both the flw and the fsw access the same cache line.

2.b) Analyze the dynamics of the data cache by assuming that task T1 executes one iteration of the loop body after two iterations of the loop body of task T0. Assume that all cache lines of the two cores are initially invalid. Answer the following questions precisely, schematically, concisely, and tabularly:

2.b.ii) Show the cache contents, MESI state and LRU bit value at the end of the execution sequence T0 (i=0), T0 (i=1), T1(i=0), T0 (i=2), T0 (i=3), T1 (i=1).

CORE 0								EXEC	CORE 1							
Task T0	Iterazione:	0	Miss	1		Hit	0									
	Istruzione:			flw f15, 0(x10)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=0	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	E	1	-	-	I	FLW	-	-	-	I	0	-	-	I
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
Task T0	Iterazione:	0	Miss	2		Hit	0									
	Istruzione:			fsw f15, -4(x11)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=0	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	E	0	0x100006	B[0]	M	FSW	-	-	-	I	0	-	-	I
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
Task T0	Iterazione:	1	Miss	2		Hit	1									
	Istruzione:			flw f15, 0(x10)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=1	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	E	1	0x100006	B[0]	M	FLW	-	-	-	I	0	-	-	I
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
Task T0	Iterazione:	1	Miss	2		Hit	2									
	Istruzione:			fsw f15, -4(x11)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=1	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	E	0	0x100006	B[0]	M	FSW	-	-	-	I	0	-	-	I
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
									Task T1	Iterazione:	0	Miss	1		Hit	0
								Esegue T1		Istruzione:			flw f15, 0(x10)			
	Via0			LRU	Via1			CORE 1		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=0	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	0	0x100006	B[0]	M	FLW	0	0x100002	A[0]-A[3]	S	1	-	-	I
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
									Task T1	Iterazione:	0	Miss	2		Hit	0
								Esegue T1		Istruzione:			fsw f15, -8(x11)			
	Via0			LRU	Via1			CORE 1		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=0	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	0	0x100006	B[0]-B[3]	M	FSW	0	0x100002	A[0]-A[3]	S	0	0x10000A	C[0]-C[3]	M
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
Task T0	Iterazione:	2	Miss	0		Hit	3									
	Istruzione:			flw f15, 0(x10)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=2	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	1	0x100006	B[0]-B[3]	M	FLW	0	0x100002	A[0]-A[3]	S	0	0x10000A	C[0]-C[3]	M
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
Task T0	Iterazione:	2	Miss	0		Hit	4									
	Istruzione:			fsw f15, -4(x11)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=2	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	0	0x100006	B[0]-B[3]	M	FSW	0	0x100002	A[0]-A[3]	S	0	0x10000A	C[0]-C[3]	M
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
Task T0	Iterazione:	3	Miss			Hit										
	Istruzione:			flw f15, 0(x10)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=3	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	1	0x100006	B[0]-B[3]	M	FLW	0	0x100002	A[0]-A[3]	S	0	0x10000A	C[0]-C[3]	M
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
Task T0	Iterazione:	3	Miss			Hit										
	Istruzione:			fsw f15, -4(x11)				Esegue T0								
	Via0			LRU	Via1			CORE 0		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=3	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	0	0x100006	B[0]-B[3]	M	FSW	0	0x100002	A[0]-A[3]	S	0	0x10000A	C[0]-C[3]	M
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
									Task T1	Iterazione:	1	Miss			Hit	
								Esegue T1		Istruzione:			flw f15, 0(x10)			
	Via0			LRU	Via1			CORE 1		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=1	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	0	0x100006	B[0]-B[3]	M	FLW	0	0x100002	A[0]-A[3]	S	1	0x10000A	C[0]-C[3]	M
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I
									Task T1	Iterazione:	1	Miss			Hit	
								Esegue T1		Istruzione:			fsw f15, -8(x11)			
	Via0			LRU	Via1			CORE 1		Via0			LRU	Via1		
Set ID	TAG	Data	MESI		TAG	Data	MESI	i=1	Set ID	TAG	Data	MESI		TAG	Data	MESI
0	0x100002	A[0]-A[3]	S	0	0x100006	B[0]-B[3]	M	FSW	0	0x100002	A[0]-A[3]	S	0	0x10000A	C[0]-C[3]	M
-	-	-	I	0	-	-	I		-	-	-	I	0	-	-	I