LatticeMico8

Soft Core 8-Bit Microcontroller Optimized for Lattice Programmable Devices

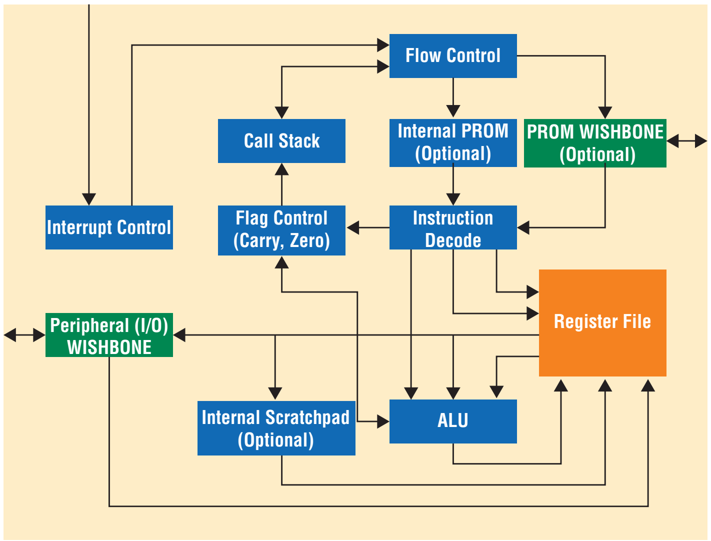
The LatticeMico8™ is an 8-bit "soft" microcontroller core optimized and fully tested for the MachXO2™ family of Programmable Logic Devices (PLDs). It can also be used as a reference design for the LatticeECP™, LatticeEC™ and LatticeXP™ families of Field Programmable Gate Arrays (FPGAs) as well as the MachXO™ family of PLDs. Combining a full 18-bit wide instruction set with 32 general purpose registers, the LatticeMico8 flexible design is suitable for a wide variety of markets, including communications, consumer, computer, medical, industrial, and automotive. The core consumes minimal device resources, less than 200 Look Up Tables (LUTs) in the smallest configuration, while maintaining a broad feature set.

The LatticeMico8 microcontroller integrates a 8-bit WISHBONE slave interface for accessing I/O peripherals and an optional external scratchpad. It also integrates an optional 8-bit WISHBONE slave interface for accessing external PROM with WISHBONE interface.

The associated LatticeMico™ System Development Tools provide a fast and easy way to implement microcontroller designs for MachXO2. The tools enable processor platform definition, software development and debug.

Additionally, and in order to encourage user experimentation, development and contributions, Lattice is providing a new open intellectual property (IP) core license, the first such license offered by any FPGA supplier. The license applies many of the concepts of the successful open source movement to IP cores targeted for programmable logic applications.

LatticeMico8 Block Diagram



```
lm8-elf-gcc -o hello_world.out -mcall-prologues
perl lm8-deployer.pl ./ hello_world.out
```

Key Features and Benefits

- **Innovative Open IP Core License**
- **Excellent Solution for a Wide Variety of Applications**
  - Consumer, computation, communications, medical, industrial, automotive
- **Optimized and Fully Tested for the MachXO2 Family**
  - Reference design for MachXO, LatticeECP/EC and LatticeXP families
- **Efficient Architecture – Utilizes <200 LUTs**
- **Broad Feature Set**
  - 18-bit wide instructions
  - Configurable 16 or 32 general-purpose registers Configurable Instruction Memory (PROM)
    - Internal, or external through WISHBONE Interface
    - Configurable to accomodate 256, 512, 1K, 2K, or 4K instructions
  - Scratchpad Memory
    - Internal, or external through WISHBONE Interface
    - Configurable upto 4Gbytes using paging (256 bytes/page)
  - Minimum Two Cycles per Instruction
  - Configurable 8, 16, or 32-deep call stack
  - Support for up to 8 external interrupt
  - Integrated hardware loader to optionally initialize PROM and scratchpad from an external non-volatile memory at power up.
- **Peripheral Components (WISHBONE)**
  - GPIO, UART, DMA controller, SPI Flash controller, MachXO2 EFB (I^{2}C, SPI, timer)
- **Easy-to-Use Develoment Tools**
  - LatticeMico System for:
    - Platform definition
    - C and Assembly software development
  - LatticeMico System operates with Lattice Diamond™ for platform definition. Includes support for:
    - Standard make
    - On-chip memory deployment
    - Non-volatile memory deployment

Open IP Core Licensing

The generated LatticeMico8 IP core and selected peripheral component HDL codes are available through a unique open IP core licensing agreement, while the GNU-based compiler, assembler, linker and debugger are licensed under the GNU GPL agreement. The main benefits of open source IP are:

- **Visibility**
  - Allows complete understanding of the detailed operation of the core
- **Flexibility**
  - User can develop alternate micro-architectures or implementations
- **Portability**
  - Architecture independence
  - Migrate to an ASIC or SoC
- **Free of Charge**

Flexible Configurations

The LatticeMico8 microcontroller offers superior design flexibility. LatticeMico8 is parameterized to allow the easy implementation of four standard configurations, each optimized for different user needs. With available external scratchpad RAM, more memory, and up to 32 registers, the LatticeMico8 delivers a flexible solution with plenty of resources.

Four Standard Configurations

	Configuration			
Resource	**1**	**2**	**3**	**4**
Registers	16	32	16	32
Internal RAM Scratch Pad	32	32	16	16
External RAM Scratch Pad	No	No	No	No

Four Standard Configurations

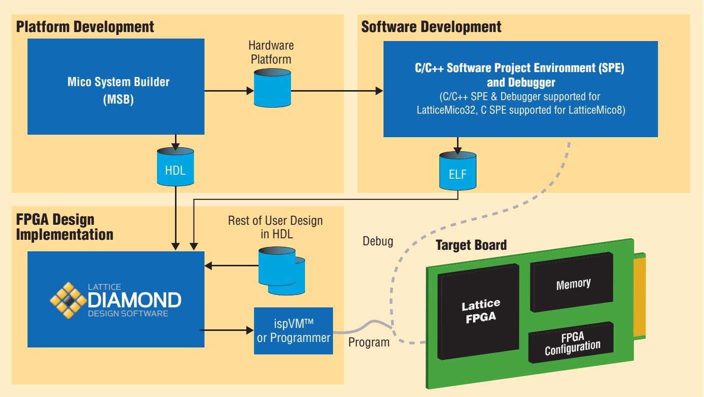
Config #	Description	Device	LUTs	Registers	SLICEs	f_{MAX} (MHz)
1	No of registers 16 Call stack depth 8 Data & I/O Addressable Range 256 PROM 512 Internal Scratchpad 32 Byte GPIO (Data width 8)	LCMXO2-1200HC-5TG100C	194	83	129	46.2
2	No of registers 32 Call stack depth 8 Data & I/O Addressable Range 256 PROM 512 Internal Scratchpad 32 Byte GPIO (Data width 8)	LCMXO2-1200HC-5TG100C	206	83	147	49
3	No of registers 16 Call stack depth 8 Data & I/O Addressable Range 256 PROM 512 Internal Scratchpad 16 Byte GPIO (Data width 8)	LCMXO2-1200HC-5TG100C	193	83	128	48
4	No of registers 32 Call stack depth 8 Data & I/O Addressable Range 256 PROM 512 Internal Scratchpad 16 Byte GPIO (Data width 8)	LCMXO2-1200HC-5TG100C	205	83	127	52.2

Lattice Development Tools

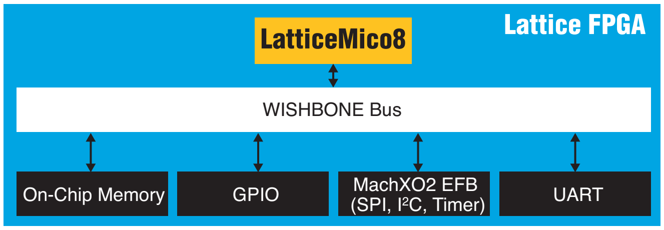
The LatticeMico System is used to implement a LatticeMico8 soft microcontroller system with attached peripheral components in a Lattice FPGA or CPLD. It is based on the Eclipse C/C++ Development Tools (CDT) environment, which is an industry open-source development and application framework for building software. The LatticeMico System contains two integrated tools that combine with Diamond to coordinate the building of an embedded controller system on an FPGA/CPLD device and write the software to drive it.

- **Mico System Builder (MSB)**
  - Generate platform description and associated HDL for hardware implementation
  - Choose peripheral components to attach to the LatticeMico8
  - Specify connectivity between peripheral components
- **C/C++ Software Project Environment (SPE)**
  - Develop the code that runs on platforms created with MSB
  - Interfaces via command line to compiler, assembler and linker tools
  - GNU-based compiler tools provide appropriate compiler, assembler, and linker if desired

LatticeMico System Development Flow


Platform Development
Mico System Builder (MSB)
Hardware Platform
HDL
Software Development
C/C++ Software Project Environment (SPE) and Debugger
(C/C++ SPE & Debugger supported for LatticeMico32, C SPE supported for LatticeMico8)
ELF
FPGA Design Implementation
Rest of User Design in HDL
LATTICE DIAMOND DESIGN SOFTWARE
ispVM™ or Programmer
Debug
Program
Target Board
Lattice FPGA
Memory
FPGA Configuration

Sample LatticeMico8 Platform Generated with Mico System Builder



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