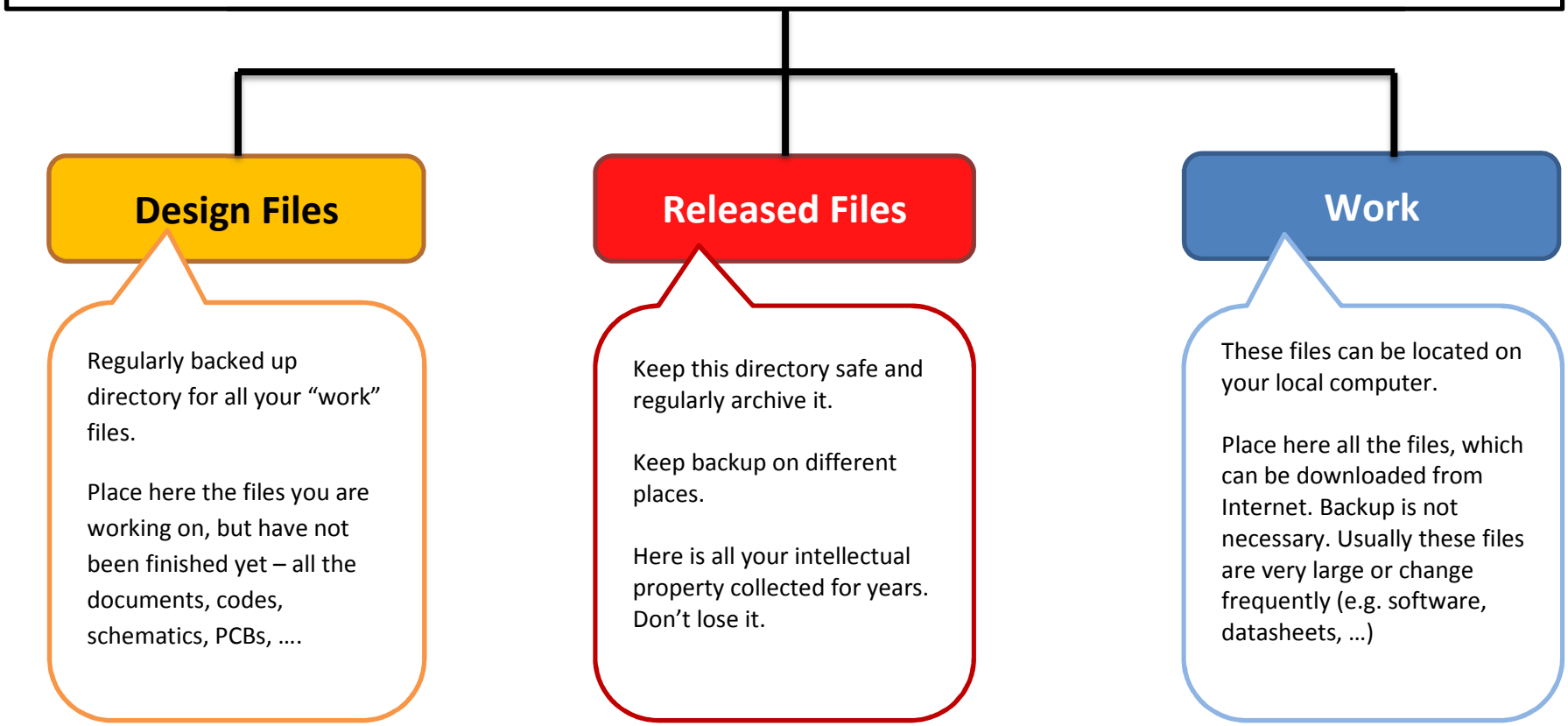
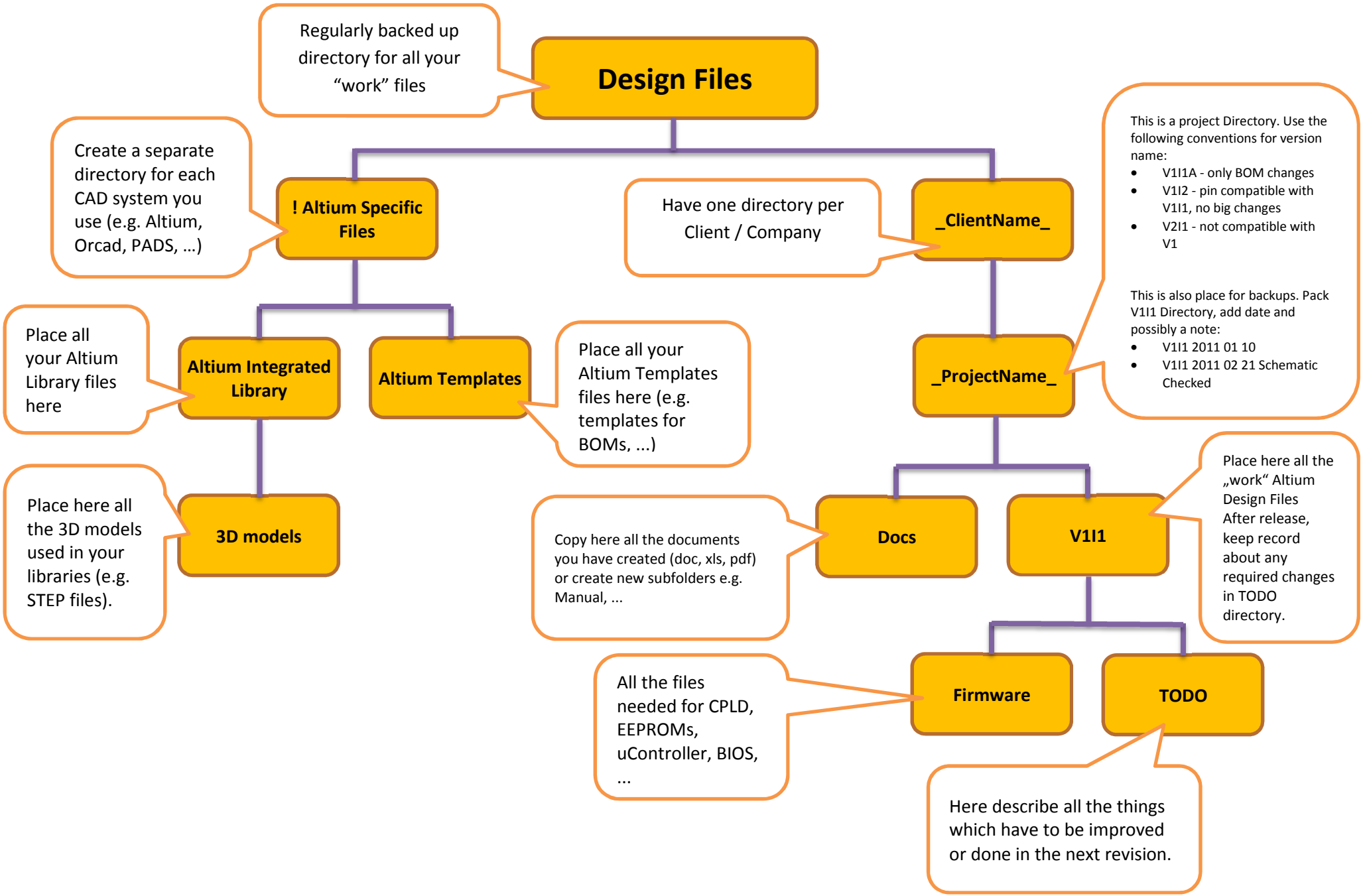
FEDEVEL Directory Template

This directory template helps you organize your documentation.
It also helps engineers to generate high standards and consistent outputs.

Version 1.0, created by Robert Feranec
Download the complete template at http://www.fedevel.com/welldoneblog



Why three main directories?
Simpler backup & easy permission control.



http://www.fedevel.com/welldoneblog/

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ONCE RELEASED:
- NEVER EVER CHAGE THE FILES IN THESE DIRECTORIES!
- NEVER WORK IN THESE DIRECTOTRIES (do not open files directly from these folders)

WHEN YOU START A NEW BOARD ISSUE, ALWAYS COPY AND USE FILES FROM THESE RELEASE DIRECTORIES AS YOUR STARTING POINT AND THEN READ TODO file

Released Files

ClientName

ProjectName

V1I1

Follow this procedure before releasing files. Confirm every action with your initials and date. IF ANY CHANGES NEEDS TO BE DONE, START THE PROCEDURE FROM BEGINNING! The procedure needs to be executed in order as defined here. Start from number 1

1) Right Click on the project -> Compile PCB project. I confirm, the project compiles with no errors: YourIntials [DAY-MONTH-YEAR]
2) Run Design -> Update PCB Document. I confirm, there are no differences between Schematic and PCB: YourIntials [DAY-MONTH-YEAR]
3) Impedance. I confirm, I have updated and check track width/gap to match required impedance (e.g 55 OHMs): YourIntials [DAY-MONTH-YEAR]
4) Polygon Action -> Repour All. I confirm, all polygons have been repoured: YourIntials [DAY-MONTH-YEAR]
5) Run Tools -> Design Rule Check -> Run Design Rule Check. I confirm, I have checked Design Rule Output File: YourIntials [DAY-MONTH-YEAR]
6) Gerber check. I confirm, I have copied and visually checked gerber files placed in \PCB Manufacturing\Gerber Output\ YourIntials [DAY-MONTH-YEAR]
7) Other files. I confirm, I have copied and checked files placed in subdirectories: YourIntials [DAY-MONTH-YEAR]

Highlight differential pairs and Take screenshots of each layer. Examples of naming screenshots:

DIFF100-L1.jpg
DIFF100-L3.jpg
DIFF90-L1.jpg
...

Why? If manufacturer can not find a particular DIFF pair on one of the layers, they will contact you.
By providing them these screenshots, they can check it by themselves.

Use the same Client name, Project name and Version as in your Design Files directory

Place PCB stackup information here.

All the files needed for CPLD, EEPROMs, uController, BIOS, ...
Start file name with component designator - the one where the file needs to be stored e.g:
U5 - AMI BIOS 0ABVQ018
U15 - Ethernet EEPROM 82574

Place following files here: 3D step file, 3D pdf

Update Schematic Cover Page to RELEASED DD-MMM-YYYY
Place here PDF version of schematic, if possible one for each BOM variant.

Place here zip file of source files, e.g copy and pack here directory from:! ALtium SourceFiles_ClientName\ProjectName_\V1I1

Step 1 - PCB Manufacturing

Step 2 - Board Assembly

Step 3 - Firmware

Step 4 - 3D

Step 5 - Schematic

Step 6 - Source Files

Gerber Output

Layers with Highlighted Differential Pairs

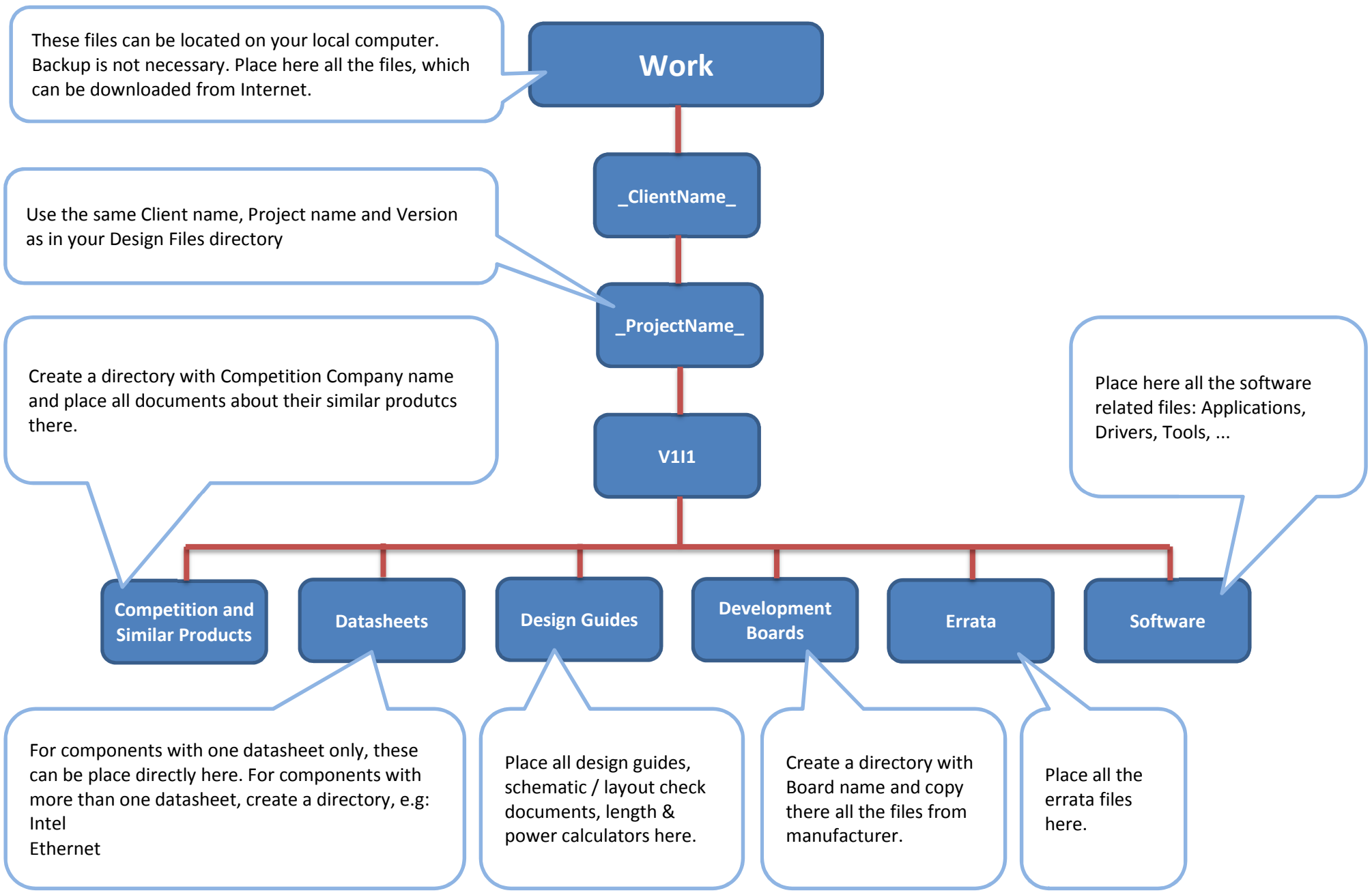
NC Drill Output

Place here gerber files.

Place here drill files and documents which explain it (e.g. for HDI PCB you can put here pdf showing drills for each layer pair)

Place following files here:

- Mechanical Drawing (Board dimensions, holes position, ..)
- TOP and BOTTOM Assembly Drawing (Component position with Reference Designator)
- TOP and BOTTOM VIEW (shows board outline, assembly layer, TOP + BOTTOM layers)
- Bill of Materials (grouped by component type)
- Component reference BOM (each component on one line: Designator, Description, Manufacturer 1, Manufacturer, Part Number 1, Package / Case, Supplier 1, Supplier Part Number 1)
- Pick and Place
- TOP and BOTTOM Layer + TOP and BOTTOM Paste Gerber Files (for stencil - if panel is done in a PCB house, ask them later for the top/bottom layers and paste for the panel)
- PDF 3D Model



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