ADVANCED CPU ARCHITECTURE HARDWARE ACCELERATION LAB

361.1.4963

Submitted by: Tomer Elis, ID 208677997

Bar Cohen Ahronson, ID 214237638

Date of experiment: 24.4.2025

Date of report submission: 24.4.2025

The Department of Electrical &
Computer Engineering

BGU

Introduction:

In this lab, we will explore synchronous processes in VHDL (VHSIC Hardware Description Language).

Fast Counter:

The Fast Counter is a counter that counts from zero to the number in the Slow Counter. After it goes up to this number it resets and starts to count again.If the counter exceeds the UpperBound its stop counting.

Slow Counter:

The Slow Counter count from zero to the UpperBound. It does it by freezing the count, until the fast number equal to his number, when that appen, the slow counter add 1 to his count.

Control :

The Control is the part of the code that “manages” the Counters.
It tells them if they need to continue to count, freezing or reset.

Signals:

cnt_slow_signal: That the output vector of the slow counter. it represents what number the slow counter got to.

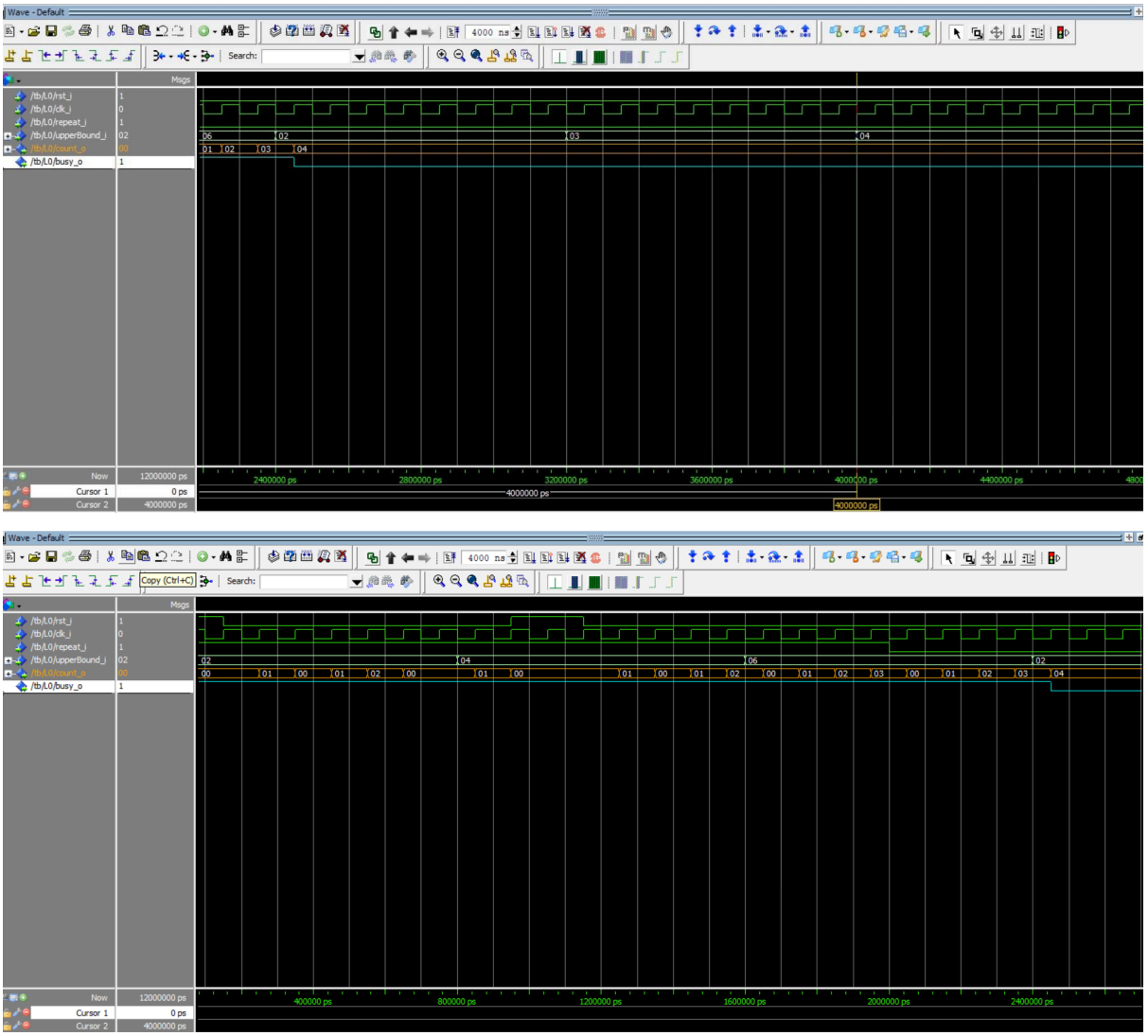
cnt_fast_signal: That the output vector of the fast counter. it represents what number the fast counter got to.

temp : This signal is a vector that stores the upperBound value.

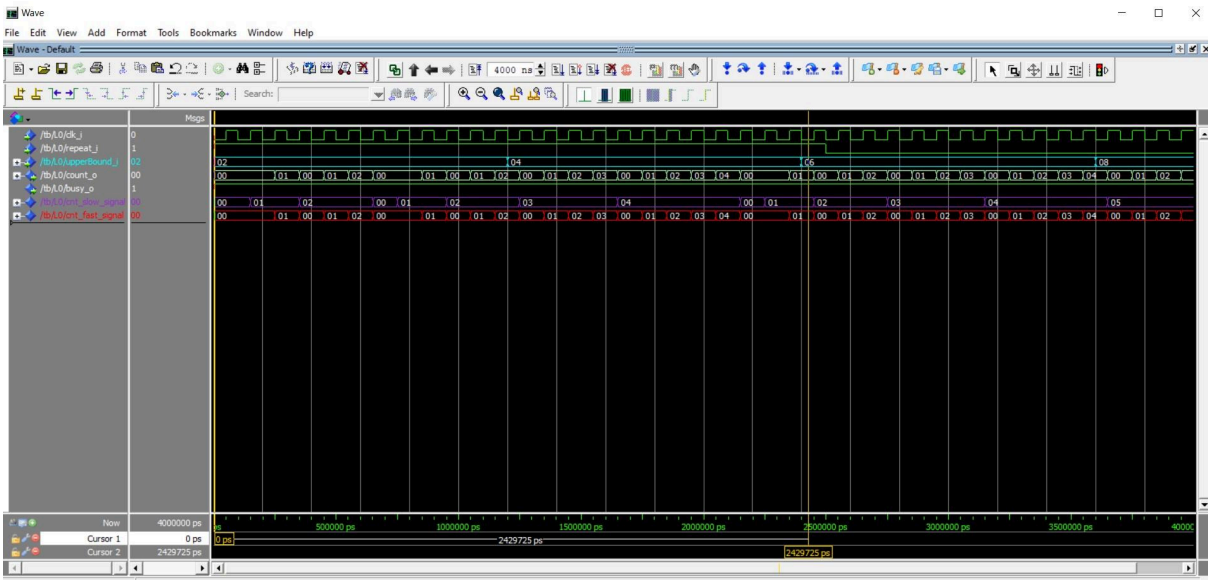
control_fast_signal: This signal is a vector that defines if the fast counter needs to continue(“00”), restart(“01”) or freeze(“10” or “11”).

control_slow_signal : This signal is a vector that defines if the slow counter needs to continue(“00”), restart(“01”) or freeze(“10” or “11”).

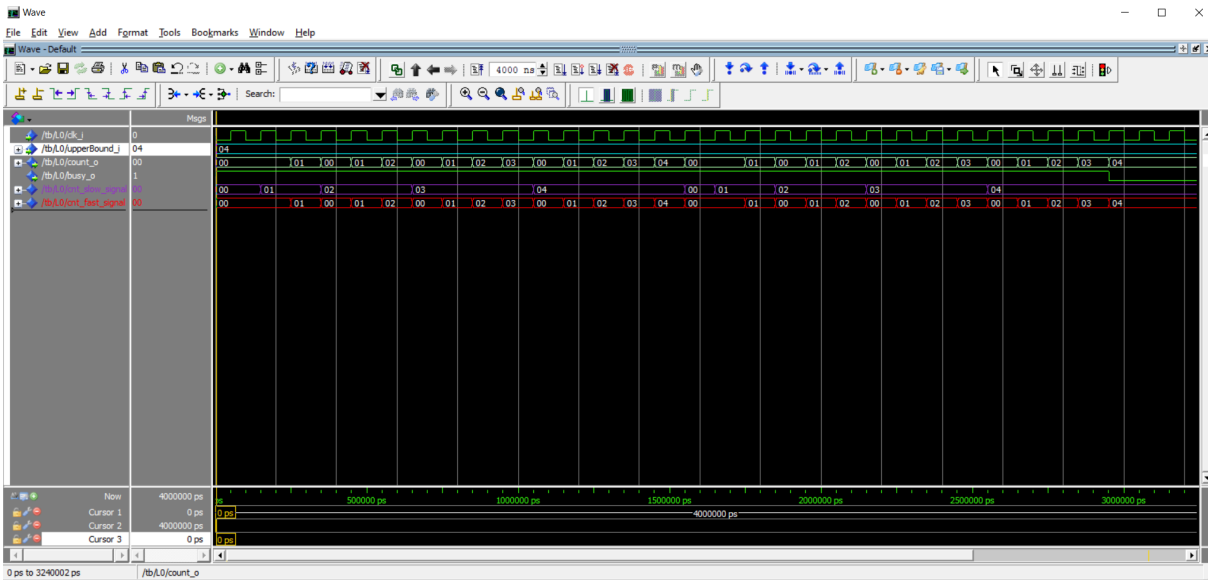
simulation



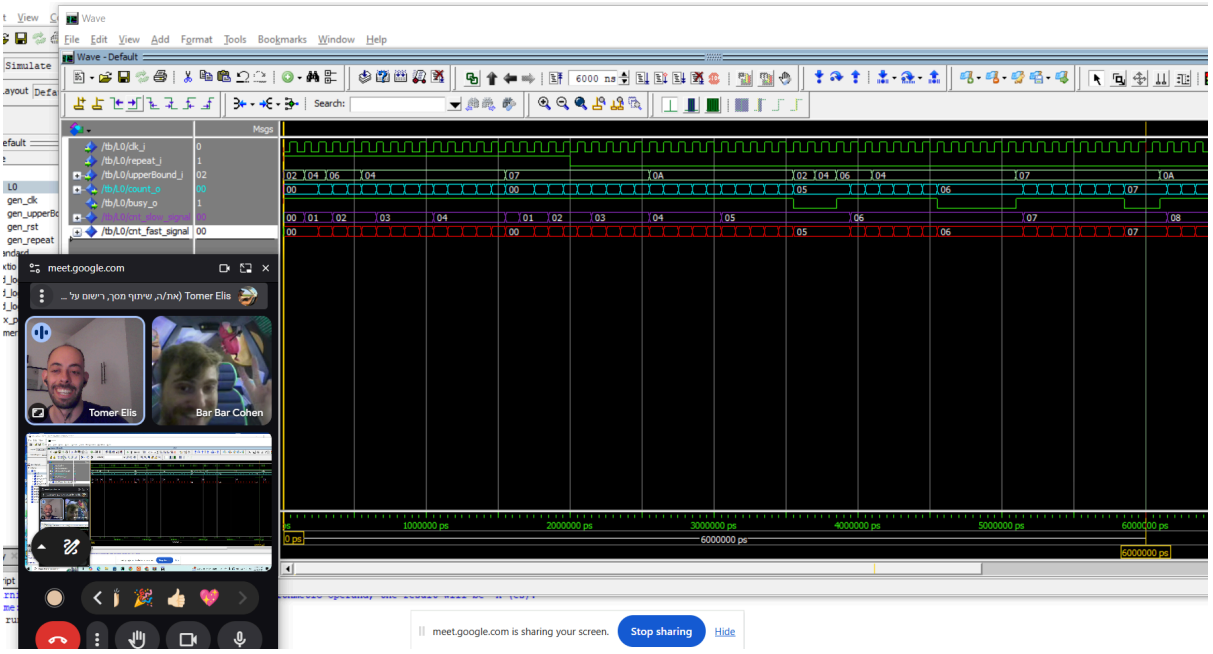
at the pictures above we can see the wave signals of TB3
in orange we can see the count which reflected the fast clock in the inner implementation.
at ~ 2400 ns we can see that busy is decreased since our Boundrate is down to “02”.



In this wave signals (TB2) we can see the inner signals of slow and fast clock (in red and purple).
another thing is that we can see how the logic of each clock working and that the "slow clock signal" wait for "fast clock signal" at each round.



Here we can see TB1 wave signals purple and red are the clocks and blue is the upperbound. since the upperbound is stuck at 4 value, we can see that our clock works periodically.



And finally our TB 🙂

in the photo we can see wave signals of Bar Bar Cohen and Tomer Elis.

we can see that the busy signal is going up and than going down since we created this tb to do so.

in blue in the count and in red and purple is our inside clocks as usual.

more details can be found in the readme file.