Release Note

CONFIDENTIAL

Initial Program Loader

Release Note: Software

R-Car H3/M3/M3N/E3/D3 Series

Renesas Electronics
www.renesas.com

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How to Use This Manual

- **[Readers]**
  This manual is intended for engineers who develop products which use the R-Car H3/M3/M3N/E3/D3 processor.

- **[Purpose]**
  This manual is intended to give users an understanding of the functions of the R-Car H3/M3/M3N/E3/D3 processor device driver and to serve as a reference for developing hardware and software for systems that use this driver.

- **[How to Read This Manual]**
  It is assumed that the readers of this manual have general knowledge in the fields of electrical
  — engineering, logic circuits, microcontrollers, and Linux.
  → Read this manual in the order of the CONTENTS.
  — To understand the functions of a multimedia processor for R-Car H3/M3/M3N/E3/D3
  → See the R-Car H3/M3.M3N/E3/D3 User's Manual.
  — To know the electrical specifications of the multimedia processor for R-Car H3/M3/M3N/E3/D3
  → See the R-Car H3/M3/M3N/E3/D3 Data Sheet.

- **[Conventions]**
  The following symbols are used in this manual.
  Data significance: Higher digits on the left and lower digits on the right
  Note: Footnote for item marked with Note in the text
  Caution: Information requiring particular attention
  Remark: Supplementary information
  Numeric representation: Binary ... ××××, 0b××××, or ××××B
  Decimal ... ××××
  Hexadecimal ... 0x×××× or ××××H
  Data type: Double word … 64 bits
  Word … 32 bits
  Half word ... 16 bits
  Byte ... 8 bits

Table of Contents

1. Introduction

1.1 Objectives

This manual explains the package construction of R-Car H3/M3/M3N/E3/D3/H3e/M3e/M3Ne/E3e/D3e Initial Program Loader.

1.2 References

[1] ARM., *Cortex-A53 MPCore Software Developers Errata Notice.*

[2] ARM., *Cortex-A57 MPCore Software Developers Errata Notice.*

[3] Renesas Electronics Corp., *Linux Interface Specification Yocto recipe Start-Up Guide.*

[4] Renesas Electronics Corp., *Initial Program Loader User's Manual.*

This manual refers to the latest edition of the references.

2. Component

The following is included in this product.

2.1 Software components

The following shows components of Trusted Firmware-A.
Initial Program Loader is designed based on the architecture of BL2.
BL31, BL32 are included R-Car H3/M3/M3N/E3/D3 Security Board Support Package. BL33 is Linux.

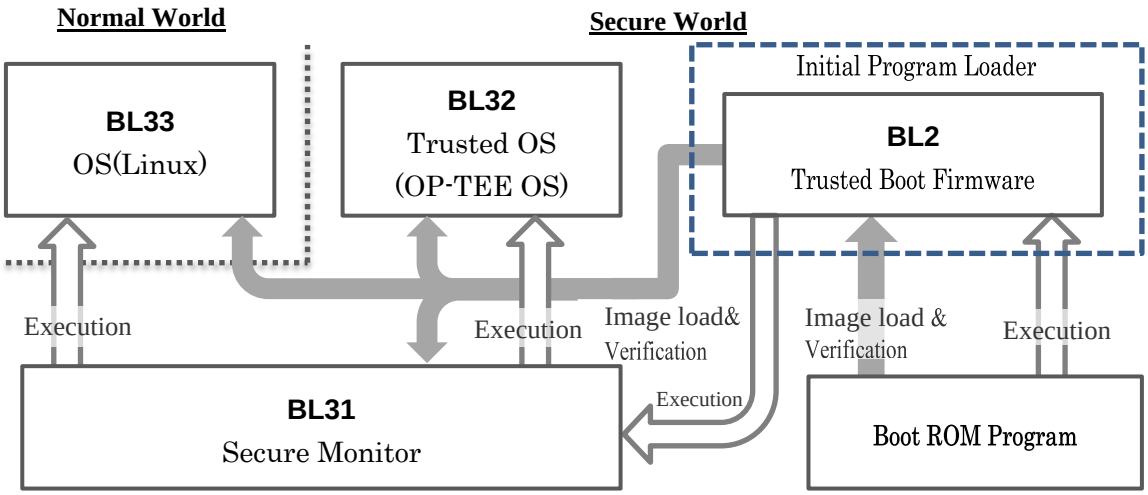

Figure 1 Software components

2.2 Software

Software is provided by the R-Car H3/M3/M3N/E3/D3 Yocto recipe.
Initial Program Loader is BL2 of Trusted Firmware-A that is porting to R-Car H3/M3/M3N/E3/D3 platform.
Initial Program Loader loads images and certificates of BL31, BL32, BL33, and verifies the images and certificates, and executes BL31.
The software is provided under a BSD 3-Clause license.

2.3 Initial Clock setting

Initial clock setting of each module at that time of exit for the Initial Program Loader is below.

2.3.1 R-Car H3 Ver.3.0

Module	Initial clock setting
Cortex-A57	1500 MHz
Cortex-A53	1200 MHz
3DGE	600 MHz
System (AXI-bus)	400 MHz
LPDDR4-SDRAM	DDR3200 (MD19=0/MD17=0)

2.3.2 R-Car M3 Ver.1.2 / Ver.1.3 / Ver.3.0

Module	Initial clock setting
Cortex-A57	1500 MHz
Cortex-A53	1200 MHz
3DGE	600 MHz
System (AXI-bus)	400 MHz
LPDDR4-SDRAM	DDR3200 (MD19=0/MD17=0)

2.3.3 R-Car M3N Ver.1.1

Module	Initial clock setting
Cortex-A57	1500 MHz
3DGE	600 MHz
System (AXI-bus)	400 MHz
LPDDR4-SDRAM	DDR3200 (MD19=0/MD17=0)

2.3.4 R-Car E3 Ver.1.1

Module	Initial clock setting
Cortex-A53	1200 MHz
3DGE	600 MHz
System (AXI-bus)	266 MHz
DDR3L-SDRAM	DDR1856 (MD19=1)

2.3.5 R-Car D3 Ver.1.1

Module	Initial clock setting
Cortex-A53	1000 MHz
3DGE	600 MHz
System (AXI-bus)	266 MHz
DDR3L-SDRAM	DDR1856 (MD19=1)

3. Arm CA53/57 Errata List

Following errata for Arm are supported by Trusted Firmware-A.

System CPU	ID	Summary of Erratum
Cortex-A53 (*1)	835769	AArch64 multiply-accumulate instruction might produce incorrect result
	843419	A load or store might access an incorrect address
	855873	An eviction might overtake a cache clean operation
	1530924	Speculative AT instruction using out-of-context translation regime could cause subsequent request to generate an incorrect translation
Cortex-A57 (*2)	813419	TLB maintenance instructions targeting EL3 may not invalidate the targeted EL3 TLB entries
	859972	Speculative instruction prefetch to Execute-never (XN) memory could cause deadlock or data integrity issue
	1319537	Speculative AT instruction using out-of-context translation regime could cause subsequent request to generate an incorrect translation

*1 The ID assigned to changes in each version document at referenced document [1].

*2 The ID assigned to changes in each version document at referenced document. [2]

4. Change History

Following change histories are representative lists.

4.1 v1.0.0

First release version.

4.2 v1.0.1

Fix and add about following restrictions and functions.

No.	Description
#77205	Version up the base version of arm-trusted-firmware. https://github.com/ARM-software/arm-trusted-firmware Commit e234ba038b0b997bd4325dad384deab5863babdd ➔ 41099f4e7468d872857c52608dcc2a51bae68174
#79228	Updated QoS setting of arm-trusted-firmware.

4.3 v1.0.2

Fix and add about following restrictions and functions.

No.	Description
#79341	Remove the unused source code of DDR initialization.
#79391	Patch to separate DDR and QoS of source code.

4.4 v1.0.3

Fix and add about following restrictions and functions.

No.	Description
#80875	Corresponding GCC5.1 for poky2.0 GCC Compiler

4.5 v1.0.4

Fix and add about following restrictions and functions.

No.	Description
#83846	Add release process of STA restriction for H3 Ver.1.1.
#83584	Add clock setting process of SCIF2 for H3 Ver.1.1.
#83588	Add frequency set process of Generic Timer for H3 Ver.1.1.

4.6 v1.0.5

Fix and add about following restrictions and functions.

No.	Description
#77213	Add monitoring for IPL process hang-up. (Using system watchdog timer).
#79113	Update IPL boot message.
#81155	Add instruction cache disable/invalidate sequence.
#85275	Add display for verification failure message.
#85610	Add implementation for verification process of the BL33x Images.
#73723	Add initial voltage setting for PMIC.
#85121	Update the DDR/QoS settings for H3-Ver.1.1.

4.7 v1.0.6

Fix and add about following restrictions and functions.

No.	Description
#84155	Support Lossy Decompression using shared memory.
#84157	Delete size of version character.
#85127	Add setting to initialize RMSTPCR registers.
#77212	Add the address of Secure Boot API and LCS Judgment API for M3.
#72331	Add setting of pin functions for M3. Update the DDR settings for M3. Update the QoS settings for H3 Ver.1.0/M3. Add the DDR software version for M3.
#87678	Delete setting of SYS-DMAC2 by IPL.
#87765	Add initializing process of IPMMU registers.
#89216	Update the DDR settings rev.0.15 for H3 Ver.1.1.

4.8 v1.0.7

Fix and add about following restrictions and functions.

No.	Description
#80050	Change the order of the CPG initialization.
#80496	Change the order of the QoS initialization.
#88794	Add SCIF2 resource release.
#86876	Modify some inline function to function.
#88259	Change the make argument default value of RCAR_SECURE_BOOT.
#90373	Update the DDR settings for M3.
#89944	Add workaround for PFC write access problem, to PFC initialization.
#90658	Update the QoS settings for M3.
#90662	Add workaround by RT-DMAC, for PFC write access problem.

4.9 v1.0.8

Fix and add about following restrictions and functions.

No.	Description
#92129	Add compile switch for Lossy. "RCAR_LOSSY_ENABLE" If this option value is 0, Lossy Decompression is disable. If this option value is 1, it is enable.
#92045	Add setting of register CA53DBGRCR.
#86598	Modify the problem BL31 built with DEBUG=1 does not start.
#88873	Modify build error that occurred when using LOGLEVEL=0 or 10.
#79402	Add settings SECURITY protection, SDRAM protection, SRAM protection.
#90662	Modify workaround by RT-DMAC, for PFC write access problem.
#92752	Update the QoS settings for M3.
#91784	Modify code to become compatible Binary in case of CA57/53 boot and CR7 boot.

4.10 v1.0.9

Fix and add about following restrictions and functions.

No.	Description
#97222	**[H/W Restriction No.58]** Change the CA5xBAR address from SystemRAM to SDRAM. (The execution module of this process is changed from Initial Program Loader to Secure Monitor)
#98480	Add the compile option of LIFEC_DBSC_PROTECT_ENABLE.
#97932	**[H/W Restriction No.38]** Fix the AXI-bus errata.(Wait 10us after the LifeC settings)
#87840	Change the load destination address of the LOADER to the 64-bit address region.
#97962	Fix the issue do not restart by software reset by SystemWDT.
#86030	Add the report message to exception handling.
#99015	Change a path of #include header file to not use a related path.
#86022	Add the feature of Suspend to RAM.
#86509	Add the eMMC boot.
#97865	**[H/W Restriction No.23]** Update the QoS settings.

4.11 v1.0.9.10

Fix and add about following restrictions and functions.

No.	Description
#100382	Clean-up to the DDR setting code.

4.12 v1.0.10

This version branched from v1.0.9.
Fix and add about following restrictions and functions.

No.	Description
#103604	Change u-boot boot address to 0x50000000 from 0x49000000.

4.13 v1.0.11

Fix and add about following restrictions and functions.

No.	Description
#107771	Integrate v1.0.9.10 and v1.0.10 into v1.0.11.

4.14 v1.0.12

Fix and add about following restrictions and functions.

No.	Description
#99411	Update H3 Ver.1.0/Ver.1.1 QoS setting rev.0.33. Update M3 Ver.1.0 QoS setting rev.0.16.
#99473	Add binary compatible build option with H3 and M3.
#101134	Change conditions for applying security settings. (CR7 boot was excluded)
#103077	Organizing constants for the certificate header (SA6) of the dummy tools.
#104125	**[H/W Restriction No.65]** Fix workaround by RT-DMAC, for PFC write access problem.
#105357	Support 40bit address for Lossy area.
#105866	Fix build error in DEBUG case.
#108783	Version up the base version of arm-trusted-firmware. https://github.com/ARM-software/arm-trusted-firmware Commit ID 6bb37adc203567c2f9322dfbe34058a5f12d4c70 [Tag: v1.3]
#108711	Update the DRVCTRL register setting.
#108757	Fix algorithm for loading multiple non-secure target program images.
#109215	Fix protection range settings for the System RAM. (0xE6320000 -> 0xE6302000).
#110057	Add build option to select the OP-TEE loading.
#110100	Change the message. It calls attention to the user when hanging with DipSW setting mismatch (especially assuming SW 7 - pin 1),

4.15 v1.0.13

Fix and add about following restrictions and functions.

No.	Description
#110616	Fix the pointer arithmetic of Lossy code that pointed out by static code analysis tool.
#114766	Correspond to new memory map.
#112792	Fix the parameter of authentication API for H3 Ver.2.0.
#114333	Change to obtain lifecycle state from library function.
#112785	Change display format of the product version.
#113054	**[H/W Restriction No.82]** Clear SError in bl2 entrypoint.
#112484	Add the PFC setting for H3 Ver.2.0.
#114296	Add MFIS register setting.
#112483	Update DDR setting for H3 Ver.2.0.
#112482	Add the QoS setting for H3 Ver.2.0, update H3 Ver.1.1, Ver.1.0, M3.
#115944	BL2: reset: Enable generic counter and enable BL2 timestamps.
#116824	plat: rcar: Initialize console only for CA5x boot.
#117769	plat: renesas: rcar: Change of the board judgement.
#117895	Update DDR setting rev.0.22.
#117377	Update H3 v20 QoS setting rev.0.12.
#117298	Add distinction to board and change the setting of GenericCounter.
#115929	Change definition name of the PLL multiplication ratio setting (MD14, MD13).
#116084	Change Add build option for disable the PMIC related function.
#116706	Add check loading area for BL33 to BL338.
#117296	Fix SRAM protection range.
#117326	Fix if BL32 loading fails, stop BL2.

4.16 v1.0.14

Fix and add about following restrictions and functions.

No.	Description
#102234	Fixed the high-speed mode setting sequence for the eMMC.
#106706	Correspond to the eMMC boot using same boot partition as the Boot ROM.
#117377	Add the QoS setting for M3 Ver.1.1, update H3 Ver.1.1, H3 Ver.2.0.
#117709	Add Board name to serial log output.
#118918	plat: renesas: rcar: Add power off for Starter Kit. plat: renesas: rcar: Add ULCB CPLD support.
#102355	Fix the comments in source codes.
#107378	Correspond to make the SDHI (DMAC) specification change.
#109690	QAC pointed out correspondence.
#114878	Fix flush process of the Console FIFO.
#119078	Modify the System/Secure Module Stop Control Settings.
#119178	plat: io_rcar: Fix typos.
#119394	Ensure unique timestamps for multiple tf_printf() calls.
#119576	Modify version display of the M3 Ver.2.0 to "M3 Ver.1.1".
#119873	Update the QoS setting for H3 Ver.2.0, M3 Ver.1.1.
#120782	Delete debug code.
#120834	BL33x loadable range check does not work properly.

4.17 v1.0.15

Fix and add about following restrictions and functions.

No.	Description
#122536	**[H/W Restriction No.71 #9]** BL2: Disable TLB cache function of IPMMU caches.
#122541	Update the QoS setting for H3 Ver.1.0/1.1/2.0, M3 Ver.1.0/1.1.
#123541	Update DDR setting (rev0.23).
#123206	plat: rcar: ddr: Add missing PMIC_ON_BOARD macro.
#123212	plat: rcar: io storage: drv_policies is rw.
#123374	Change Timeout of eMMC.
#124005	Modify conflict by the IIC for DVFS processing.
#124730	Update H3 Ver.1.0 QoS setting rev.0.36. Update H3 Ver.1.1 QoS setting rev.0.37. Update H3 Ver.2.0 QoS setting rev.0.16. Update M3 Ver.1.0 QoS setting rev.0.19. Update M3 Ver.1.1 QoS setting rev.0.13.
#126475	Changed code comment on time measurement function using the TMU ch3.
#126911	Update DDR setting (rev0.24).
#127015	Change initial voltage setting for PMIC.

4.18 v1.0.16

Fix and add about following restrictions and functions.

No.	Description
#126556	Change CPG setting.
#128036	Update H3 Ver.2.0 QoS setting rev.0.17. Update M3 Ver.1.1 QoS setting rev.0.14.
#128037	Update DDR setting (rev0.25).
#128054	Fix typos (comments of execDMA).
#128344	Replace PMIC_ON_BOARD macro with some new macros that correspond to the function.
#128539	Changed the specification of the initial voltage setting for PMIC.
#130052	Modify the variable names and comments in dummy_create.
#130980	Add the board name for serial log output.
#132663	Update H3 Ver.2.0 QoS setting rev.0.18. Update M3 Ver.1.1 QoS setting rev.0.16.
#132664	Update DDR setting (rev0.27).
#133221	Modify return and unnecessary definition of scif.
#133355	Change the ARMREG register setting.

4.19 v1.0.17

Fix and add about following restrictions and functions.

No.	Description
#134933	Delete unnecessary register setting.
#138187	Update DDR setting (rev0.28rc03).
#138578	Add M3N Ver.1.0 QoS setting rev.0.03.
#138579	Add PFC setting for M3N.
#138580	Add CPG setting for M3N.
#138581	Change CA57DBGRCR and CA53DBGRCR setting.
#138583	Add M3N to product name display.
#138945	Change eMMC driving abilities for H3 and M3.
#140324	Change eMMC driving abilities for M3N.
#140401	Increased the loading size of BL2 in SA0.
#142666	Add build option for jump to LinuxKernel.
#143047	Update M3N Ver.1.0 QoS setting rev.0.04.
#143846	Update DDR setting (rev0.28).

4.20 v1.0.18

Fix and add about following restrictions and functions.

No.	Description
#138602	Add build option for enable to D-Cache.
#145028	Version up the base version to v1.4 of arm-trusted-firmware.
#145380	Update DDR setting (rev0.29).
#145382	Update H3 Ver.2.0 QoS setting rev.0.19. Update M3 Ver.1.1 QoS setting rev.0.17. Update M3N Ver.1.0 QoS setting rev.0.05.
#147942	Increased the loading size of BL32 in SA6.
#148068	Delete debug code.
#148069	Change literal to macro definition.
#148259	Add the cache operation (Invalidate of data cache).
#148774	**[H/W Restriction No.100]** Disable TLB cache function of IPMMU caches in M3N.
#148878	Fix D-Cache disable routine in BL2.
#148946	Fix console_flush function dose not called when warm boot.

4.21 v1.0.19

Fix and add about following restrictions and functions.

No.	Description
#153452	Add E3 to LSI option.
#153471	In case of E3, Change the size of SystemRAM from 384KB to 128KB.
#153473	Add E3 to the LSI display.
#153475	Add support Ebisu board.
#153476	Change HyperFlash clock display for E3.
#153481	Add CPG setting for E3.
#153482	Add PFC/GPIO setting for E3.
#153483	Change LifeC setting for E3.
#153491	Change the clock setting of SCIF2 according to the setting of MD12.
#153492	Change EXTAL clock for E3.
#153496	Change the eMMC channel for E3.
#153500	Add processing of Suspend To RAM for E3.
#153504	Add DDR setting for E3(rev0.06).
#153505	Add E3 Ver.1.0 QoS setting rev.0.02. Update M3N Ver.1.0 QoS setting rev.0.06.
#153758	**[H/W Restriction No.100]** Disable TLB cache function of IPMMU caches in E3.
#153882	Add support the dummy certificate of IPL for E3.
#153905	Add display the MD12 setting.
#154814	Fix the LSI_CUT judgement of PFC setting.
#156414	Change definition of end address of system ram for BL2.

4.22 v1.0.20

Fix and add about following restrictions and functions.

No.	Description
#159080	[H/W Restriction No.100] Disable TLB function on IPMMU-PV1 cache on H3 Ver.2.0.
#159566	Update DDR setting (rev.0.31).
#159685	Update H3 Ver.3.0 QoS setting rev.0.06.
#150645	Fix the IPL cannot load images to 40-bit address space with eMMC when D-Cache enables.
#156429	Add processing to read MSTP status into BL2.
#156434	Delete unnecessary register setting.
#157784	Add the SWTCNT setting of E3.
#161026	Change the unit of transfer size to 256 bytes for RPC, and improved DMA transfer processing.
#161030	Add DDR Memory Config log output.

4.23 v1.0.21

Fix and add about following restrictions and functions.

No.	Description
#163056	Fix a problem in parameter check of DMA driver.
#163935	Fix processing to check loadable area range.
#165816	Add processing of preserve the DRAM contents during a system reset.
#166160	Correct the definition name indicating LSI version.
#168077	Update DDR setting (rev.0.33).
#168078	Update H3 Ver.3.0 QoS setting rev.0.0.7
#169262	Fix processing to check propriety of DMA transfer by eMMC driver.
#169922	Add Ver.1.2 to version display of M3 Ver.1.1.

4.24 v1.0.22

Fix and add about following restrictions and functions.

No.	Description
#173825	Update CPG setting.
#174602	Add support Ebisu-4D board.
#179177	Change the timing to invalidate of instruction cache.
#179843	Fixed a bug in the exception handler.
#181599	Update DDR setting for E3(rev0.09).

4.25 v1.0.23

Fix and add about following restrictions and functions.

No.	Description
#171378	plat: rcar: BL2: Correct MMU configuration plat: rcar: Fix suspicious line in platform.mk
#174614	Update IPL boot message.
#174599	Change the definition value of BL2_LIMIT to end of System RAM.
#175691	Version up the base version to v1.5 of arm-trusted-firmware.
#184306	Update DDR setting (rev.0.34).
#186854	Modify the alignment of l2_tzram_layout to CACHE_WRITEBACK_GRANULE.
#186937	Update H3 Ver.3.0 QoS setting rev.0.08. Update M3N Ver.1.1 QoS setting rev.0.07. Update E3 Ver.1.0 QoS setting rev.0.03.
#187695	Fix the system WDT detection log is not output when D-Cache is enabled.
#187706	Change the timer counter of micro_wait to the Generic Timer.
#187734	Fix to log the timestamp at beginning of line.
#188692	Change the timer counter for processing time measurement to the Generic Timer.
#189516	Modify the DDR log output of IPL boot message.

4.26 v2.0.0

Fix and add about following restrictions and functions.

No.	Description
#189099	Update DDR setting for E3(rev0.11).
#189874	Change the condition of data transfer end of SCIF transfer.
#190677	Modify address area in the DDR memory config log output.
#191380	Update H3 Ver.2.0 QoS setting rev.0.20. Update H3 Ver.3.0 QoS setting rev.0.10. Update M3 Ver.1.1 QoS setting rev.0.18. Update M3N Ver.1.1 QoS setting rev.0.08. Update E3 Ver.1.0 QoS setting rev.0.05.
#191223	Modify load destination variable of the Cert Header to static.
#193407	**[H/W Restriction No.100]** Disable TLB function of IPMMU cache on E3 Ver.1.1. Disable TLB function of IPMMU-PV0 cache on E3 Ver.1.x.

4.27 v2.0.1

Fix and add about following restrictions and functions.

No.	Description
#197435	Add support for E3 Ver.1.1.
#197445	Add support for M3 Ver.1.3/3.0.
#202611	Add DDR setting for M3 Ver.3.0.
#202611	Add QoS setting for M3 Ver.3.0.

4.28 v2.0.2

Fix and add about following restrictions and functions.

No.	Description
#206891	Change periodic write DQ training option.
#209051	Add new board revision for H3ULCB.
#208548	Remove duplicate line in qos.mk.
#209224	Change subslot cycle.
#209214	Update DDR setting rev.0.35.

4.29 v2.0.3

No update. Only BL31 update.

4.30 v2.0.4

Fix and add about following restrictions and functions.

No.	Description
#206891	Clean-up to the DDR setting code for H3, M3 and M3N.
#218148	Update DDR setting rev.0.36 for H3, M3 and M3N.
#218147	Clean-up to the DDR sub function code.
#218192	Clean-up to the PFC setting code for H3, M3 and M3N.
#216956	Modify PFC code.
#217963	Change RPC PHY calibration setting.
#218147	Clean-up to the DDR setting code for E3.
#218146	Update DDR setting rev.0.12 for E3.
#218138	Clean-up to the QoS setting code.
#197435	Update M3 Ver.3.0 QoS setting rev.0.03.
#223097	Update M3 Ver.3.0 QoS setting rev.0.04.
#224074	Update DDR setting rev.0.37 for H3, M3 and M3N.

4.31 v2.0.5

Fix and add about following restrictions and functions.

No.	Description
#240418	Fixed the issue that image certification is success despite certifying with certificate for another image.

4.32 v2.0.6

Fix and add about following restrictions and functions.

No.	Description
#231341	Update DDR setting rev.0.38 for H3, M3 and M3N.
#241525	Add the M3-W Ver.3.0/SIP Starter Kit.
#243451	Update DDR setting rev.0.39 for H3, M3 and M3N.
#247734	Update DDR setting rev.0.40 for H3, M3 and M3N.

4.33 v3.0.0

Fix and add about following restrictions and functions.

No.	Description
#285917	rcar_gen3: Version up the base version of Trusted Firmawre-A from v1.5 to v2.3 https://github.com/ARM-software/arm-trusted-firmware Commit ID 8ff55a9e14a23d7c7f89f52465bcc6307850aa33 [Tag: v2.3]
#285917	rcar_gen3: plat: BL2: Add check process of the data section size
#285917	rcar_gen3: plat: BL2: Change MMU configurations
#285917	rcar_gen3: plat: BL2: Update DDR setting for H3, M3, M3N
#285917	rcar_gen3: plat: BL2: Change the memory map for OP-TEE
#297028	rcar_gen3: drivers: ddr: Add function to judge a DDR rank
#299128	rcar_gen3: plat: Fix a memory type
#300079	rcar_gen3: plat: Add DRAM size judgment by PRR register
#300079	rcar_gen3: plat: Add a DRAM size setting for M3N
#300079	rcar_gen3: plat: Delete FDT function calls

4.34 v3.0.1

Fix and add about following restrictions and functions.

No.	Description
#310490	rcar-gen3: plat: BL2: Modify SWDT counter setting for R-Car D3
#310490	rcar-gen3: plat: BL2: Update DDR setting for R-Car D3
#310490	rcar-gen3: plat: BL2: Remove access to RMSTPCRn registers in R-Car D3
#310490	rcar-gen3: plat: BL2: Add process of SSCG setting for R-Car D3
#310490	rcar-gen3: plat: BL2: Fix version judgment for R-Car D3
#310490	rcar-gen3: plat: BL2: Fix build error when PMIC_ROHM_BD9571 option is OFF(0)
#310490	rcar-gen3: plat: BL2: Modify LifeC register setting for R-Car D3
#304368	rcar-gen3: plat: BL2: Add TCR_EL1 clearing at the entry point of BL2
#314057	rcar-gen3: plat: BL2: Fix to support of booting from eMMC for R-Car D3

4.35 v3.0.2

Fix and add about following restrictions and functions.

No.	Description
#319375	rcar-gen3: plat: BL2: Fix to error if image load size is zero
#327370	rcar-gen3: plat: BL2: Fix cache maintenance process of reading cert header
#318481	rcar_gen3: plat: Update IPL and Secure Monitor Rev.3.0.2
#318481	rcar-gen3: plat: Fix source file to make about GICv2
#300079	rcar_gen3: plat: Generate two memory nodes for larger than 2 GiB channel 0
#300079	rcar_gen3: plat: Factor out DT memory node generation
#300079	rcar_gen3: plat: Fix DRAM size judgment by PRR register
#300079	Revert "rcar_gen3: plat: Delete FDT function calls"
#322396	rcar_gen3: plat: BL2: Fix disabling MFIS write protection for RCar-D3
#314059	rcar-gen3: plat: BL2: Enable SPI interrupts for BL2 SWDT
#299300	rcar-gen3: plat: BL2: Fix to load image when option BL2_DCACHE_ENABLE is enabled
#318481	rcar_gen3: plat: BL31: Update make file in response to version upgrade

4.36 v3.0.3

Fix about following functions.

No.	Description
#342838	rcar-gen3: plat: BL2: Fix load address range check

5. Confirming the execution software components

When you confirm executing Initial Program Loader, please follow the documents [3] .
The hardware environment is below.

- SoC
  R-Car H3/M3/M3N/E3/D3
- Board
  System Evaluation Board "Salvator-X"
  System Evaluation Board "Salvator-XS"
  System Evaluation Board "Ebisu"
  System Evaluation Board "Ebisu-4D"
  System Evaluation Board "Draak"

6. Restrictions

There is no restriction in this revision.

REVISION HISTORY	Initial Program Loader Release Note: Software

Rev.	Date	Description	
		Page	Summary
1.0.0	Sep. 30, 2015	—	New creation.
1.0.1	Nov. 23, 2015	1	1.2 References Updated Linux Interface Specification Yocto recipe Start-Up Guide has updated.
		3	3.Changes between previous revision Updated changes between previous revision.
1.0.2	Dec. 07, 2015	3	3.Change History (rename from “3.Change between previous revision”) 3.3 add history of v1.0.2.
1.0.3	Feb. 12, 2016	3	3.Change History 3.4 add history of v1.0.3.
1.0.4	Feb. 23, 2016	3	3.Change History 3.5 add history of v1.0.4.
1.0.5	Mar. 25, 2016	2	2.Component 2.3. Initial clock setting Added the Initial clock setting information.
		4	3.Change History 3.6 add history of v1.0.5.
		6	5.Restrictions Updated the description of the contents are not supported in this revision.
1.0.6	Apr. 27, 2016	1	1.1 Objectives Added platform ‘M3’. 1.2 References Updated Linux Interface Specification Yocto recipe Start-Up Guide has updated. Add Initial Program Loader User's Manual.
		2	2.1 Software components 2.2 Software Added platform ‘M3’.
		3	2.3. Initial clock setting Added the Initial clock setting information of R-Car M3.
		5	3.Change History 3.7 add history of v1.0.6.
		6	4.Confirming the execution software components Add platform ‘M3’.
		7	5.Restrictions Added restriction about DRAM split setting and option of LOG_LEVEL.
1.0.7	May 27, 2016	1	1.2 References Add description about revision of the references.
		3	2.3. Initial clock setting Changed LPDDR4-SDRAM information of R-Car M3.
		5	3.Change History 3.8 add history of v1.0.7.
		7	5.Restrictions Deleted restriction about DRAM split setting.
1.0.8	Jun. 30, 2016	6	3.Change History 3.8 add history of v1.0.8.
		8	5.Restrictions Removed a restriction in this revision (4).
1.0.9	Aug. 29, 2016	6	3.Change History 3.9 add history of v1.0.9.
		8	5.Restrictions Removed a restriction in this revision.
1.0.9.10	Nov. 2, 2016	6	3.Change History 3.10 add history of v1.0.9.10.
1.0.10	Oct. 26, 2016	7	3.Change History

			3.11 add history of v1.0.10.
1.0.11	Nov. 22, 2016	7	3.Change History 3.12 add history of v1.0.11.
1.0.12	Dec. 22, 2016	7	3.Change History 3.13 add history of v1.0.12.
1.0.13	Mar. 15, 2017	2,3	2.3 Initial Clock setting Changed "R-Car H3 WS" to "R-Car H3 Ver." Added the Initial clock setting information of R-Car H3 Ver.2.0.
		8	3.Change History 3.13 add history of v1.0.13.
1.0.14	Apr. 10, 2017	2,3	2.3 Initial Clock setting Changed to 2.3.4 R-Car M3 Ver.1.0 / Ver.1.1 from 2.3.4 R-Car M3.
		9	3.Change History 3.16 add history of v1.0.14.
		10	4. Confirming the execution software components Added the "Salvator-XS" board.
1.0.15	Jun. 14, 2017	9	3.Change History 3.17 add history of v1.0.15.
1.0.16	Aug. 24, 2017	—	Fixed the format of the document (trademark, etc.)
		10	3.Change History 3.18 add history of v1.0.16.
1.0.17	Nov. 14, 2017	—	R-Car M3N support.
		3	2.3 Initial Clock setting Added the Initial clock setting information of R-Car M3N Ver.1.0.
		10	3.Change History 3.19 add history of v1.0.17.
1.0.18	Jan. 12, 2018	11	3.Change History 3.20 add history of v1.0.18.
		13	5.Restrictions Added restriction on image loading in eMMC boot when D-Cache is enabled.
1.0.19	Mar. 14, 2018	—	R-Car E3 support.
		3	2.3 Initial Clock setting Added the Initial clock setting information of R-Car E3 Ver.1.0.
		11	3.Change History 3.21 add history of v1.0.19.
		12	4. Confirming the execution software components Added the "Ebisu" board of E3.
1.0.20	Apr. 11, 2018	3	2.3 Initial Clock setting 2.3.3 R-Car H3 Ver.2.0 / Ver.3.0 Added the R-Car H3 Ver.3.0.
		12	3.Change History 3.22 add history of v1.0.20.
		14	5.Restrictions Removed a restriction in revision 1.0.18. Added restriction on image loading.
1.0.21	Jun. 11, 2018	3	2.3 Initial Clock setting 2.3.4 R-Car M3 Ver.1.0 / Ver.1.1 / Ver.1.2 Added the R-Car M3 Ver.1.2.
		12	3.Change History 3.23 add history of v1.0.21.
		14	5.Restrictions Removed a restriction in revision 1.0.20.
1.0.22	Sep. 3, 2018	12	3.Change History 3.24 add history of v1.0.22.

1.0.23	Oct. 12, 2018	2	2.1 Software components Removed the BL1 AP Trusted ROM in Figure 1.
		13	3.Change History 3.25 add history of v1.0.23.
		14	4.Confirming the execution software components Added the "Ebisu-4D" board of E3.
2.0.0	Nov. 26, 2018	—	Fixed the format of the document (Address List.)
		13	3.Change History 3.26 add and updated the history of v2.0.0.
2.0.1	Feb. 15, 2019	13	2.3 Initial Clock setting Added the Initial clock setting information of R-Car M3 Ver.1.3/3.0 and E3 Ver.1.1. 3.Change History 3.27 add history of v2.0.1. Update restrictions.
2.0.2	Mar. 11, 2019	13	3.Change History 3.28 add history of v2.0.2.
2.0.3	Mar. 22, 2019	-	Updated only BL31 software.
2.0.4	Jul. 12, 2019	14	3.Change History 3.30 add history of v2.0.4.
2.0.5	Dec. 13, 2019	15	3.Change History 3.31 add history of v2.0.5.
2.0.6	Feb. 7, 2020	15	3.Change History 3.32 add history of v2.0.6.
3.0.0	Dec. 9, 2020	2 3	Changed the software name from ARM Trusted Firmware to Trusted Firmware-A. Removed the description of older versions H3 Ver.1.0/1.1 and M3 Ver.1.0/1.1.
		15	3.Change History 3.33 add history of v3.0.0.
		17	5.Restrictions Added the description that RCAR_BL2_DCACHE=1 is not supported.
3.0.1	Apr. 6, 2021	—	R-Car D3 support.
		3	2.3 Initial Clock setting Added the Initial clock setting information of R-Car D3 Ver.1.0/1.1.
		15	3.Change History 3.34 add history of v3.0.1.
		16	4.Confirming the execution software components Added the "Draak" board of D3.
3.0.2	Aug. 16, 2021	-	Add information of Gen3e.
		1	1.2 References Added new reference documents about Arm CA53/57 Errata.
		4	3. Arm CA53/57 Errata List Add new chapter Arm CA53/57 Errata List.
		17	4.Change History 4.35 add history of v3.0.2.

		19	5.Restrictions Removed the description that RCAR_BL2_DCACHE=1 is not supported.
3.0.3	Dec. 01, 2021	17	4. Change History 4.36 add history of v3.0.3.

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Colophon 7.0

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Initial Program Loader
Release Note

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