Preliminary

R-CarH3-SiP System Evaluation Board "Salvator-X"

RTP0RC7795SEB00010S

Rev.0.08

Preliminary

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Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.08
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R-CarH3_Sipのシンボルは
「R-CarH3SiP基板設計仕様書_r1.00（BGA_Rev.0.0096）」にて作成。

Layout Note:
Following signals need Ground guard.

AUDIO_CLKA
AUDIO_CLKB
AUDIO_CLKC

AUDIO_CLKOUT
AUDIO_CLKOUT3
SCIF_CLK, SCIF_CLK until X1-pin3

SD0_CLK_V,SD0_CLK_SOC
SD3_CLK_V,SD3_CLK_SOC
MMC0_CLK_V,MMC0_CLK_SOC

AVB_TXCREFCLK
AVB_TXC_25
AVB_RXC_25

QSPI0_SPCLK_18, QSPI0_SPCLK_sw
QSPI1_SPCLK_18, QSPI1_SPCLK_sw

VTHSENSE0_18 until TH1
VTHREF0_18 until TH2

U1A

SRU(3.3V)

<21,23> AUDIO_CLKA — AB38 AUDIO_CLKA_A
<21,23> AUDIO_CLKB — A34 GP5_12/HSCK0/AUDIO_CLKB_A
<19> AUDIO_CLKC — C39 GP5_21/MSIOF0_SS2/AUDIO_CLKC_A
<21> AUDIO_CLKOUT — G37 GP5_18/MSIOF0_SYNC/AUDIO_CLKOUT_A
<21,23> AUDIO_CLKOUT3 — B39 GP5_19/MSIOF0_SS1/AUDIO_CLKOUT3_A

SSI(3.3V)

<21,23> SSI_SCK0129 — M39 SSI_SCK0129
<21,23> SSI_WS0129 — J37 SSI_WS0129
<21,23> SSI_SDATA0 — K37 SSI_SDATA0
<21,23> SSI_SDATA1 — L37 SSI_SDATA1_A

<19,23> SSI_SCK4 — P39 GP6_08/SSI_SCK4
<19,23> SSI_WS4 — T37 GP6_09/SSI_WS4
<19,23> SSI_SDATA4 — P38 GP6_10/SSI_SDATA4

SCIF(3.3V)

D3.3V — C1 0.1uF 1005 10V
X1 NZ2520SB[14.7456MHz/50ppm] (4 VCC, 1 STn, 2 GND, 3 OUT)
SERIES_TERM: R1 0 — SCIF_CLK — AB39 GP6_23/AUDIO_CLKB_B/SCIF_CLK_A

<22> SCIF2_TXD — F38 GP5_10/TX2_A
<22> SCIF2_RXD — F39 GP5_11/RX2_A

SDHI0/DBG2(3.3V/1.8V)

Note: "SD0_WP"and "SD0_CD" signal is fixed at 3.3V.

SDHI0 (CLK,CMD,DAT[3:0])
(1) Matched trace length.

<14> SD0_WP — D29 SD0_WP
<14> SD0_CD — D30 SD0_CD
<14> SD0_DAT3_V — D31 SD0_DAT3/ASEBRK2
<14> SD0_DAT2_V — D32 SD0_DAT2/TDI2
<14> SD0_DAT1_V — C31 SD0_DAT1/TMS2
<14> SD0_DAT0_V — B31 SD0_DAT0/TCK2
<14> SD0_CMD_V — A31 SD0_CMD/TRST2_N
<14> SD0_CLK_V — R3 1005 22 SD0_CLK_SOC — A30 SD0_CLK/TDO2

3.3V
3.3V
3.3V/1.8V

SDHI3(3.3V/1.8V)

Note: "SD3_WP"and "SD3_CD" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD3.

SDHI3 (CLK,CMD,DAT[3:0])
(1) Matched trace length.

<14,23> GP4_16/SD3_DAT7/WP_V — D20 GP4_16/SD3_DAT7/SD3_WP
<14,23> GP4_15/SD3_DAT6/CD_V — D21 GP4_15/SD3_DAT6/SD3_CD
<14,23> SD3_DAT3_V — A21 GP4_12/SD3_DAT3
<14,23> SD3_DAT2_V — C23 GP4_11/SD3_DAT2
<14,23> SD3_DAT1_V — B23 GP4_10/SD3_DAT1
<14,23> SD3_DAT0_V — A23 GP4_09/SD3_DAT0
<14,23> SD3_CMD_V — C20 GP4_08/SD3_CMD
<14,23> SD3_CLK_V — R8 1005 22 SD3_CLK_SOC — A24 GP4_07/SD3_CLK

3.3V/1.8V

MMC(3.3V/1.8V)_[SDHI1,2]

MMC (CLK,CMD,DAT[7:0])
(1) Matched trace length.

<15> MMC0_DTA7_V — D27 GP3_11/SD1_DAT3/SD2_DAT7
<15> MMC0_DTA6_V — C27 GP3_10/SD1_DAT2/SD2_DAT6
<15> MMC0_DTA5_V — B27 GP3_09/SD1_DAT1/SD2_DAT5
<15> MMC0_DTA4_V — A27 GP3_08/SD1_DAT0/SD2_DAT4
<15> MMC0_DTA3_V — D23 GP4_05/SD2_DAT3
<15> MMC0_DTA2_V — D24 GP4_04/SD2_DAT2
<15> MMC0_DTA1_V — C25 GP4_03/SD2_DAT1
<15> MMC0_DTA0_V — D26 GP4_02/SD2_DAT0
<15> MMC0_CMD_V — A25 GP4_01/SD2_CMD
<15> MMC0_CLK_V — R9 1005 22 MMC0_CLK_SOC — A26 GP4_00/SD2_CLK
<15> MMC0_DS_V — B25 GP4_06/SD2_DS

3.3V/1.8V

GPIO

Note: "SD3_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD3.

GPIO_Unused(1.8V/3.3V)

<23> GP4_13/SD3_DAT4_V — B21 GP4_13/SD3_DAT4
<23> GP4_14/SD3_DAT5_V — C21 GP4_14/SD3_DAT5
<23> GP4_17/SD3_DS_V — C22 GP4_17/SD3_DS

Note: "SD1_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD1.

GPIO_Unused(1.8V/3.3V)

<23> GP3_06/SD1_CLK_V — A28 GP3_06/SD1_CLK
<23> GP3_07/SD1_CMD_V — A29 GP3_07/SD1_CMD

GPIO_Unused(3.3V)

<23> GP6_04 — M37 GP6_04/SSI_SDATA2_A
<23> GP6_21 — V36 GP6_21/SSI_SDATA9_A

GPIO_PU

<10,23> GP6_17/SSI_SCK78 — U39 GP6_17/SSI_SCK78
<10,23> GP6_18/SSI_WS78 — U37 GP6_18/SSI_WS78
<10,23> GP6_19/SSI_SDATA7 — V39 GP6_19/SSI_SDATA7
<10,23> GP6_20/SSI_SDATA8 — V37 GP6_20/SSI_SDATA8

D3.3V — R15 10k 1005

<10> GP5_13/HRX0 — D39 GP5_13/HRX0
<10> GP5_14/HTX0 — D38 GP5_14/HTX0
<10> GP5_15/HCTS0n — C38 GP5_15/HCTS0#
<10> GP5_16/HRTS0n — G38 GP5_16/HRTS0#

<10> GP5_24/MLB_SIG — J39 GP5_24/MLB_SIG
<10> GP5_25/MLB/IOEX_INTn — J38 GP5_25/MLB_DAT

R-CarH3SiP
H3SIP_BGA_r0096_003

EtherAVB

2.5V
AVB_RX_CTL — A16 AVB_RX_CTL_25 <20>
AVB_RXC — B19 AVB_RXC_25 <20>
AVB_RD0 — A13 AVB_RD0_25 <20>
AVB_RD1 — B13 AVB_RD1_25 <20>
AVB_RD2 — A14 AVB_RD2_25 <20>
AVB_RD3 — B14 AVB_RD3_25 <20>

R724~R729:Close to U1(H3SiP)

2.5V
AVB_TX_CTL — A8 R724 1005 24.9 1% — AVB_TX_CTL_25 <20>
AVB_TXC — A19 R725 1005 24.9 1% — AVB_TXC_25 <20>
AVB_TD0 — A18 R726 1005 24.9 1% — AVB_TD0_25 <20>
AVB_TD1 — B18 R727 1005 24.9 1% — AVB_TD1_25 <20>
AVB_TD2 — A17 R728 1005 24.9 1% — AVB_TD2_25 <20>
AVB_TD3 — B17 R729 1005 24.9 1% — AVB_TD3_25 <20>

3.3V
AVB_TXCREFCLK — A12 AVB_TXCREFCLK <20>
AVB_MDIO — A9 AVB_MDIO <20>
AVB_MDC — A15 AVB_MDC <20>
GP2_10/AVB_MAGIC — B15 GP2_10/PHY_RESETn <20>
AVB_PHY_INT — B16 AVB_PHY_INT <20>
AVB_LINK — B9 AVB_LINK <20>
AVB_AVTP_MATCH_A[wired or SCL5] — B11 AVB_AVTP_MATCH <20>
AVB_AVTP_CAPTURE_A[wired or SDA5] — A11 AVB_AVTP_CAPTURE <20>

QSPI(1.8V)

PCB配線注意事項
シンボル内点線内の信号（QSPI_xxxxxx_FLASH）は、
SW1,SW2近くで接続のこと。

QSPI0_SPCLK — W3 QSPI0_SPCLK_18
QSPI0_SSL — Y3 QSPI0_SSL_18
QSPI0_MOSI/IO0 — AC5 QSPI0_MOSI_IO0_18
QSPI0_MISO/IO1 — AB4 QSPI0_MISO_IO1_18
QSPI0_IO2 — Y6 QSPI0_IO2_18
QSPI0_IO3 — AB6 QSPI0_IO3_18

SW1_CHS-06A
QSPI0_SPCLK_sw <9>
QSPI0_SSL_sw <9>
QSPI0_MOSI_IO0_sw <9>
QSPI0_MISO_IO1_sw <9>
QSPI0_IO2_sw <9>
QSPI0_IO3_sw <9>

QSPI1_SPCLK — V3 QSPI1_SPCLK_18
QSPI1_SSL — V5 QSPI1_SSL_18
QSPI1_MOSI/IO0 — AC7 QSPI1_MOSI_IO0_18
QSPI1_MISO/IO1 — AE5 QSPI1_MISO_IO1_18
QSPI1_IO2 — AE4 QSPI1_IO2_18
QSPI1_IO3 — AC3 QSPI1_IO3_18

SW2_CHS-06A
QSPI1_SPCLK_sw <9>
QSPI1_SSL_sw <9>
QSPI1_MOSI_IO0_sw <9>
QSPI1_MISO_IO1_sw <9>
QSPI1_IO2_sw <9>
QSPI1_IO3_sw <9>

RPC_INT# — Y7
RPC_WP# — V6
RPC_RESET# — V7

Do not stuff.
R604 0* 1005

D1.8V — R2 10k 1005 — SW3 CHS-01A

QSPI0_SPCLK_FLASH — W4
QSPI0_SSL_FLASH — AA3
QSPI0_MOSI_IO0_FLASH — AB5
QSPI0_MISO_IO1_FLASH — AC4
QSPI0_IO2_FLASH — AA6
QSPI0_IO3_FLASH — AC6

Do not stuff

QSPI1_SPCLK_FLASH — V4
QSPI1_SSL_FLASH — W5
QSPI1_MOSI_IO0_FLASH — AB7
QSPI1_MISO_IO1_FLASH — AD5
QSPI1_IO2_FLASH — AD4
QSPI1_IO3_FLASH — AB3

D1.8V — R4 10k 1005; R5 10k* 1005; R6 10k 1005; R7 10k 1005

RPC_INT_N_FLASH — AA7
RPC_WP_N_FLASH — W6
RPC_RESET_N_FLASH — W7
RSTO_N_FLASH — Y4

T.SENSE(1.8V)

Matched trace length.
Trace like as differential pair.

VTHSENSE0 — AF4 VTHSENSE0_18 — C2 0.1uF 1005 10V — TH1 VTHSENSE
VTHREF0 — AG4 VTHREF0_18 — C3 0.1uF 1005 10V — TH2 VTHREF

After tying the GND side of both Cx and Cx, tie to the internal GND plane.

(3.3V) SDHI_PW

GP5_00/SCK0 — K39 GP5_00/SD0_PWEN <14>
GP5_01/RX0 — A35 GP5_01/SD0_PWSEL <25>
GP5_02/TX0 — B35 GP5_02/SD3_PWEN <14>
GP5_03/CTS0# — F37 GP5_03/SD3_PWSEL <25>
GP5_04/RTS0#/TANS — G39 GP5_04/SD1_PWSEL <25>
GP5_09/SCK2 — L39 GP5_09/SD2_PWSEL <25>

LVDS_bklight_Cnt

GP6_07/SSI_SDATA3 — N37 GP6_07/LVDS_BLEN <18,23>

SoftSW

D3.3V — R10 100k 1005

GP5_17/MSIOF0_SCK — A38 GP5_17/SOFTSW0
GP5_20/MSIOF0_TXD — A37 GP5_20/SOFTSW1
GP5_22/MSIOF0_RXD — B37 GP5_22/SOFTSW2
GP5_23/MLB_CLK — AA39 GP5_23/MLB/SOFTSW3 <10>

GP5_17/SOFTSW0 — CP1 MSIOF_SCK
GP5_20/SOFTSW1 — CP2 MSIOF_TXD
GP5_22/SOFTSW2 — CP3 MSIOF_RXD
AUDIO_CLKOUT — CP4 MSIOF_SYNC

SW4 CHS-04A
GP5_17/SOFTSW0 — R11 2k 1005
GP5_20/SOFTSW1 — R12 2k 1005
GP5_22/SOFTSW2 — R13 2k 1005
GP5_23/MLB/SOFTSW3 — R14 2k 1005

LED/TactSW

GP6_11/SSI_SCK5 — R39 GP6_11/GP_LED/TSW0 <22,23>
GP6_12/SSI_WS5 — R37 GP6_12/GP_LED/TSW1 <22,23>
GP6_13/SSI_SDATA5 — P37 GP6_13/GP_LED/TSW2 <22,23>

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R-CarH3 SDHI/QSPI

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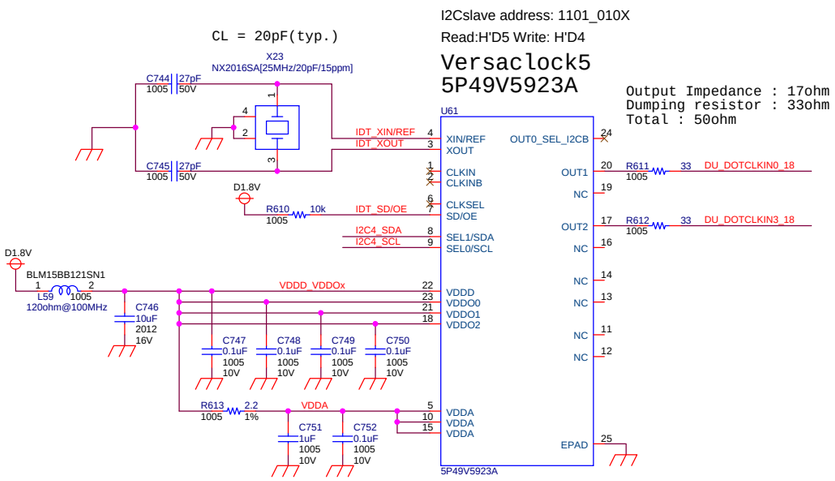

I2Cslave address: 1101_010X
Read:H'D5 Write: H'D4

Versaclock5
5P49V5923A

Output Impedance : 17ohm
Dumping resistor : 33ohm
Total : 50ohm

Note.
1. Set OEn bit to output clock.
2. I2C is 3.3V signal.
3. C752(0.10uF) is for pin 5

Versaclock5 have Internal Pull-down Resistor(100k-300k)
CLKIN
CLKINB
SEL1/SDA
SEL0/SCL
OUT0_SEL_I2CB --> 0 = Use I2C (Default)
CLKSEL --> 0 = XIN/REF, XOUT (Default)
1 = CLKIN, CLKINB
SD/OE --> = OE and active low

Layout Note:
Following signals need Ground guard.

DU_DOTCLKIN0_18
DU_DOTCLKIN0_18 until U61-pin20
DU_DOTCLKIN1_18
DU_DOTCLKIN1_18 until X21-pin3
DU_DOTCLKIN2_18
DU_DOTCLKIN2_18 until X22-pin3
DU_DOTCLKIN3_18
DU_DOTCLKIN3_18 until U61-pin17
XTAL_18, EXTAL_18 until X4-pin3

EXT_LPO
EXTALR_SOC, EXTALR_SOC until X5-pin3,

CLKOUT_SOC,CLKOUT

TCK_18

WE0n [CAN_CLK(40MHz)]

Be carefull !!
See Pin Assignment.

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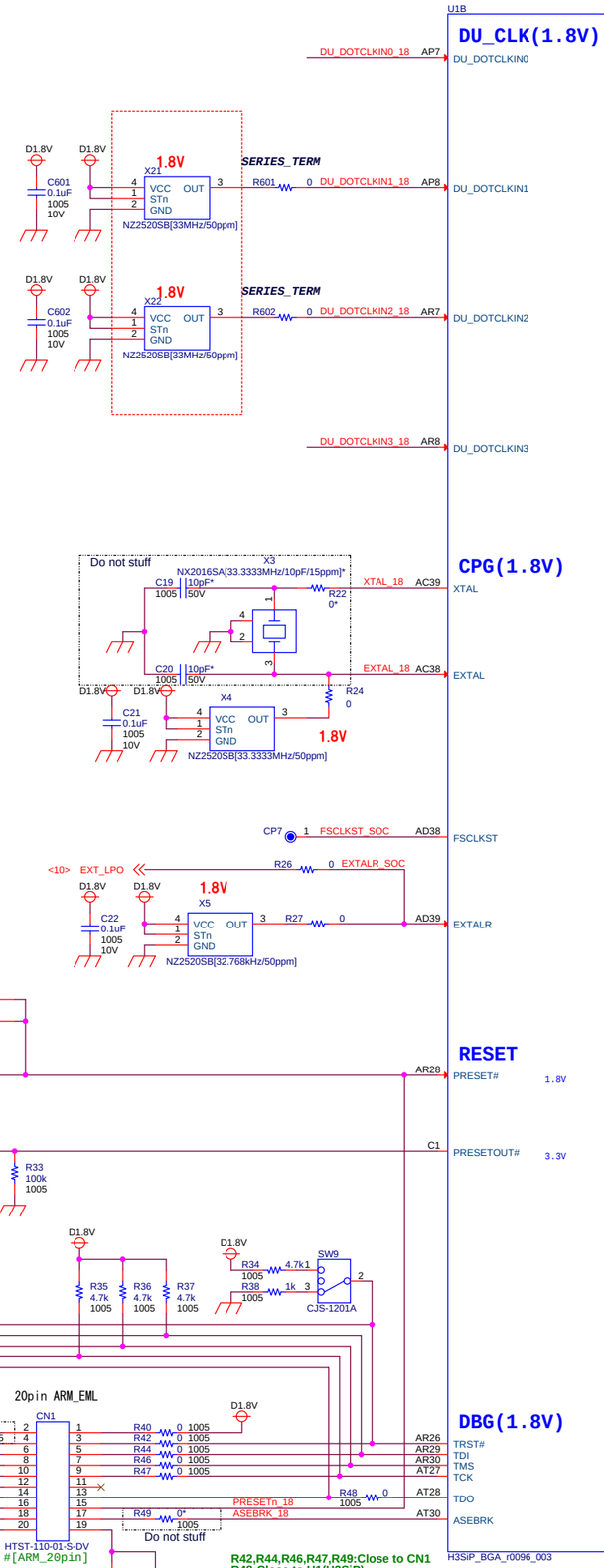

R-CarH3 DU/LBSC

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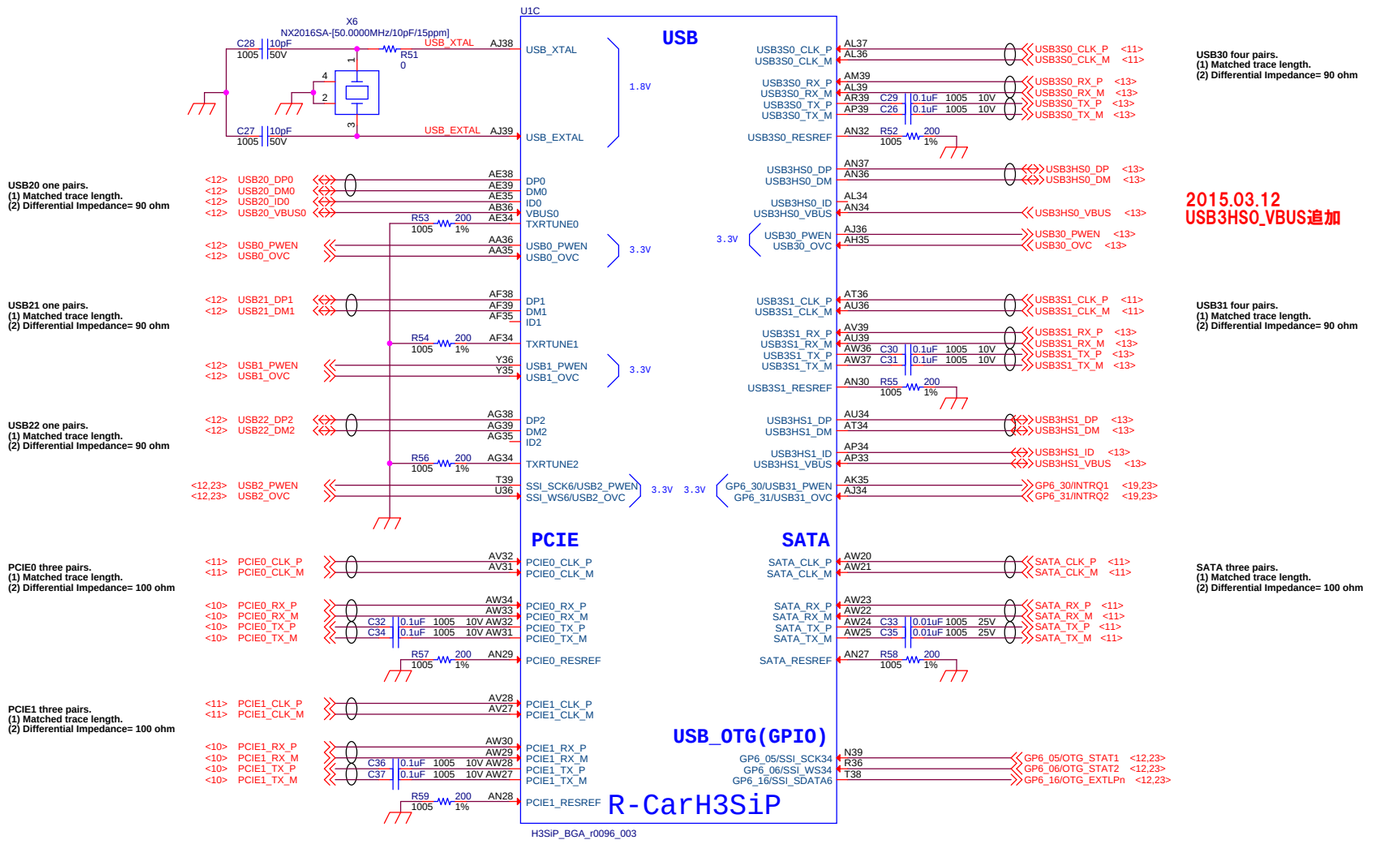
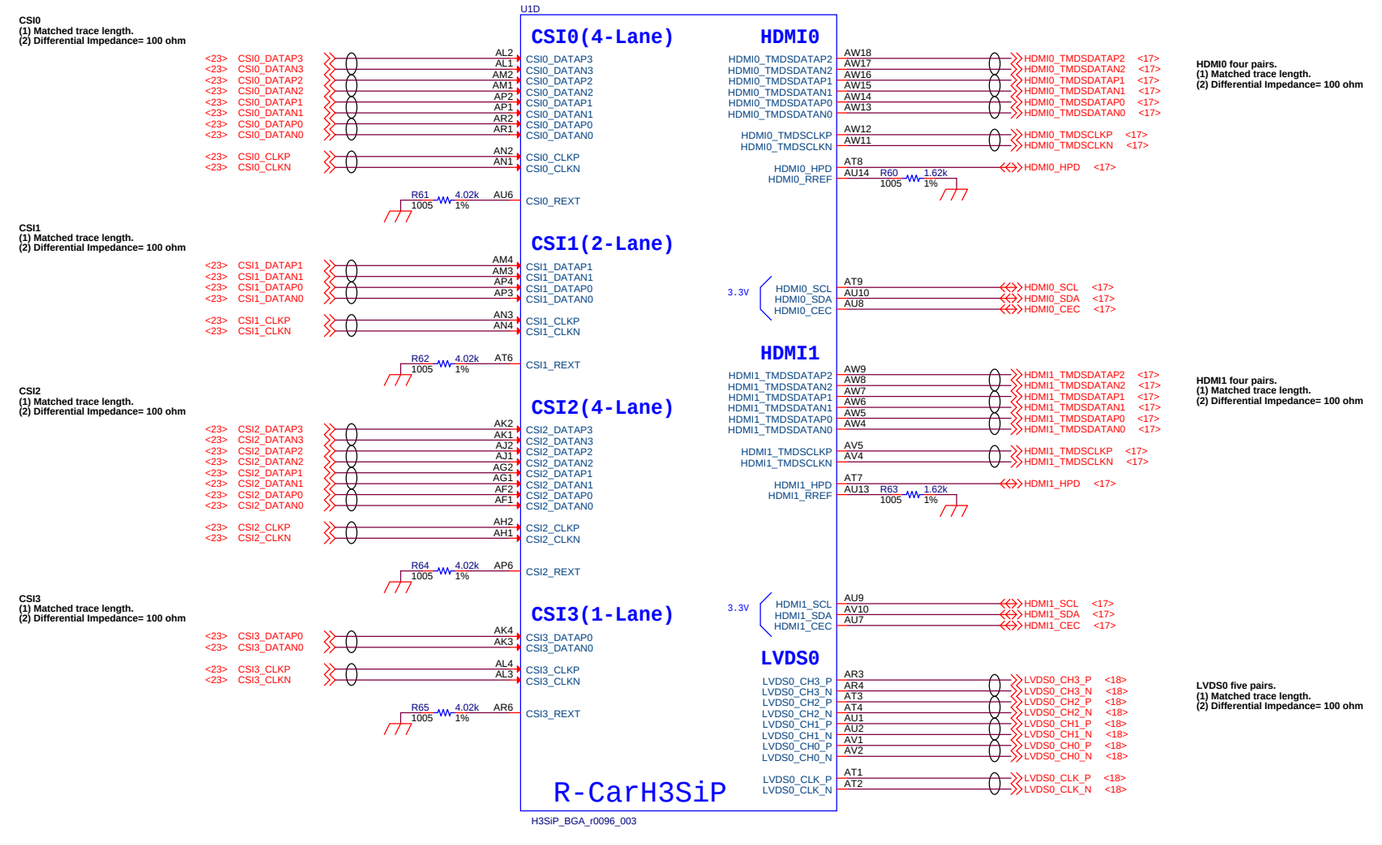
Layout Note:
Following signals need Ground guard.

USB_XTAL, USB_EXTAL
GP6_30/INTRQ1 [AUDIO_CLKOUT2_B(50MHz)]
GP6_31/INTRQ2 [AUDIO_CLKOUT3_B(50MHz)]





TXRTUNEn (n=0,1,2)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
USB3Sn_RESREF (n=0,1)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
PCIEn_RESREF (n=0,1)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
SATA_RESREF
Pull-down(GND) : 200ohm +-1% 100ppm/°C
CSIn_REXT (n=0-3)
Pull-down(GND) : 4.02kohm
HDMIn_RREF (n=0,1)
Pull-down(GND) : 1620ohm +-1%

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R-CarH3 USB/HDMI

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Out of U1 / Back of U1

U1J

D1.8V
C792 1uF 1005 10V
C793 0.1uF 1005 10V
C41 0.01uF 1005 25V
C794 1uF 1005 10V
C795 0.1uF 1005 10V
C61 0.01uF 1005 25V
VDD0.8V
C797 1uF 1005 10V
C798 0.1uF 1005 10V
C46 0.01uF 1005 25V
VDD0.8V
C801 1uF 1005 10V
C802 0.1uF 1005 10V
C58 0.01uF 1005 25V

AT11 VDDQ18_CSI0
AR10 VDDQ18_CSI1
AT10 VDDQ18_CSI2
AR9 VDDQ18_CSI3
AP11 VDDQ09_CSI0
AR11 VDDQ09_CSI1
AP10 VDDQ09_CSI2
AP9 VDDQ09_CSI3

D1.8V
C89 0.1uF 1005 10V
VDD0.8V
C92 0.1uF 1005 10V
AT12 VDDQ18_LVDS
AP13 VDDQ09_LVDS

VLDO_2.5V
C97 0.1uF 1005 10V
C19 D19 VDDQ25_ETH

R-CarH3SiP
H3SiP_BGA_r0096_003

Out of U1 / Back of U1

U1H

D3.3V
L3 1.0uH 1608 5%
VDD0.8V
C800 0.1uF 1005 10V
C50 2.2uF 1608 10V
C52 0.01uF 1005 25V
C38 0.1uF 1005 10V
VDD33_SATA
AT16 VDD33_SATA
AP17 VDD09_SATA

D3.3V
L4 1.0uH 1608 5%
D3.3V
L5 1.0uH 1608 5%
VDD0.8V
C796 0.1uF 1005 10V
C63 2.2uF 1608 10V
C55 2.2uF 1608 10V
C44 0.01uF 1005 25V
C64 0.1uF 1005 10V
C56 0.1uF 1005 10V
VDD33_PCIE0
VDD33_PCIE1
AT18 VDD33_PCIE0
AT17 VDD33_PCIE1
AR18 VDD09_PCIE0
AP18 VDD09_PCIE1

D3.3V
L6 1.0uH 1608 5%
D3.3V
L8 1.0uH 1608 5%
VDD0.8V
C799 0.1uF 1005 10V
C93 2.2uF 1608 10V
C69 2.2uF 1608 10V
C74 0.01uF 1005 25V
C94 0.1uF 1005 10V
C49 0.1uF 1005 10V
VDD33_USB30
VDD33_USB31
AR22 VDD33_USB30
AT20 VDD33_USB31
AR20 VDD09_USB30
AR19 VDD09_USB31

D3.3V
D3.3V
C803 4.7uF 2012 25V
C804 4.7uF 2012 25V
C102 0.01uF 1005 25V
C80 0.01uF 1005 25V
AU22 VDDQ33_USB3HS0
AU19 VDDQ33_USB3HS1

D3.3V
D3.3V
C103 4.7uF 2012 25V
C85 4.7uF 2012 25V
C104 0.01uF 1005 25V
C86 0.01uF 1005 25V
AP20 VDDQ33_USB3HSH0
AP19 VDDQ33_USB3HSH1

VDD0.8V
VDD0.8V
C105 0.1uF 1005 10V
C87 0.1uF 1005 10V
C106 0.01uF 1005 25V
C88 0.01uF 1005 25V
AU20 VDD09_USB3HS0
AU18 VDD09_USB3HS1

D3.3V
C807 4.7uF 2012 25V
C125 0.01uF 1005 25V
AN23 VDDQ33_USB2

D3.3V
D3.3V
D3.3V
C120 4.7uF 2012 25V
C115 4.7uF 2012 25V
C110 4.7uF 2012 25V
C121 0.01uF 1005 25V
C116 0.01uF 1005 25V
C111 0.01uF 1005 25V
AP23 VDDQ33_USB2H0
AP22 VDDQ33_USB2H1
AP21 VDDQ33_USB2H2

VDD0.8V
VDD0.8V
VDD0.8V
C808 0.1uF 1005 10V
C809 0.1uF 1005 10V
C810 0.1uF 1005 10V
C122 0.01uF 1005 25V
C117 0.01uF 1005 25V
C112 0.01uF 1005 25V
AT25 VDD09_USB20
AT24 VDD09_USB21
AT23 VDD09_USB22

D1.8V
D1.8V
C811 1uF 1005 10V
C812 1uF 1005 10V
C813 0.1uF 1005 10V
C814 0.1uF 1005 10V
C137 1000pF 1005 50V
C131 1000pF 1005 50V
AR15 VDDQ18_HDMI0
AT15 VDDQ18_HDMI1

VDD0.8V
C815 1uF 1005 10V
C816 0.1uF 1005 10V
C134 1000pF 1005 50V
AP15 VDDQ09_HDMI0
AT14 VDDQ09_HDMI0
AP14 VDDQ09_HDMI1
AR14 VDDQ09_HDMI1

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H3SiP_BGA_r0096_003

Back of U1 / Out of U1

VDD18_CPGPLL0 AG27 VDD_CPGPLL0 R67 1005 1 1% D1.8V
C51 1uF 1005 10V
VSS_CPGPLL0 AH27

VDD18_CPGPLL1 AK7 VDD_CPGPLL1 R68 1005 1 1% D1.8V
C43 1uF 1005 10V
VSS_CPGPLL1 AL7

VDD18_CPGPLL2 AD26 VDD_CPGPLL2 R69 1005 1 1% D1.8V
C65 1uF 1005 10V
VSS_CPGPLL2 AE26

VDD18_CPGPLL3 U25 VDD_CPGPLL3 R66 1005 1 1% D1.8V
C70 1uF 1005 10V
VSS_CPGPLL3 U26

VDD18_CPGPLL4 T25 VDD_CPGPLL4 R70 1005 1 1% D1.8V
C81 1uF 1005 10V
VSS_CPGPLL4 T26

VDD18_LVDSPLL1 AP12 VDD_LVDSPLL1
C90 0.1uF 1005 10V
C805 10uF 2012 16V
L7 1005 BLM15AX601SN1 1 2 D1.8V
Rated current=500mA

VDD09_LVDSPLL2 AR13 VDD09_LVDSPLL2
C99 0.1uF 1005 10V
C806 10uF 2012 16V
L9 1005 BLM15AX601SN1 1 2 VDD0.8V
Rated current=500mA

VDD18_DUPLL0 AK28 VDD_DUPLL0 R71 1005 1 1% D1.8V
C107 1uF 1005 10V
VSS_DUPLL0 AJ28

VDD18_DUPLL1 AK26 VDD_DUPLL1 R72 1005 1 1% D1.8V
C114 1uF 1005 10V
VSS_DUPLL1 AJ26

VDD18_MLBPLL AE28 VDD_MLBPPLL1 R73 1005 1 1% D1.8V
C119 1uF 1005 10V
VSS_MLBPLL AF28

VLDO_SD0 R74 0 1005
VLDO_SD1 R75 0 1005
VLDO_SD2 R76 0 1005
VLDO_SD3 R77 0 1005

VDDQVA_SD0 C30
VDDQVA_SD1 C28
VDDQVA_SD2 C26
VDDQVA_SD3 C24
C126 0.1uF 1005 10V
C127 0.1uF 1005 10V
C128 0.1uF 1005 10V
C129 0.1uF 1005 10V

MPLLTEST V30
Do not stuff
R78 1005 49.9* 1%

Back of U1 / Out of U1

点線外はU1裏以外のコンデンサ

SiP_board_r012.mcmを元にコンデンサ配置
↓ その後
容量指定、追加コンデンサ指定により回路変更あり

CONFIDENTIAL

R-CarH3 POWER1

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Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.08
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Preliminary

```
Capacitor-Pin Combination
D3.3V(VDDQ33)
  C142---J33
  C143---L26
  C144---N27
  C145---N33
  C146---T33
  C147---U28,U29
  C148---W28,W29
  C149---AD25,AE24
  C150---AH5
  C151---AJ27
  C152---AJ5
  C153---AK24
  C154---AM7
  C604---AN25
  C605---AN5
  C606---AP24
  C607---AR16
  =17pcs
```

```
Capacitor-Pin Combination
D1.8V(VDDQ18)
  C157---Y5,AA5
  C158---AD3,AE2,AE3
  C159---AD6,AE6
  C160---AF26,AF27,AG26
  C608---AH6
  C609---AJ10
  C610---AN26
  C611---AP16
  =8pcs
```

```
Capacitor-Pin Combination
VDD0.8V(VDD)
  C162---M3
  C163---N5
  C164---R3
  C165---U6
  C166-+-W27
  Cxxx-+
  C167---AA28
  C168---AD11
  C169---AF13
  C170---AF15
  C171---AF17,AG18
  C172---AF19
  C173---AF21
  C174---AG20
  C175---AG22,AG23
  C176---AH11
  Cxxx---AH10
  C177---AJ18
  C178---AJ22
  C179---AK11
  C180---AK23
  C181---AN10
  C182---AN12
  C183---AN14
  C184---AN16
  C185---AN18
  C186---AN20
  C187---AN22
  =28pcs
```

```
Capacitor-Pin Combination
DVFS0.8V(VDD_DVFS)
  C190---Y10,Y11,AA10
  C191---Y12,AA12
  C192---Y14
  C193---AA13,AA14
  C194---AB12,AC12
  C195---AB14,AB15
  C196---AC10,AC11
  C197---AC13,AC14,AD14,AD15,AE14
  C198---AD12,AE11,AE12,AF11
  C199---AE10
  C200---AE16
  C201---AE18
  C202---AE21
  C203---AG12
  C204---AG14
  C205---AG16
  C206---AH13,AJ14
  C207---AH15
  C208---AH17,AJ16
  C209---AH19
  C210---AH21
  C211---AJ12,AK13
  C212---AJ20
  C213---AK15
  C214---AK17
  C215---AK19
  C216---AK21
  =27pcs
```

[VDD]
Back of U1
=26pcs

[VDD_DVFS]
Back of U1
=27pcs

[VDDQ33]
Back of U1
=17pcs

[VDDQ18]
Back of U1
=8pcs

R-Car H3 SiP socket hole is connected to GND.

SKT1
SIP_SOCKET_HOLE

Vout=1.86V
Imax=500mA

Do not stuff

TEST_IC*

R82 2k 1005 R1 = 24.0k R2 = 200k Iadj = 20nA
Vout = 200mV * (1+(R2/R1)) - Iadj*R2
= 1.8627V

[Other Value]
R1 = 36k
R2 = 300k
Vout = 1.8607V

SoC Guide
EFUSEVDDQ ramp-up slew rate must be slower than 1.86V/31us.

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R-Car H3 POWER2

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Title	R-Car H3-SiP System Evaluation Board (Salvator-X)		
Size A2	Document Number R-Car H3-SiP System Evaluation Board (Salvator-X)		Rev 0.08
Date: Friday, April 10, 2015	Sheet 6	of 25	

Preliminary

Capacitor-Pin Combination
DDR0_1.1V(VDDQVA_DDR0)
C612---B34,C34
C613---C32
C614---C36
C615---D28
C616---D34
C617---D37
C618---E30,E32
C619---E34
C620---E36
C621---F28
C622---F32
C623---G28
C624---G30
C625---G34
C626---G36
C627---H36
C628---K28,L28
C629---K36
C630---L30
C631---L34
C632---L36,M36
C633---M34
C634---N29
C635---N36
C636---P30
C637---P34
C638---R30
C639---R34
C640---R35
C641---T30
C642---T35
C643---W35
C644---Y30,AA29
C645---Y33,AA33
C646---Y34,AA34
C647---Y37
C648---AC30
C649---AC34
C650---AC36
C651---AD28
C652---AD34,AD35
C653---AE19
C654---AE29
C655---AE30
C656---AE36
C657---AG24,AH25
C658---AG29,AG30
C659---AG36,AH36
C660---AH37
C661---AJ33
C662---AK29
C663---AK34
C664---AL33
C665---AM34
C666---AN31
=55pcs

Capacitor-Pin Combination
DDR0_1.8V(VDD1_M0/M1)
C268---F31
C269---F35
C270---M30
C271---M33
C734---AC29
C735---AC35
C736---AJ30
C740---AJ35
=8pcs

Capacitor-Pin Combination
DDR1_1.8V(VDD1_M2/M3)
C272---F8
C273---F10
C274---F19
C275---F23
C737---M7
C738---M10
C739---M19
C741---M23
=8pcs

U1E

AE19	VDDQVA_DDR0	VDDQVA_DDR1	P25
AG24	VDDQVA_DDR0	VDDQVA_DDR1	L25
AH25	VDDQVA_DDR0	VDDQVA_DDR1	K25
D28	VDDQVA_DDR0	VDDQVA_DDR1	G25
F28	VDDQVA_DDR0	VDDQVA_DDR1	F25
G28	VDDQVA_DDR0	VDDQVA_DDR1	D25
K28	VDDQVA_DDR0	VDDQVA_DDR1	R24
L28	VDDQVA_DDR0	VDDQVA_DDR1	M24
AD28	VDDQVA_DDR0	VDDQVA_DDR1	K24
N29	VDDQVA_DDR0	VDDQVA_DDR1	G24
AA29	VDDQVA_DDR0	VDDQVA_DDR1	E24
AE29	VDDQVA_DDR0	VDDQVA_DDR1	R22
AG29	VDDQVA_DDR0	VDDQVA_DDR1	P22
AK29	VDDQVA_DDR0	VDDQVA_DDR1	M22
E30	VDDQVA_DDR0	VDDQVA_DDR1	L22
G30	VDDQVA_DDR0	VDDQVA_DDR1	G22
L30	VDDQVA_DDR0	VDDQVA_DDR1	E22
P30	VDDQVA_DDR0	VDDQVA_DDR1	D22
R30	VDDQVA_DDR0	VDDQVA_DDR1	R20
T30	VDDQVA_DDR0	VDDQVA_DDR1	P20
Y30	VDDQVA_DDR0	VDDQVA_DDR1	L20
AC30	VDDQVA_DDR0	VDDQVA_DDR1	F20
AE30	VDDQVA_DDR0	VDDQVA_DDR1	R18
AG30	VDDQVA_DDR0	VDDQVA_DDR1	P18
AN31	VDDQVA_DDR0	VDDQVA_DDR1	N18
C32	VDDQVA_DDR0	VDDQVA_DDR1	M18
E32	VDDQVA_DDR0	VDDQVA_DDR1	L18
F32	VDDQVA_DDR0	VDDQVA_DDR1	K18
Y33	VDDQVA_DDR0	VDDQVA_DDR1	G18
AA33	VDDQVA_DDR0	VDDQVA_DDR1	E18
AJ33	VDDQVA_DDR0	VDDQVA_DDR1	C18
AL33	VDDQVA_DDR0	VDDQVA_DDR1	P16
B34	VDDQVA_DDR0	VDDQVA_DDR1	L16
C34	VDDQVA_DDR0	VDDQVA_DDR1	K16
D34	VDDQVA_DDR0	VDDQVA_DDR1	G16
E34	VDDQVA_DDR0	VDDQVA_DDR1	F16
G34	VDDQVA_DDR0	VDDQVA_DDR1	D16
L34	VDDQVA_DDR0	VDDQVA_DDR1	AD13
M34	VDDQVA_DDR0	VDDQVA_DDR1	P13
P34	VDDQVA_DDR0	VDDQVA_DDR1	N13
R34	VDDQVA_DDR0	VDDQVA_DDR1	L13
Y34	VDDQVA_DDR0	VDDQVA_DDR1	K13
AA34	VDDQVA_DDR0	VDDQVA_DDR1	G13
AC34	VDDQVA_DDR0	VDDQVA_DDR1	F13
AD34	VDDQVA_DDR0	VDDQVA_DDR1	D13
AK34	VDDQVA_DDR0	VDDQVA_DDR1	R12
AM34	VDDQVA_DDR0	VDDQVA_DDR1	M12
R35	VDDQVA_DDR0	VDDQVA_DDR1	E12
T35	VDDQVA_DDR0	VDDQVA_DDR1	R11
W35	VDDQVA_DDR0	VDDQVA_DDR1	K11
AD35	VDDQVA_DDR0	VDDQVA_DDR1	G11
C36	VDDQVA_DDR0	VDDQVA_DDR1	AG10
E36	VDDQVA_DDR0	VDDQVA_DDR1	R10
G36	VDDQVA_DDR0	VDDQVA_DDR1	P10
H36	VDDQVA_DDR0	VDDQVA_DDR1	L10
K36	VDDQVA_DDR0	VDDQVA_DDR1	G10
L36	VDDQVA_DDR0	VDDQVA_DDR1	E10
M36	VDDQVA_DDR0	VDDQVA_DDR1	D10
N36	VDDQVA_DDR0	VDDQVA_DDR1	C10
AC36	VDDQVA_DDR0	VDDQVA_DDR1	G8
AE36	VDDQVA_DDR0	VDDQVA_DDR1	E8
AG36	VDDQVA_DDR0	VDDQVA_DDR1	D8
AH36	VDDQVA_DDR0	VDDQVA_DDR1	C8
D37	VDDQVA_DDR0	VDDQVA_DDR1	R7
Y37	VDDQVA_DDR0	VDDQVA_DDR1	P7
AH37	VDDQVA_DDR0	VDDQVA_DDR1	L7
		VDDQVA_DDR1	R6
		VDDQVA_DDR1	M6
		VDDQVA_DDR1	K6
		VDDQVA_DDR1	H6
		VDDQVA_DDR1	E6
		VDDQVA_DDR1	C6
		VDDQVA_DDR1	R5
		VDDQVA_DDR1	L5
		VDDQVA_DDR1	D5
		VDDQVA_DDR1	P4
		VDDQVA_DDR1	L4
		VDDQVA_DDR1	K4
		VDDQVA_DDR1	H4
		VDDQVA_DDR1	G4

AC29	VDD1_M01	F31	VDD1_M01
AC35	VDD1_M01	F35	VDD1_M01
AJ30	VDD1_M01	M30	VDD1_M01
AJ35	VDD1_M01	M33	VDD1_M01
F19	VDD1_M23	F8	VDD1_M23
F23	VDD1_M23	F10	VDD1_M23
M19	VDD1_M23	M7	VDD1_M23
M23	VDD1_M23	M10	VDD1_M23

DDR0_1.1V / DDR1_1.1V

W39 M01BKUP — R84 0 1005 — R85 10k* 1005 — BKUP_CTRL_11 <25>
Do not stuff
D17 M23BKUP — R86 0 1005 — R87 10k* 1005

DDR0_1.1V
R91 240.0 1% 1005 V33 ZQ0_M0
R92 240.0 1% 1005 V34 ZQ1_M0
R93 240.0 1% 1005 AD36 ZQ2_M0
R94 240.0 1% 1005 AB25 M0ZQ
R95 240.0 1% 1005 A32 ZQ0_M1
R99 240.0 1% 1005 A33 ZQ1_M1
R100 240.0 1% 1005 F36 ZQ2_M1
R101 240.0 1% 1005 W25 M1ZQ

DDR1_1.1V
R102 240.0 1% 1005 A20 ZQ0_M2
R103 240.0 1% 1005 A22 ZQ1_M2
R107 240.0 1% 1005 F24 ZQ2_M2
R108 240.0 1% 1005 W15 M2ZQ
R109 240.0 1% 1005 A7 ZQ0_M3
R110 240.0 1% 1005 A10 ZQ1_M3
R111 240.0 1% 1005 F12 ZQ2_M3
R115 240.0 1% 1005 AF6 M3ZQ

ZQn (n=0,1)
Pull-up(DDRIO) : 240ohm +-1%

MnZQ (n=0-3)
Pull-down(GND) : 240ohm +-1%

Do not stuff

CP8	M0ATB0	AH33	M0ATB0
CP9	M0ATB1	AH34	M0ATB1
CP10	M1ATB0	G27	M1ATB0
CP11	M1ATB1	F27	M1ATB1
CP12	M2ATB0	G26	M2ATB0
CP13	M2ATB1	F26	M2ATB1
CP14	M3ATB0	AF5	M3ATB0
CP15	M3ATB1	AG6	M3ATB1

R-CarH3SiP
H3SiP_BGA_r0096_003

VDD09_DDRPLL0 — L68 1005 LQG15HH2N0S02 2.0nH 300mA — VDD0.8V
VDD09_DDRPLL0CA: AA25, AA26, AA27, AC26, AC27
VDD09_DDRPLL0DQ01
VDD09_DDRPLL0DQ23
C276 0.033uF 1005 16V
C277 0.033uF 1005 16V
C789 0.033uF 1005 16V

VDD09_DDRPLL1 — L69 1005 LQG15HH2N0S02 2.0nH 300mA — VDD0.8V
VDD09_DDRPLL1CA: Y25, Y26, Y27, V26, V27
VDD09_DDRPLL1DQ01
VDD09_DDRPLL1DQ23
C279 0.033uF 1005 16V
C280 0.033uF 1005 16V
C790 0.033uF 1005 16V

VDD09_DDRPLL2 — L70 1005 LQG15HH2N0S02 2.0nH 300mA — VDD0.8V
VDD09_DDRPLL2CA: U13, U14, U15, T15, T14
VDD09_DDRPLL2DQ01
VDD09_DDRPLL2DQ23
C282 0.033uF 1005 16V
C284 0.033uF 1005 16V
C791 0.033uF 1005 16V

VDD09_DDRPLL3 — L71 1005 LQG15HH2N0S02 2.0nH 300mA — VDD0.8V
VDD09_DDRPLL3CA: V10, V11, V12, W10, AG7
VDD09_DDRPLL3DQ01
VDD09_DDRPLL3DQ23
L72 1005 LQG15HH2N0S02 2.0nH 300mA — VDD0.8V
C285 0.033uF 1005 16V
C286 0.033uF 1005 16V
C287 0.1uF 1005 10V

Back of U1

DDR0_1.1V

DDR0_1.1V: C242 4.7uF 2012 25V; C243 4.7uF 2012 25V; C244 4.7uF 2012 25V; C245 4.7uF 2012 25V
DDR0_1.1V: C220 10uF 2012 16V; C221 10uF 2012 16V
DDR0_1.1V: C612–C631 0.1uF 1005 10V
DDR0_1.1V: C632–C651 0.1uF 1005 10V
DDR0_1.1V: C652–C666 0.1uF 1005 10V

[DDR0_1.1V]
Back of U1
=55pcs

DDR1_1.1V

DDR1_1.1V: C264 4.7uF 2012 25V; C265 4.7uF 2012 25V; C266 4.7uF 2012 25V; C267 4.7uF 2012 25V
DDR1_1.1V: C255 10uF 2012 16V; C256 10uF 2012 16V
DDR1_1.1V: C667–C686 0.1uF 1005 10V
DDR1_1.1V: C687–C706 0.1uF 1005 10V
DDR1_1.1V: C707–C726 0.1uF 1005 10V
DDR1_1.1V: C727–C733 0.1uF 1005 10V

[DDR1_1.1V]
Back of U1
=67pcs

DDR0_1.8V

[DDR0_1.8V]
Back of U1
=8pcs

DDR0_1.8V: C268 C269 C270 C271 C740 C734 C735 C736 0.1uF 1005 10V

DDR1_1.8V

[DDR0_1.8V]
Back of U1
=8pcs

DDR1_1.8V: C272 C273 C274 C275 C737 C741 C738 C739 0.1uF 1005 10V

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R-CarH3 LPDDR_POWER

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Title	R-CarH3-SiP System Evaluation Board (Salvator-X)		
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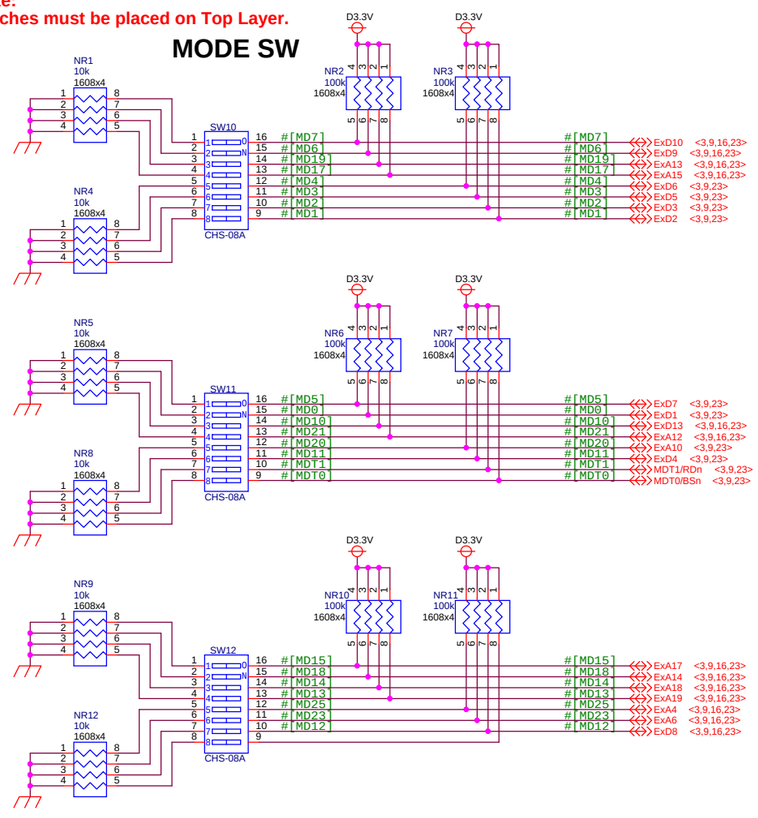
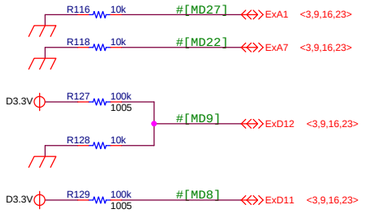
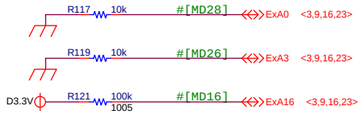
Preliminary

Layout Note:
Mode switches must be placed on Top Layer.

MODE SW







[Design Note]
It is not necessary to setup MD24.

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MODE_SW

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Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.08
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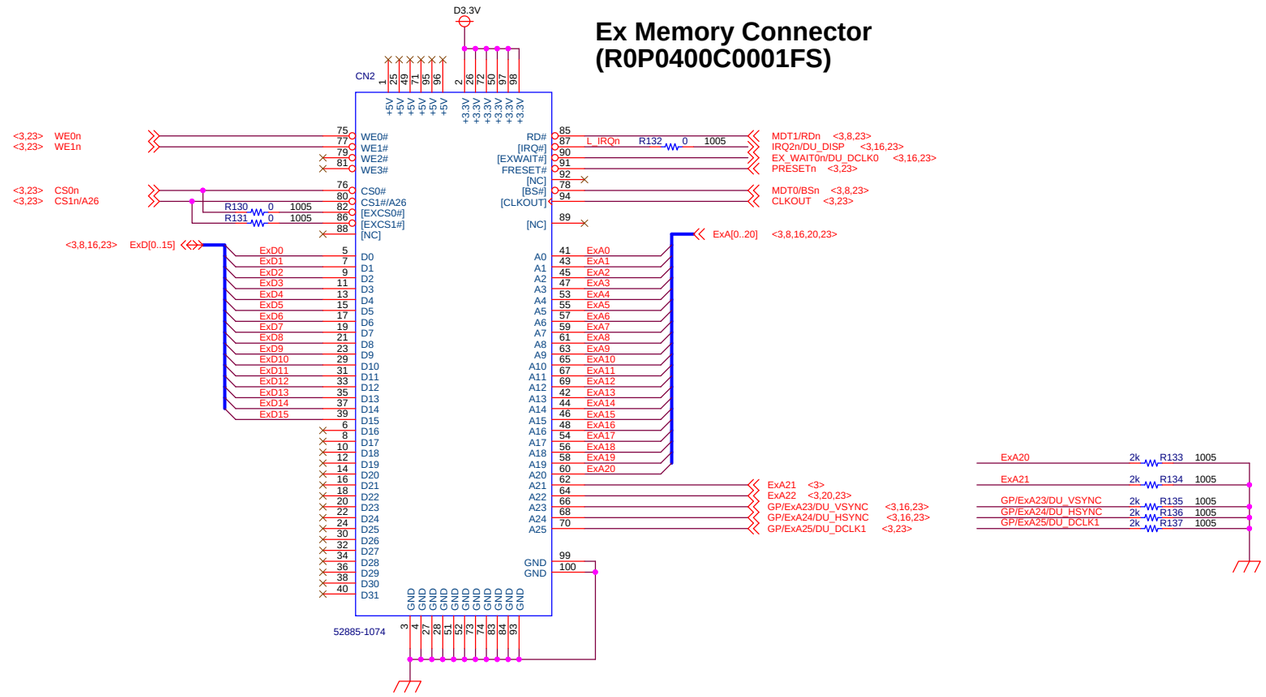
Preliminary

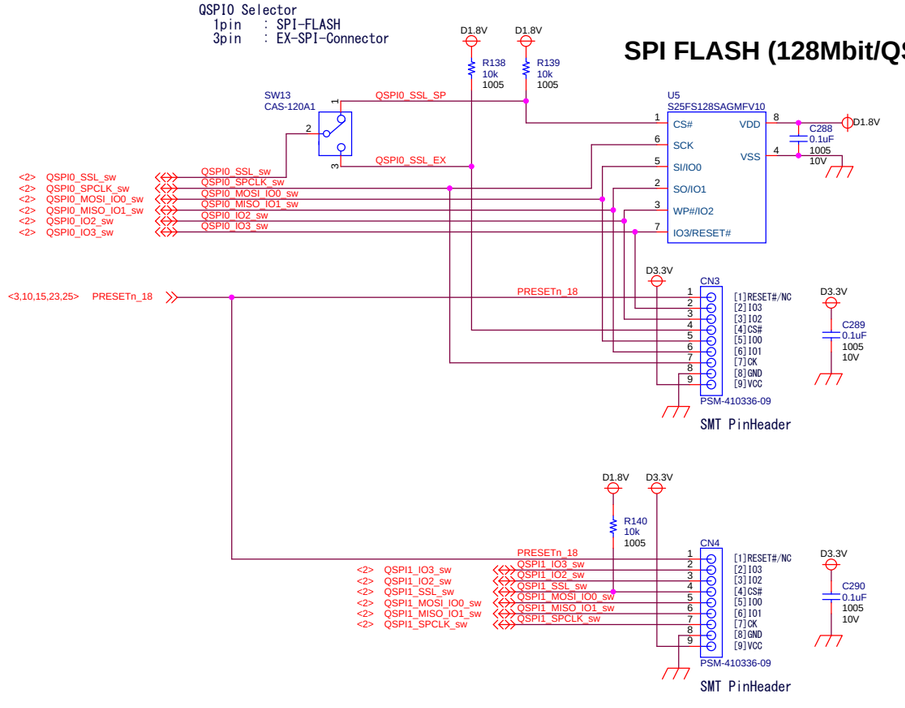
Layout Note:
Following signals need Ground guard.

CLKOUT
QSPI0_SPCLK_18, QSPI0_SPCLK_SP
QSPI1_SPCLK_18, QSPI1_SPCLK_EX

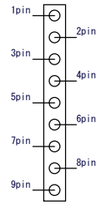
Ex Memory Connector (R0P0400C0001FS)



SPI FLASH (128Mbit/QSPI0)



EX-SPI Connector (QSPI0)



EX-SPI Connector (QSPI1)

S25FS128SAGMFV10

```
S25FS 128 S AG M F V 10
##### ### # ## # # # ##
                      +---- 10   = SOIC-8pin
                     +----- V    = Automotive In-Cabin (-40C to +105C)
                    +------ F    = Lead(Pb)-free
                   +------- M    = SOIC
                  +-------- AG   = 133 MHz
                 +--------- S    = 0.65um MirrorBit Process Technology
                +---------- 128  = 128Mbit
               +----------- S25FS = Spansion Memory 1.8 Volt-Only
```

EX-SPI-Flash-Board generate VIO=1.8V from D3.3V for internal using.

QSPI_FLASH/FL_CN

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Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
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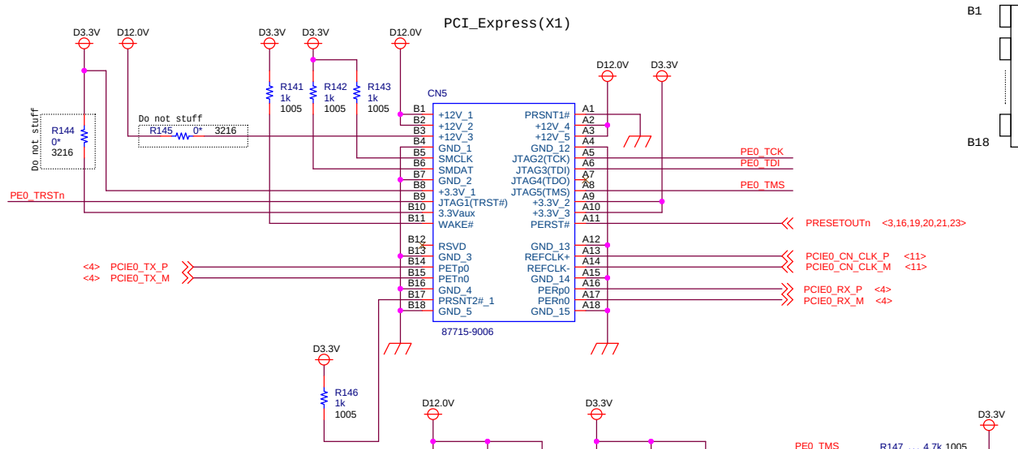
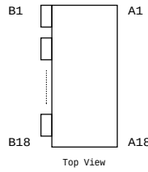
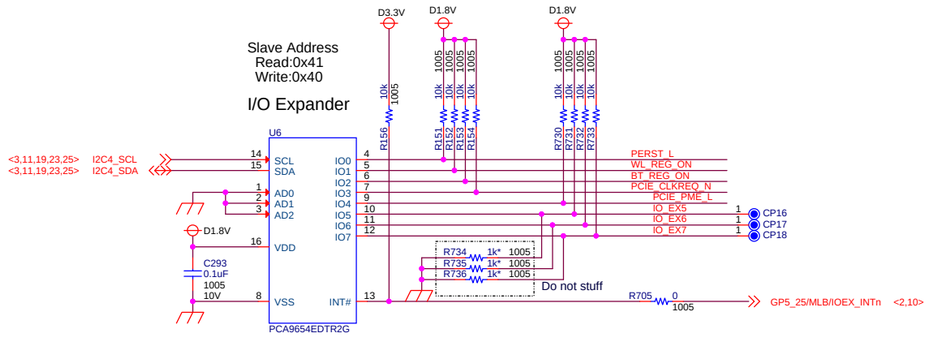
Preliminary

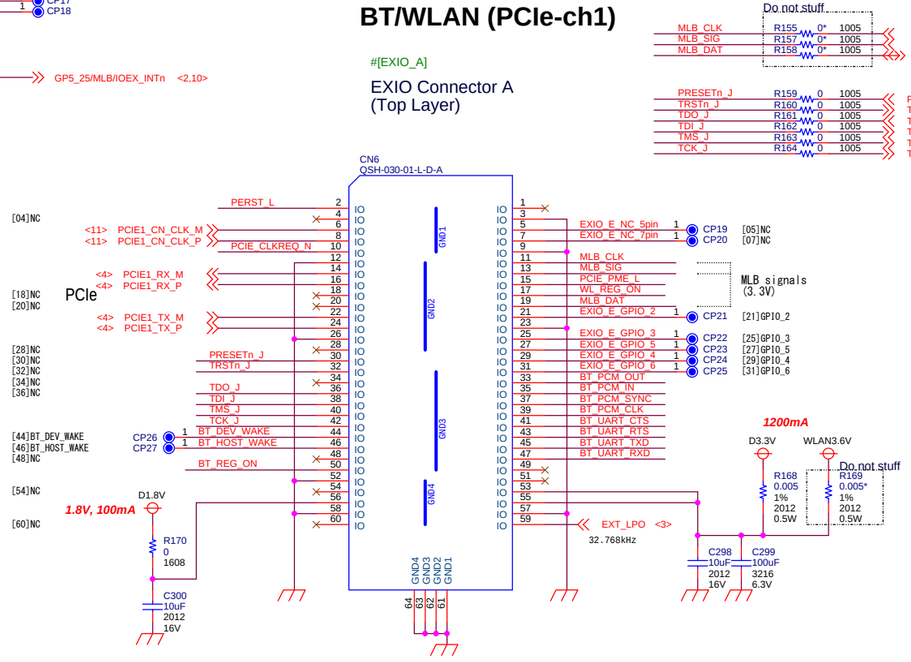
PCIE (PCIe-ch0)

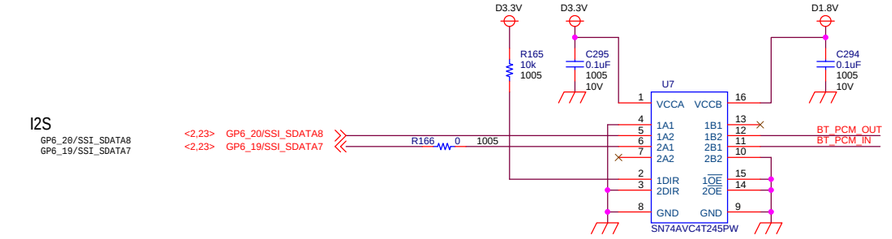


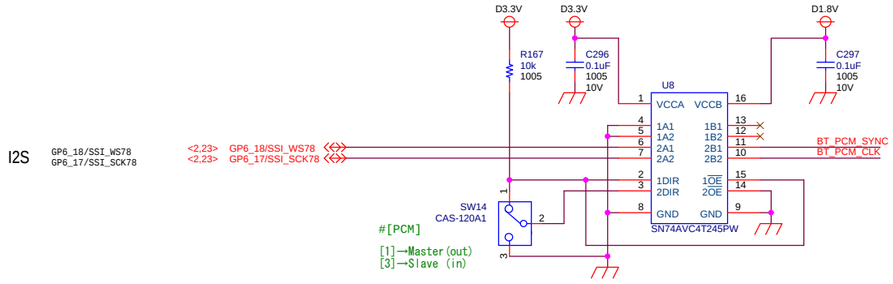


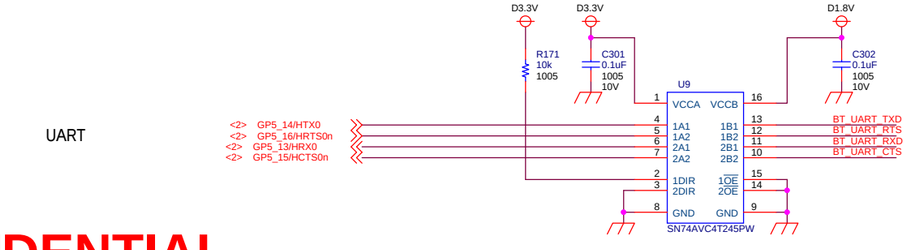


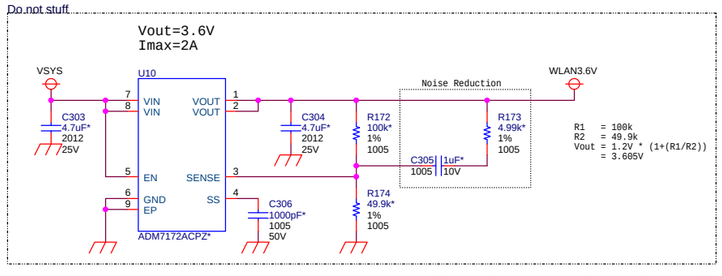
BT/WLAN (PCIe-ch1)











BCM89359 based module EVB Pin Assign (@2015/01/20)

No.	Pin Name	No.	Pin Name
2	PCIE_PRST_N	1	NC
4	NC	3	GND
6	PCIE_REFCLK_N	5	NC
8	PCIE_REFCLK_P	7	NC
10	PCIE_CLKREQ_N	9	GND
12	GND	11	NC
14	PCIE_TDN	13	NC
16	PCIE_TDP	15	PCIE_PME_L or WL_HOST_WAKE
18	NC	17	WL_REG_ON
20	NC	19	NC
22	PCIE_RDN	21	GPIO_2
24	PCIE_RDP	23	GND
26	GND	25	GPIO_3
28	NC	27	GPIO_5
30	NC	29	GPIO_4
32	NC	31	GPIO_6
34	NC	33	BT_PCM_IN
36	NC	35	BT_PCM_OUT
38	NC	37	BT_PCM_SYNC
40	NC	39	BT_PCM_CLK
42	NC	41	BT_UART_RTS
44	BT_DEV_WAKE	43	BT_UART_CTS
46	BT_HOST_WAKE	45	BT_UART_RXD
48	NC	47	BT_UART_TXD
50	BT_REG_ON	49	NC
52	GND	51	NC
54	NC	53	VDD
56	VIO	55	VDD
58	GND	57	GND
60	NC	59	LPO_IN

-60pin Connector on BT/WLAN EVB
OTH-030-01-L-D-A (Samtec)

-Dimensions
45mm x 35mm

CONFIDENTIAL

Default Unit is "mm"

PCIe ch0/ch1

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Title	R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)		Rev 0.08
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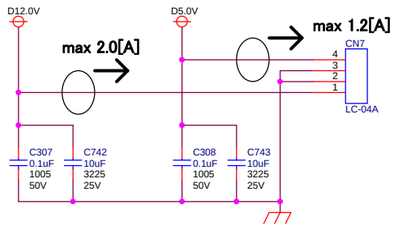
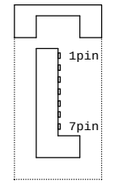
Preliminary

Serial ATA Drive power supply connector

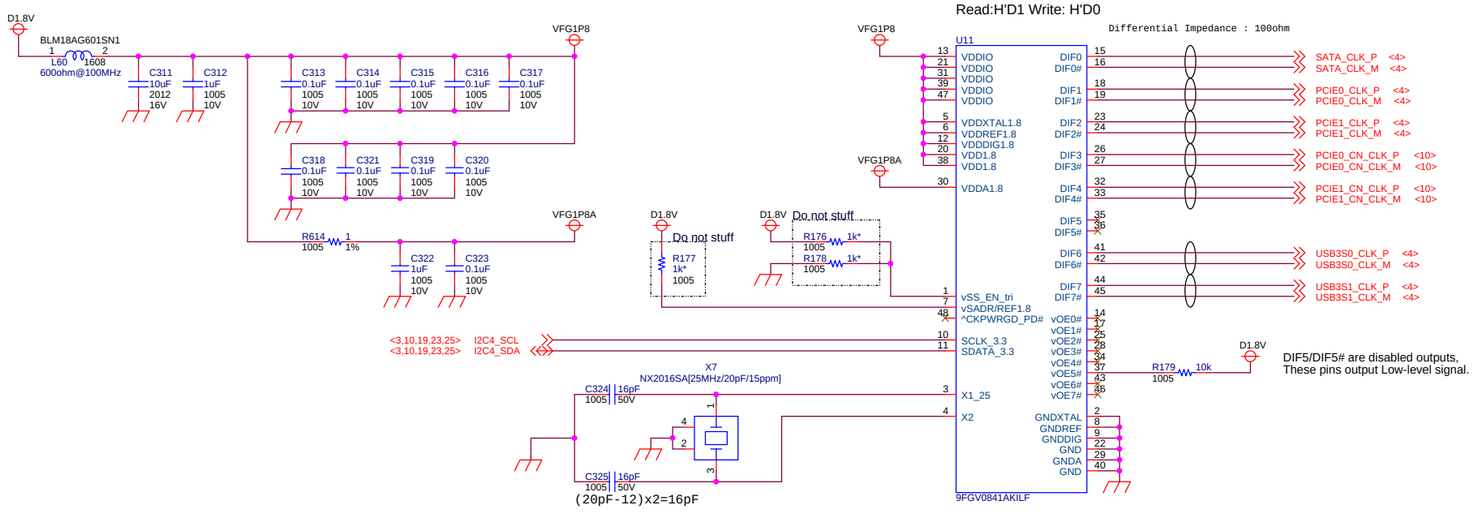


Serial ATA signal connector



Serial ATA signal connector
Top View

I2Cslave address: 1101_000X
Read:H'D1 Write: H'D0



DIF5/DIF5# are disabled outputs,
These pins output Low-level signal.

v : prefix indicates internal 120KOhm pull down resistor
^ : prefix indicates internal 120KOhm pull up resistor

Power Management Table

CKPWRGD_PD#	SMBus OE bit	DIFx			REF
		OEx#	True O/P	Comp. O/P	
0	X	X	Low	Low	Hi-Z
1	1	0	Running	Running	Running
1	0	1	Low	Low	Low

SMBus Address Selection Table (I2C Slave address)

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

Select Spread Spectrum Table

vSS_EN_tri	Spread Spectrum
0	Spread Off
M	-0.25%
1	-0.5%

'M' is Mid Voltage = 0.5VDD = 0.9V.
This setting can be controled by software.
Refer to datasheet chapter of "SMBus Table : SS Readback and Control Register"

CONFIDENTIAL

Default Unit is "mm"

Serial ATA

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Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.08
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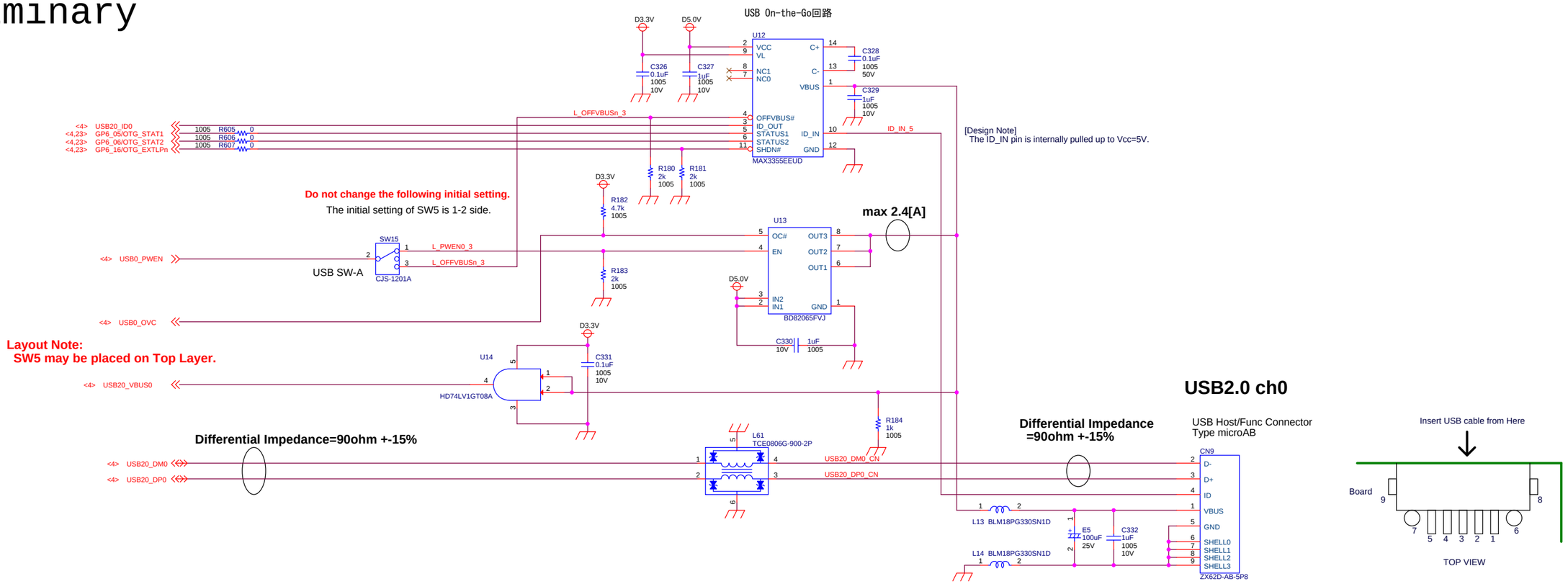
Preliminary



CONFIDENTIAL

USB2.0

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Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.08
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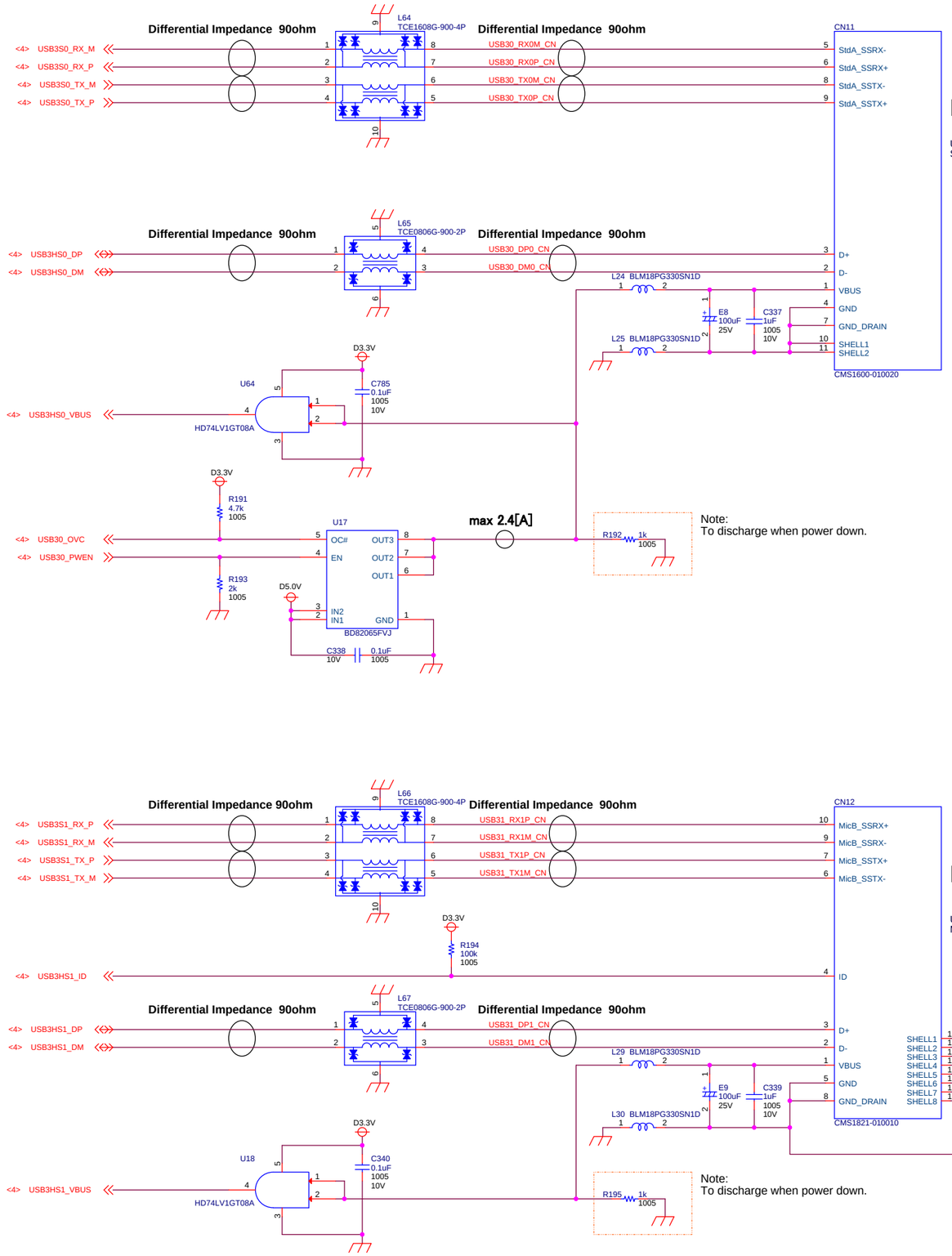
Preliminary



CONFIDENTIAL

USB3.0

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Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.08
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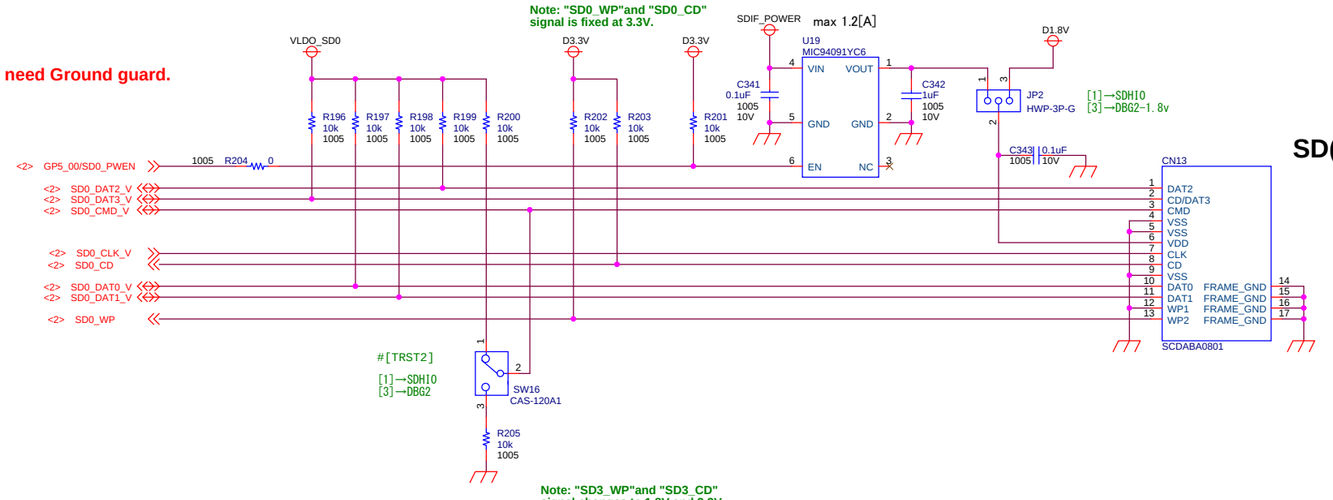
Preliminary

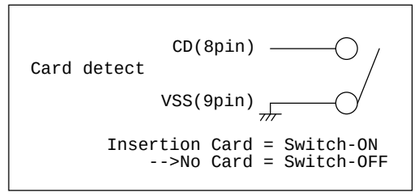
Layout Note:
Following signals need Ground guard.

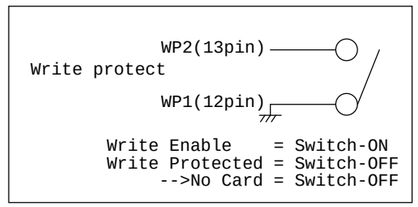
SD0_CLK_V

Note: "SD0_WP"and "SD0_CD" signal is fixed at 3.3V.



SD(CH0)

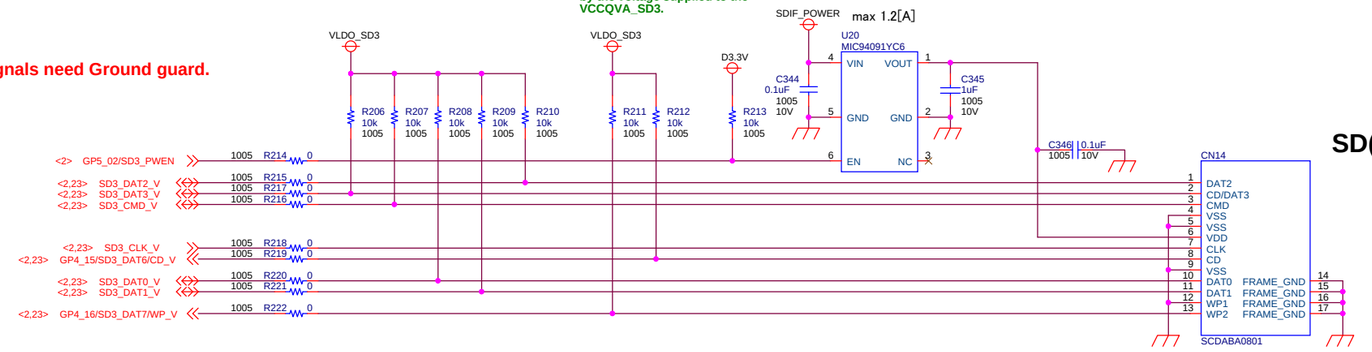




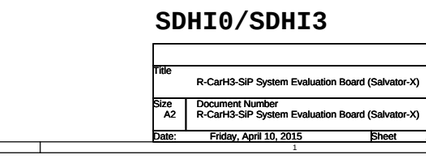
Layout Note:
Following signals need Ground guard.

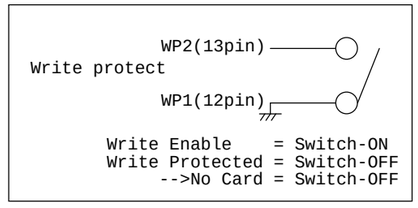
SD3_CLK_V

Note: "SD3_WP"and "SD3_CD" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD3.

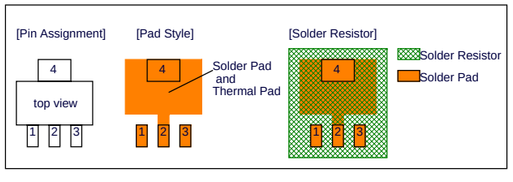


SD(CH3)

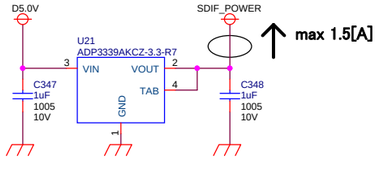




Layout Note:
Pad Configuration for ADP3339



D3.3V for SDIF Power



CONFIDENTIAL

SDHI0/SDHI3

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Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.08
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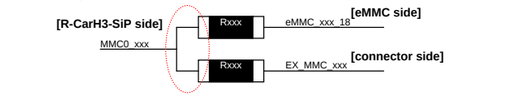
Preliminary

Layout Note:
As short as possible from junction of MMC0_xxx to two Rxxx.



Do not stuff

<2>	MMC0_DTA0_V	R225 0 1005	R617 0* 1005	eMMC_D0_18	EX_MMC_D0_V	<23>
<2>	MMC0_DTA1_V	R226 0 1005	R619 0* 1005	eMMC_D1_18	EX_MMC_D1_V	<23>
<2>	MMC0_DTA2_V	R227 0 1005	R620 0* 1005	eMMC_D2_18	EX_MMC_D2_V	<23>
<2>	MMC0_DTA3_V	R228 0 1005	R618 0* 1005	eMMC_D3_18	EX_MMC_D3_V	<23>
<2>	MMC0_DTA4_V	R229 0 1005	R621 0* 1005	eMMC_D4_18	EX_MMC_D4_V	<23>
<2>	MMC0_DTA5_V	R231 0 1005	R622 0* 1005	eMMC_D5_18	EX_MMC_D5_V	<23>
<2>	MMC0_DTA6_V	R230 0 1005	R623 0* 1005	eMMC_D6_18	EX_MMC_D6_V	<23>
<2>	MMC0_DTA7_V	R232 0 1005	R626 0* 1005	eMMC_D7_18	EX_MMC_D7_V	<23>
<2>	MMC0_CMD_V	R233 0 1005	R627 0* 1005	eMMC_CMD_18	EX_MMC_CMD_V	<23>
<2>	MMC0_CLK_V	R234 0 1005	R628 0* 1005	eMMC_CLK_18	EX_MMC_CLK_V	<23>
<2>	MMC0_DS_V	R235 0 1005	R629 0* 1005	eMMC_DS_18	EX_MMC_DS_V	<23>

Layout Note:
Following signals need Ground guard.

MMC0_CLK_V, eMMC_CLK_18, EX_MMC_CLK_V

Layout Note:
Matched Trace Length from R-CarH3-SiP to eMMC. max 400Mbps/pin

Group 1
- MMC0_DTA[7:0]_V + eMMC_D[7:0]_18
- MMC0_CMD_V + eMMC_CMD_18
- MMC0_CLK_V + eMMC_CLK_18
- MMC0_DS_V + eMMC_DS_18

D1.8V — R616 0 — eMMC_VCCQ

Rated current=1A

eMMC_VCCQ — NR14 47k 1608x4 (4 3 2 1 / 5 6 7 8)

eMMC_VCCQ — NR15 47k 1608x4 (4 3 2 1 / 5 6 7 8)

eMMC_VCCQ — R223 47k — R224 47k* — Do not stuff

[Design Note]
NAND Memory Power(VCC): 2.7 - 3.6V
eMMC Interface Power(VCCQ): 1.70-1.95V

eMMC(1.8V)

[Pin Function]

U22A
KLMBG4GESD-B031

SD2_DAT0 / MMC0_DTA0	eMMC_D0_18	A3	DATA0	VCC_1 E6
SD2_DAT1 / MMC0_DTA1	eMMC_D1_18	A4	DATA1	VCC_2 F5
SD2_DAT2 / MMC0_DTA2	eMMC_D2_18	A5	DATA2	VCC_3 J10
SD2_DAT3 / MMC0_DTA3	eMMC_D3_18	B2	DATA3	VCC_4 K9
SD1_DAT0 / MMC0_DTA4	eMMC_D4_18	B3	DATA4	
SD1_DAT1 / MMC0_DTA5	eMMC_D5_18	B4	DATA5	VCCQ_1 C6
SD1_DAT2 / MMC0_DTA6	eMMC_D6_18	B5	DATA6	VCCQ_2 M4
SD1_DAT3 / MMC0_DTA7	eMMC_D7_18	B6	DATA7	VCCQ_3 N4
				VCCQ_4 P3
				VCCQ_5 P5
SD2_CMD / MMC0_CMD	eMMC_CMD_18	M5	CMD	
				VDDI C2
SD2_CLK / MMC0_CLK	eMMC_CLK_18	M6	CLK	
SD2_DS / MMC0_DS	eMMC_DS_18	H5	DS	
				VSS_1 A6
				VSS_2 E7
				VSS_3 G5
				VSS_4 H10
				VSS_5 J5
		K5	RST_n	VSS_6 K8
				VSSQ_1 C4
				VSSQ_2 N2
				VSSQ_3 N5
				VSSQ_4 P4
				VSSQ_5 P6

D3.3V — C363 2.2uF 1608 10V

[Design Note]
Sets pull-down resistor(47kohm) at the DS pin.
For detail, See "Table 217 - HS400 Capacitance and Resistors on eMMC specification" in JESD84-B51.pdf

R236 47k

eMMC_VCCQ — Do not stuff — R624 47k*

<3,9,10,23,25> PRESETn_18 — R625 0 1005

[Candidate of Part Number]
(1) samsung, KLMBG4GESD-B031
(2) micron, MTFC16GAKAECN-AIT
(3) smi, under development.

[Design Note]
In case of using SDHI1 through EXIO connector 'CN27', that is "EXIO_B",

DISMOUNT follwoing resistors.
R229, R231, R230, R232(0ohm/1005).
and MOUNT following resistors.
R621, R622, R623, R626(0ohm/1005).

[Design Note]
In case of using SDHI2 through EXIO connector 'CN27', that is "EXIO_B",

DISMOUNT follwoing resistors.
R229, R231, R230, R232(0ohm/1005).
and MOUNT following resistors.
R621, R622, R623, R626(0ohm/1005).

DISMOUNT follwoing resistors
R225, R226, R227, R228, R233, R234, R235(0ohm/1005)
R625(0ohm/1005) for PRESETn_18
and MOUNT following resistors.
R617, R619, R620, R618, R627, R628, R629(0ohm/1005)

and MOUNT following resistors.
R224(47k/1608) to prevent eMMC's CLK-pin floating.
R624(47k/1608) to prevent eMMC's RST_n-pin floatting.

D3.3V — C349 0.1uF 1005 10V — C351 0.1uF 1005 10V — C354 2.2uF 1608 10V

D3.3V — C352 0.1uF 1005 10V — C350 0.1uF 1005 10V — C353 2.2uF 1608 10V

eMMC_VCCQ — C355 0.1uF 1005 10V — C356 0.1uF 1005 10V — C357 2.2uF 1608 10V

eMMC_VCCQ — C358 0.1uF 1005 10V — C359 0.1uF 1005 10V — C360 2.2uF 1608 10V

eMMC_VCCQ — C361 0.1uF 1005 10V — C362 2.2uF 1608 10V

U22B
KLMBG4GESD-B031

NC

A1	NC_1	K1	NC_66	
A2	NC_2	K2	NC_67	
A3	NC_3	K3	NC_68	
A9	NC_4	K12	NC_69	
A10	NC_5	K13	NC_70	
A11	NC_6	K14	NC_71	
A12	NC_7	L1		
A13	NC_8	L2	NC_72	
A14	NC_9	L3	NC_73	
B1		L12	NC_74	
B2	NC_10	L13	NC_75	
B8	NC_11	L14	NC_76	
B9	NC_12		NC_77	
B10	NC_13	M1		
B11	NC_14	M2	NC_78	
B12	NC_15	M3	NC_79	
B13	NC_16	M7	NC_80	
B14	NC_17	M8	NC_81	
	NC_18	M9	NC_82	
C1		M10	NC_83	
C2	NC_19	M11	NC_84	
C3	NC_20	M12	NC_85	
C5	NC_21	M13	NC_86	
C7	NC_22	M14	NC_87	
C8	NC_23		NC_88	
C9	NC_24	N1		
C10	NC_25	N3	NC_89	
C11	NC_26	N6	NC_90	
C12	NC_27	N7	NC_91	
C13	NC_28	N8	NC_92	
C14	NC_29	N9	NC_93	
D1		N10	NC_94	
D2	NC_30	N11	NC_95	
D3	NC_31	N12	NC_96	
D4	NC_32	N13	NC_97	
D12	NC_33	N14	NC_98	
D13	NC_34		NC_99	
D14	NC_35	P1		
	NC_36	P2	NC_100	
E1		P8	NC_101	
E2	NC_37	P9	NC_102	
E3	NC_38	P11	NC_103	
E12	NC_39	P12	NC_104	
E13	NC_40	P13	NC_105	
E14	NC_41	P14	NC_106	
	NC_42		NC_107	

RFU

F1		A7		
F2	NC_43	E5	RFU_1	
F3	NC_44	E8	RFU_2	
F12	NC_45	G3	RFU_3	
F13	NC_46	G10	RFU_4	
F14	NC_47	K6	RFU_5	
	NC_48	K7	RFU_6	
G1		K10	RFU_7	
G2	NC_49	P7	RFU_8	
G12	NC_50	P10	RFU_9	
G13	NC_51		RFU_10	
G14	NC_52			
	NC_53			

VSF

H1		E9		
H2	NC_54	E10	VSF_1	
H3	NC_55	C10	VSF_2	
H12	NC_56		VSF_3	
H13	NC_57			
H14	NC_58			
	NC_59			
J1				
J2	NC_60			
J3	NC_61			
J12	NC_62			
J13	NC_63			
J14	NC_64			
	NC_65			

MMC0

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Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.08
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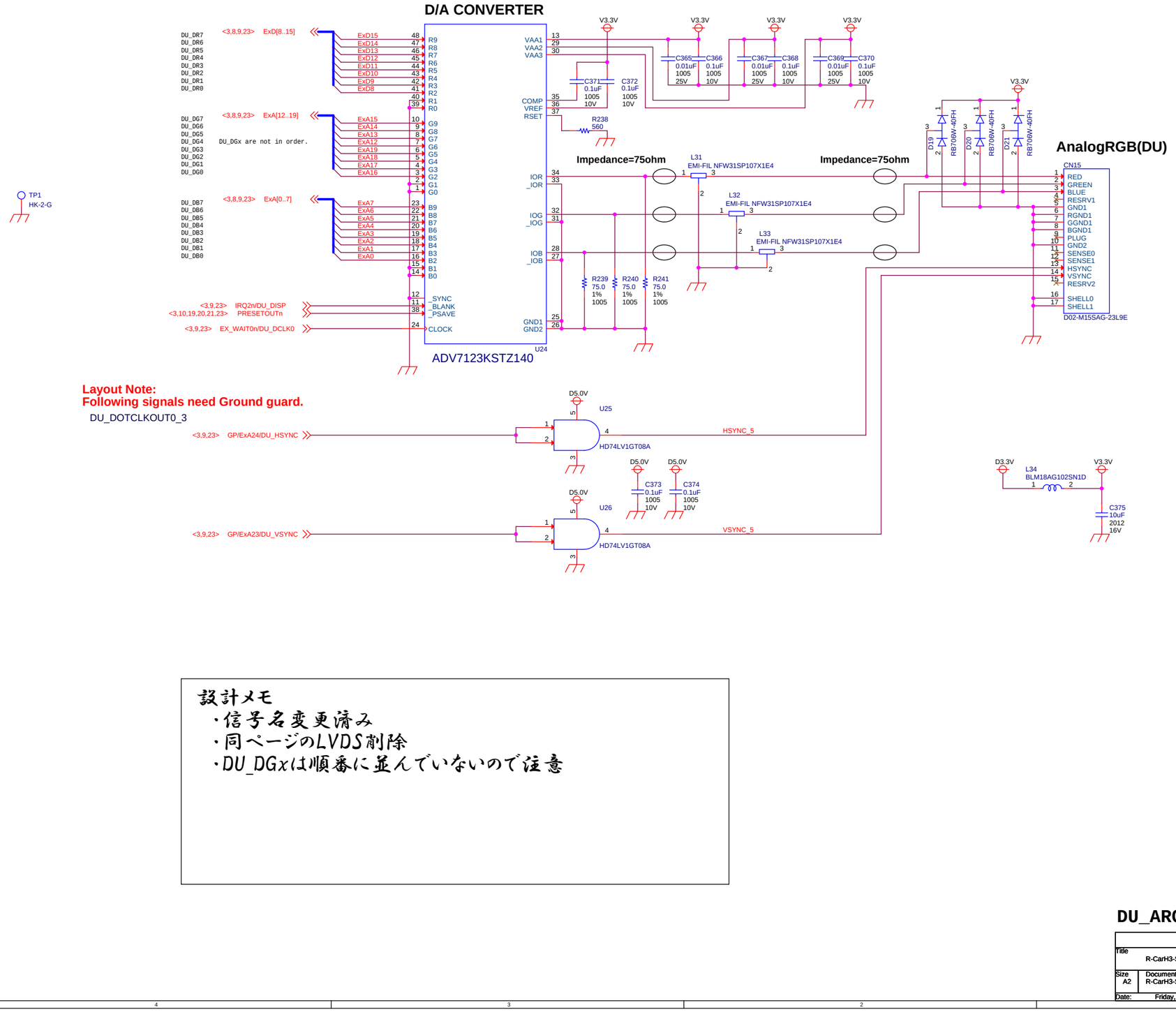

設計メモ
・信号名変更済み
・同ページのLVDS削除
・DU_DGxは順番に並んでいないので注意

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DU_ARGB

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Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
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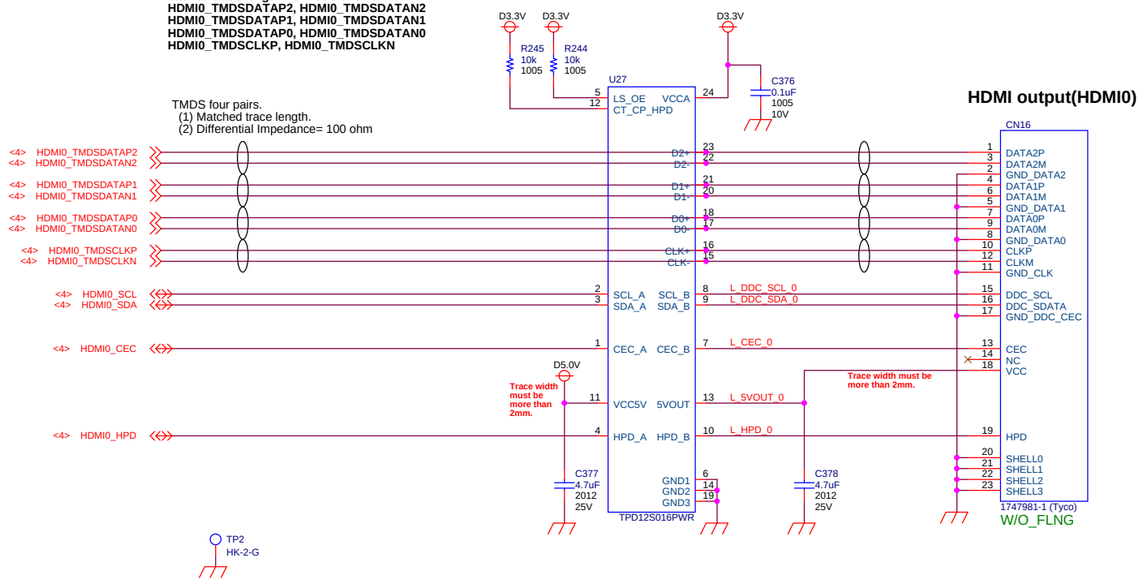
Layout Note:

Matched trace length from SoC until CN16
HDMI0_TMDSDATAP2, HDMI0_TMDSDATAN2
HDMI0_TMDSDATAP1, HDMI0_TMDSDATAN1
HDMI0_TMDSDATAP0, HDMI0_TMDSDATAN0
HDMI0_TMDSCLKP, HDMI0_TMDSCLKN

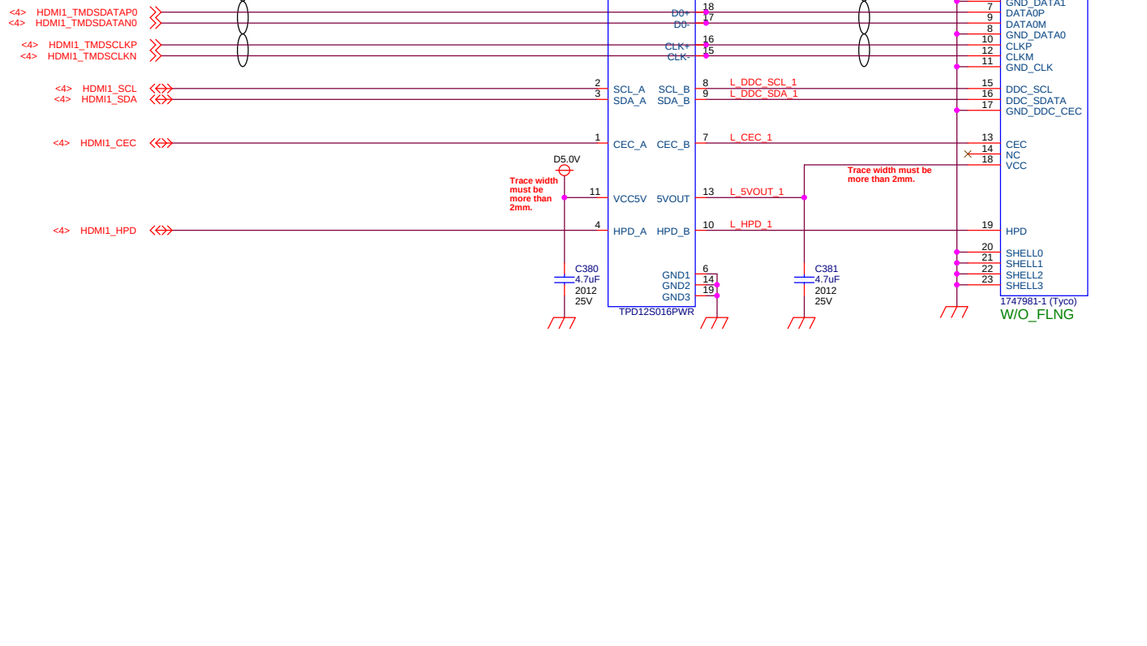
HDMI COMPANION CHIP
WITH ESD PROTECTION, I2C LEVEL SHIFTER



Layout Note:

Matched trace length from SoC until CN17
HDMI1_TMDSDATAP2, HDMI1_TMDSDATAN2
HDMI1_TMDSDATAP1, HDMI1_TMDSDATAN1
HDMI1_TMDSDATAP0, HDMI1_TMDSDATAN0
HDMI1_TMDSCLKP, HDMI1_TMDSCLKN

HDMI COMPANION CHIP
WITH ESD PROTECTION, I2C LEVEL SHIFTER



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HDMI_OUT

17

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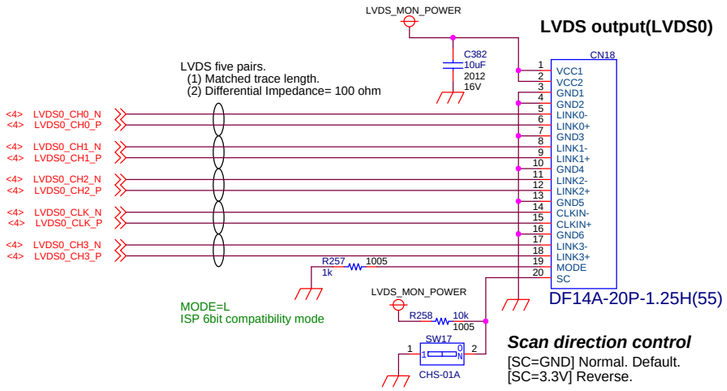

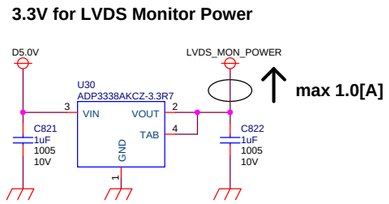

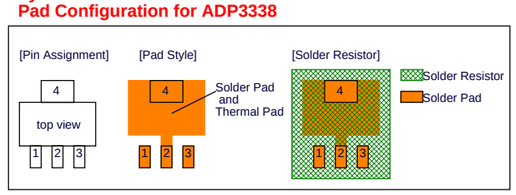

GP2_07 / PWM1 / A21	VOUTA of LTC2644	Brightness
Low Level	0.0V	max
High Level	2.5V	min
PWM	(tPWH / tPERIOD) x 2.5V	variable

[Design Note]
LTC2644HMS-L8#TRPBF for Automotive.

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LVDS0

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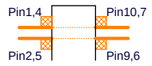
VIDEO DECODER FOR MIPI CSI-2 (channel 0, channel 1)

Layout Note:
Connect INx with OUTx under the RCLAMP0524. See below figure.



Layout Note:
Connect the shell of 1747981-1 with ground.
The 1747981-1 has four through holes.

HDMI Input Connector TYPE A(Standard)

CN20
1747981-1 (Tyco)
Place at Top layer.

TMDS four pairs Differential Impedance 100ohm +-10% Matched trace length.

Note:
ESD Protection diode array.

D22, D23, D25: RCLAMP0524PATCT

TMDS four pairs Differential Impedance 100ohm +-10% Matched trace length.

U31
ADV7482WBBCZ

Differential Impedance 100ohm +-10% Matched trace length from ADV7482 to R-CarH3-SiP ADV_CSI0_xxxx + CSI0_xxxx

Differential Impedance 100ohm +-10% Matched trace length from ADV7482 to R-CarH3-SiP ADV_CSI1_xxxx + CSI1_xxxx

CVBS Input Connector

CN21
LPR6520-1501F
Impedance 75ohm

Layout Note:
Following signals need Ground guard.
CVBS_AIN8(CN21 to U31-pinC10)

LC filters for ADV7482W

L35 BLM18AG102SN1D Rated current=400mA — D1.8V — MVDD_A1.8V — C398 10uF 2012 16V
L36 BLM18AG102SN1D Rated current=400mA — D1.8V — CVDD_A1.8V — C401 10uF 2012 16V
L37 BLM18AG102SN1D Rated current=400mA — D3.3V — TVDD_A3.3V — C404 10uF 2012 16V
L38 BLM18AG102SN1D Rated current=400mA — D1.8V — DVDD_D1.8V — C409 10uF 2012 16V
L39 BLM18AG102SN1D Rated current=400mA — D1.8V — AVDD_A1.8V — C414 10uF 2012 16V
L40 BLM18AG102SN1D Rated current=400mA — D3.3V — DVDDIO_D3.3V — C418 10uF 2012 16V
L41 BLM18AG102SN1D Rated current=400mA — D1.8V — PVDD_A1.8V — C421 10uF 2012 16V

MVDD_A1.8V: C391 0.1uF 1005 10V; C392 0.01uF 1005 25V; C393 0.1uF 1005 10V; C394 0.01uF 1005 25V; C395 0.1uF 1005 10V; C396 0.01uF 1005 25V
CVDD_A1.8V: C399 0.1uF 1005 10V; C400 0.01uF 1005 25V
TVDD_A3.3V: C402 0.1uF 1005 10V; C403 0.01uF 1005 25V
DVDD_D1.8V: C405 0.1uF 1005 10V; C406 0.01uF 1005 25V; C407 0.1uF 1005 10V; C408 0.01uF 1005 25V
AVDD_A1.8V: C410 0.1uF 1005 10V; C411 0.01uF 1005 25V
DVDDIO_D3.3V: C412 0.1uF 1005 10V; C413 0.01uF 1005 25V
PVDD_A1.8V: C416 0.1uF 1005 10V; C417 0.01uF 1005 25V

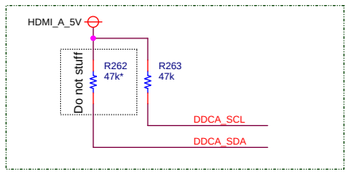
X8 NX2016SA[28.63636MHz/30pF/15ppm]
C390 47pF 1005 50V; C397 47pF 1005 50V

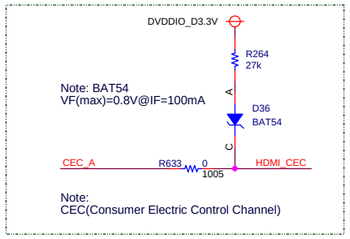
Layout Note:
Following signals need Ground guard.
GP6_30/INTRQ1, GP6_31/INTRQ2

[Design Note]
INTRQ[2:1] are configured as open-drain at the initial state. This setting can be changed.

I2C bus slave address:
ALSB==0: 0xE0 for write, 0xE1 for read.
ALSB==1: 0xE2 for write, 0xE3 for read.

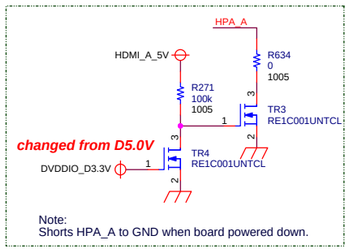
[Design Note]
Remove four resistors above in case of using other pin function.
ADV7482W supports 8-channel TDM output mode.



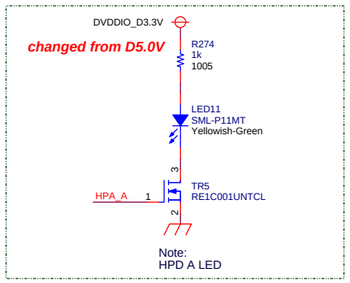


Note: BAT54
VF(max)=0.8V@IF=100mA

Note:
CEC(Consumer Electric Control Channel)



Note:
Shorts HPA_A to GND when board powered down.



Note:
HPD A LED

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MIPI CSI-2_VIN

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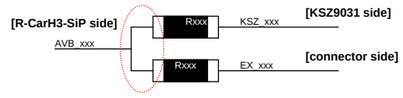
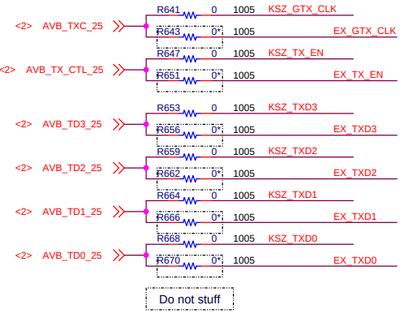
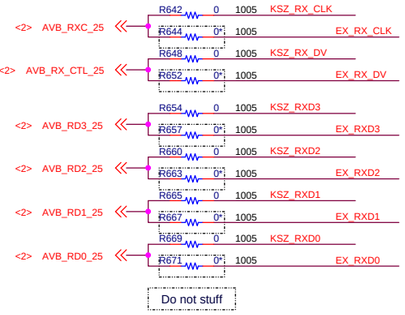
Ethernet AVB GbPHY and PHY Connector

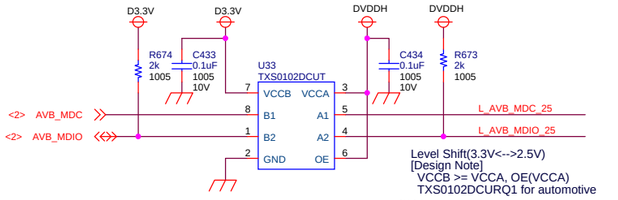
Layout Note:
As short as possible from junction of AVB_xxx to two Rxxx.

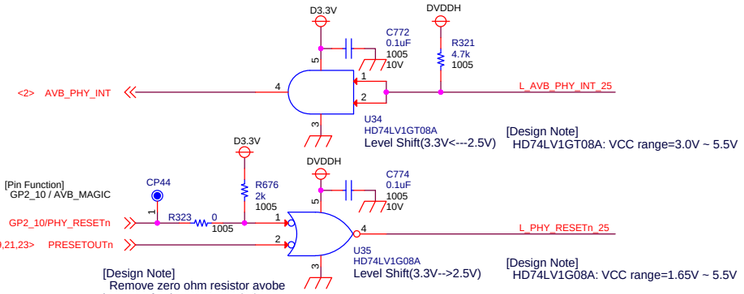


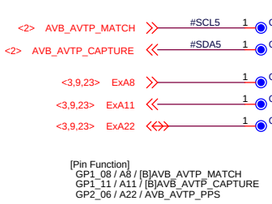
Layout Note:
Matched Trace Length from R-CarH3-Sip to KSZ9031.
(max 250Mbps/pin)
Group 1
AVB_TXC + KSZ_GTX_CLK
AVB_TX_CTL_KSZ_TX_EN
AVB_TD[3:0] + KSZ_TXD[3:0]
Group 2
AVB_RXC + KSZ_RX_CLK
AVB_RX_CTL + KSZ_RX_DV
AVB_RD[3:0] + KSZ_RXD[3:0]





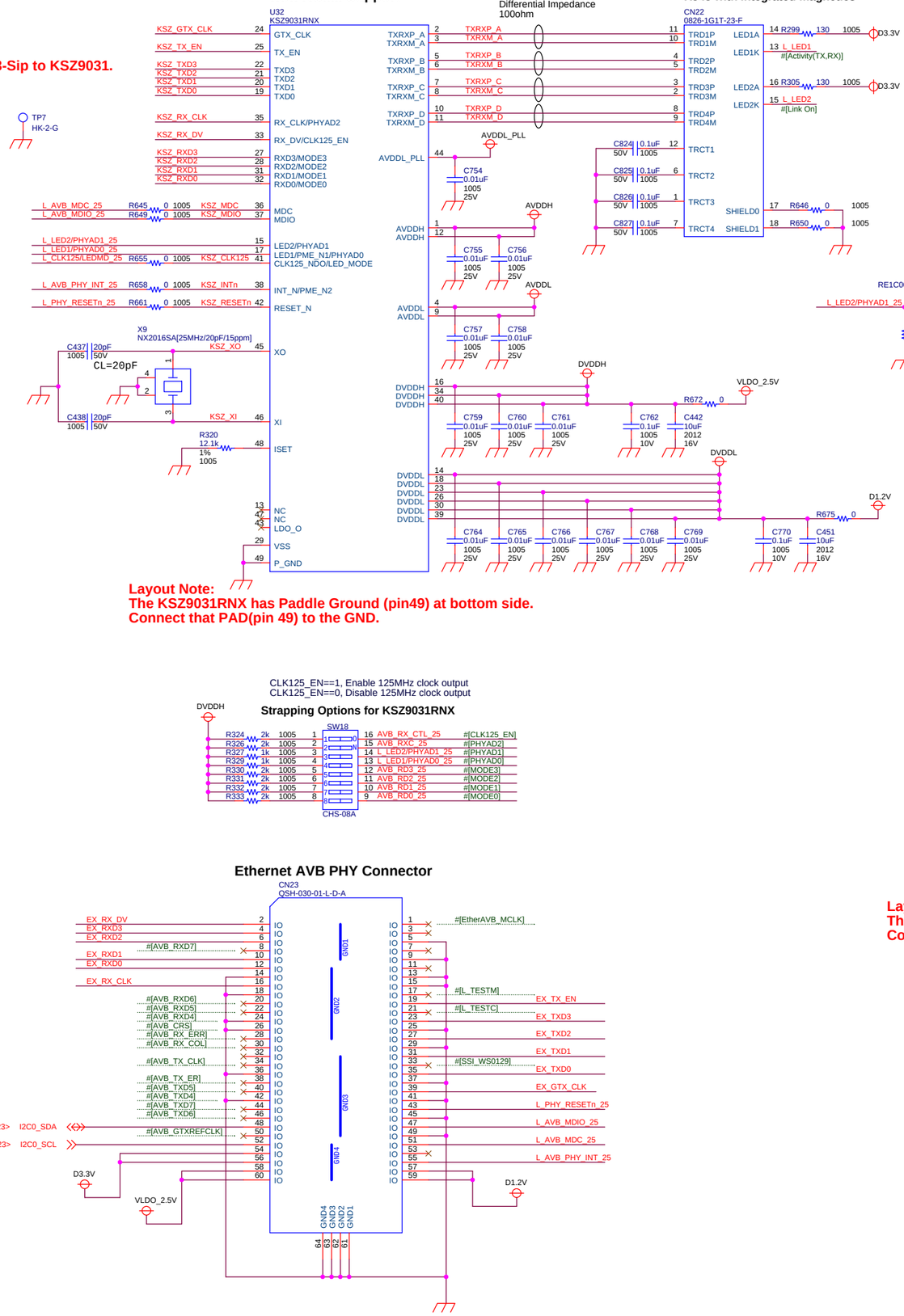






[Pin Function]
GP1_08 / A8 / [B]AVB_AVTP_MATCH
GP1_11 / A11 / [B]AVB_AVTP_CAPTURE
GP2_06 / A22 / AVB_AVTP_PPS

Gigabit Ethernet Transceiver with RGMII Support



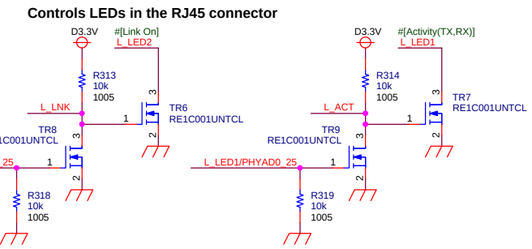
Layout Note:
The KSZ9031RNX has Paddle Ground (pin49) at bottom side.
Connect that PAD(pin 49) to the GND.

Layout Note:
Following signals need Ground guard.

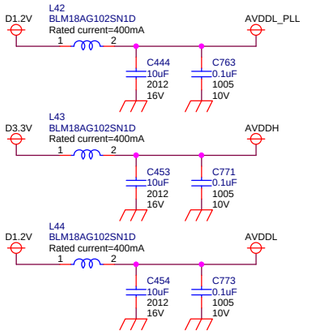
AVB_TXCREFCLK, CLK125/LEDMD_25 (125MHz)
AVB_TXC_25, KSZ_GTX_CLK, EX_GTX_CLK (125MHz)
AVB_RXC_25, KSZ_RX_CLK, EX_RX_CLK (125MHz)

Following pin has pull-down resistor at the initial state.
[2.5V-I/O]
AVB_RX_CTL, AVB_RXC, AVB_RD[3:0]
AVB_TX_CTL, AVB_TXC, AVB_TD[3:0]
[3.3V-I/O]
AVB_TXCREFCLK, AVB_MAGIC, AVB_PHY_INT, AVB_LINK

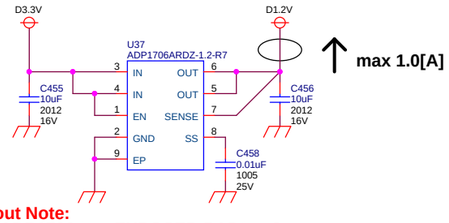
Controls LEDs in the RJ45 connector



LC filters for KSZ9031RNX



Local Regulator for KSZ9031RNX, PHY Connector



Layout Note:
The ADP1706 has EXPOSED PAD(pin9) at bottom side.
Connect that EXPOSED PAD(pin 9) to the GND.

CLK125_EN==1, Enable 125MHz clock output
CLK125_EN==0, Disable 125MHz clock output

Strapping Options for KSZ9031RNX

Ethernet AVB PHY Connector

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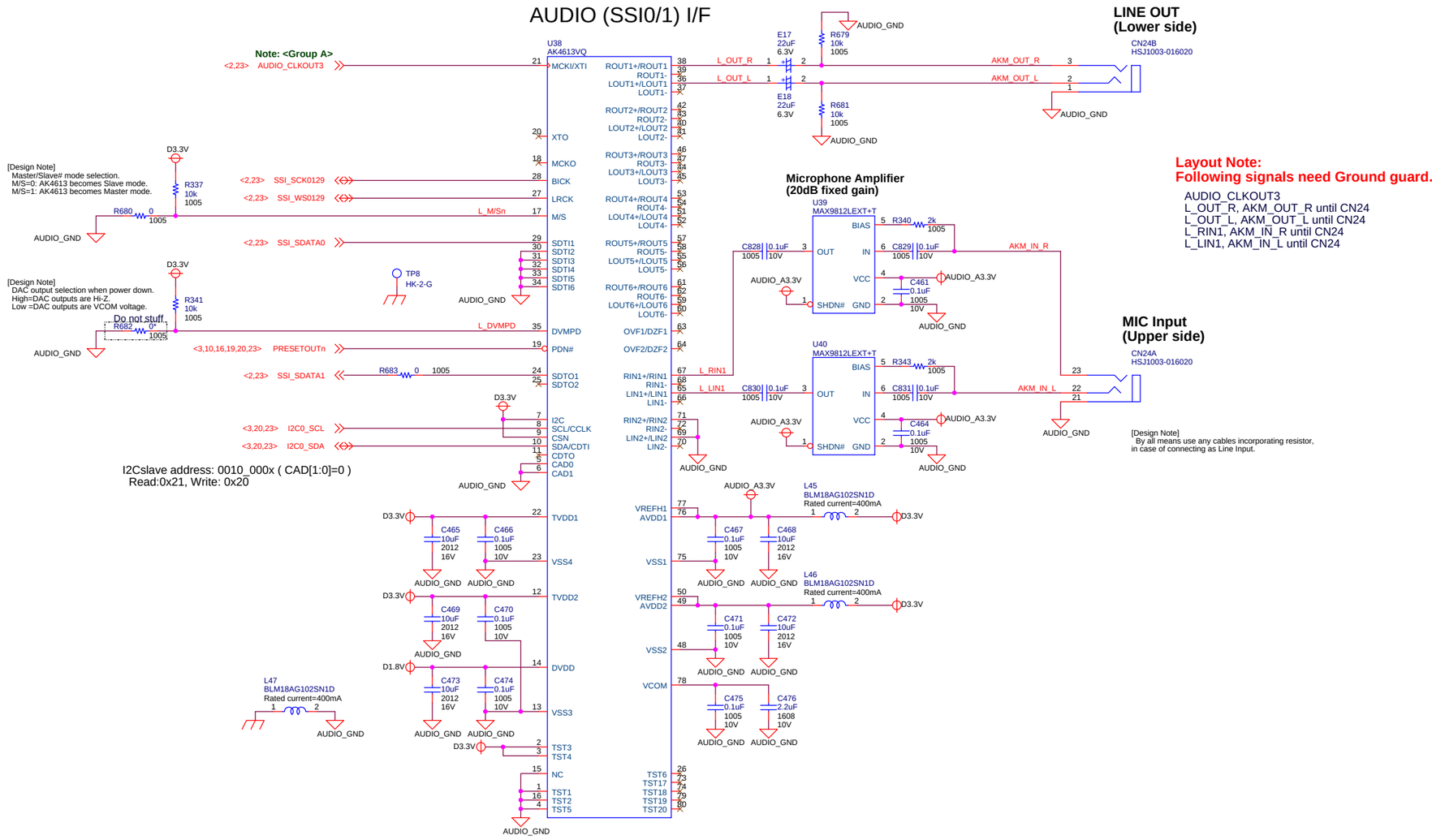
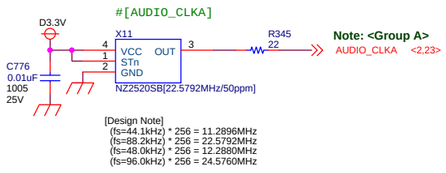
AUDIO (SSI0/1) I/F



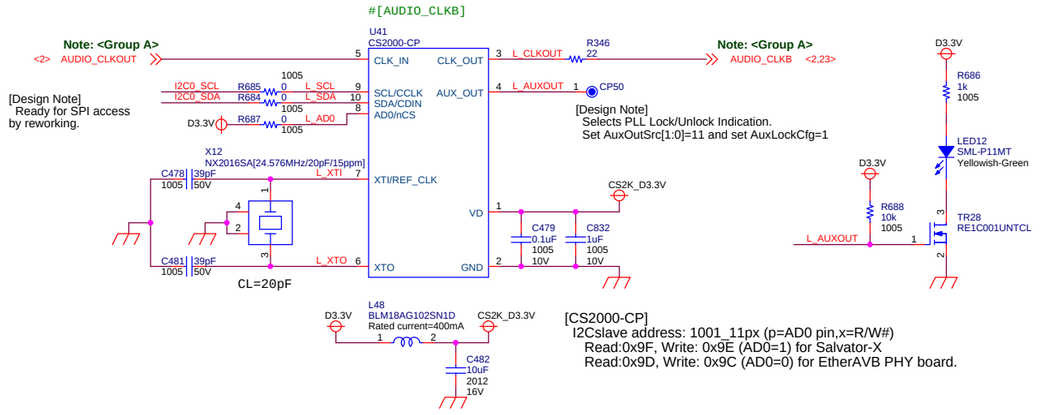
Audio Clock for 44.1kHz, 88.2kHz



Layout Note:
Following signals need Ground guard.

AUDIO_CLKA until X11-pin3
AUDIO_CLKB until U41-pin3
AUDIO_CLKOUT

Audio Clock for 48kHz, 96kHz, and for EtherAVB



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AUDIO(AK4613VQ)

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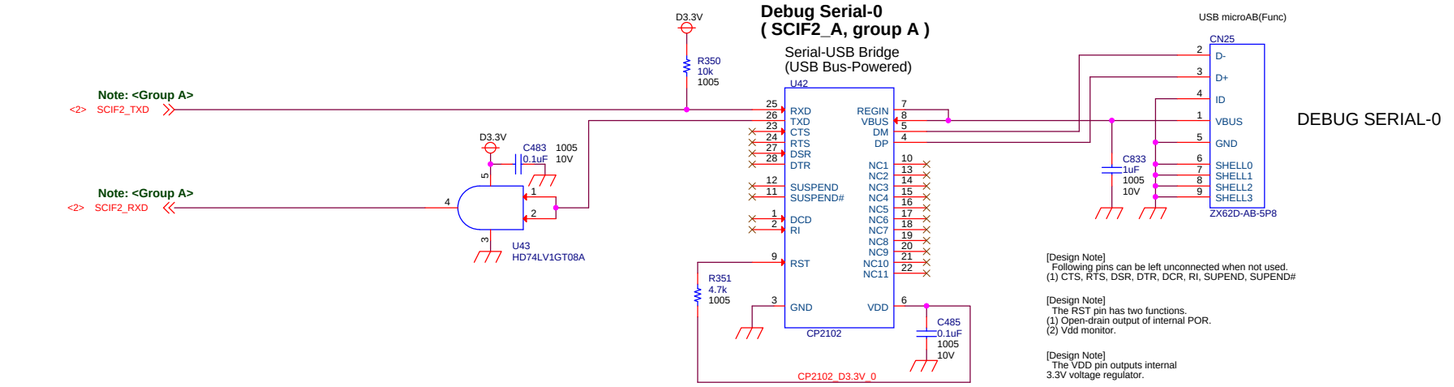
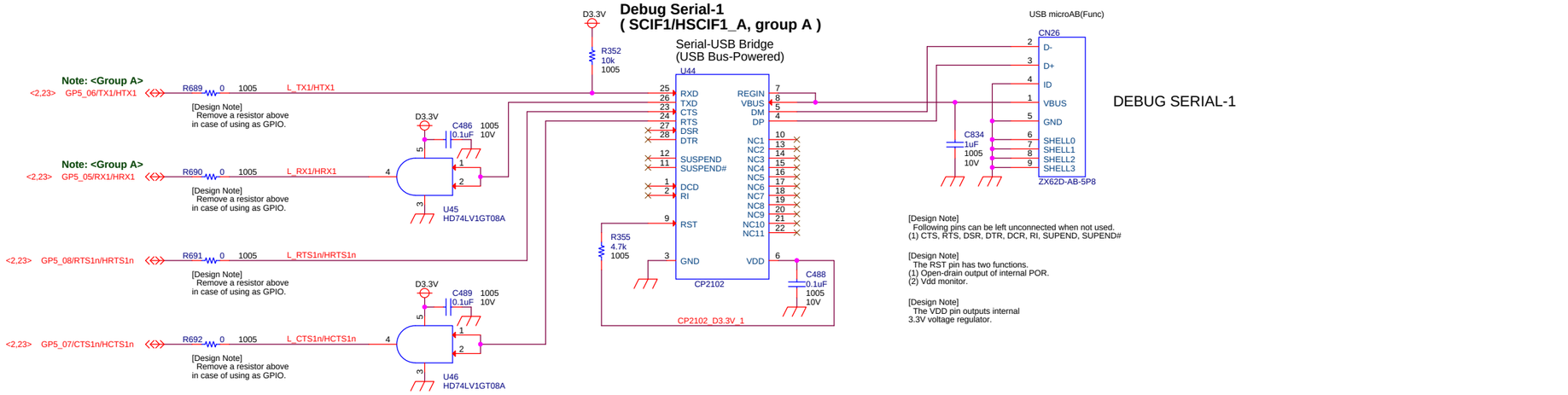
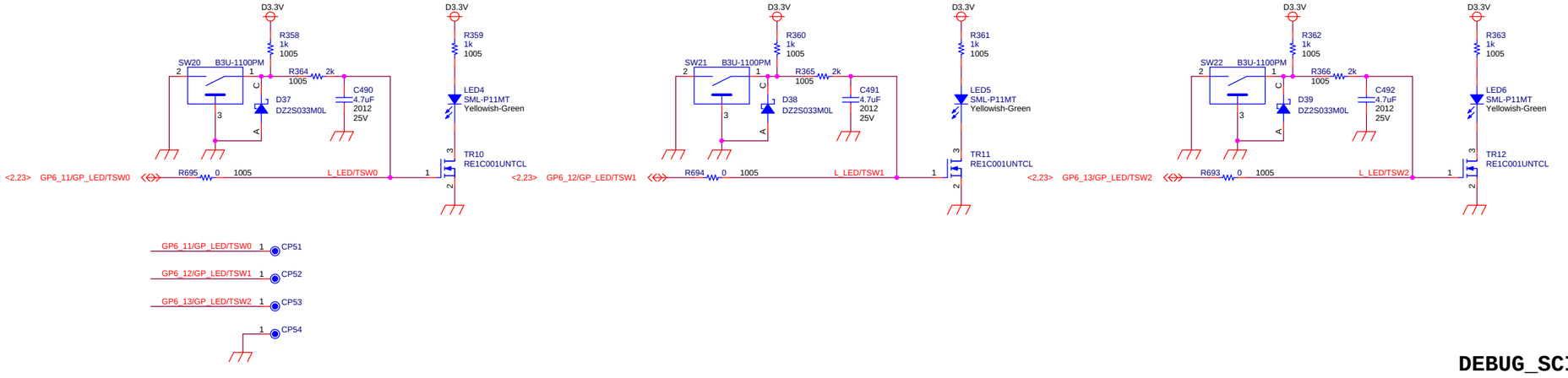




GPLED / Tact Switch

General Purpose LEDs or Tactile Switches
Following LEDs and Switches are connected to GPIO of R-CarH3-SiP



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DEBUG_SCIF/LED/TactSW 22

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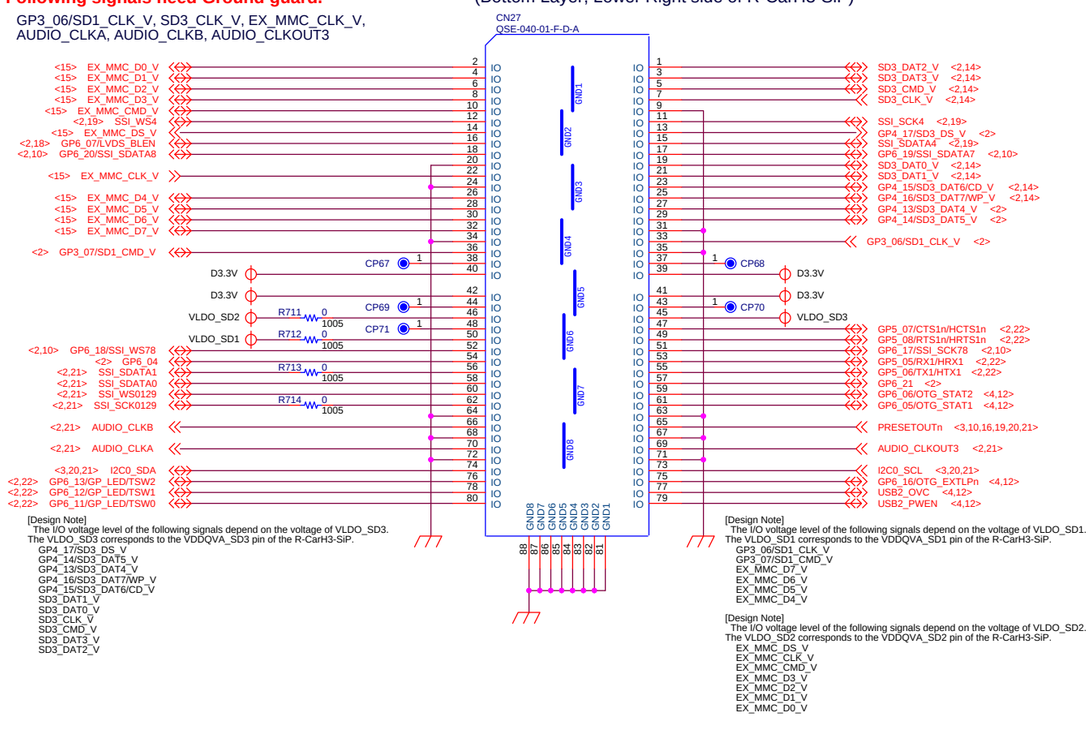
EXIO Connector A: BT/WLAN connector.
EXIO Connector B: SSI connector.
EXIO Connector C: MIPI CSI-2 connector.
EXIO Connector D: LBSC connector (Not for NOR Flash board)

#[EXIO_B]

EXIO Connector B (SSI)
(Bottom Layer, Lower Right side of R-CarH3-SiP)

Layout Note:
Following signals need Ground guard.

GP3_06/SD1_CLK_V, SD3_CLK_V, EX_MMC_CLK_V, AUDIO_CLKA, AUDIO_CLKB, AUDIO_CLKOUT3



[Design Note]
The I/O voltage level of the following signals depend on the voltage of VLDO_SD3.
The VLDO_SD3 corresponds to the VDDQVA_SD3 pin of the R-CarH3-SiP.
GP4_17/SD3_DS_V
GP4_14/SD3_DAT5_V
GP4_13/SD3_DAT4_V
GP4_16/SD3_DAT7/WP_V
GP4_15/SD3_DAT6/CD_V
SD3_DAT1_V
SD3_DAT0_V
SD3_CLK_V
SD3_CMD_V
SD3_DAT3_V
SD3_DAT2_V

[Design Note]
The I/O voltage level of the following signals depend on the voltage of VLDO_SD1.
The VLDO_SD1 corresponds to the VDDQVA_SD1 pin of the R-CarH3-SiP.
GP3_06/SD1_CLK_V
GP3_07/SD1_CMD_V
EX_MMC_D7_V
EX_MMC_D6_V
EX_MMC_D5_V
EX_MMC_D4_V

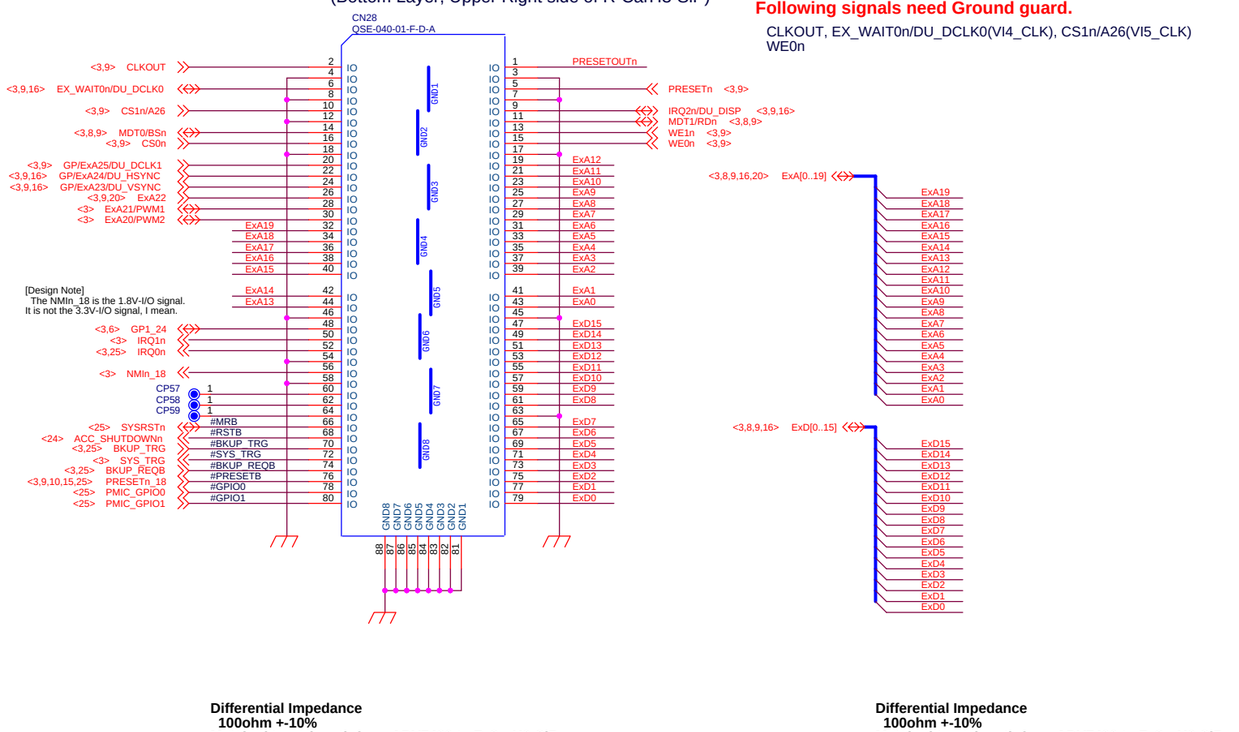
[Design Note]
The I/O voltage level of the following signals depend on the voltage of VLDO_SD2.
The VLDO_SD2 corresponds to the VDDQVA_SD2 pin of the R-CarH3-SiP.
EX_MMC_DS_V
EX_MMC_CLK_V
EX_MMC_CMD_V
EX_MMC_D3_V
EX_MMC_D2_V
EX_MMC_D1_V
EX_MMC_D0_V

#[EXIO_D]

EXIO Connector D (LBSC)
(Bottom Layer, Upper Right side of R-CarH3-SiP)

Layout Note:
Following signals need Ground guard.

CLKOUT, EX_WAIT0n/DU_DCLK0(VI4_CLK), CS1n/A26(VI5_CLK)
WE0n

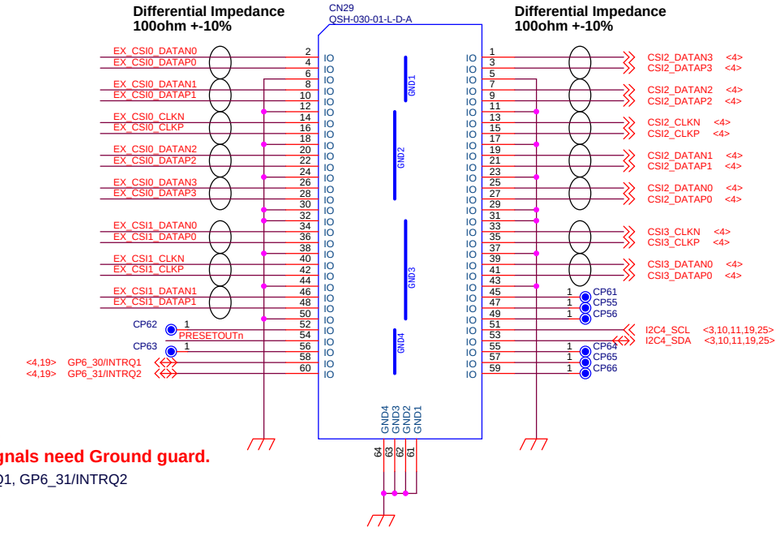


[Design Note]
The NMIn_18 is the 1.8V-I/O signal.
It is not the 3.3V-I/O signal, I mean.

#[EXIO_C]

EXIO Connector C (MIPI CSI-2)
(Bottom Layer, Upper Left side of R-CarH3-SiP)

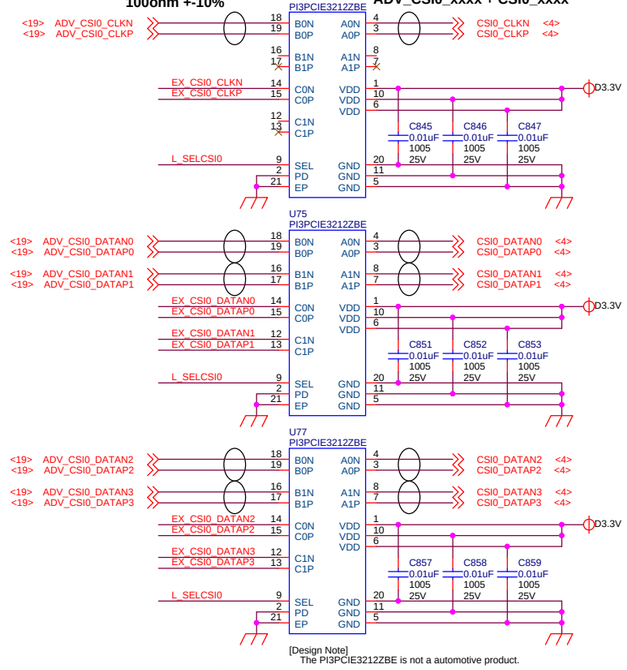
Differential Impedance
100ohm +-10%



Layout Note:
Following signals need Ground guard.

GP6_30/INTRQ1, GP6_31/INTRQ2

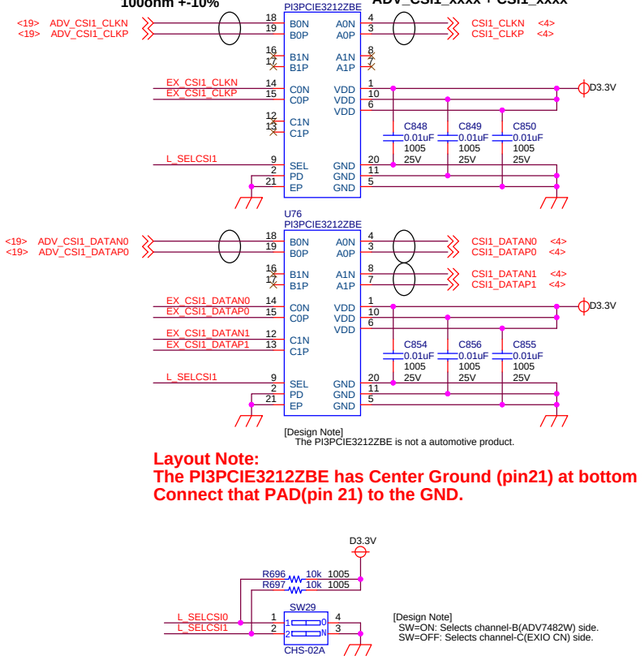
Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI0_xxxx + CSI0_xxxx



[Design Note]
The PI3PCIE3212ZBE is not a automotive product.

Layout Note:
The PI3PCIE3212ZBE has Center Ground (pin21) at bottom side.
Connect that PAD(pin 21) to the GND.

Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI1_xxxx + CSI1_xxxx



[Design Note]
The PI3PCIE3212ZBE is not a automotive product.

Layout Note:
The PI3PCIE3212ZBE has Center Ground (pin21) at bottom side.
Connect that PAD(pin 21) to the GND.

[Design Note]
SW=ON: Selects channel-B(ADV7482W) side.
SW=OFF: Selects channel-C(EXIO CN) side.

EXIO_CN/MIPI_SW

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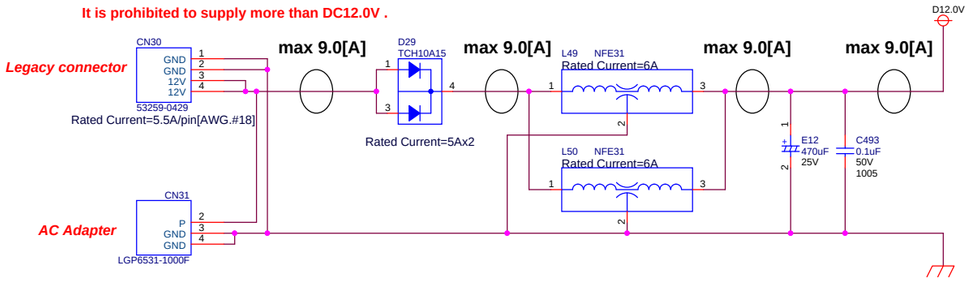
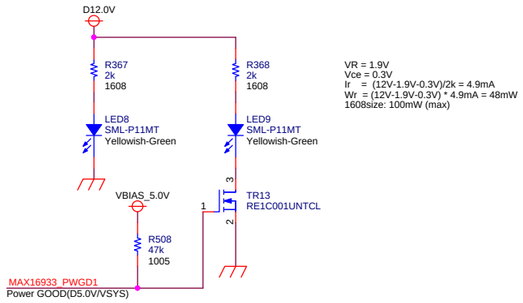
It is impossible to supply DC5.0V and DC3.3V through CN30 and CN31.

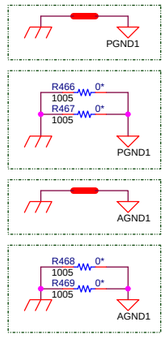
It is prohibited to supply more than DC12.0V .



LED8 and LED9 are Yellowish Green LEDs indicate Power Good.
LED8 turns on after detecting DC12.0V.
LED9 turns on after detecting D5.0V and VSYS.



VR = 1.9V
Vce = 0.3V
Ir = (12V-1.9V-0.3V)/2k = 4.9mA
Ww = (12V-1.9V-0.3V) * 4.9mA = 48mW
1608size: 100mW (max)

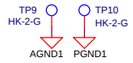


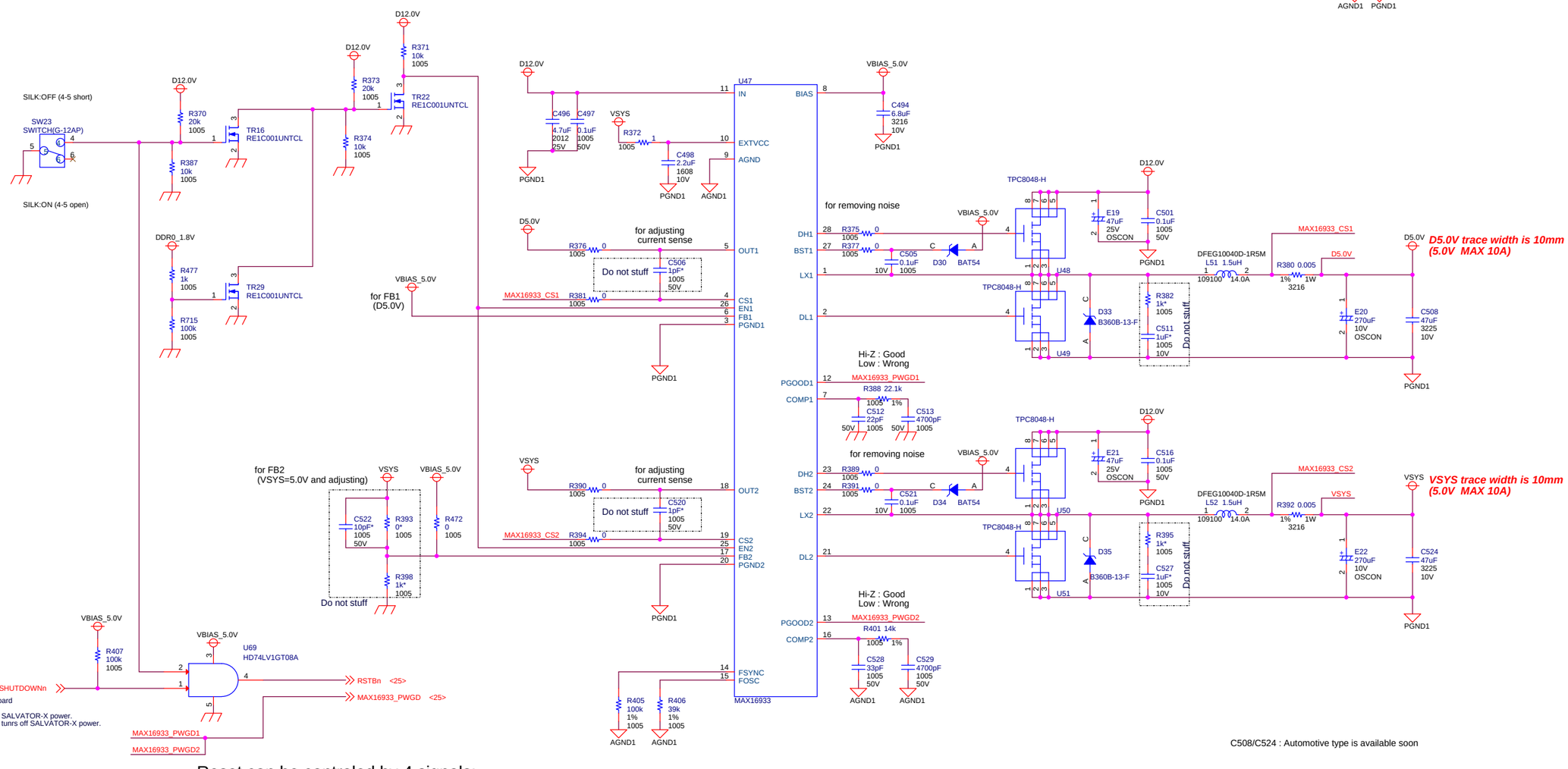
One Point Ground is more than "0.6mm VIA x 2"
Connect each other under the Exposed Pad by Layout tool.

Extra One Point Ground.
Connect each other by Layout tool.
Do not Stuff.

One Point Ground is more than "0.6mm VIA x 2"
Connect each other under the Exposed Pad by Layout tool.

Extra One Point Ground.
Connect each other by Layout tool.
Do not Stuff.



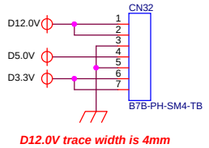


C508/C524 : Automotive type is available soon

Reset can be controled by 4 signals;
SW23(ACC Switch)
EXIO(SYSCON) : ACC_SHUTDOWNn
PowerGood D5.0V: MAX16933_PWGD1
PowerGood VSYS: MAX16933_PWGD2

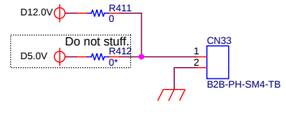
Any trigger;
Low : Reset/DDR BackUp
All triggers;
High : Active (awake Reset)

Power Supply Connector for I/O board.



D12.0V trace width is 4mm
D5.0V trace width is 2mm
D3.3V trace width is 4mm

Power Supply Connector for CPU FAN.
Place Top Layer.



Power 5V/VSYS

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RSTB
Low : Reset or DDR back-up (need to set)
High : Active (awake reset)

Reset Switch

RSTBMODE(Low=Level, Hi=Pulse)

Do not Stuff

thermistor

RSTB : Internal pull-up(100k V3P3) with schmid.

MRB: Internal pull-up(100k V3P3)

SYNC : Internal pull-down(100k)

AVS0/AVS1 : Internal pull-down(100k)

BOOST :Internal pull-down(100k)

BKUP_REQB Internal pull-down(100k)

Do not stuff

Do not stuff

I2Cslave address: 0110_000x
Read:0x61, Write: 0x60

I2C EEPROM for PMIC

I2Cslave address: 1010_000x
Read:0xA1, Write: 0xA0

[Design Note]
WP=GND means writeable.
VCC range=1.7V ~ 5.5V

U57 Layout Note:
GND can be changed to MASTER GND, if to connect AGND2 is difficult.

SYSTEM Reset LED

Back up LED

C540/C542 : Automotive type is available soon

Current-Sense Amplifiers with ADC for DVFS0.8V

I2Cslave address: 1111_111x
Read:0xFF, Write: 0xFE

U58/U59 Layout Note:
GND can be changed to MASTER GND, if to connect PGND2 is difficult.

Current-Sense Amplifiers with ADC for VDD0.8V

I2Cslave address: 1111_100x
Read:0xF9, Write: 0xF8

TOP VIEW of BD9571MWV-M

Exposed PAD

U67 Layout Note:
BD9571MWV-M has a exposed pad at bottom side.
CONNECT to MASTER GND.

VSYS=5.0V trace width is 10mm

D5.0V trace width is 10mm

GND

One Point Ground (But number of via need to consider).
Connect each other by Layout tool.

Extra One Point Ground.
Connect each other by Layout tool.
Do not Stuff.

DVFS : DCDC controler

for Current-Sense Amplifier (U58)

DVFS0.8V trace width is 16mm
(0.8V MAX 16A)
0.500V - 1.200V (25mV step)

FB_DVFS/REMOTE_M_DVFS Layout Note:
these are led from the neiborhood of SoC ball in pairs.

for measurement Target Impedance Layout solder side.

VD09: DCDC controler

for Current-Sense Amplifier (U59)

VDD0.8V trace width is 8mm
(0.8V MAX 8A)
0.500V - 1.200V (25mV step)

FB_VD09 Layout Note: this is led from the neiborhood of SoC ball.

for measurement Target Impedance Layout solder side.

DDR0C-DDR1C: LDO

DDR0_1.8V/DDR1_1.8V
(1.8V MAX 170mA)

DDR0: DCDC

DDR0_1.1V trace width is 4mm
(1.8V MAX 4A)

DDR1: DCDC

DDR1_1.1V trace width is 4mm
(1.8V MAX 4A)

VD18: DCDC

D1.8V trace width is 3mm
(1.8V MAX 3A)
1.625V - 2.000V (25mV step)

VD33: DCDC

D3.3V trace width is 3mm
(3.3V MAX 3A)
2.800V - 3.800V (100mV step)

VD25: LDO

VLDO2.5V
(2.5V MAX 300mA)
2.150V - 2.900V (50mV step)

SD0-SD3: LDO

VLDO_SD0/VLDO_SD1/VLDO_SD2/VLDO_SD3
(1.8V/3.3V MAX 170mA)

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Power PMIC

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