User's Manual

RENESAS

CONFIDENTIAL

Linux Interface Specification Kernel Core

User's Manual: Software

R-Car H3/M3/M3N/E3/D3/V3U/V3H Series

Renesas Electronics
www.renesas.com

Rev.3.00 Dec. 2021

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Trademark

- Linux® is the registered trademark of Linus Torvalds in the U.S. and other countries.
- Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
- Other company names and product names mentioned herein are registered trademarks or trademarks of their respective owners.
- Registered trademark and trademark symbols (® and ™) are omitted in this document

How to Use This Manual

- **[Readers]**
  This manual is intended for engineers who develop products which use the R-Car H3/M3/M3N/E3/D3/V3U/V3H processor.

- **[Purpose]**
  This manual is intended to give users an understanding of the functions of the R-Car H3/M3/M3N/E3/D3/V3U/V3H processor device driver and to serve as a reference for developing hardware and software for systems that use this driver.

- **[How to Read This Manual]**
  It is assumed that the readers of this manual have general knowledge in the fields of electrical
  — engineering, logic circuits, microcontrollers, and Linux.
  → Read this manual in the order of the CONTENTS.
  — To understand the functions of a multimedia processor for R-Car H3/M3/M3N/E3/D3/V3U/V3H
  → See the R-Car H3/M3/M3N/E3/D3/V3U/V3H User's Manual.
  — To know the electrical specifications of the multimedia processor for R-Car H3/M3/M3N/E3/D3/V3U/V3H
  → See the R-Car H3/M3/M3N/E3/D3/V3U/V3H Data Sheet.

- **[Conventions]**
  The following symbols are used in this manual.
  Data significance: Higher digits on the left and lower digits on the right
  Note: Footnote for item marked with Note in the text
  Caution: Information requiring particular attention
  Remark: Supplementary information
  Numeric representation: Binary ... ××××, 0b××××, or ××××B
  Decimal ... ××××
  Hexadecimal ... 0x×××× or ××××H
  Data type: Double word … 64 bit
  Word … 32 bits
  Half word ... 16 bits
  Byte ... 8 bits

Table of Contents

1. Overview

1.1 Overview

This manual explains the part that added for the R-Car H3/M3/M3N/E3/D3/V3U/V3H in the basic functions of the Linux kernel for the R-Car H3-SiP/M3-SiP/E3/D3/V3U/V3H System Evaluation Board. Detailed explanation is skipped because the interface of this module is based on Linux.

This kernel is based on v5.10

1.2 Function

This kernel supports the following functions.

- Single Processing / SMP
- big.LITTLE (R-Car H3 , M3)
- I-Cache / D-Cache / L2 Cache
- Clock Pulse Generator (CPG)
- Pin Function Controller (PFC)
- Kernel System Timer
  - ARM architected timer
  - High Resolution Timer (hrtimers)
- Device Tree
- Multiplatform Configuration (Legacy board Configuration is not-support)
- Refer to IPMMU User's Manual documentation for the following function:
  - IPMMU
- Refer to Power Management User's Manual documentation for the following function:
  - CPU Hotplug
  - CPU Idle
  - CPU Freq (DVFS/AVS)
  - Runtime PM
  - System Suspend To RAM
- Safe Rendering Support

1.3 Reference

1.3.1 Standard

There is no reference document on standards.

1.3.2 Related documents

The following table shows the document related to this kernel.

Table 1-1 Related document (R-Car H3/M3/M3N/E3/D3/V3U/V3H)

Number	Issue	Title	Edition	Date
-	Renesas Electronics	R-Car Series, 3rd Generation User's Manual:Hardware	Rev.2.20	Jun. 30, 2020
	Renesas Electronics	R-Car V3U Series User's Manual	Rev.0.5	Jul. 31, 2020
-	Renesas Electronics	R-CarH3-SiP System Evaluation Board Salvator-X Hardware Manual RTP0RC7795SIPB0011S	Rev.1.09	May. 11, 2017
-	Renesas Electronics	R-CarM3-SiP System Evaluation Board Salvator-X Hardware Manual RTP0RC7796SIPB0011S	Rev.0.04	Oct. 3, 2016
-	Renesas Electronics	R-CarH3-SiP/M3-SiP/M3N-SiP System Evaluation Board Salvator-XS Hardware Manual	Rev.2.04	Jul. 17, 2018
-	Renesas Electronics	R-CarE3 System Evaluation Board Ebisu Hardware Manual RTP0RC77990SEB0010S	Rev.0.03	Apr.11, 2018
-	Renesas Electronics	R-CarE3 System Evaluation Board Ebisu-4D (E3 board 4xDRAM) Hardware Manual	Rev.1.01	Jul. 19, 2018
	Renesas Electronics	R-CarV3U System Evaluation Board Falcon Hardware Manual	Rev.0.01	Sep. 11, 2020
	Renesas Electronics	R-CarV3H System Evaluation Board Condor-I	Rev.0.02	Nov. 2019
	Renesas Electronics	R-Car V3H_2 Additional Document for User's Manual: Hardware	Rev.0.50	Jul 2020
	Renesas Electronics	R-CarD3 System Evaluation Board Hardware Manual RTP0RC77995SEB0010S	Rev.1.20	Jul. 25, 2017

1.4 Restrictions

- None.

2. Terminology

The following table shows the terminology related to this kernel.

Table 2-1 Terminology

Terms	Explanation
CPG	**C**lock **P**ulse **G**enerator
MSSR	**M**odule **S**tandby, **S**oftware **R**eset
PFC	**P**in **F**unction **C**ontroller
DVFS	**D**ynamic **V**oltage **F**requency **S**caling
AVS	**A**daptive **V**oltage **S**caling
GIC	**G**eneric **I**nterrupt **C**ontroller
DIV6	**Div**iders with **6**-bit (1 to 64) ratio
IOMMU	**I**nput/**O**utput **M**emory **M**anagement **U**nit
Runtime PM	**Runtime** **P**ower **M**anagement
PMIC	**P**ower **M**anagement **I**ntegrated **C**ircuit
PSCI	**P**ower **S**tate **C**oordinate **I**nterface
APMU	**A**dvanced **P**ower **M**anagement **U**nit for AP-System Core
CA57	**C**ortex **A57** for AP-System Core
CA53	**C**ortex **A53** for AP-System Core
SPI	**S**hared **P**rocessor **I**nterrupts
PPI	**P**er **P**rocessor **I**nterrupts
CMA	**C**ontinuous **M**emory **A**llocator
MMP	**M**ulti**M**edia **P**ackage
VMSA	**V**irtual **M**emory **S**ystem **A**rchitecture
IPMMU	**M**emory **M**anagement **U**nit for H/W **IP**

3. Operating Environment

3.1 Hardware Environment

The following table shows the hardware needed to use this kernel.

Table 3-1 Hardware environment (R-Car H3/M3/M3N/E3/D3/V3U/V3H)

Name	Version	Manufacturer
R-CarH3-SiP System Evaluation Board Salvator-X	-	Renesas Electronics
R-CarM3-SiP System Evaluation Board Salvator-X	-	Renesas Electronics
R-CarH3-SiP/M3-SiP/M3N-SiP System Evaluation Board Salvator-XS	-	Renesas Electronics
R-CarE3 System Evaluation Board Ebisu	-	Renesas Electronics
R-CarE3 System Evaluation Board Ebisu-4D	-	Renesas Electronics
R-CarV3U System Evaluation Board Falcon		Renesas Electronics
R-CarV3H System Evaluation Board Condor-i	-	Renesas Electronics
R-CarD3 System Evaluation Board Draak		Renesas Electronics

3.2 Module Configuration

The following figure shows the configuration of the Interrupt / Clock.

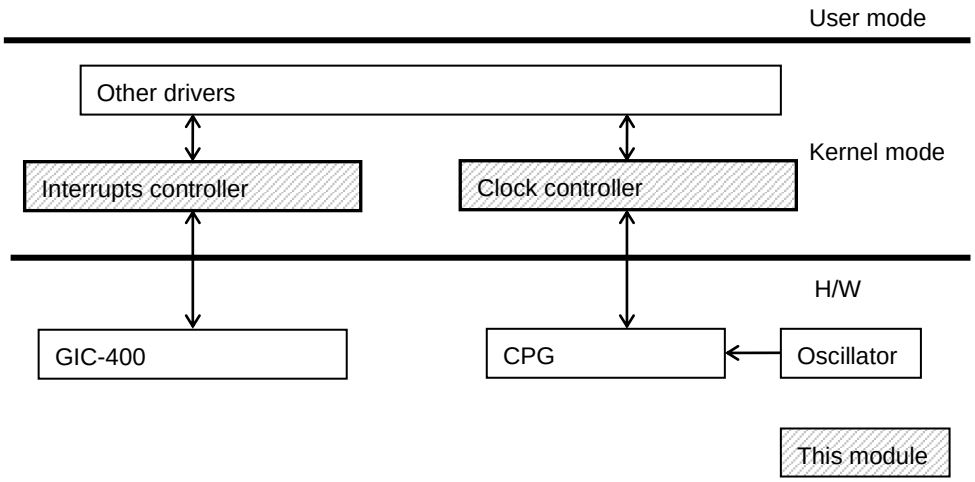

Figure 3-1 Interrupt / Clock Configuration

4. Memory management

4.1 Physical memory

This kernel manages the following memory.

Table 4-1 Physical memory (R-Car H3 Ver.2.0)

Kind of memory	size	Physical address
Main memory	3968MB	0x00-48000000 ~ 0x00-7fffffff 0x05-00000000 ~ 0x05-3fffffff 0x06-00000000 ~ 0x06-3fffffff 0x07-00000000 ~ 0x07-3fffffff

Table 4-2 Physical memory (R-Car H3 Ver.3.0)

Kind of memory	size	Physical address
Main memory	8064MB	0x00-48000000 ~ 0x00-bfffffff 0x05-00000000 ~ 0x05-7fffffff 0x06-00000000 ~ 0x06-7fffffff 0x07-00000000 ~ 0x07-7fffffff

Table 4-3 Physical memory (R-Car M3 Ver.1.x)

Kind of memory	size	Physical address
Main memory	3968MB	0x00-48000000 ~ 0x00-bfffffff 0x06-00000000 ~ 0x06-7fffffff

Table 4-4 Physical memory (R-Car M3 Ver.3.0)

Kind of memory	size	Physical address
Main memory	8064MB	0x00-48000000 ~ 0x00-bfffffff 0x04-80000000 ~ 0x04-ffffffff 0x06-00000000 ~ 0x06-ffffffff

Table 4-5 Physical memory (R-Car M3N)

Kind of memory	size	Physical address
Main memory	1920MB	0x00-48000000 ~ 0x00-bfffffff

Table 4-6 Physical memory (R-Car E3 System Evaluation Board Ebisu)

Kind of memory	size	Physical address
Main memory	896MB	0x00-48000000 ~ 0x00-7fffffff

Table 4-7 Physical memory (R-Car E3 System Evaluation Board Ebisu-4D)

Kind of memory	size	Physical address
Main memory	1920MB	0x00-48000000 ~ 0x00-bfffffff

Table 4-8 Physical memory (R-Car D3)

Kind of memory	size	Physical address
Main memory	384MB	0x00-48000000 ~ 0x00-5fffffff

Table 4-9 Physical memory (R-Car V3U System Evaluation Board)

Kind of memory	size	Physical address
Main memory	8064MB	0x00-48000000 ~ 0x00-bfffffff 0x05-00000000 ~ 0x05-7fffffff 0x06-00000000 ~ 0x06-7fffffff 0x07-00000000 ~ 0x07-7fffffff

Table 4-10 Physical memory (R-Car V3H System Evaluation Board)

Kind of memory	size	Physical address
Main memory	1920MB	0x00-48000000 ~ 0x00-bfffffff

4.2 Memory map

The following Figure shows the kernel memory map.

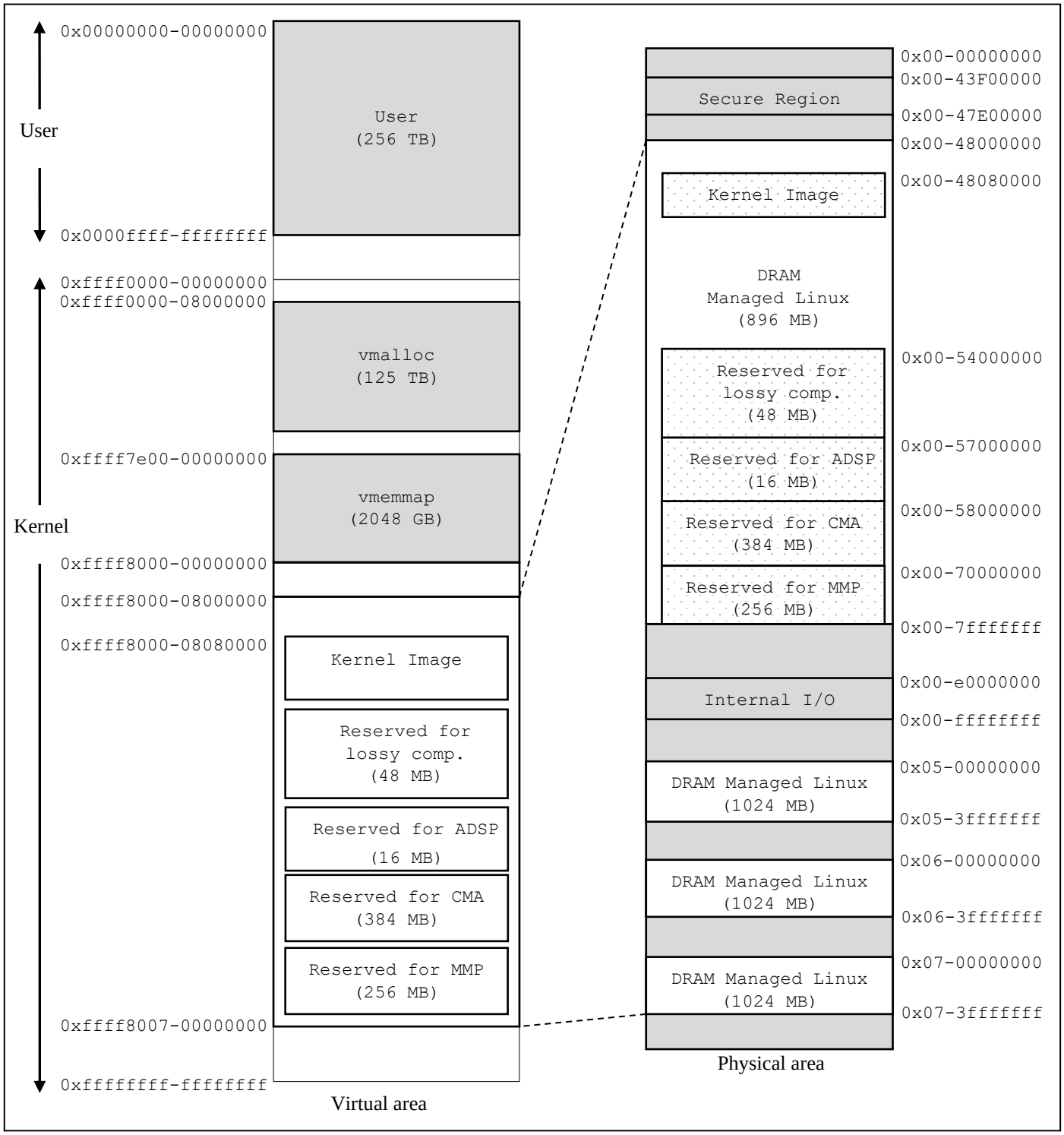

Figure 4-1 Memory map of kernel (R-Car H3 Ver.2.0)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

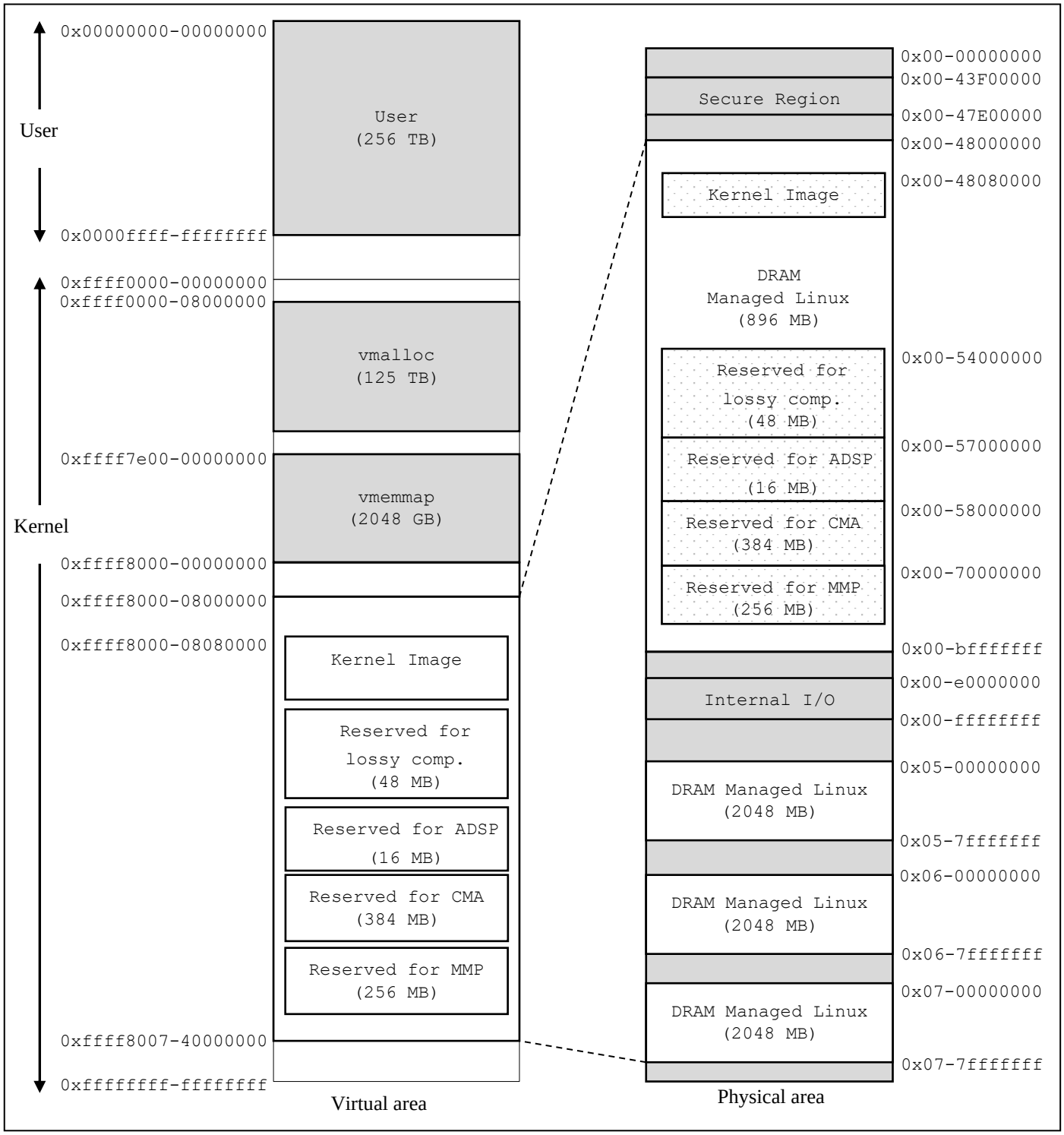

Figure 4-2 Memory map of kernel (R-Car H3 Ver.3.0)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

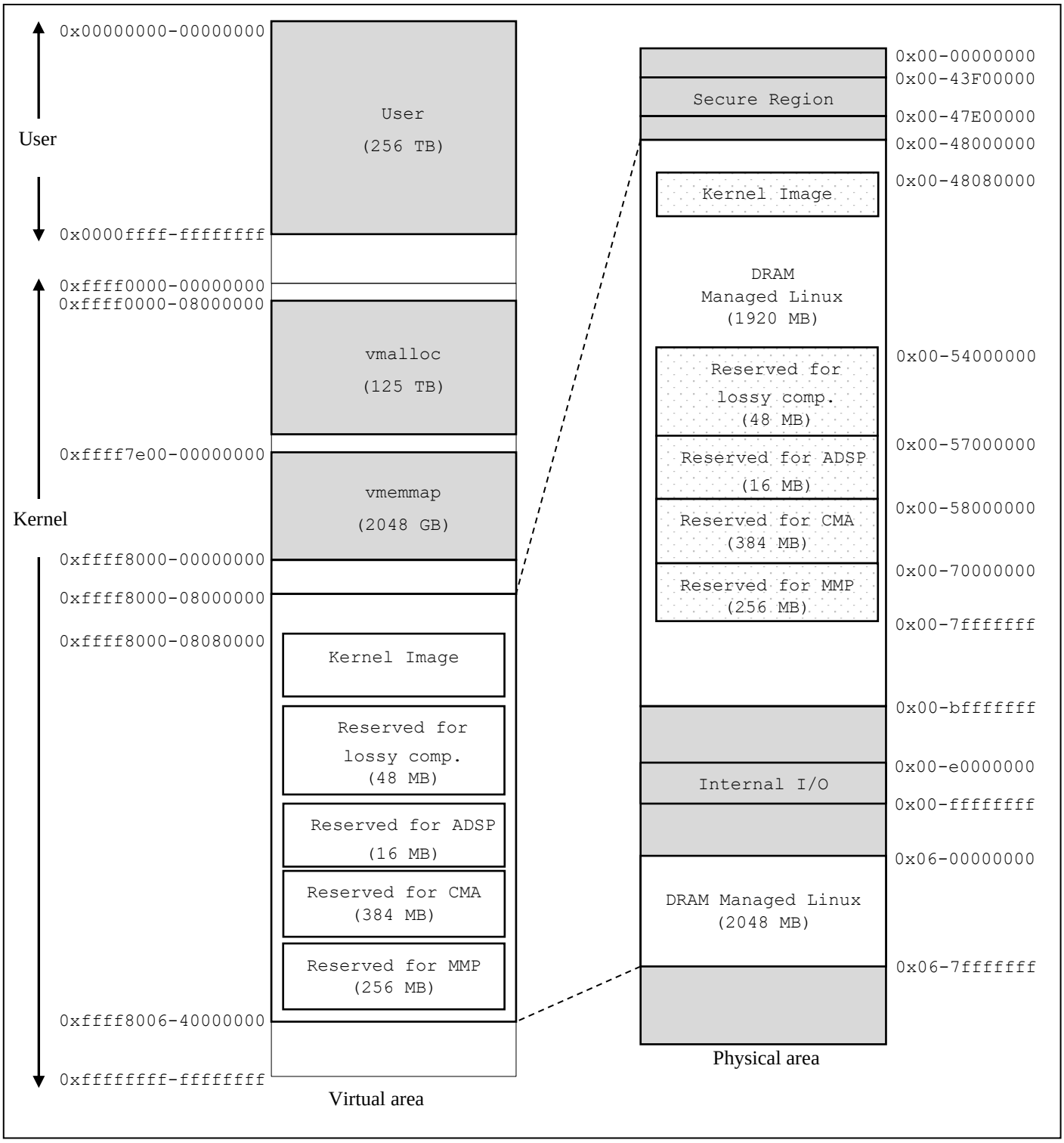

Figure 4-3 Memory map of kernel (R-CarM3 Ver.1.x)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

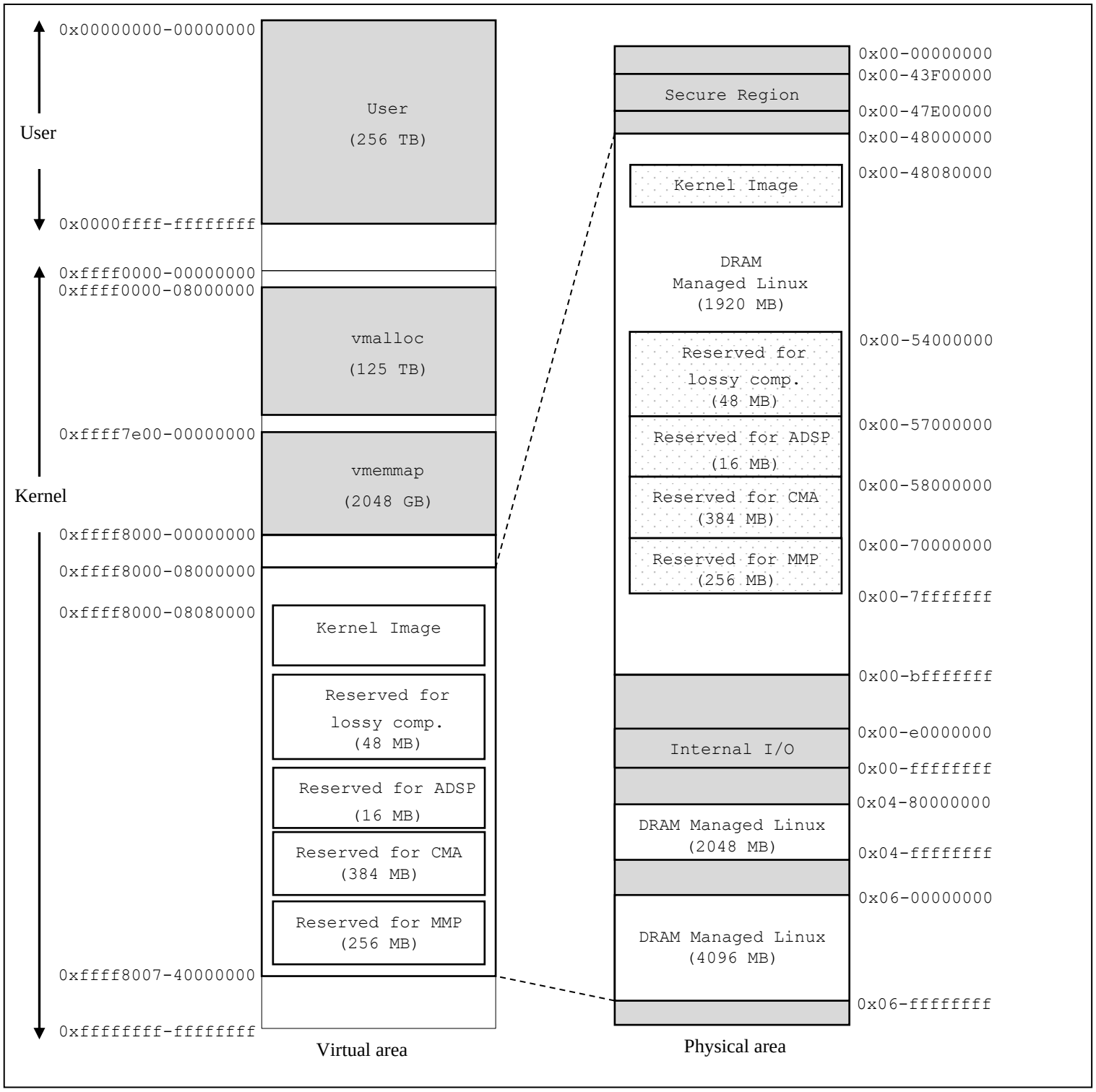

Figure 4-4 Memory map of kernel (R-CarM3 Ver.3.0)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

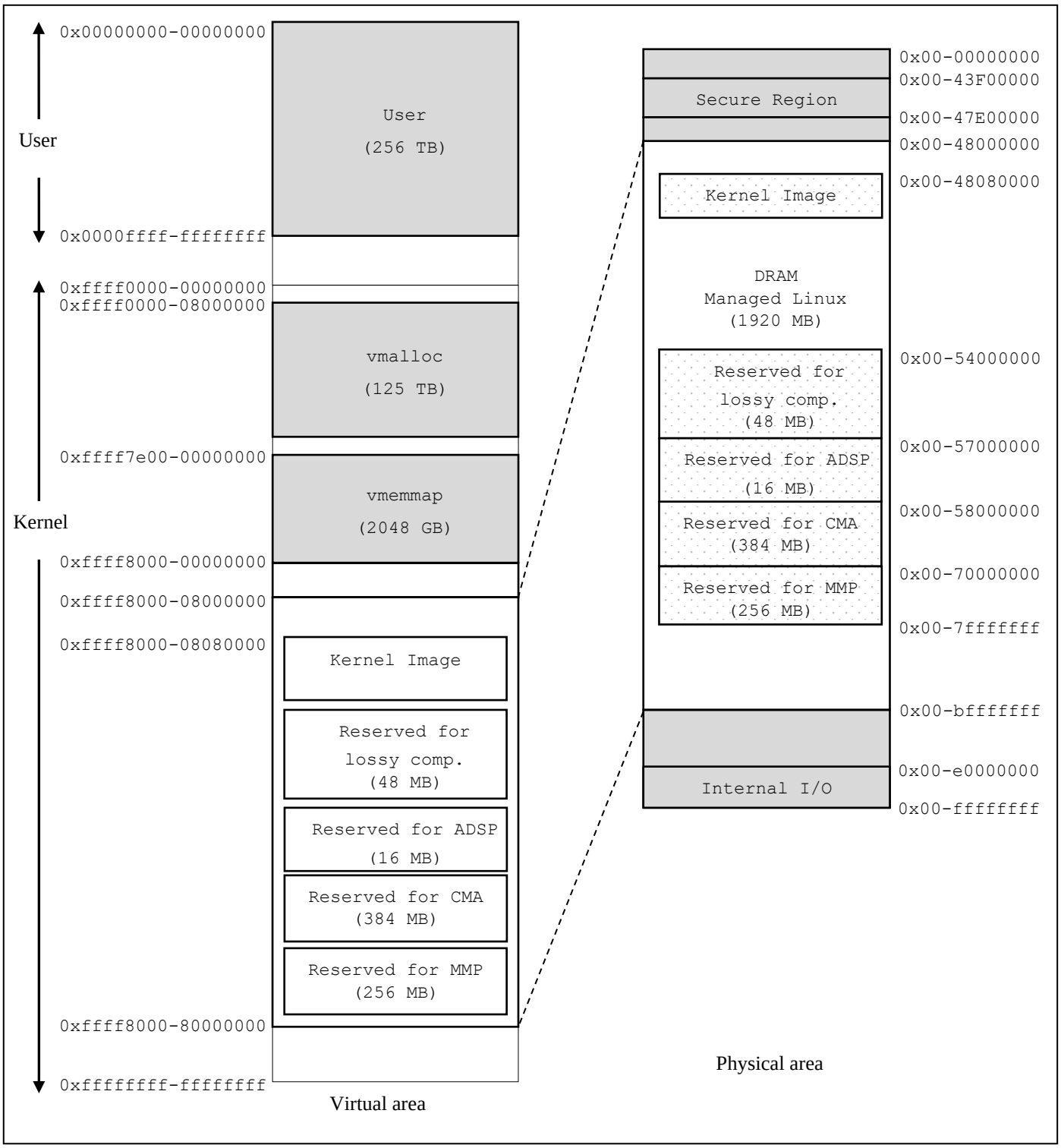

Figure 4-5 Memory map of kernel (R-Car M3N)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

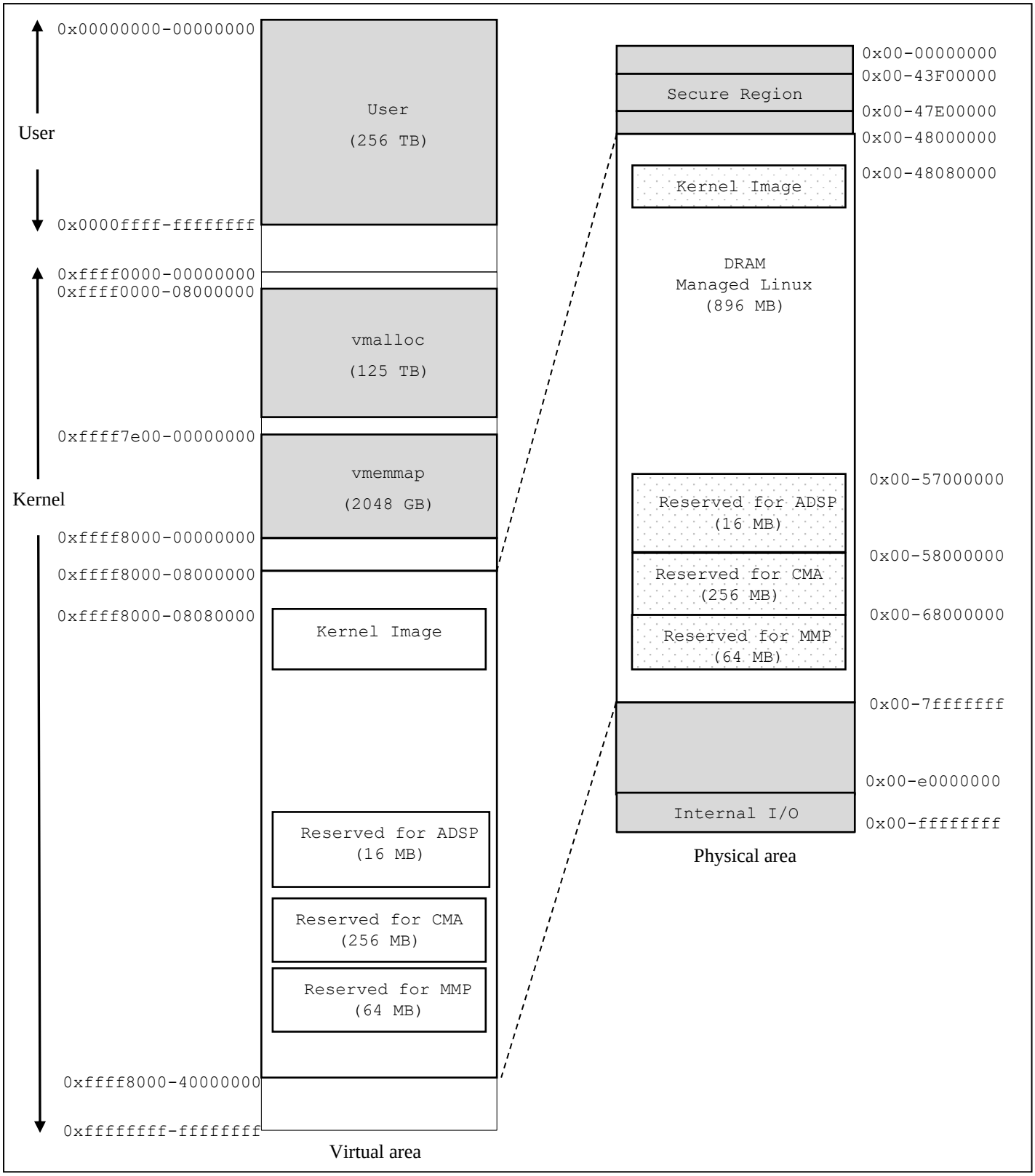

Figure 4-6 Memory map of kernel (R-Car E3 System Evaluation Board Ebisu)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

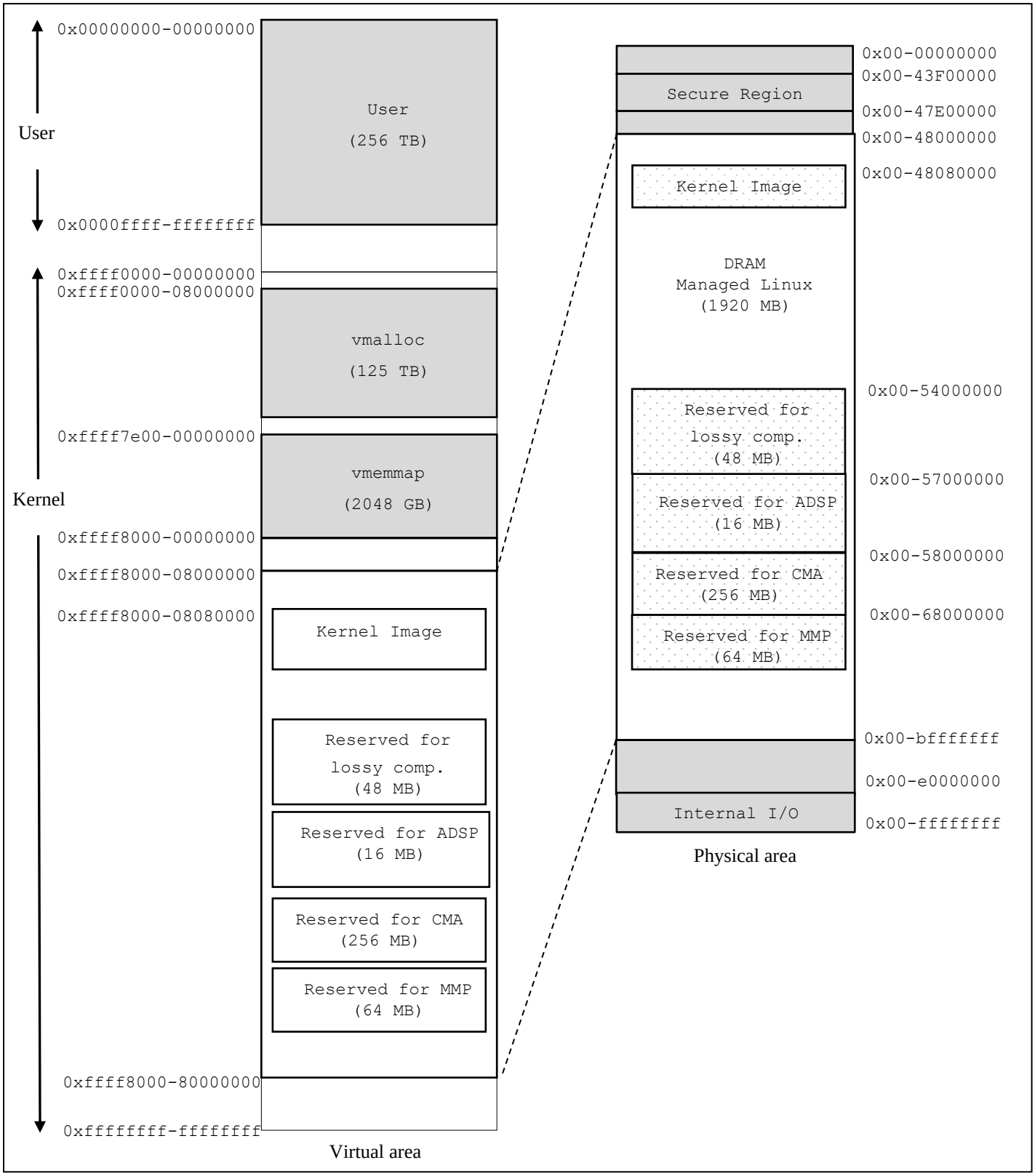

Figure 4-7 Memory map of kernel (R-Car E3 System Evaluation Board Ebisu-4D)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

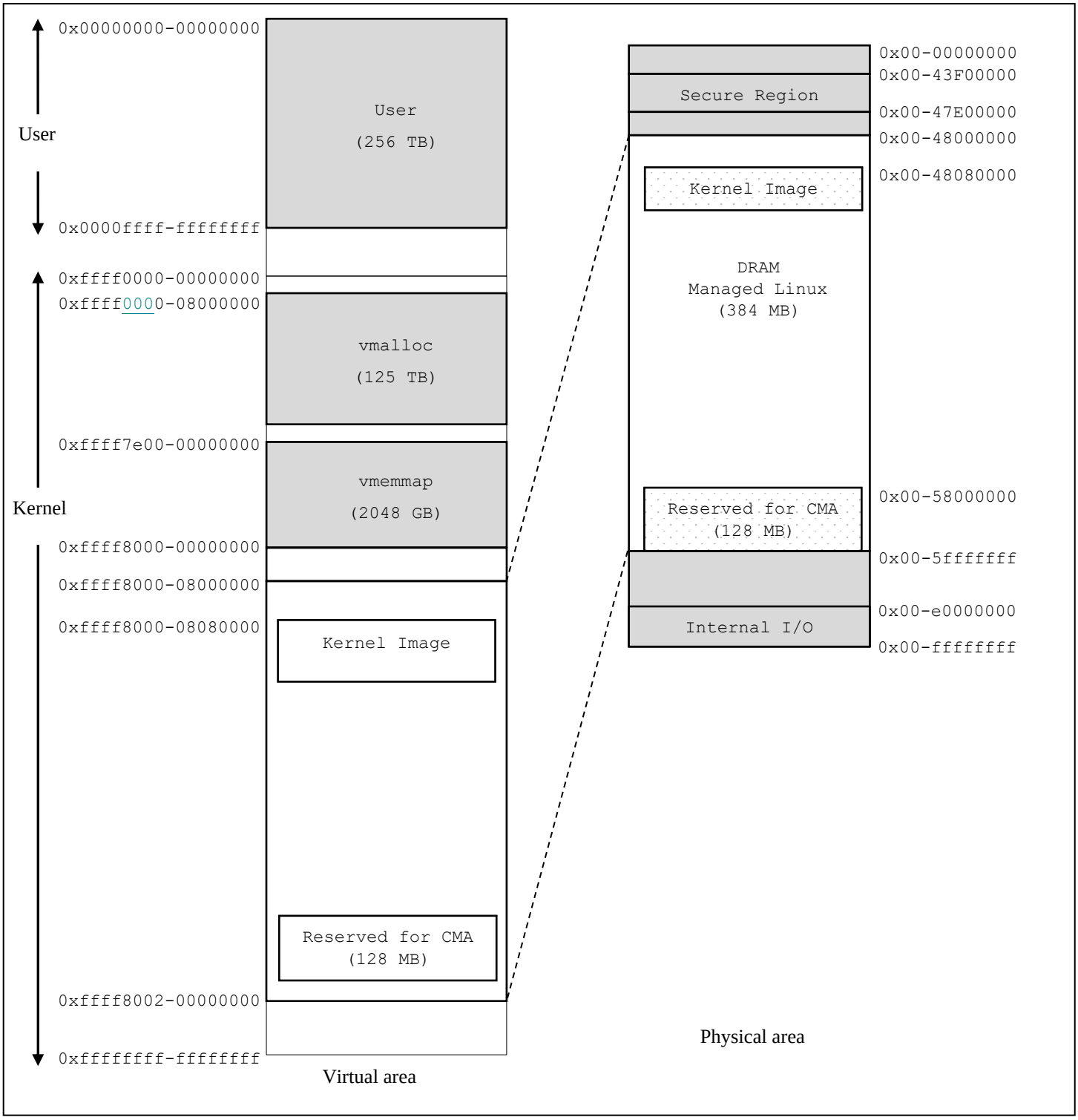

Figure 4-8 Memory map of kernel (R-Car D3)

- Note)
- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

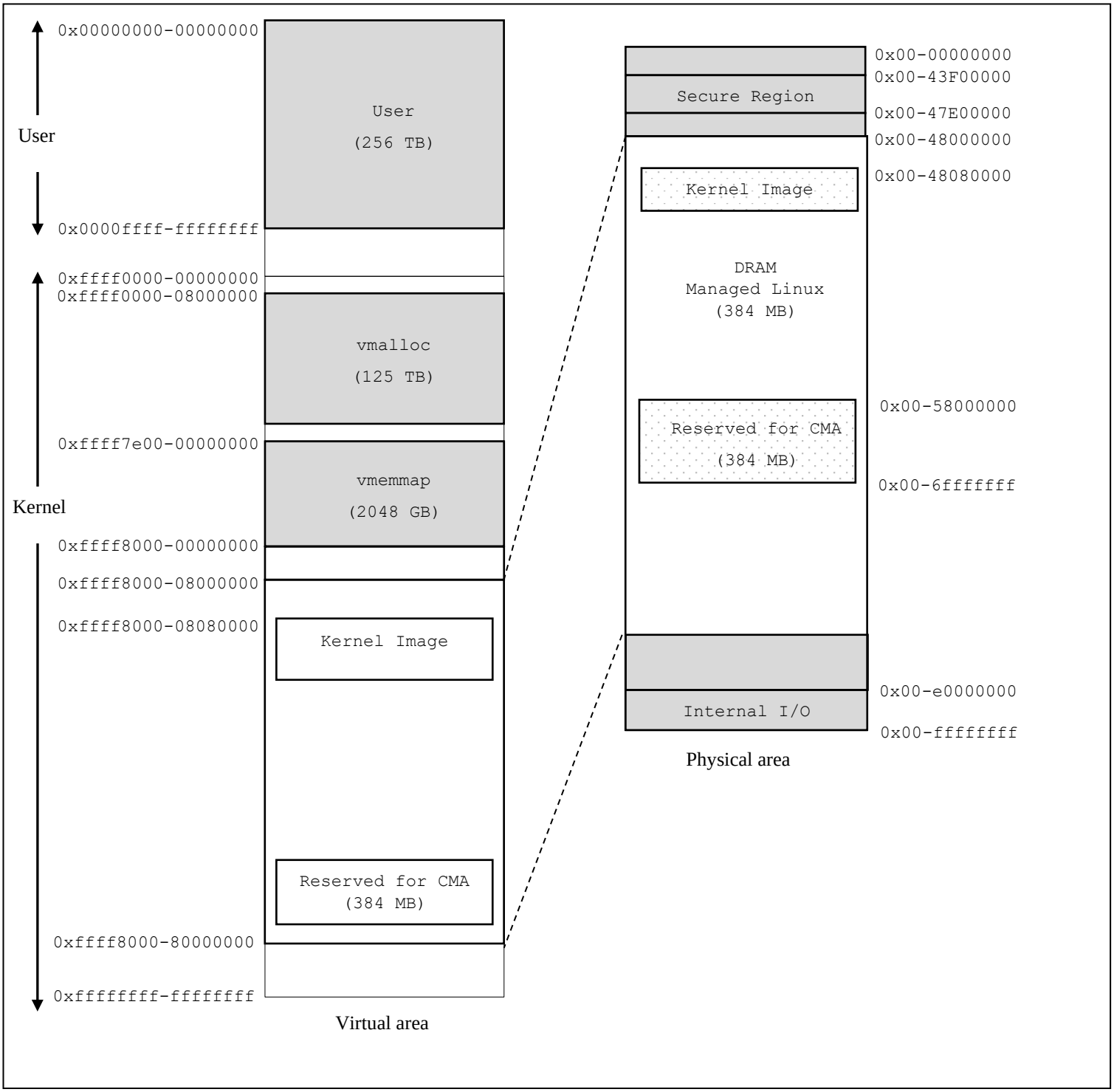

Figure 4-9 Memory map of kernel (R-Car V3U System Evaluation Board)

- Kernel uses 4KB page size (VA_BITS=48) and 4 levels of translation tables.

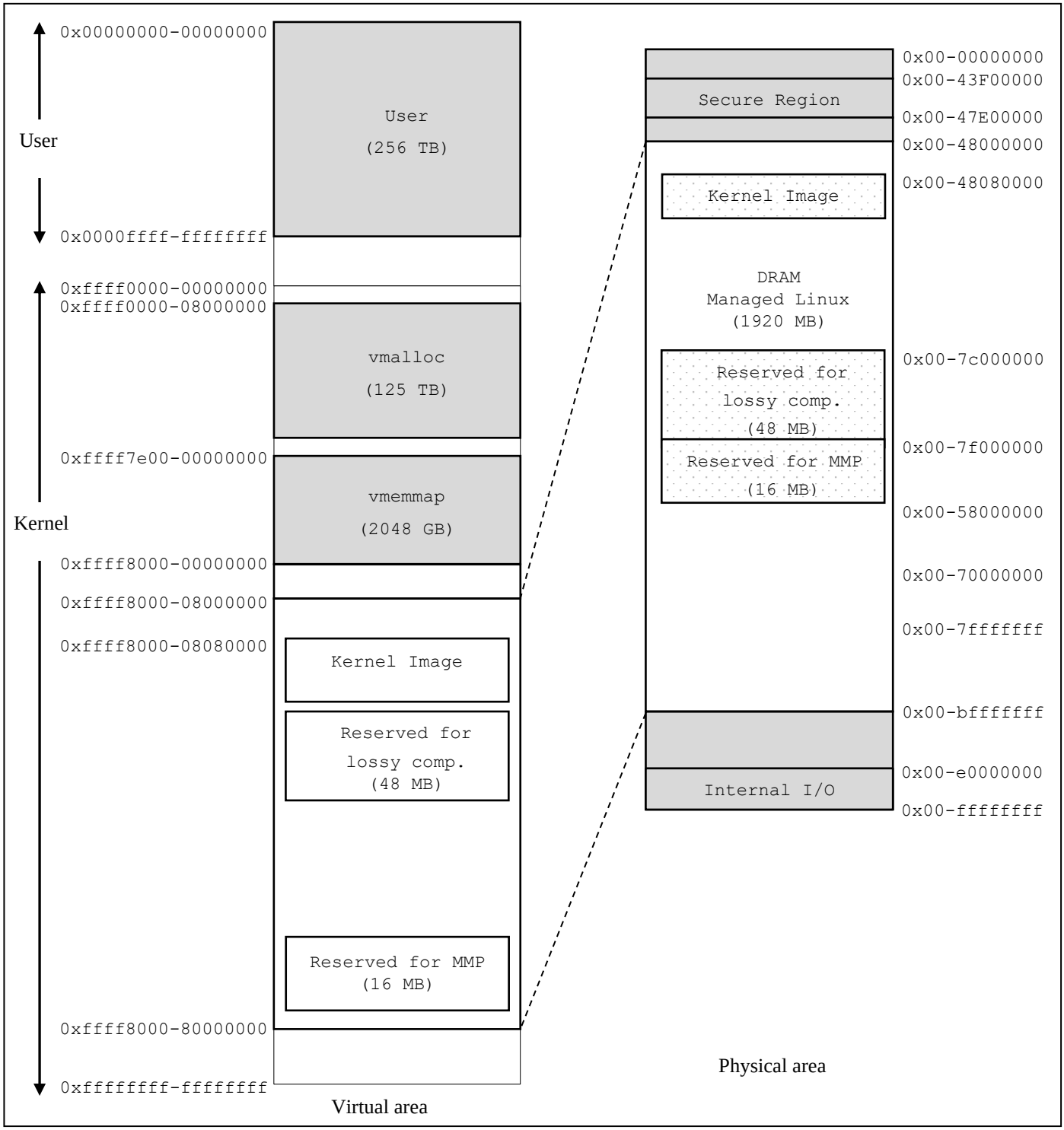

Figure 4-10 Memory map of kernel (R-Car V3H System Evaluation Board)

5. Detail

This kernel controls the following devices on the R-Car R-CarH3-SiP/M3-SiP/E3/D3/V3U/V3H System Evaluation Board.

- R-Car H3, R-Car M3, R-Car M3N, R-Car E3, R-Car D3, R-Car V3U and R-Car V3H (SoC for car infotainment)
- LPDDR4-3200 8Gbyte (R-Car H3 Ver.3.0 and R-Car M3 Ver.3.0), 4Gbyte (R-Car H3 Ver.2.0 and R-Car M3 Ver.1.x), 2Gbyte (R-Car M3N)
- DDR3/DDR3L-1866 1Gbyte (R-Car E3 System Evaluation Board Ebisu)
- DDR3/DDR3L-1866 2Gbyte (R-Car E3 System Evaluation Board Ebisu-4D)
- DDR3/DDR3L-1866 512MByte (R-Car D3)
- LPDDR4X-4266, 2Gbytes (R-Car V3U System Evaluation Board)
- LPDDR4-SDRAM 2Gbyte (R-Car V3H)

This kernel controls the following modules in R-Car H3.

- ARM Cortex-A57 MPCore 4 CPUs + ARM Cortex-A53 MPCore 4 CPUs
- L2 Cache
- IPMMU
- Generic Counter
- CPG (Clock Pulse Generator)
- RESET
- GIC-400/IRQC (Interrupt Controller)
- PFC (Pin Function Controller)
- SCIF1 (Serial Communication Interface)
- SCIF2 (Serial Communication Interface)

This kernel controls the following modules in R-Car M3.

- ARM Cortex-A57 MPCore 2 CPUs + ARM Cortex-A53 MPCore 4 CPUs
- L2 Cache
- IPMMU
- Generic Counter
- CPG (Clock Pulse Generator)
- RESET
- GIC-400/IRQC (Interrupt Controller)
- PFC (Pin Function Controller)
- SCIF1 (Serial Communication Interface)
- SCIF2 (Serial Communication Interface)

This kernel controls the following modules in R-Car E3.

- ARM Cortex-A53 Dual MPCore 1.2GHz
- L2 Cache
- IPMMU
- Generic Counter
- CPG (Clock Pulse Generator)

- RESET
- GIC-400/IRQC (Interrupt Controller)
- PFC (Pin Function Controller)
- Serial Communication Interface

This kernel controls the following modules in R-Car D3.

- ARM Cortex-A53 MPCore 1 CPUs
- Generic Counter
- CPG (Clock Pulse Generator)
- RESET
- GIC-400/IRQC (Interrupt Controller)
- PFC (Pin Function Controller)
- SCIF1 (Serial Communication Interface)

This kernel controls the following modules in R-Car V3U.

- ARM Cortex-A76 Octa Core (dual core per cluster) 1.8GHz
- L2 Cache
- IPMMU
- Generic Counter
- CPG (Clock Pulse Generator)
- RESET
- GIC-600/IRQC (Interrupt Controller)
- PFC (Pin Function Controller)
- Serial Communication Interface

This kernel controls the following modules in R-Car V3H.

- ARM Cortex-A53 Quad MPCore 1.0GHz
- L2 Cache
- IPMMU
- Generic Counter
- CPG (Clock Pulse Generator)
- RESET
- GIC-400/IRQC (Interrupt Controller)
- PFC (Pin Function Controller)
- Serial Communication Interface

6. External Interface

The functions provided by this kernel explain with reference to the following description format.

[Overview]	Presents an overview of a function.
[Function Name]	Explains the name of the function.
[Calling format]	Explains the format for calling the function.
[Argument]	Explains the argument(s) of the function.
[Return value]	Explains the return value(s) of the function.
[Feature]	Explains the features of the function.
[Remark]	Explains points to be noted when using the function.

6.1 Device Tree

The device tree is a data structure that describes hardware information.

By separating hardware-specific properties such as base address, interrupt number, pin control, and clock from the device driver to the device tree, the reusability of the device driver can be improved. Also, it is possible to use one Linux kernel image with multiple hardware.

For detailed information on Device Tree, refer to the document (Documentation/devicetree/) included in the Linux kernel source code, "Device Tree Specification" published on devicetree.org.

To customize the device driver supported by R-Car H3/M3/M3N/E3/D3/V3U/V3H Linux BSP using the device tree, refer to the user’s manual of each device driver.

Refer to the Table 6-1 for Device Tree, the defined Processor, Board, Memory Size, and Included Files dependencies.

Table 6-1 Device Tree List

Processor	Version	Board	Memory Size	Device Tree	Included Files
H3 SiP	1.0 1.1	Salvator-X	4GB	r8a77950-salvator-x.dts	r8a77950.dtsi salvator-common.dtsi salvator-x.dtsi
	2.0 3.0	Salvator-X	4GB	r8a77951-salvator-x.dts	r8a77951.dtsi salvator-common.dtsi salvator-x.dtsi
				r8a779m1-salvator-x.dts[*1]	r8a779m1.dtsi salvator-common.dtsi salvator-x.dtsi
		Salvator-XS	4GB/ 8GB	r8a77951-salvator-xs.dts	r8a77951.dtsi salvator-common.dtsi salvator-xs.dtsi
				r8a779m1-salvator-xs.dts[*1]	r8a779m1.dtsi salvator-common.dtsi salvator-xs.dtsi
M3 SiP	1.0 1.1 1.2 1.3	Salvator-X	4GB	r8a77960-salvator-x.dts	r8a77960.dtsi salvator-common.dtsi salvator-x.dtsi
		Salvator-XS	4GB	r8a77960-salvator-xs.dts	r8a77960.dtsi salvator-common.dtsi salvator-xs.dtsi
	3.0	Salvator-XS	4GB/ 8GB	r8a77961-salvator-xs.dts	r8a77961.dtsi salvator-common.dtsi salvator-xs.dtsi
				r8a779m3-salvator-xs.dts[*1]	r8a779m3.dtsi salvator-common.dtsi salvator-xs.dtsi
M3N SiP	1.0 1.1	Salvator-X	2GB	r8a77965-salvator-x.dts	r8a77965.dtsi salvator-common.dtsi salvator-x.dtsi
				r8a779m5-salvator-x.dts[*1]	r8a779m5.dtsi salvator-common.dtsi salvator-x.dtsi
		Salvator-XS	2GB	r8a77965-salvator-xs.dts	r8a77965.dtsi salvator-common.dtsi salvator-xs.dtsi
				r8a779m5-salvator-xs.dts[*1]	r8a779m5.dtsi salvator-common.dtsi salvator-xs.dtsi
E3 SoC	1.0	Ebisu	1GB	r8a77990-es10-ebisu.dts	r8a77990-es10.dtsi
		Ebisu-4D	2GB	r8a77990-es10-ebisu-4d.dts	r8a77990-es10-ebisu.dts
	1.1	Ebisu	1GB	r8a77990-ebisu.dts	r8a77990.dtsi
		Ebisu-4D	2GB	r8a77990-ebisu-4d.dts	r8a77990-ebisu.dts
D3 Soc	1.0	Draak	2GB	r8a77995-draak.dts	r8a77995.dtsi
V3U Soc	1.0	Falcon	8GB	r8a779a0-falcon.dts	r8a779a0.dtsi
V3H Soc	1.0	Condor	2GB	r8a77980-condor.dts	r8a77980.dtsi
	2.0	Condor i	2GB	r8a77980-es2-condor.dts	r8a77980-es2.dtsi

Note: 1. Those devices support 2 GHz in CPU clock.

6.2 Interrupt Control

6.2.1 Interface specification

Detailed explanation is skipped because the interrupt control functions such as the request_irq is based on Linux.

6.2.2 Definitions

This section explains the description form about interrupt.

6.2.2.1 Definitions of the interrupt

A definitions of the interrupt is described on device tree. The example of device tree is as follows.

(1) Using the interrupt definitions

```
#include <dt-bindings/interrupt-controller/arm-gic.h>

i2c0: i2c@e6500000 {
       interrupts = <GIC_SPI 287 IRQ_TYPE_LEVEL_HIGH>;
};
```

Figure 6-1 Examples of device tree for interrupt definition

The format of a "interrupts" property is as follows.

- The 1st cell is a flag which indicates the type of interrupts.
  0 (GIC_SPI) for SPI interrupts, 1 (GIC_PPI) for PPI interrupts..
- The 2nd cell contains the interrupt number for the interrupt type.
  SPI interrupts are in the range [0-987]
  PPI interrupts are in the range [0-15]
- The 3rd cell is the flags, encoded as follows:
  1 (IRQ_TYPE_EDGE_RISING) = low-to-high edge triggered
  2 (IRQ_TYPE_EDGE_FALLING) = high-to-low edge triggered (invalid for SPIs)
  4 (IRQ_TYPE_LEVEL_HIGH) = active high level-sensitive
  8 (IRQ_TYPE_LEVEL_LOW) = active low level-sensitive (invalid for SPIs)

6.2.2.2 Get definitions of the interrupt

The example which gets the definitions of the interrupt from a device tree is as follows.

```
static int rcar_i2c_probe(struct platform_device *pdev) {
       …
       irq = platform_get_irq(pdev, 0);
       ret = devm_request_irq(dev, irq, rcar_i2c_irq, 0, dev_name(dev), priv);
       …
};
```

Figure 6-2 Examples of getting interrupt from device tree

6.3 Pin Control

6.3.1 Interface specification

Detailed explanation is skipped because the pin control functions such as the pinctrl_request_gpio is based on Linux.

6.3.2 Definitions

6.3.2.1 Definitions of the Pin Control

A definitions of the Pin Control is described on device tree. The example of device tree is as follows.

(1) pin configuration definitions

```
&pfc {
    scif1_pins: scif1 {
        groups = "scif1_data_a", "scif1_ctrl";
        function = "scif1";
    };
};
```

Figure 6-3 Examples of device tree for pin configuration definitions

The pin configuration required properties:

- groups:
  A list of strings describes the name of pin groups.
  An example defines "scif1_data_a" and "scif1_ctrl" for SCIF1.
- function :
  A string describes the name of the function used to mux the pin groups.
  An example defines "scif1" for SCIF1.

Valid values for group and function names can be found in the group and function arrays of the PFC data file corresponding to the SoC.

```
static const char * const scif1_groups[] = {
    "scif1_data_a",
    "scif1_clk",
    "scif1_ctrl",
    "scif1_data_b",
};
static const struct sh_pfc_function pinmux_functions[] = {
    ...
    SH_PFC_FUNCTION(scif1),
    ...
};
```

Figure 6-4 PFC data file (Refer to drivers/pinctrl/sh-pfc/pfc-r8a7795.c)

(2) Using the pin configuration definitions

```
&scif1 {
    pinctrl-0 = <&scif1_pins>;
    pinctrl-names = "default";
};
```

Figure 6-5 Examples of device tree for pin configuration definitions

An example specifies "scif1_pins" for SCIF1.

Please refer to Documentation/devicetree/bindings/pinctrl/pinctrl-bindings.txt file for the complete information of each properties.

6.3.2.2 Supported pin configuration parameters

The pin configuration parameters use the generic pinconf bindings defined in Documentation/devicetree/bindings/pinctrl/pinctrl-bindings.txt.
The supported parameters are bias-disable, bias-pull-up, bias-pull-down, drive-strength and power-source. For pins that have a configurable I/O voltage, the power-source value should be the nominal I/O voltage in millivolts.

(1) bias-disable, bias-pull-up and bias-pull-down parameters

```
&pfc {
    usb1_pins: usb1 {
        ovc {
            pins = "GP_6_27";
            bias-pull-up;
        };

        pwen {
            pins = "GP_6_26";
            bias-pull-down;
        };
    };
};
```

Figure 6-6 Examples of device tree for pin pull-up/pull-down parameters

- pins, groups:
  Select pins to specify pull-up/pull-down control:
  pins: A list of strings describes the name of pins.
  groups: A list of strings describes the name of pin groups.
  An example defines "GP_6_27" pin and "GP_6_26" pin for USB ch1.

- bias-disable, bias-pull-up, bias-pull-down:
  Select the definition that indicates the pull-up/pull-down control of the pins:
  bias-disable = pull-up/down control is disabled
  bias-pull-up = pull up the pin
  bias-pull-down = pull down the pin
  An example parameter, "GP_6_27" pin is set to pull-up and "GP_6_26" pin is set to pull-down.

Please refer to Table 6.14 "Configuration of Registers in PUEN0-3" and Table 6.16 "Configuration of Registers in PUD0-3" in the "R-Car Series, 3rd Generation User's Manual: Hardware" for the pins that can set the pull-up/pull-down control.

(2) drive-strength parameter

This function is not supported by R-Car E3.

```
&pfc {
    avb_pins: avb {
        pins_mdc {
            groups = "avb_mdc";
            drive-strength = <24>;
        };

        pins_mii_tx {
            pins = "PIN_AVB_TX_CTL", "PIN_AVB_TXC", "PIN_AVB_TD0",
                  "PIN_AVB_TD1", "PIN_AVB_TD2", "PIN_AVB_TD3";
            drive-strength = <12>;
        };
    };
};
```

Figure 6-7 Examples of device tree for pin drive-strength parameters

- pins, groups:

  Select pins to specify drive capability:

  pins: A list of strings describes the name of pins.

  groups: A list of strings describes the name of pin groups.

  An example defines "avb_mdc" pin groups and PIN_AVB_TX_CTL", "PIN_AVB_TXC", "PIN_AVB_TD0", "PIN_AVB_TD1", "PIN_AVB_TD2" and "PIN_AVB_TD3" pins for Ethernet.

- drive-strength:

  Set a value to specify the drive capacity:

value	drive capability
3	2/8
6	2/8
9	3/8
12	4/8
15	5/8
18	6/8
21	7/8
24	full

  An example parameter, "avb_mdc" pin groups is set to full drive capability and PIN_AVB_TX_CTL", "PIN_AVB_TXC", "PIN_AVB_TD0", "PIN_AVB_TD1", "PIN_AVB_TD2" and "PIN_AVB_TD3" pin are set to 4/8 drive capability.

Please refer to the Table 6.6 "Configuration of Registers in DRVCTRL0-3" in the "R-Car Series, 3rd Generation User's Manual: Hardware" for the pins that can set the drive capability.

This function is not supported by R-Car E3.

(3) power-source parameter

```
&pfc {
    sdhi0_pins: sd0 {
        groups = "sdhi0_data4", "sdhi0_ctrl";
        power-source = <3300>;
    };

    sdhi0_pins_uhs: sd0_uhs {
        groups = "sdhi0_data4", "sdhi0_ctrl";
        power-source = <1800>;
    };
};
```

Figure 6-8 Examples of device tree for pin power-source parameters

- pins, groups:

  Select pins to specify I/O voltage:

  pins: A list of strings describes the name of pins.

  groups: A list of strings describes the name of pin groups.

  An example defines "sdhi0_data4" and "sdhi0_ctrl" pin groups for SDHI0.

- power-source:

  Set a value to specify the I/O voltage:

  1800: set 1.8 voltage.

  3300: set 3.3 voltage.

  An example parameter, "sd0" pinctrl node is set to 3.3 voltage and "sd0_uhs" pinctrl node is set to 1.8 voltage.

Please refer to the Table 6.12 "Configuration of Registers in POCCTRL0" in the "R-Car Series, 3rd Generation User's Manual: Hardware" for the pins that can set the voltage.

6.4 Clock Control

6.4.1 Interface specification

The following table shows the Clock control interface function.

Table 6-2 Clock control interface function

Chapter	Function Name	Description
6.4.1.1	devm_clk_get	Get the Clock
6.4.1.2	devm_clk_put	Release the Clock source
6.4.1.3	clk_prepare_enable	Enable the Clock
6.4.1.4	clk_disable_unprepare	Disable the Clock
6.4.1.5	clk_get_rate	Get the Clock Frequency
6.4.1.6	clk_round_rate	Adjust the Clock Frequency
6.4.1.7	clk_set_rate	Set the Clock Frequency
6.4.1.8	clk_set_parent	Set the Parent Clock
6.4.1.9	clk_get_parent	Get the Parent Clock

The example of include is as follows.

```
#include <linux/clk.h>
```

6.4.1.1 Get the Clock

[Overview] Get the Clock structure

[Function Name] devm_clk_get

[Calling format] struct clk *devm_clk_get(struct device *dev, const char *id);

[Argument] dev : Device structure (May be NULL if you use id)
id : Clock name strings (May be NULL if you use dev)

[Return value] Clock structure: Check using the IS_ERR().
0 : Success
Other : Invalid dev or id

[Feature] Return the Clock structure of Clock name if the specified name in any arguments matches the Clock name registered.

[Remark] Must be release the Clock structure by the devm_clk_put once if you want to get the Clock structure of same name.

6.4.1.2 Release the Clock

[Overview] Release the Clock source

[Function Name] devm_clk_put

[Calling format] struct clk *devm_clk_put(struct device *dev, const char *id);

[Argument] dev : Device structure (May be NULL if you use id)
id : Clock name strings (May be NULL if you use dev)

[Return value] Clock structure: Check using the IS_ERR().
0 : Success
Other : Invalid dev or id

[Feature] Release the Clock source if it has been already gotten the Clock.

[Remark]

6.4.1.3 Enable the Clock

[Overview] Enable the specified Clock

[Function Name] clk_prepare_enable

[Calling format] int clk_prepare_enable(struct clk *clk);

[Argument] clk : Clock structure got in devm_clk_get

[Return value] 0 : Success
Negative value : Error

[Feature] Enable the specified the Clock. Enable the Clock if the Clock with the parent Clock disabled.

[Remark]

6.4.1.4 Disable the Clock

[Overview] Disable the specified Clock

[Function Name] clk_disable_unprepare

[Calling format] void clk_disable_unprepare(struct clk *clk);

[Argument] clk : Clock structure got in devm_clk_get

[Return value] none

[Feature] Disable the specified the Clock. Disable the Clock if the parent Clock is not used.

[Remark] Must disable the Clock each if you enable the same Clock in the multiple points.

6.4.1.5 Get the Clock Frequency

[Overview] Get the specified Clock Frequency

[Function Name] clk_get_rate

[Calling format] unsigned long clk_get_rate(struct clk *clk);

[Argument] clk : Clock structure got in clk_get

[Return value] The current clock rate (unit : Hz)

[Feature] Get the specified Clock Frequency

[Remark]

6.4.1.6 Adjust the Clock Frequency

[Overview] Adjust the specified Clock Frequency

[Function Name] clk_round_rate

[Calling format] long clk_round_rate(struct clk *clk, unsigned long rate);

[Argument] clk : Clock structure got in clk_get
rate : Frequency (unit : Hz)

[Return value] Desired the Clock rate (unit : Hz)

[Feature] Return the value close to the frequency specified by the second argument rate in the frequency that can be set for the specified Clock.

[Remark] The frequency setting must call clk_set_rate because clk_round_rate does not set the frequency.

6.4.1.7 Set the Clock Frequency

[Overview] Set the specified Clock Frequency

[Function Name] clk_set_rate

[Calling format] int clk_set_rate(struct clk *clk, unsigned long rate);

[Argument] clk : Clock structure got in clk_get
rate : Frequency (unit : Hz)

[Return value] 0 : Success
Negative value : Error

[Feature] Set the value of the specified frequency by the second argument rate.

[Remark]

6.4.1.8 Set the parent Clock

[Overview] Set the specified parent Clock

[Function Name] clk_set_parent

[Calling format] int clk_set_parent(struct clk *clk, struct clk *parent);

[Argument] clk : Clock structure got in clk_get
parent : Clock structure got in clk_get or clk_get_parent

[Return value] 0 : Success
Negative value : Error

[Feature] Set the parent Clock of the specified Clock to the specified Clock.

[Remark] The Clock pattern that is not connected to the H / W can also specify, you must set refer to the H / W specification.

6.4.1.9 Get the parent Clock

[Overview] Get the specified parent Clock

[Function Name] clk_get_parent

[Calling format] struct clk *clk_get_parent(struct clk *clk);

[Argument] clk : Clock structure got in clk_get

[Return value] Clock structure : Check using the IS_ERR().
0 : Success

[Feature] Get the current the parent Clock for the specified Clock.

[Remark]

6.4.2 Definitions

6.4.2.1 Definitions of the clock

A definitions of the clock is described on device tree. The example of device tree is as follows.

(1) Using the CPG core clock definitions

```
        a57_0: cpu@0 {
            clocks =<&cpg CPG_CORE R8A7795_CLK_Z>;
        };
```

Figure 6-9 Examples of device tree for CPG core definitions

The format of a "clocks" property is as follows:

The 1st cell is a node or label of CPG clock to be used.
The 2nd cell must be set to CPG_CORE.
The 3rd cell contains the identifier of CPG/MSSR driver.
An example defines R8A7795_CLK_Z for Z ϕ .

Valid values for identifier of the CPG/MSSR driver can be found in the struct cpg_core_clk data arrays corresponding to the SoC.

```
static const struct cpg_core_clk r8a7795_core_clks[] __initconst = {
    ...
    DEF_BASE("z",          R8A7795_CLK_Z,   CLK_TYPE_GEN3_Z,   CLK_PLL0),
    ...
};
```

Figure 6-10 struct cpg_core_clk data arrays (Refer to drivers/clk/renesas/r8a7795-cpg-mssr.c)

(2) Using the CPG module clock definitions

```
        i2c0: i2c@e6500000 {
            clocks = <&cpg CPG_MOD 931>;
            power-domains = <&cpg>;
        };
```

Figure 6-11 Examples of device tree for MSSR module clocks definitions

The format of a "clocks" property is as follows:

The 1st cell is a node or label of CPG clock to be used.
The 2nd cell must be set to CPG_MOD.
The 3rd cell contains the identifier of CPG/MSSR driver.
An example defines 931 for MSSR register offset 9, bit 31.

The format of a "power-domains" property is as follows:

The 1st cell is a node or label of CPG clock to be used.
About this property, follow the Power Management User's Manual documentation in the environment where the Power Management is supported.

Valid values for identifier of the CPG/MSSR driver can be found in the struct mssr_mod_clk data arrays corresponding to the SoC.

```
static const struct mssr_mod_clk r8a7795_mod_clks[] __initconst = {
    ...
    DEF_MOD("i2c0",          931,   R8A7795_CLK_S3D2),
    ...
};
```

Figure 6-12 struct cpg_mod_clk data arrays (Refer to drivers/clk/renesas/r8a7795-cpg-mssr.c)

6.4.2.2 Get definitions of the clock

The example which gets the definitions of the clock from a device tree is as follows.

```
static int rcar_i2c_probe(struct platform_device *pdev) {
       struct device *dev = &pdev->dev;
       …
       priv->clk = devm_clk_get(dev, NULL);
       …
};
```

Figure 6-13 Examples of getting clock from device tree

The following table shows the core clocks that can be supported in the clock control. About module clocks, please refer source for more information (driver/clk/renesas/<r8a xxx>-cpg-mssr.c).

Table 6-3 Support Core Clock (R-Car H3 Ver.2.0/Ver.3.0)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
EXTALR	id: "extalr"	External input clock for clock source of RCLK.
PLL0	id: ".pll0"	PLL circuit 0
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1_div2"	2 dividings of PLL circuit 1
	id: ".pll1_div4"	4 dividings of PLL circuit 1
PLL2	id: ".pll2"	PLL circuit 2
PLL3	id: ".pll3"	PLL circuit 3

PLL4	id: ".pll4"“	PLL circuit 4
Zφ	id: "z"	System CPU (Cortex-A57) clock
Z2φ	id: "z2"	System CPU (Cortex-A53) clock
ZGφ	id: "zg"	3DGE clock
ZTRφ	id: "ztr"	Trace interface clock
ZTRD2φ	id: "ztrd2"	System trace interface clock
ZTφ	id: "zt"	Internal trace clock
ZXφ	id: "zx"	Cache coherent interconnect clock
CLφ	id: "cl"	CPG clock
S0φ	id: ".s0"	Clock source of S0D1 ϕ and S0D12 ϕ
S0D1φ	id: "s0d1"	
S0D2φ	id: "s0d2"	
S0D3φ	id: "s0d3"	
S0D4φ	id: "s0d4"	ADG
S0D6φ	id: "s0d6"	
S0D12φ	id: "s0d12"	
S1φ	id: ".s1"	Clock source of S1D1 ϕ , S1D2 ϕ , and S1D4 ϕ
S1D1φ	id: "s1d1"	MP, ADSP
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d4"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	AXI-bus
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	AXI-bus
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	
SDSRC ϕ	id: ".sdsrc"	Clock source of SD0φ, SD1φ, SD2φ and SD3φ
SD0φ	id: "sd0"	SD-IF0 clock
SD1φ	id: "sd1"	SD-IF1 clock
SD2φ	id: "sd2"	SD-IF2 clock
SD3φ	id: "sd3"	SD-IF3 clock
MSOφ	id: "mso"	MSIOF clock
CANFDφ	id: "canfd"	CANFD clock
HDMIφ	id: "hdmi"	HDMI clock
CSI0 ϕ	id: "csi2"	CSI2 clock
CPφ	id: "cp"	Common peripheral clock, EXTAL x 1/2
RCLK	id: ".r"	internal RCLK clock
	id: "r"	RCLK clock
OSCCLK	id: "osc"	System Watchdog timer clock

Table 6-4 Support Core Clock (R-Car M3 Ver.1.x)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
EXTALR	id: "extalr"	External input clock for clock source of RCLK.
PLL0	id: ".pll0"	PLL circuit 0
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1_div2"	2 dividings of PLL circuit 1
	id: ".pll1_div4"	4 dividings of PLL circuit 1
PLL2	id: ".pll2"	PLL circuit 2
PLL3	id: ".pll3"	PLL circuit 3
PLL4	id: ".pll4"‟	PLL circuit 4
Zφ	id: "z"	System CPU (Cortex-A57) clock
Z2φ	id: "z2"	System CPU (Cortex-A53) clock
ZGφ	id: "zg"	3DGE clock
ZTRφ	id: "ztr"	Trace interface clock
ZTRD2φ	id: "ztrd2"	System trace interface clock
ZTφ	id: "zt"	Internal trace clock
ZXφ	id: "zx"	Cache coherent interconnect clock
S0φ	id: ".s0"	Clock source of S0D1φ, S0D2φ, S0D3φ, S0D4φ, S0D6φ, S0D8φ and S0D12φ
S0D1φ	id: "s0d1"	
S0D2φ	id: "s0d2"	
S0D3φ	d: "s0d3	
S0D4φ	id: "s0d4"	ADG
S0D6φ	id: "s0d6"	
S0D8φ	id: "s0d8"	
S0D12φ	id: "s0d12"	
S1φ	id: ".s1"	Clock source of S1D1 ϕ , S1D2 ϕ , and S1D4 ϕ
S1D1φ	id: "s1d1"	IMP,ADSP
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d4"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	AXI-bus
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	AXI-bus
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	

CLφ	id: "cl"	CPG clock
SDSRC ϕ	id: ".sdsrc"	Clock source of SD0φ, SD1φ, SD2φ and SD3φ
SD0φ	id: "sd1"	SD-IF0 clock
SD1φ	id: "sd1"	SD-IF1 clock
SD2φ	id: "sd2"	SD-IF2 clock
SD3φ	id: "sd3"	SD-IF3 clock
MSOφ	id: "mso"	MSIOF clock
CANFDφ	id: "canfd"	CANFD clock
HDMIφ	id: "hdmi"	HDMI clock
CSI0 ϕ	id: "csi2"	CSI2 clock
CPφ	id: "cp"	Common peripheral clock, EXTAL x 1/2
RCLK	id: ".r"	internal RCLK clock
	id: "r"	RCLK clock
OSCCLK	id: "osc"	System Watchdog timer clock

Table 6-5 Support Core Clock (R-Car M3 Ver.3.0)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
EXTALR	id: "extalr"	External input clock for clock source of RCLK.
PLL0	id: ".pll0"	PLL circuit 0
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1_div2"	2 dividings of PLL circuit 1
	id: ".pll1_div4"	4 dividings of PLL circuit 1
PLL2	id: ".pll2"	PLL circuit 2
PLL3	id: ".pll3"	PLL circuit 3
PLL4	id: ".pll4"‟	PLL circuit 4
Zφ	id: "z"	System CPU (Cortex-A57) clock
Z2φ	id: "z2"	System CPU (Cortex-A53) clock
ZGφ	id: "zg"	3DGE clock
ZTRφ	id: "ztr"	Trace interface clock
ZTRD2φ	id: "ztrd2"	System trace interface clock
ZTφ	id: "zt"	Internal trace clock
ZXφ	id: "zx"	Cache coherent interconnect clock
S0φ	id: ".s0"	Clock source of S0D1φ, S0D2φ, S0D3φ, S0D4φ, S0D6φ, S0D8φ and S0D12φ
S0D1φ	id: "s0d1"	
S0D2φ	id: "s0d2"	
S0D3φ	d: "s0d3	
S0D4φ	id: "s0d4"	ADG
S0D6φ	id: "s0d6"	
S0D8φ	id: "s0d8"	
S0D12φ	id: "s0d12"	
S1φ	id: ".s1"	Clock source of S1D1 ϕ , S1D2 ϕ , and S1D4 ϕ
S1D1φ	id: "s1d1"	IMP,ADSP
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d4"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	AXI-bus
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	AXI-bus
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	

CLφ	id: "cl"	CPG clock
SDSRC ϕ	id: ".sdsrc"	Clock source of SD0φ, SD1φ, SD2φ and SD3φ
SD0φ	id: "sd1"	SD-IF0 clock
SD1φ	id: "sd1"	SD-IF1 clock
SD2φ	id: "sd2"	SD-IF2 clock
SD3φ	id: "sd3"	SD-IF3 clock
MSOφ	id: "mso"	MSIOF clock
CANFDφ	id: "canfd"	CANFD clock
HDMIφ	id: "hdmi"	HDMI clock
CSI0 ϕ	id: "csi2"	CSI2 clock
CPφ	id: "cp"	Common peripheral clock, EXTAL x 1/2
RCLK	id: ".r"	internal RCLK clock
	id: "r"	RCLK clock
OSCCLK	id: "osc"	System Watchdog timer clock

Table 6-6 Support Core Clock (R-Car M3N)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
EXTALR	id: "extalr"	External input clock for clock source of RCLK.
PLL0	id: ".pll0"	PLL circuit 0
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1_div2"	2 dividings of PLL circuit 1
	id: ".pll1_div4"	4 dividings of PLL circuit 1
PLL3	id: ".pll3"	PLL circuit 3
PLL4	id: ".pll4""	PLL circuit 4
Zφ	id: "z"	System CPU (Cortex-A57) clock
ZGφ	id: "zg"	3DGE clock
ZTRφ	id: "ztr"	Trace interface clock
ZTRD2φ	id: "ztrd2"	System trace interface clock
ZTφ	id: "zt"	Internal trace clock
ZXφ	id: "zx"	Cache coherent interconnect clock
S0φ	id: ".s0"	Clock source of S0D1φ, S0D2φ, S0D3φ, S0D4φ, S0D6φ, S0D8φ and S0D12φ
S0D1φ	id: "s0d1"	
S0D2φ	id: "s0d2"	
S0D3φ	d: "s0d3	
S0D4φ	id: "s0d4"	ADG
S0D6φ	id: "s0d6"	
S0D8φ	id: "s0d8"	
S0D12φ	id: "s0d12"	
S1φ	id: ".s1"	Clock source of S1D1φ, S1D2φ, and S1D4φ
S1D1φ	id: "s1d1"	IMP,ADSP
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d4"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	AXI-bus
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	AXI-bus
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	

CLφ	id: "cl"	CPG clock
SDSRCφ	id: ".sdsrc"	Clock source of SD0φ, SD1φ, SD2φ and SD3φ
SD0φ	id: "sd1"	SD-IF0 clock
SD1φ	id: "sd1"	SD-IF1 clock
SD2φ	id: "sd2"	SD-IF2 clock
SD3φ	id: "sd3"	SD-IF3 clock
MSOφ	id: "mso"	MSIOF clock
CANFDφ	id: "canfd"	CANFD clock
HDMIφ	id: "hdmi"	HDMI clock
CSI0φ	id: "csi2"	CSI2 clock
CPφ	id: "cp"	Common peripheral clock, EXTAL x 1/2
RCLK	id: ".r"	internal RCLK clock
	id: "r"	RCLK clock
OSCCLK	id: "osc"	System Watchdog timer clock

Table 6-7 Support Core Clock (R-Car D3)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
PLL0	id: ".pll0"	PLL circuit 0
	id: ".pll0d2"	dividing PLL0 by 2
	id: ".pll0d3"	dividing PLL0 by 3
	id: ".pll0d5"	dividing PLL0 by 5
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1d2"	dividing PLL1 by 2
PLL3	id: ".pll3"	PLL circuit 3
Z2φ	id: "z2"	System CPU (Cortex-A53) clock
ZGφ	id: "zg"	3DGE clock
ZTRφ	id: "ztr"	Trace interface clock
ZTφ	id: "zt"	Internal trace clock
ZXφ	id: "zx"	Cache coherent interconnect clock
S0φ	id: ".s0"	Clock source of S0D1φ
S0D1φ	id: "s0d1"	
S1φ	id: ".s1"	Clock source of S1D1φ, S1D2φ, and S1D4φ
S1D1φ	id: "s1d1"	I
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d4"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	
PEφ	id: ".pe"	Clock source of S1D4Cφ, S3D1Cφ, S3D2Cφ, and S3D4Cφ
S1D4Cφ	id: "s1d4c"	
S3D1Cφ	id: "s3d1c"	
S3D2Cφ	id: "s3d2c"	
S3D4Cφ	id: "s3d4c"	
CLφ	id: "cl"	CPG clock
CRφ	id: "cr"	
CPφ	id: "cp"	

CPEXφ	id: "cpex"	
OSCCLK	id: "osc"	System Watchdog timer clock
SDSRCφ	id: ".sdsrc"	Clock source of SD0φ
SD0φ	id: "sd1"	SD-IF0 clock
MSOφ	id: "mso"	MSIOF clock
CANFDφ	id: "canfd"	CANFD clock
RCLK	id: ".r"	internal RCLK clock
	id: "r"	RCLK clock

Table 6-8 Support Core Clock (R-Car E3)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
PLL0	id: ".pll0"	PLL circuit 0
	id: ".pll0d4"	4 dividings of PLL circuit 0
	id: ".pll0d6"	6 dividings of PLL circuit 0
	id: ".pll0d8"	8 dividings of PLL circuit 0
	id: ".pll0d20"	20 dividings of PLL circuit 0
	id: ".pll0d24"	24 dividings of PLL circuit 0
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1d2"	2 dividings of PLL circuit 1
PLL3	id: ".pll3"	PLL circuit 3
Z2φ	id: "z2"	System CPU (Cortex-A53) clock
ZGφ	id: "zg"	3DGE clock
ZTRφ	id: "ztr"	Trace interface clock
ZTφ	id: "zt"	Internal trace clock
ZXφ	id: "zx"	Cache coherent interconnect clock
CLφ	id: "cl"	CPG clock
S0φ	id: ".s0"	Clock source of S0D1φ, S0D3φ, S0D6φ, S0D12φ and S0D24φ
S0D1φ	id: "s0d1"	
S0D3φ	id: "s0d3"	
S0D6φ	id: "s0d6"	
S0D12φ	id: "s0d12"	
S0D24φ	id: "s0d24"	
S1φ	id: ".s1"	Clock source of S1D1φ, S1D2φ, and S1D4φ
S1D1φ	d: "s1d1"	
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d3"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	

PEφ	id: ".pe"	Clock source of S1D4Cφ, S3D1Cφ, S3D2Cφ, and S3D4Cφ
S1D4Cφ	id: "s1d4c"	TMU4
S3D1Cφ	id: "s3d1c"	HSCIF/R-NANDC
S3D2Cφ	id: "s3d2c"	TMU1-3
S3D4Cφ	id: "s3d4c"	SCIF/PWM
CLφ	id: "cl"	CPG clock
SDSRCφ	id: ".sdsrc"	Clock source of SD0φ
SD0φ	id: "sd1"	SD-IF0 clock
SD1φ	id: "sd1"	SD-IF1 clock
SD3φ	id: "sd3"	SD-IF3 clock
MSOφ	id: "mso"	MSIOF clock
CANFDφ	id: "canfd"	CANFD clock
CPφ	id: "cp"	Common peripheral clock, EXTAL x 1/2
RCLK	id: ".r"	internal RCLK clock
	id: "r"	RCLK clock
OCO	Id: “.oco”	On Chip Oscillator
OSCCLK	id: "osc"	System Watchdog timer clock

Table 6-9 Support Core Clock (R-Car V3U)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
EXTALR	id: "extalr"	External input clock for clock source of RCLK.
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1_div2"	2 dividings of PLL circuit 1
PLL4	id: ".pll4"	PLL circuit 4
	id: ".pll4_div2"	2 dividings of PLL circuit 4
PLL5	id: ".pll5"	PLL circuit 5
	id: ".pll_div2"	2 dividings of PLL circuit 5
	id: ".pll_div4"	4 dividings of PLL circuit 5
PLL20	id: ".pll20"	PLL circuit 20
	id: ".pll20_div2"	2 dividings of PLL circuit 20
PLL21	id: ".pll21"	PLL circuit 21
	id: ".pll21_div2"	2 dividings of PLL circuit 21
PLL30	id: ".pll30"	PLL circuit 30
	id: ".pll30_div2"	2 dividings of PLL circuit 30
PLL31	id: ".pll31"	PLL circuit 31
	id: ".pll31_div2"	2 dividings of PLL circuit 31
S1φ	id: ".s1"	Clock source of S1D1φ, S1D2φ, S1D4φ, S1D8φ and S1D12φ
S1D1φ	d: "s1d1"	
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d3"	
S1D8φ	id: "s1d8"	
S1D12φ	id: "s1d12"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	

SGφ	id: ".sg"	Clock source of SGD1φ, SGD2φ, and SGD4φ
SGD1φ	id: "sgd1"	
SGD2φ	id: "sgd2"	
SGD4φ	id: "sgd4"	
SDSRCφ	id: ".sdsrc"	Clock source of SD0φ
SD0φ	id: "sd0"	SD-IF0 clock
RPCφ	id: ".rpc"	RPC-IF clock
RPCD2φ	id: ".rpcd2"	RPC-IF clock
Z0φ	id: "z0"	Cortex-A76 (Sub-System 0) clock
Z1φ	id: "z1"	Cortex-A76 (Sub-System 1) clock
ZXφ	id: "zx"	Cache coherent interconnect clock
ZSφ	id: "zs"	Core sight Debugger
ZTφ	id: "zt"	Core sight Debugger
ZTRφ	id: "ztr"	Core sight Debugger
ZRφ	id: "zr"	Cortex-52
CNNDSPφ	id: "cnndsp"	CNN, DSP clock
VIPφ	id: "vip"	Vision IP
ADGHφ	id: "adgh"	Either AVB
ICUφ	id: "icu"	ICUMX clock
ICUD2φ	id: "icud2"	ICUMX clock
VCBUSφ	id: "vcbus"	Vision IP
CLφ	id: "cl"	CPG clock
CPFUSAφ	id: "cbfusa"	Clock monitor
CPφ	id: "cp"	Common peripheral clock, EXTAL x 1/2
CLK13Mφ	id: "clk13m"	
MSOφ	id: "mso"	MSIOF clock
CANFDφ	id: "canfd"	CANFD clock
CSI0φ	id: "csi0"	CSI2 clock
DSIφ	id: "dsi"	DSI clock
FRAYφ	id: "fray"	FlexRay clock
IPCφ	id: "ipc"	IPC clock
POSTφ	id: "post"	Power-on Self Test clock
POST2φ	id: "post2"	Power-on Self Test 2 clock
POST3φ	id: "post3"	Power-on Self Test 3 clock
POST4φ	id: "post4"	Power-on Self Test 4 clock
OSCCLKφ	id: "osc"	System Watchdog timer clock
RCLKφ	id: "r"	RCLK clock
OCOφ	Id: “.oco”	On Chip Oscillator

Table 6-10 Support Clock (R-Car V3H)

H/W Clock	Clock Name	Remark
EXTAL	id: "extal"	External input clock
	id: ".main"	Dividing of EXTAL Input (About a division value, see Table 8.4a of "R-Car Series, 3rd Generation User's Manual: Hardware")
EXTALR	id: "extalr"	External input clock for clock source of RCLK.
PLL1	id: ".pll1"	PLL circuit 1
	id: ".pll1_div2"	2 dividings of PLL circuit 1
	id: ".pll1_div4"	4 dividings of PLL circuit 1
PLL2	id: ".pll2"	PLL circuit 2
PLL3	id: ".pll3"	PLL circuit 3
Z2φ	id: "z2"	System CPU (Cortex-A53) clock
ZTRφ	id: "ztr"	Trace interface clock
ZTRD2φ	id: "ztrd2"	System trace interface clock
ZTφ	id: "zt"	Internal trace clock
ZXφ	id: "zx"	Cache coherent interconnect clock
S0φ	id: ".s0"	Clock source of S0D1φ, S0D2φ, S0D3φ, S0D4φ, S0D6φ, S0D12φ and S0D24φ
S0D1φ	id: "s0d1"	
S0D2φ	id: "s0d2"	
S0D3φ	d: "s0d3	
S0D4φ	id: "s0d4"	ADG
S0D6φ	id: "s0d6"	
S0D12φ	id: "s0d12"	
S0D24φ	id: "s0d24"	
S1φ	id: ".s1"	Clock source of S1D1 ϕ , S1D2 ϕ , and S1D4 ϕ
S1D1φ	id: "s1d1"	IMP,ADSP
S1D2φ	id: "s1d2"	
S1D4φ	id: "s1d4"	
S2φ	id: ".s2"	Clock source of S2D1φ, S2D2φ, and S2D4φ
S2D1φ	id: "s2d1"	AXI-bus
S2D2φ	id: "s2d2"	
S2D4φ	id: "s2d4"	
S3φ	id: ".s3"	Clock source of S3D1φ, S3D2φ, and S3D4φ
S3D1φ	id: "s3d1"	AXI-bus
S3D2φ	id: "s3d2"	
S3D4φ	id: "s3d4"	

CLφ	id: "cl"	CPG clock
SDSRC ϕ	id: ".sdsrc"	Clock source of SD0φ
SD0φ	id: "sd0"	SD-IF0 clock
MSOφ	id: "mso"	MSIOF clock
RPCϕ	id:"rpc"	RPC-IF clock
RPCD2ϕ	id:"rpcd2"	RPC-IF clock
CANFDφ	id: "canfd"	CANFD clock
CSI0φ	id: "csi0"	CSI0 clock
CPφ	id: "cp"	Common peripheral clock, EXTAL x 1/2
CPEXϕ	Id:"cpex"	EXTAL x 1/2
OSCCLK	id: "osc"	System Watchdog timer clock
DISP	id: "disp"	Clock supply control for display module
TMU1	Id:"tmu0"	Clock supply control for Timer module
	Id:"tmu1"	
	Id:"tmu2"	
	Id:"tmu3"	
	Id:"tmu4"	
SCIF0	id: "scif0"	Clock supply control for SCIF module
SCIF1	id: "scif1"	
SCIF3	id: "scif3"	
SCIF4	id: "scif4"	
MSIOF0	id: "msiof0"	Clock supply control for MSIOF module
MSIOF1	id: "msiof1"	
MSIOF2	id: "msiof2"	
MSIOF3	id: "msiof3"	
SYS-DMAC1	id: "sys_dmac1"	Clock supply control for SYS-DMAC module
SYS-DMAC2	id: "sys_dmac2"	
CMT0	id: "cmt0"	Clock supply control for CMT module
CMT1	id: "cmt1"	
CMT2	id: "cmt2"	
CMT3	id: "cmt3"	
SDIF	id: "sdif"	Clock supply control for SDHI module
PCIEC0	id: "pciec0"	Clock supply control for PCIEC module
RWDT	id: "rwdt"	Clock supply control for RCLK Watchdog Timer module
HSCIF0	id: "hscif0"	Clock supply control for HSCIF module
HSCIF1	id: "hscif1"	
HSCIF2	id: "hscif2"	
HSCIF3	id: "hscif3"	
THS/TSC	id: "thermal"	Clock supply control for THS/CIVM module
PWM	id: "pwm"	Clock supply control for PWM module
FCPVD0	id: "fcpvd0"	Clock supply control for FCP module
VSP (VSPD0)	id: "vspd0"	Clock supply control for VSP module

IMPPSC1	Id:"imppsc1"	Clock supply control for IMP-X5 module
IMPPSC0	Id:"imppsc0"	
IMPDMA1	Id:"impdma1"	
IMPDMA0	Id:"impdma0"	
IMP-OCV4	Id:"imp-ocv4"	
IMP-OCV3	Id:"imp-ocv3"	
IMP-OCV2	Id:"imp-ocv2"	
IMP0	id: "imp0"	
IMP1	id: "imp1"	
IMP2	id: "imp2"	
IMP3	id: "imp3"	
IMP4	id: "imp4"	
CSI41	id: "csi41"	Clock supply control for CSI2 module
CSI40	id: "csi40"	
DU0	id: "du0"	Clock supply control for DU module
LVDS-IF	id: "lvds"	Clock supply control for LVDS-IF module
VIN0	id: "vin0"	Clock supply control for VIN module
VIN1	id: "vin1"	
VIN2	id: "vin2"	
VIN3	id: "vin3"	
VIN4	id: "vin4"	
VIN5	id: "vin5"	
VIN6	id: "vin6"	
VIN7	id: "vin7"	
EAVB-IF	id: "etheravb"	Clock supply control for EthernetAVB-IF module
GETHER	Id:”gether”	Clock supply control for Gether module
IMR0	id: "imr0"	Clock supply control for IMR-LX4 module
IMR1	id: "imr1"	
IMR2	id: "imr2"	
IMR3	id: "imr3"	
IMR4	id: "imr4"	
IMR5	id: "imr5"	
GPIO0	id: "gpio0"	Clock supply control for GPIO module
GPIO1	id: "gpio1"	
GPIO2	id: "gpio2"	
GPIO3	id: "gpio3"	
GPIO4	id: "gpio4"	
GPIO5	id: "gpio5"	
CAN-FD	id: "can-fd"	Clock supply control for CAN-FD module
I2C-IF0	id: "i2c0"	Clock supply control for I2C-IF module
I2C-IF1	id: "i2c1"	
I2C-IF2	id: "i2c2"	
I2C-IF3	id: "i2c3"	

I2C-IF4	id: "i2c4"	
ISP0	id: “isp0”	
ISP1	id:“isp1”	
RTDMO	id:”rtdmo”	
RTDM1	id:”rtdm1”	
INTC-EX	id:”intc-ex”	
INTC-AP	Id:”intc-ap”	

7.big.LITTLE support

The task scheduling in big.LITTLE is based on "Completely Fair Scheduler" as standard. With just defining the flags of sched_domain in rcar-topology module, this scheduler becomes the behavior with capacity aware.

7.1 How to enable and disable big.LITTLE support

The big.LITTLE support is enabled by default in R-Car H3/M3.

If you disable the big.LITTLE support, please disable Cortex-A53 CPUs at booting. For the procedure in details, please refer to Yocto recipe Start-Up Guide.

Note: When only Cortex-A57 CPUs are booted, it ignores the flags of sched_domain defined by rcar-topology module.

REVISION HISTORY	Linux Interface Specification Kernel Core User's Manual: Software

Rev.	Date	Description	
		Page	Summary
0.1	Sep. 25, 2015	—	New creation.
0.2	Nov. 20, 2015	1	1.2 Function Move some functions to Power Management User's Manual.
		2	1.4 Restrictions Several PFC functions are supported. Several CPG functions are supported.
		5	3.2 Module Configuration Move figure to Power Management User's Manual.
		7	4.2 Memory map Add the reserve area of CMA and multimedia to a Figure 4-1.
		11,12	6.2.2 Definitions Add the spec of pin configuration.
		18	6.3.2.1 Definitions of the clock Add several clock definition.
		21-25	6.3.2.2 Get definitions of the clock Update the support clock of a table.
0.3	Mar. 18, 2016	1	1.1 Overview Update base kernel to v4.4.
		2	1.4 Restrictions Reboot are supported.
		3	2 Terminology Replace MSTP to MSSR.
		17,18	6.3.2.1 Definitions of the clock Replace the definition of the clock.
		18-22	6.3.2.2 Get definitions of the clock Update the support clock of a table.
0.4	Apr. 15, 2016	All	Add R-Car M3 support
		2	1.3.2 Related document Update Table 1-3 of Hardware User's Manual and System Evaluation Board Salvator-X Hardware Manual.
		3	2 Terminology Add CMA and MMP.
		8	4.2 Memory Map Add reserve area of MMP and ADSP to a Figure 4-1.

0.5	Aug. 12, 2016	1	1.1 Overview Update base kernel to v4.6.
		2	1.3.2 Related document Update Table 1-3 of Hardware User's Manual and System Evaluation Board Salvator-X Hardware Manual.
		2	1.4 Restrictions IPMMU are supported.
		3	2 Terminology Adds VMSA and IPMMU.
		4	3.1 Hardware Environment Update Table 3-1 of Hardware environment.
		6-7	4.2 Memory Map Update 4KB page size (VA_BITS=48) and 4 levels of translation tables to Figure 4-1, Figure 4-2.
		8	5 Detail Add IPMMU to the kernel control module of R-Car H3 and R-Car M3.
		11	6.2.2.1 Definitions of the Pin Control Replace pin configuration definitions
		18-19	6.3.2.1 Definitions of the clock Replace the definition file of a struct cpg_core_clk data arrays.
		19-28	6.3.2.2 Get definitions of the clock Update the support clock of a table.
		29	7 IPMMU support Add the description of IPMMU which supports an IOMMU framework.
0.6	Dec. 16, 2016	1	1.1 Overview Update base kernel to v4.9.
		11	6.2.2.1 Definitions of the Pin Control Change a reference file name to drivers/pinctrl/sh-pfc/pfc-r8a7795-es1.c.
		19-29	6.3.2.2 Get definitions of the clock Update the support clock of a table.
0.7	Mar. 15, 2017	2	1.3.2 Related document Update Table 1-3 of Hardware User's Manual and System Evaluation Board Salvator-XS Hardware Manual.
		4	3.1 Hardware Environment Update Table 3-1 of Hardware environment.
		19-34	6.3.2.2 Get definitions of the clock Update the support clock of a table.
0.8	Jun. 14, 2017	-	Fix H/W revision notation from WS to Ver.
		1	1.3.2 Related document Update Table 1-1 of Hardware User's Manual.
1.00	Aug. 8, 2017	All	Update document format.
1.01	Oct. 24, 2017	All	Add R-Car M3N support.

1.50	Jan. 29, 2018	1	1.1 Overview Update base kernel to v4.14.
		1	1.2 Function Change big.LITTLE support to enabled by default. Move some functions to IPMMU User's Manual.
		2	1.3.2 Related document Update Table 1-1 of Hardware User's Manual.
		9	5 Detail Change ARM Cortex-A53 MPCore support to enabled by default.
		13-15	6.2.2.2 Supported pin configuration parameters Add the supported parameters for bias-disable, bias-pull-up, bias-pull-down, drive-strength and power-source.
		22	6.3.2.2 Get definitions of the clock Delete support clock for R-Car H3 Ver.1.x.
		22-32	6.3.2.2 Get definitions of the clock Update the support clock of a table.
		38	Delete IPMMU support section.
		38	7 big.LITTLE support Add the description of big.LITTLE supports.
1.51	Mar. 28, 2018	All	Add R-Car E3 support.
1.52	Apr. 25, 2018	5	4.1 Physical memory Add memory information for R-Car H3 Ver.3.0.
		7	4.2 Memory map Add memory map for R-Car H3 Ver.3.0.
		10	4.2 Memory map Update the memory map of R-Car E3 in Figure 4-4. — Reduce reserve area of CMA and MMP. — Delete reserve area of lossy comp.
		11	5 Detail Add memory detail for R-Car H3 Ver.3.0.
1.53	Jun. 27, 2018	1	1.1 Overview Update base kernel to v4.14.35
1.54	Sep. 26, 2018	2	1.3.2 Related document Update Table 1-1 of Hardware User's Manual.
		32	6.3.2.2 Get definitions of the clock Update the support clock in Table 6-3.

1.55	Oct. 29, 2018	1	1.1 Overview Update base kernel to v4.14.70-ltsi-rc1
		2	1.3.2 Related document Update Table 1-1 of Hardware User's Manual.
		4	3.1 Hardware Environment Update Table 3-1 of Hardware environment.
		5	4.1 Physical memory Add the memory information for R-Car E3 System Evaluation Board Ebisu-4D.
		9	4.2 Memory map Fix the memory map of R-Car M3N in Figure 4-4. — Fix the mistake of the upper limit address of the virtual area.
		11	4.2 Memory map Add the memory map of R-Car E3 System Evaluation Board Ebisu-4D.
		12	5 Detail Add the memory detail of R-Car E3 System Evaluation Board Ebisu-4D
		25-44	6.3.2.2 Get definitions of the clock Update the support clock of a table.
2.00	Dec. 25, 2018	1	1.1 Overview Update base kernel to v4.14.75-ltsi
		2	1.3.2 Related document Update Table 1-1 of Hardware User's Manual.
		4	3.1 Hardware Environment Update Table 3-1 of Hardware environment.
		-	Update AddressList
2.01	Apr. 17, 2019	All	Add R-Car M3 Ver.3.0 support.
		2	1.3.2 Related document Update Table 1-1 of Hardware User's Manual.
		5	4.1 Physical memory Add the memory information for R-Car M3 Ver.3.0.
		10	4.2 Memory map Add the memory map of R-Car M3 Ver.3.0.
		14	5 Detail Add memory detail for R-Car M3 Ver.3.0.
		16	6 Device Tree Add the description of the device tree information.
		28-53	6.3.2.2 Get definitions of the clock Update the support clock of a table.
		-	Update AddressList
2.02	Jun. 26, 2019	20	6.3.2.2 Supported pin configuration parameters Update drive capability according to R-CarGen3_HW_EC_Manual_Errata_for_Rev150_Apr_10_2019.xlsx.
2.50	Apr. 24, 2020	-	Add R-Car V3U support
		1	1.1 Overview Update base kernel to v5.4.
2.51	Dec. 1, 2020	2	1.3.2 Related document Update the title of [R-Car V3U Series User's Manual] and update the Edition and Date columns at table 1-1
		30-40	6.4.2.2 Get definitions of the clock Remove module clocks from gen3 support clock table, and change the name of

			table from [Support Clock] into [Support Core Clock]
		40-41	6.4.2.2 Get definitions of the clock Update Support Core Clock (R-Car V3U) table
2.52	Jan . 29, 2021	-	Add R-Car V3H support
2.53	Apr. 21, 2021	-	Add R-Car D3 support
		-	Add Kernel 5.10 support
2.54	Aug. 16, 2021	20	Update the dts files for Table 6-1 Device Tree List
3.00	Dec. 10, 2021	-	Add Kernel 5.10.41 support

CONFIDENTIAL

Linux Interface Specification Kernel Core
User's Manual: Software

Publication Date: Rev.0.1 Sep. 25, 2015
Rev.3.00 Dec. 10, 2021

Published by: Renesas Electronics Corporation

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc. Milpitas Campus
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics America Inc. San Jose Campus
6024 Silver Creek Valley Road, San Jose, CA 95138, USA
Tel: +1-408-284-8200, Fax: +1-408-284-2775

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, #06-02 Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengaturcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia
Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0

ルネサス エレクトロニクス株式会社

■営業お問合せ窓口

http://www.renesas.com

※営業お問合せ窓口の住所は変更になることがあります。最新情報につきましては、弊社ホームページをご覧ください。

ルネサス エレクトロニクス株式会社 〒135-0061 東京都江東区豊洲3-2-24（豊洲フォレシア）

■技術的なお問合せおよび資料のご請求は下記へどうぞ。
総合お問合せ窓口：https://www.renesas.com/contact/

Colophon 3.1

Linux Interface Specification
Kernel Core

Renesas Electronics Corporation