Preliminary

R-CarH3-SiP/M3-SiP/M3N-SiP System Evaluation Board ″Salvator-XS″
RTP0RC7795SIPB0012S

Rev.3.02

Preliminary

CONFIDENTIAL

P01: TITLE
P02: R-CarH3_SD/QSPI
P03: R-CarH3_DU/LBSC
P04: R-CarH3_USB/HDMI
P05: R-CarH3_NEW_POW1
P06: R-CarH3_NEW_POW2
P07: R-CarH3_LPDDR_POW
P08: MODE_SW
P09: QSPI_FLASH/FL_CN
P10: PCI-E ch0/ch1
P11: Serial ATA
P12: USB2.0
P13: USB3.0
P14: SDHI0/SDHI3
P15: MMC0
P16: DU_ARGB
P17: HDMI_OUT
P18: LVDS0
P19: MIPI CSI-2_VIN
P20: EtherAVB(GbPHY, PHY_CN)
P21: Audio(AK4613VQ)
P22: DEBUG_SCIF/LED/TactSW
P23: EXIO_CN/MIPI_SW
P24: POWER 5V/VSYS
P25: POWER PMIC
P26: POWER PMIC2

Note:
 This schematics is common to R-CarH3SiP and R-CarM3SiP
 but several pin functions and resistance values are changed.
 <M3SIP> stands for the case of R-CarM3SiP.
 <M3N-SIP> stands for the case of R-CarM3N-SiP.

Title	R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)		
Size A2	Document Number R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)		Rev 3.02
Date: Tuesday, December 25, 2018		Sheet 1 of 26	

Preliminary

CONFIDENTIAL

Layout Note:
Following signals need Ground guard.

AUDIO_CLKA
AUDIO_CLKB
AUDIO_CLKC

AUDIO_CLKOUT
AUDIO_CLKOUT3
SCIF_CLK, SCIF_CLK until X1-pin3

SD0_CLK_V,SD0_CLK_SOC
SD3_CLK_V,SD3_CLK_SOC
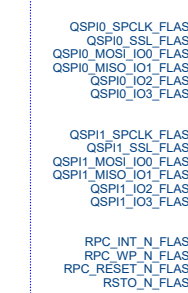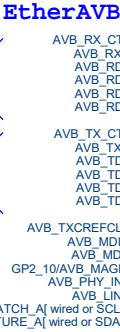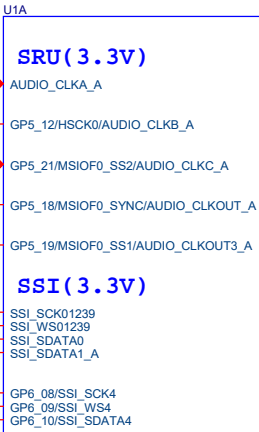MMC0_CLK_V,MMC0_CLK_SOC

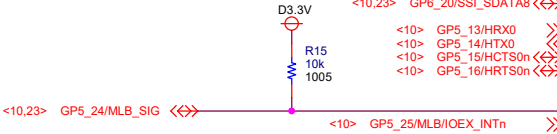AVB_TXCREFCLK
AVB_TXC_25
AVB_RXC_25

QSPI0_SPCLK_18, QSPI0_SPCLK_sw
QSPI1_SPCLK_18, QSPI1_SPCLK_sw

VTHSENSE0_18 until TH1
VTHREF0_18 until TH2

SRU(3.3V)
AUDIO_CLKA_A — AB38 — <21> AUDIO_CLKA
A34 — <21> AUDIO_CLKB
GP5_12/HSCK0/AUDIO_CLKB_A
C39 — <19> AUDIO_CLKC
GP5_21/MSIOF0_SS2/AUDIO_CLKC_A
G37 — <21> AUDIO_CLKOUT
GP5_18/MSIOF0_SYNC/AUDIO_CLKOUT_A
B39 — <21,23> AUDIO_CLKOUT3
GP5_19/MSIOF0_SS1/AUDIO_CLKOUT3_A

SSI(3.3V)
M39 — <21,23> SSI_SCK0129
J37 — <21,23> SSI_WS0129
K37 — <21,23> SSI_SDATA0
L37 — <21,23> SSI_SDATA1
SSI_SCK01239
SSI_WS01239
SSI_SDATA0
SSI_SDATA1_A
P39 — <19,23> SSI_SCK4
T37 — <19,23> SSI_WS4
P38 — <19,23> SSI_SDATA4
GP6_08/SSI_SCK4
GP6_09/SSI_WS4
GP6_10/SSI_SDATA4

SCIF(3.3V)
AB39 SCIF_CLK — SERIES_TERM R1 0
GP6_23/AUDIO_CLKB_B/SCIF_CLK_A
X1 — VCC OUT — STn GND
NZ2520SB[14.7456MHz/50ppm]
C1 0.1uF 1005 10V
D3.3V

F38 — <22> SCIF2_TXD
F39 — <22> SCIF2_RXD
GP5_10/TX2_A
GP5_11/RX2_A

E39 — <22,23> GP5_05/RX1/HRX1
E38 — <22,23> GP5_06/TX1/HTX1
H38 — <22,23> GP5_07/CTS1n/HCTS1n
H39 — <22,23> GP5_08/RTS1n/HRTS1n
GP5_05/RX1_A/HRX1_A
GP5_06/TX1_A/HTX1_A
GP5_07/CTS1#/HCTS1#_A
GP5_08/RTS1#/HRTS1#_A

SDHI0/DBG2(3.3V/1.8V)
Note: "SD0_WP" and "SD0_CD" signal is fixed at 3.3V.
D29 — <14,23> SD0_WP
D30 — <14,23> SD0_CD
D31 — <14> SD0_DAT3_V
D32 — <14> SD0_DAT2_V
C31 — <14> SD0_DAT1_V
B31 — <14> SD0_DAT0_V
A31 — <14> SD0_CMD_V
A30 — <14> SD0_CLK_V — R3 22 SD0_CLK_SOC 1005
SD0_WP
SD0_CD
SD0_DAT3/ASEBRK2
SD0_DAT2/TDI2
SD0_DAT1/TMS2
SD0_DAT0/TCK2
SD0_CMD/TRST2_N
SD0_CLK/TDO2

SDHI0 (CLK,CMD,DAT[3:0])
(1) Matched trace length.
(2) Single ended impedance = 50ohm

SDHI3(3.3V/1.8V)
Note: "SD3_WP" and "SD3_CD" signal changes to 1.8V
and 3.3V by the voltage supplied to the
VDDQVA_SD3.
D20 — <14,23> GP4_16/SD3_DAT7/SD3_WP
D21 — <14,23> GP4_15/SD3_DAT6/CD_V
A21 — <14,23> SD3_DAT3_V
C23 — <14,23> SD3_DAT2_V
B23 — <14,23> SD3_DAT1_V
A23 — <14,23> SD3_DAT0_V
C20 — <14,23> SD3_CMD_V — R8 22 SD3_CLK_SOC 1005
A24 — <14,23> SD3_CLK_V
GP4_16/SD3_DAT7/SD3_WP
GP4_15/SD3_DAT6/SD3_CD
GP4_12/SD3_DAT3
GP4_11/SD3_DAT2
GP4_10/SD3_DAT1
GP4_09/SD3_DAT0
GP4_08/SD3_CMD
GP4_07/SD3_CLK

SDHI3 (CLK,CMD,DAT[3:0])
(1) Matched trace length.
(2) Single ended impedance = 50ohm

MMC(3.3V/1.8V)_[SDHI1,2]
D27 — <15> MMC0_DTA7_V — R795 33 1005 MMC0_DAT7_SOC
C27 — <15> MMC0_DTA6_V — R796 33 1005 MMC0_DAT6_SOC
B27 — <15> MMC0_DTA5_V — R797 33 1005 MMC0_DAT5_SOC
A27 — <15> MMC0_DTA4_V — R798 33 1005 MMC0_DAT4_SOC
GP3_11/SD1_DAT3/SD2_DAT7
GP3_10/SD1_DAT2/SD2_DAT6
GP3_09/SD1_DAT1/SD2_DAT5
GP3_08/SD1_DAT0/SD2_DAT4
D23 — <15> MMC0_DTA3_V — R799 33 1005 MMC0_DAT3_SOC
C25 — <15> MMC0_DTA2_V — R800 33 1005 MMC0_DAT2_SOC
D26 — <15> MMC0_DTA1_V — R801 33 1005 MMC0_DAT1_SOC
D24 — <15> MMC0_DTA0_V — R802 33 1005 MMC0_DAT0_SOC
A26 — <15> MMC0_CMD_V — R803 33 1005 MMC0_CMD_SOC
B26 — <15> MMC0_CLK_V — R9 33 1005 MMC0_CLK_SOC
GP4_05/SD2_DAT3
GP4_04/SD2_DAT2
GP4_03/SD2_DAT1
GP4_02/SD2_DAT0
GP4_01/SD2_CMD
GP4_00/SD2_CLK
B25 — <15> MMC0_DS_V — R804 33 1005 MMC0_DS_SOC
GP4_06/SD2_DS

MMC (CLK,CMD,DAT[7:0],DS)
(1) Matched trace length.
(2) Single ended impedance < 75ohm
(3) Distance of SiP and eMMC < 50mm
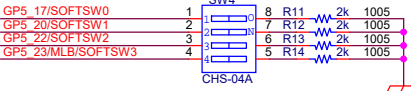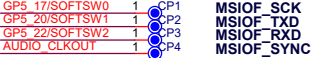(4) Distance of SiP and Resistor < 20mm
Resistor: R9, R795-R804

GPIO
GPIO_Unused(1.8V/3.3V)
Note: "SD3_xxx" signal changes to 1.8V and 3.3V by
the voltage supplied to the VDDQVA_SD3.
B21 — <23> GP4_13/SD3_DAT4_V
C21 — <23> GP4_14/SD3_DAT5_V
C22 — <23> GP4_17/SD3_DS_V
GP4_13/SD3_DAT4
GP4_14/SD3_DAT5
GP4_17/SD3_DS

GPIO_Unused(1.8V/3.3V)
Note: "SD1_xxx" signal changes to 1.8V and 3.3V by
the voltage supplied to the VDDQVA_SD1.
A28 — <23> GP3_06/SD1_CLK_V
A29 — <23> GP3_07/SD1_CMD_V
GP3_06/SD1_CLK
GP3_07/SD1_CMD

GPIO_PU
M37 — <4,23> GP6_04
V36 — <4,23> GP6_21
GP6_04/SSI_SDATA2_A
GP6_21/SSI_SDATA9_A

GPIO_PU
U39 — <10,23> GP6_17/SSI_SCK78
U37 — <10,23> GP6_18/SSI_WS78
V39 — <10,23> GP6_19/SSI_SDATA7
V37 — <10,23> GP6_20/SSI_SDATA8
GP6_17/SSI_SCK78
GP6_18/SSI_WS78
GP6_19/SSI_SDATA7
GP6_20/SSI_SDATA8

R763 10k 1005 GP4_13/SD3_DAT4_V
R764 10k 1005 GP4_14/SD3_DAT5_V
R765 10k 1005 GP4_17/SD3_DS_V
R766 10k 1005 GP3_06/SD1_CLK_V
R767 10k 1005 GP3_07/SD1_CMD_V

D3.3V
R15 10k 1005
D39 — <10> GP5_13/HRX0
D38 — <10> GP5_14/HTX0
C38 — <10> GP5_15/HCTS0n
G38 — <10> GP5_16/HRTS0n
GP5_13/HRX0
GP5_14/HTX0
GP5_15/HCTS0#
GP5_16/HRTS0#
J39 — GP5_24/MLB_SIG
J38 — GP5_25/MLB_DAT
<10,23> GP5_24/MLB_SIG
<10> GP5_25/MLB/IOEX_INTn

EtherAVB (RX_CTL,RXC,RD[3:0],TX_CTL,TXC,TD[3:0])
(1) Matched trace length.
(2) Single ended impedance = 50ohm

2.5V
A16 — AVB_RX_CTL — B19 AVB_RX_CTL_25 <20>
AVB_RXC — AVB_RXC_25 <20>
A13 — AVB_RD0 — B13 AVB_RD0_25 <20>
A14 — AVB_RD1 — B14 AVB_RD1_25 <20>
AVB_RD2 — AVB_RD2_25 <20>
AVB_RD3 — AVB_RD3_25 <20>

R724~R729:Close to U1(H3SiP)
2.5V
A8 — AVB_TX_CTL — R724 1005 24.9 1% AVB_TX_CTL_25 <20>
A19 — AVB_TXC — R725 1005 24.9 1% AVB_TXC_25 <20>
B18 — AVB_TD0 — R726 1005 24.9 1% AVB_TD0_25 <20>
A18 — AVB_TD1 — R727 1005 24.9 1% AVB_TD1_25 <20>
A17 — AVB_TD2 — R728 1005 24.9 1% AVB_TD2_25 <20>
B17 — AVB_TD3 — R729 1005 24.9 1% AVB_TD3_25 <20>

A12 — AVB_TXCREFCLK — AVB_TXCREFCLK <20>
A9 — AVB_MDIO — AVB_MDIO <20>
A15 — AVB_MDC — AVB_MDC <20>
B15 — GP2_10/AVB_MAGIC — AVB_MDC <20>
B16 — GP2_10/AVB_PHY_RESETn — GP2_10/PHY_RESETn <20>
B9 — AVB_PHY_INT — AVB_PHY_INT <20>
B11 — AVB_LINK — AVB_LINK <20>
A10 — AVB_AVTP_MATCH_A[wired or SCL5] — AVB_AVTP_MATCH <20>
A11 — AVB_AVTP_CAPTURE_A[wired or SDA5] — AVB_AVTP_CAPTURE <20>
3.3V

QSPI(1.8V)
W3 — QSPI0_SPCLK — QSPI0_SPCLK_18
Y3 — QSPI0_SSL — QSPI0_SSL_18
AC5 — QSPI0_MOSI/IO0 — QSPI0_MOSI_IO0_18
AB4 — QSPI0_MISO/IO1 — QSPI0_MISO_IO1_18
Y6 — QSPI0_IO2 — QSPI0_IO2_18
AB6 — QSPI0_IO3 — QSPI0_IO3_18

V3 — QSPI1_SPCLK — QSPI1_SPCLK_18
V5 — QSPI1_SSL — QSPI1_SSL_18
AC7 — QSPI1_MOSI/IO0 — QSPI1_MOSI_IO0_18
AE5 — QSPI1_MISO/IO1 — QSPI1_MISO_IO1_18
AE4 — QSPI1_IO2 — QSPI1_IO2_18
AC3 — QSPI1_IO3 — QSPI1_IO3_18

Y7 — RPC_INT#
V6 — RPC_WP#
V7 — RPC_RESET# — R604 0* 1005 — Do not stuff. — D1.8V
R2 10k 1005 SW3 CHS-01A

W4 — QSPI0_SPCLK_FLASH
AA5 — QSPI0_SSL_FLASH
AC4 — QSPI0_MOSI_IO0_FLASH
AA6 — QSPI0_MISO_IO1_FLASH
AC6 — QSPI0_IO2_FLASH
— QSPI0_IO3_FLASH

V4 — QSPI1_SPCLK_FLASH
W5 — QSPI1_SSL_FLASH
AB7 — QSPI1_MOSI_IO0_FLASH
AD5 — QSPI1_MISO_IO1_FLASH
AB4 — QSPI1_IO2_FLASH
AB3 — QSPI1_IO3_FLASH

Do not stuff
D1.8V D1.8V D1.8V D1.8V
AA7 — RPC_INT_N_FLASH
W6 — RPC_WP_N_FLASH
V7 — RPC_RESET_N_FLASH
— RSTO_N_FLASH
R4 10k 1005 R5 10k* 1005 R6 10k 1005 R7 10k 1005

SW1 CHS-06A
QSPI1_SSL_18 — QSPI1_SSL_sw <9>
QSPI1_SPCLK_18 — QSPI1_SPCLK_sw <9>
QSPI0_MOSI_IO0_18 — QSPI0_SPCLK_sw <9>
QSPI0_IO2_18 — QSPI0_IO2_sw <9>
QSPI0_MOSI_IO0_18 — QSPI0_MOSI_IO0_sw <9>
QSPI0_MISO_IO1_18 — QSPI0_MISO_IO1_sw <9>

SW2 CHS-06A
QSPI1_SSL_18 — QSPI0_SSL_sw <9>
QSPI1_MOSI_IO0_18 — QSPI0_IO3_sw <9>
QSPI1_IO3_18 — QSPI0_IO3_sw <9>
QSPI1_MISO_IO1_18 — QSPI1_IO3_sw <9>
QSPI1_IO2_18 — QSPI1_IO2_sw <9>

T.SENSE(1.8V)
Matched trace length.
Trace like as differential pair.
AF4 — VTHSENSE0_18 — VTHSENSE
VTHSENSE0
AG4 — VTHREF0_18 — VTHREF
VTHREF0
C2 1005 10V
C3 0.1uF 10V
TH1 VTHSENSE
TH2 VTHREF
After tying the GND side of both Cx and Cx,
tie to the internal GND plane.

SDHI_PW
B35 — GP5_02/SD0_PWEN <14>
A35 — GP5_01/SD0_PWSEL <25>
B29 — GP3_15/SD3_PWEN <14,23>
C29 — GP3_14/SD3_PWSEL <23,25>
GP5_02/TX0
GP5_01/RX0
GP3_15/SD1_WP[wired or SDA0]
GP3_14/SD1_CD[wired or SCL0]
F37 — GP5_03/SD1_PWSEL <25>
L39 — GP5_09/SD2_PWSEL <25>
GP5_03/CTS0#
GP5_09/SCK2

LVDS_bklight_Cnt
N37 — GP6_07/LVDS_BLEN <18,23>
GP6_07/SSI_SDATA3

SoftSW
A38 — GP5_17/SOFTSW0
A37 — GP5_20/SOFTSW1
B37 — GP5_22/SOFTSW2
AA39 — GP5_23/MLB_CLK
GP5_17/MSIOF0_SCK
GP5_20/MSIOF0_TXD
GP5_22/MSIOF0_RXD
GP5_23/MLB/SOFTSW3 <10>
D3.3V
R10 100k 1005

LED/TactSW
R39 — GP6_11/GP_LED/TSW0 <22,23>
R37 — GP6_12/GP_LED/TSW1 <22,23>
P37 — GP6_13/GP_LED/TSW2 <22,23>
GP6_11/SSI_SCK5
GP6_12/SSI_WS5
GP6_13/SSI_SDATA5

MSIOF_SCK / MSIOF_TXD / MSIOF_RXD / MSIOF_SYNC
GP5_17/SOFTSW0 CP1
GP5_20/SOFTSW1 CP2
GP5_22/SOFTSW2 CP3
AUDIO_CLKOUT CP4

SW4 CHS-04A
GP5_17/SOFTSW0 — R11 2k 1005
GP5_20/SOFTSW1 — R12 2k 1005
GP5_22/SOFTSW2 — R13 2k 1005
GP5_23/MLB/SOFTSW3 — R14 2k 1005

U1A
R-CarH3SiP_pin_list(rev1.52)(B)

R-CarH3SiP

R-CarH3 SDHI/QSPI

U1

Title block
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Rev: 3.02
Date: Tuesday, December 25, 2018
Sheet: 2 of 26

2

Preliminary

I2Cslave address: 1101_010X
Read:H'D5 Write: H'D4

Versaclock6
5P49V6901A

CL = 20pF(typ.)

X23
NX2016SA(25MHz/20pF/15ppm)

Output Impedance : 17ohm
Dumping resistor : 33ohm
Total : 50ohm

Note.
1. Set OEn bit to output clock.
2. I2C inputs are 5V tolerant.
3. C752(0.10uF) is for pin 5

CLKIN
CLKINB
SEL1/SDA
SEL0/SCL
OUT0_SEL_I2CB --> 0 = Use I2C (Default)
CLKSEL --> 0 = XIN/REF, XOUT (Default)
          1 = CLKIN, CLKINB
SD/OE   --> = OE and active low

Versaclock6 have Internal Pull-down Resistor(100k-300k)

Layout Note:
Following signals need Ground guard.
DU_DOTCLKIN0_18
DU_DOTCLKIN0_18 until U61-pin20
DU_DOTCLKIN1_18
DU_DOTCLKIN1_18 until X21-pin3
DU_DOTCLKIN2_18
DU_DOTCLKIN2_18 until X22-pin3
DU_DOTCLKIN3_18
DU_DOTCLKIN3_18 until U61-pin17
XTAL_18, EXTAL_18 until X4-pin3
EXT_LPO
EXTALR_SOC, EXTALR_SOC until X5-pin3,
CLKOUT_SOC,CLKOUT
TCK_18
WE0n   [CAN_CLK(40MHz)]

Do not stuff
NX2016SA[16.64MHz/10pF/15ppm]*

DU_CLK(1.8V)
LBSC_D(3.3V)
LBSC_A/DU(3.3V)
CPG(1.8V)
LBSC/DU(3.3V)
RESET
PRESET# : Internal pull-down. (100k typ.)
INTC
IRQ2# : ExMEM
IRQ0# : PMIC
I2C(3.3V)
IIC_DVFS(3.3V)
IIC_DVFS is pulled-up to V3P3 at page of PMIC.
AVS(3.3V)
SYSTEM(1.8V)
DBG(1.8V)
MLB(3.3V)

This Level-Shifter is for disconnecting U1 and V3P3 voltage while D3.3V is not supplied.

20pin ARM_EML
Top View
HTST-110-01-S-DV
[ARM_20pin]

Be carefull !!
See Pin Assignment.

R42,R44,R46,R47,R49:Close to CN1
R48:Close to U1(H3SiP)
R-CarH3SiP_pin_list(rev1.52)(B)

R-CarH3SiP

For SDRAM Backup Signals

MLB_REF
Bypass Capacitor : 8 pF~10 pF

R-CarH3 DU/LBSC

3

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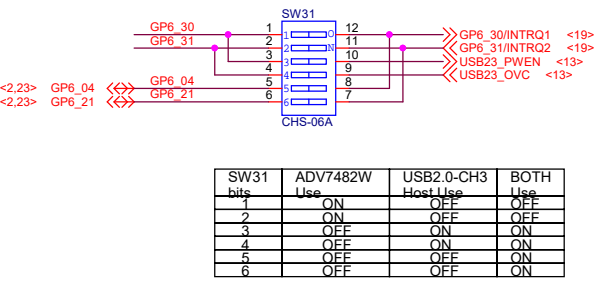Date: Tuesday, December 25, 2018   Sheet   3   of   26

Preliminary

USB

X6
NX2016SA-[50.0000MHz/10pF/15ppm]

U1C

1.8V

PCIE0

PCIE1/SATA

USB_OTG(GPIO)

R-CarH3SiP

R-CarH3SiP_pin_list(rev1.52)(B)

R-CarH3 USB/HDMI

CSI0(4-Lane)   HDMI0

U1D

CSI1(2-Lane)

HDMI1

CSI2(4-Lane)

LVDS0

R-CarH3SiP

R-CarH3SiP_pin_list(rev1.52)(B)

USB20 one pairs.
(1) Matched trace length.
(2) Differential Impedance= 90 ohm

USB21 one pairs.
(1) Matched trace length.
(2) Differential Impedance= 90 ohm

USB22 one pairs.
(1) Matched trace length.
(2) Differential Impedance= 90 ohm

PCIE0 three pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

PCIE1 three pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

USB30 four pairs.
(1) Matched trace length.
(2) Differential Impedance= 90 ohm

USB23 one pairs.
(1) Matched trace length.
(2) Differential Impedance= 90 ohm

CSI0
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

CSI1
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

CSI2
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

HDMI0 four pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

HDMI1 four pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

LVDS0 five pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

TXRTUNEn (n=0,1,2,3)
    Pull-down(GND) : 200ohm +-1% 100ppm/°C
USB3Sn_RESREF (n=0,1)
    Pull-down(GND) : 200ohm +-1% 100ppm/°C
PCIEn_RESREF (n=0,1)
    Pull-down(GND) : 200ohm +-1% 100ppm/°C
SATA_RESREF
    Pull-down(GND) : 200ohm +-1% 100ppm/°C
CSIn_REXT (n=0,1,2)
    Pull-down(GND) : 200ohm or Not use resistor <for H3Sip>
    Pull-down(GND) : 4.02kohm <for M3SiP>
HDMIn_RREF (n=0,1)
    Pull-down(GND) : 1620ohm +-1%

SW31

CHS-06A

SW31	ADV7482W	USB2.0-CH3	BOTH
bits	Use	Host Use	Use
1	ON	OFF	OFF
2	ON	OFF	OFF
3	OFF	ON	ON
4	OFF	ON	ON
5	OFF	OFF	OFF
6	OFF	OFF	ON

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Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)

Size: A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev: 3.02

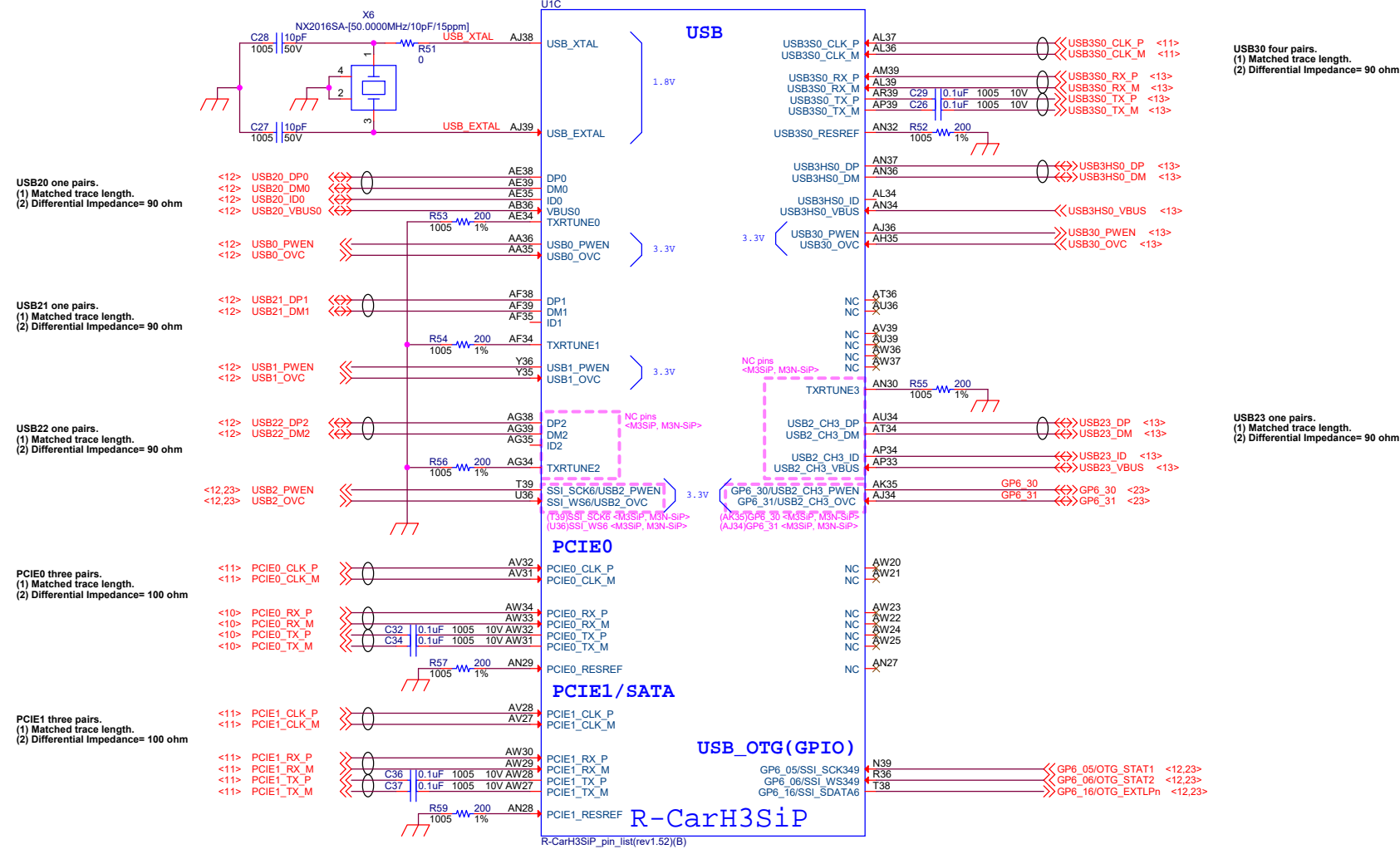Date: Tuesday, December 25, 2018   Sheet 4 of 26

4

Preliminary

Out of U1   Back of U1

U1J

R-CarH3SiP

R-CarH3SiP_pin_list(rev1.52)(B)

U1H

R-CarH3SiP

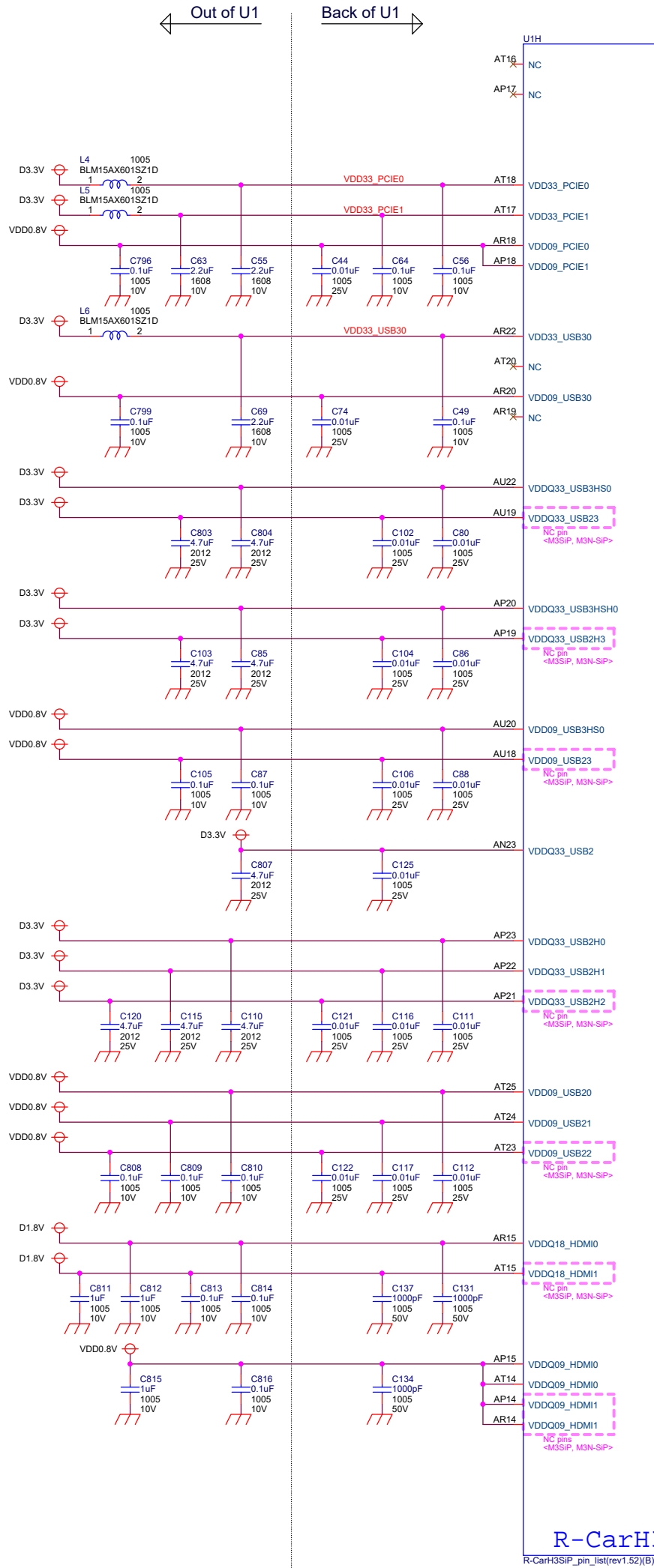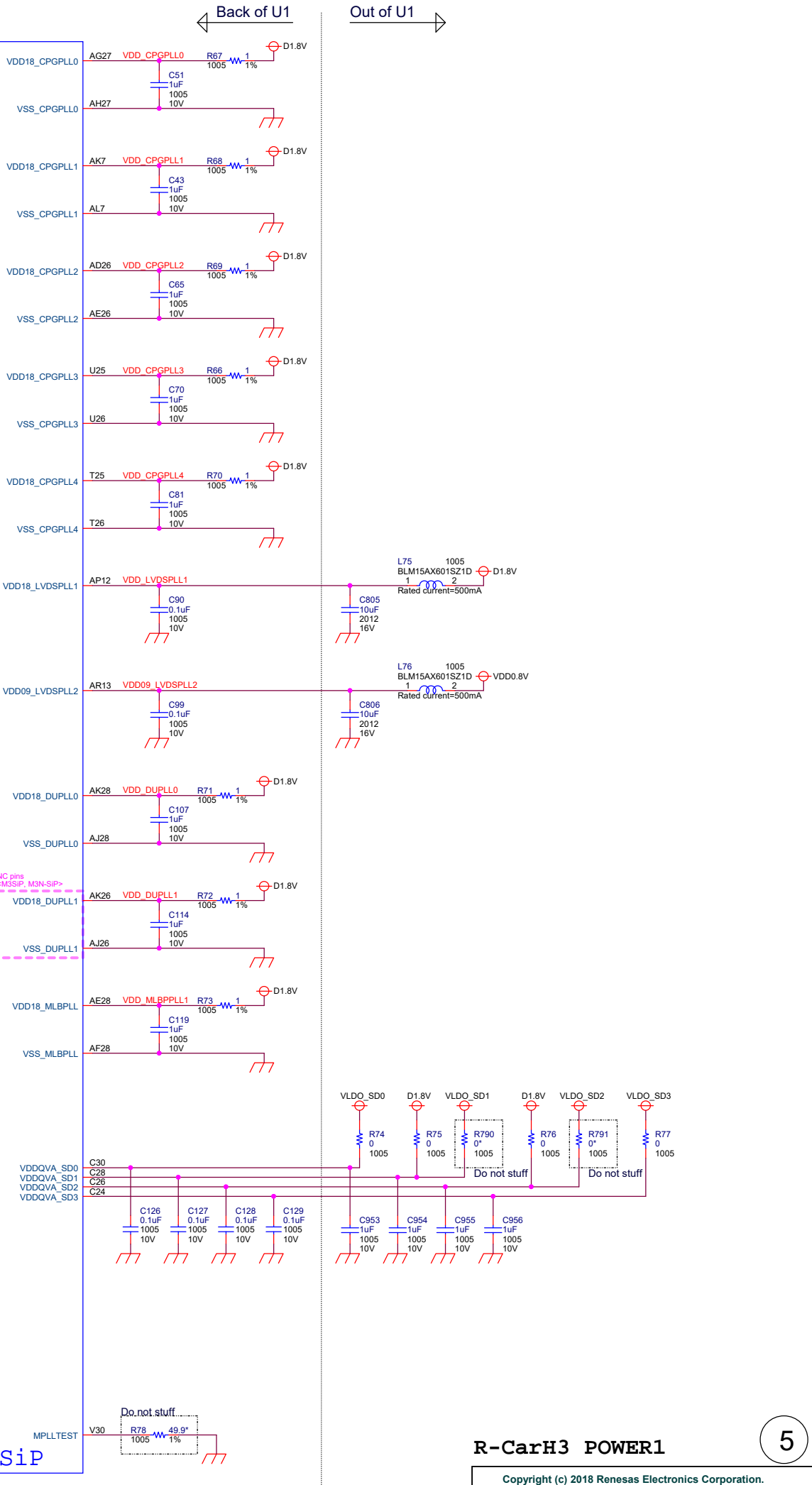R-CarH3SiP_pin_list(rev1.52)(B)

Left block (U1J) pin labels:
- AT11 VDDQ18_CSI0
- AR10 VDDQ18_CSI1
- AT10 VDDQ18_CSI2 — NC pin <M3SiP, M3N-SiP>
- AR9 NC
- AP11 VDD09_CSI0
- AR11 VDD09_CSI1
- AP10 VDD09_CSI2 — NC pin <M3SiP, M3N-SiP>
- AP9 NC
- AT12 VDDQ18_LVDS
- AP13 VDDQ09_LVDS
- C19 VDDQ25_ETH
- D19 VDDQ25_ETH

Capacitors left (U1J):
- C792 1uF 1005 10V
- C793 0.1uF 1005 10V
- C41 0.01uF 1005 25V
- C794 1uF 1005 10V
- C795 0.1uF 1005 10V
- C61 0.01uF 1005 25V
- C797 1uF 1005 10V
- C798 0.1uF 1005 10V
- C46 0.01uF 1005 25V
- C801 1uF 1005 10V
- C802 0.1uF 1005 10V
- C58 0.01uF 1005 25V
- C89 0.1uF 1005 10V
- C92 0.1uF 1005 10V
- C952 1uF 1005 10V
- C949 0.1uF 1005 10V

Rails: D1.8V, VDD0.8V, VLDO_2.5V

Middle block (U1H) pin labels:
- AT16 NC
- AP17 NC
- AT18 VDD33_PCIE0
- AT17 VDD33_PCIE1
- AR18 VDD09_PCIE0
- AP18 VDD09_PCIE1
- AR22 VDD33_USB30
- AT20 NC
- AR20 VDD09_USB30
- AR19 NC
- AU22 VDDQ33_USB3HS0
- AU19 VDDQ33_USB23 — NC pin <M3SiP, M3N-SiP>
- AP20 VDDQ33_USB3HSH0
- AP19 VDDQ33_USB2H3 — NC pin <M3SiP, M3N-SiP>
- AU20 VDD09_USB3HS0
- AU18 VDD09_USB23 — NC pin <M3SiP, M3N-SiP>
- AN23 VDDQ33_USB2
- AP23 VDDQ33_USB2H0
- AP22 VDDQ33_USB2H1
- AP21 VDDQ33_USB2H2 — NC pin <M3SiP, M3N-SiP>
- AT25 VDD09_USB20
- AT24 VDD09_USB21
- AT23 VDD09_USB22 — NC pin <M3SiP, M3N-SiP>
- AR15 VDDQ18_HDMI0
- AT15 VDDQ18_HDMI1
- AP15 VDDQ09_HDMI0
- AT14 VDDQ09_HDMI0
- AP14 VDDQ09_HDMI1
- AR14 VDDQ09_HDMI1 — NC pins <M3SiP, M3N-SiP>
- V30 MPLLTEST

Inductors:
- L4 1005 BLM15AX601SZ1D
- L5 1005 BLM15AX601SZ1D
- L6 1005 BLM15AX601SZ1D

Right block (U1H) pin labels:
- AG27 VDD18_CPGPLL0
- AH27 VSS_CPGPLL0
- AK7 VDD18_CPGPLL1
- AL7 VSS_CPGPLL1
- AD26 VDD18_CPGPLL2
- AE26 VSS_CPGPLL2
- U25 VDD18_CPGPLL3
- U26 VSS_CPGPLL3
- T25 VDD18_CPGPLL4
- T26 VSS_CPGPLL4
- AP12 VDD18_LVDSPLL1
- AR13 VDD09_LVDSPLL2
- AK28 VDD18_DUPLL0
- AJ28 VSS_DUPLL0
- AK26 VDD18_DUPLL1
- AJ26 VSS_DUPLL1
- AE28 VDD18_MLBPLL1
- AF28 VSS_MLBPLL1
- C30 VDDQVA_SD0
- C28 VDDQVA_SD1
- C26 VDDQVA_SD2
- C24 VDDQVA_SD3

Right resistors/rails:
- R67 0 1005 1% → D1.8V, C51 1uF 1005 10V
- R68 0 1005 1% → D1.8V, C43 1uF 1005 10V
- R69 0 1005 1% → D1.8V, C65 1uF 1005 10V
- R66 0 1005 1% → D1.8V, C70 1uF 1005 10V
- R70 0 1005 1% → D1.8V, C81 1uF 1005 10V
- R71 0 1005 1% → D1.8V, C107 1uF 1005 10V
- R72 0 1005 1% → D1.8V, C114 1uF 1005 10V
- R73 0 1005 1% → D1.8V, C119 1uF 1005 10V
- VDD_MLBPLL1

- L75 1005 BLM15AX601SZ1D → D1.8V Rated current=500mA, C90 0.1uF 1005 10V, C805 10uF 2012 16V
- L76 1005 BLM15AX601SZ1D → VDD0.8V Rated current=500mA, C99 0.1uF 1005 10V, C806 10uF 2012 16V

NC pins <M3SiP, M3N-SiP>

Bottom right SD rails:
VLDO_SD0, D1.8V, VLDO_SD1, D1.8V, VLDO_SD2, VLDO_SD3
- R74 0 1005
- R75 0 1005
- R790 0* 1005 Do not stuff
- R76 0 1005
- R791 0* 1005 Do not stuff
- R77 0 1005
- C126 0.1uF 1005 10V, C127 0.1uF 1005 10V, C128 0.1uF 1005 10V, C129 0.1uF 1005 10V
- C953 1uF 1005 10V, C954 1uF 1005 10V, C955 1uF 1005 10V, C956 1uF 1005 10V

Do not stuff: R78 1005 49.9* 1%

R-CarH3 POWER1

(5)

Preliminary

Capacitor-Pin Combination
VDD0.8V(VDD)
```
C162---M3
C163---N5
C879---R3
C165---U6
C880---W27

C167---AA28
C881---AD11
C874-+
C875-+
C876-+
C877-+
C882---AF13
C883---AF15
C171---AF17,AG18
C172---AF19
C173---AF21
C174---AG20
C175---AG22,AG23
C884---AH11

C177---AJ18
C885---AJ22
C886---AK11
C180---AK23
C887---AN10
C888---AN12
C889---AN14
C890---AN16
C891---AN18
C892---AN20
C893---AN22
=28-2+4=30pcs
```

Capacitor-Pin Combination
D3.3V(VDDQ33)
```
C142---J33
C143---L26
C144---N27
C145---N33
C146---T33
C147---U28,U29
C148---W28,W29
C149---AD25,AE24
C150---AH5
C151---AJ27
C152---AJ5
C153---AK24
C154---AM7
C604---AN25
C605---AN5
C606---AP24
C607---AR16
=17pcs
```

Capacitor-Pin Combination
D1.8V(VDDQ18)
```
C157---Y5,AA5
C158---AD3,AE2,AE3
C159---AD6,AE6
C160---AF26,AF27,AG26
C608---AH6
C609---AJ10
C610---AN26
C611---AP16
=8pcs
```

Capacitor-Pin Combination
DVFS0.8V(VDD_DVFS)
```
C863---Y10,Y11,AA10
C861-+
C864---Y12,AA12
C865---Y14
C862-+
C878-+
C866---AA13,AA14
C867---AB12,AC12
C195---AB14,AB15
C868---AC10,AC11
C869---AC13,AC14,AD14,AD15,AE14
C198---AD12,AE11,AE12,AF11
C870---AE10
C200---AE16
C201---AE18
C871---AE21
C203---AG12
C204---AG14
C205---AG16
C206---AH13,AJ14
C872---AH15
C873---AH17,AJ16
C209---AH19
C210---AH21
C211---AJ12,AK13
C212---AJ20
C213---AK15
C214---AK17
C215---AK19
C216---AK21
=27+3=30pcs
```

R-CarH3SiP

R-CarH3SiP_pin_list(rev1.52)(B)

[VDD]
Back of U1 =32pcs

VDD0.8V

C162	C163	C165	C167	C171	C172	C173	C174	C175	C177	C180	C874	C875	C876	C877	C879
0.047uF	0.22uF	0.22uF	0.022uF	4700pF	4700pF	0.01uF	0.01uF	0.01uF	0.01uF	0.01uF	0.22uF	0.47uF	2.2uF	4.7uF	10uF
1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1608	1608	2012
50V	16V	16V	50V	50V	50V	50V	50V	50V	50V	50V	16V	10V	6.3V	6.3V	16V

VDD0.8V

C880	C881	C882	C883	C884	C885	C886	C887	C888	C889	C890	C891	C892	C893	C929	C930
0.01uF	0.47uF	0.01uF	0.01uF	0.047uF	0.01uF	0.01uF	0.47uF	0.022uF	0.047uF	0.022uF	0.022uF	0.022uF	0.047uF	0.22uF	0.10uF
1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005
50V	10V	50V	50V	50V	50V	50V	10V	50V	50V	50V	50V	50V	50V	50V	50V

[VDD_DVFS]
Back of U1 =31pcs

DVFS0.8V

C195	C198	C200	C201	C203	C204	C205	C206	C209	C210	C211	C212	C213	C214	C215	C216
0.01uF	0.1uF	0.022uF	0.033uF	0.01uF	0.1uF	0.047uF	0.068uF	0.01uF	0.01uF	0.015uF	0.022uF	0.22uF	0.022uF	0.015uF	0.047uF
1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005
50V	50V	50V	16V	50V	50V	50V	50V	50V	50V	50V	16V	50V	50V	50V	50V

DVFS0.8V

C861	C862	C863	C864	C865	C866	C867	C868	C869	C870	C871	C872	C873	C878	C963
10uF	2.2uF	2.2uF	0.033uF	0.015uF	0.01uF	0.01uF	0.015uF	0.01uF	0.022uF	0.01uF	0.47uF	0.47uF	4.7uF	10uF
2012	1608	1608	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1608	2012
16V	6.3V	6.3V	16V	50V	50V	50V	50V	50V	50V	50V	10V	10V	6.3V	16V

DVFS0.8V

C964	C965
47uF	47uF
3225	3225
6.3V	6.3V

DVFS0.8V Do not stuff

C966
47uF*
3225
6.3V

[VDDQ33]
Back of U1 =17pcs

D3.3V

C142	C143	C144	C145	C146	C147	C148	C149	C150	C151	C152	C153	C154	C604	C605	C606	C607
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF
1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005	1005
10V	10V	10V	10V	10V	10V	10V	10V	10V	10V	10V	10V	10V	10V	10V	10V	10V

D3.3V

C155	C156
10uF	10uF
2012	2012
16V	16V

[VDDQ18]
Back of U1 =8pcs

D1.8V

C157	C158	C159	C160	C608	C609	C610	C611
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF
1005	1005	1005	1005	1005	1005	1005	1005
10V	10V	10V	10V	10V	10V	10V	10V

D1.8V

C161
10uF
2012
16V

R-CarH3_Sip socket hole is connected to GND.

SKT1
SIP_SOCKET_HOLE
SIP

U4 TEST_IC
```
IN    OUT
NC_1  AGND
NC_2  PGND
SHDN# ADJ
```

C217 4.7uF 2012 25V
R80 1005
<3,23> GP1_24
R82 2k 1005
R79 200k 1% 1005
C218 22uF 3216 10V
R83 24k 1% 1005
V_TEST

JP1 HWP-2P-G
R81 10k 1005
C219 0.1uF 1005 10V

R-CarH3SiP
R-CarH3SiP_pin_list(rev1.52)(B)

R-CarH3 POWER2

Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size: A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev: 3.02
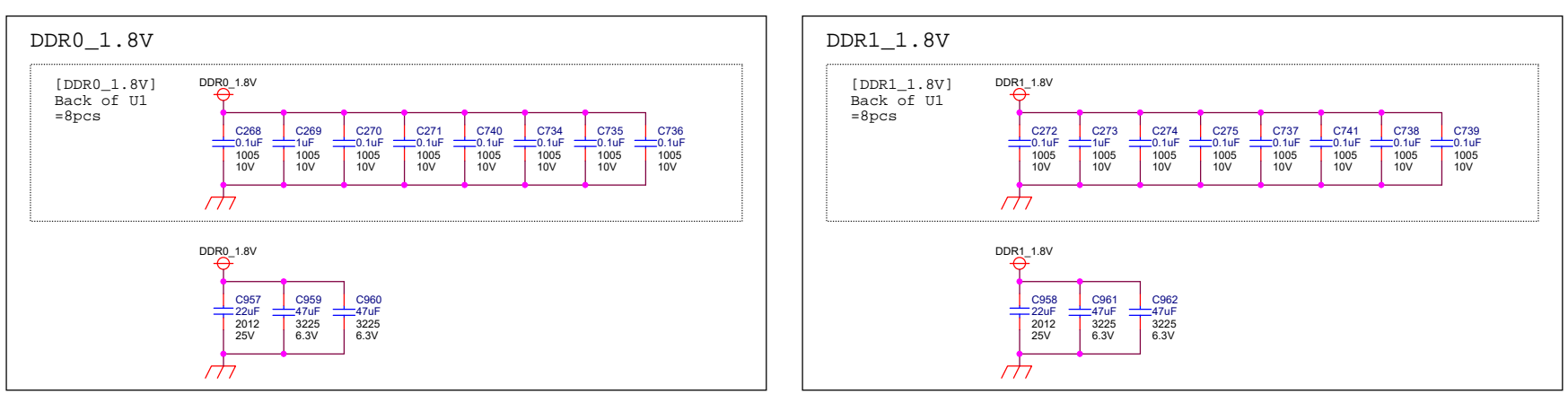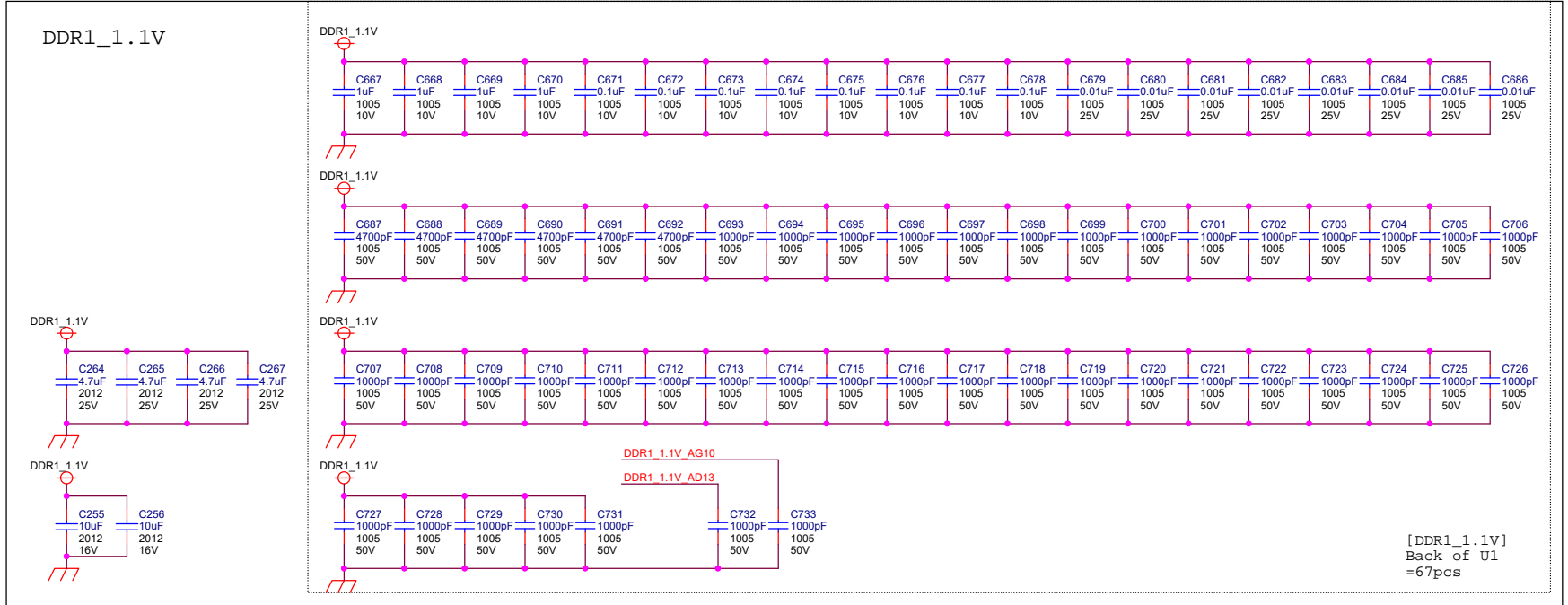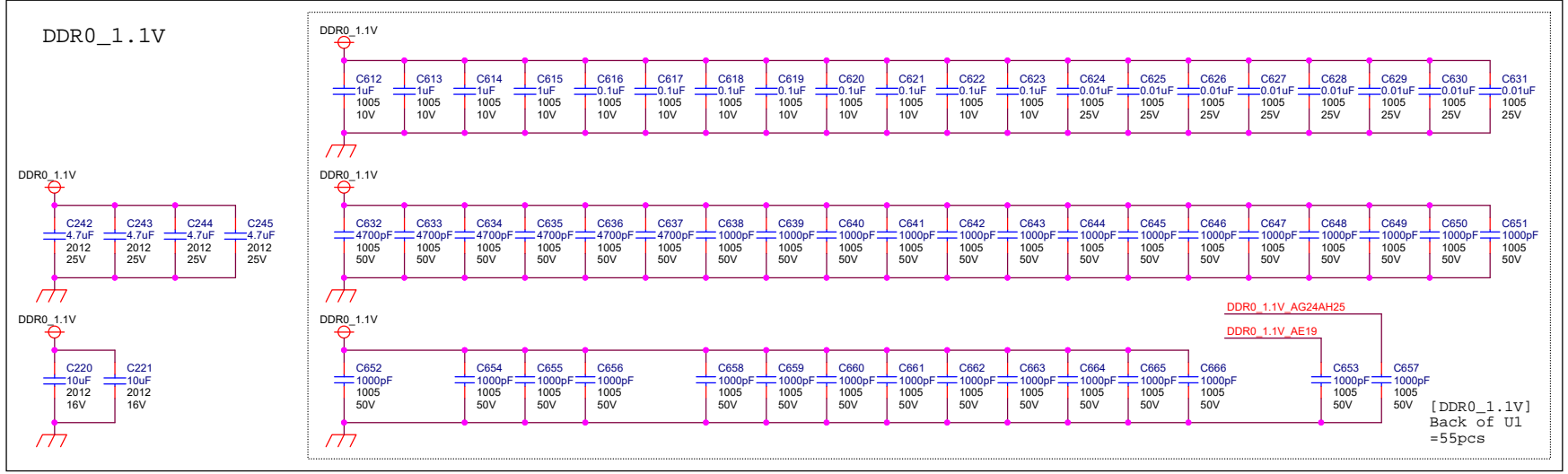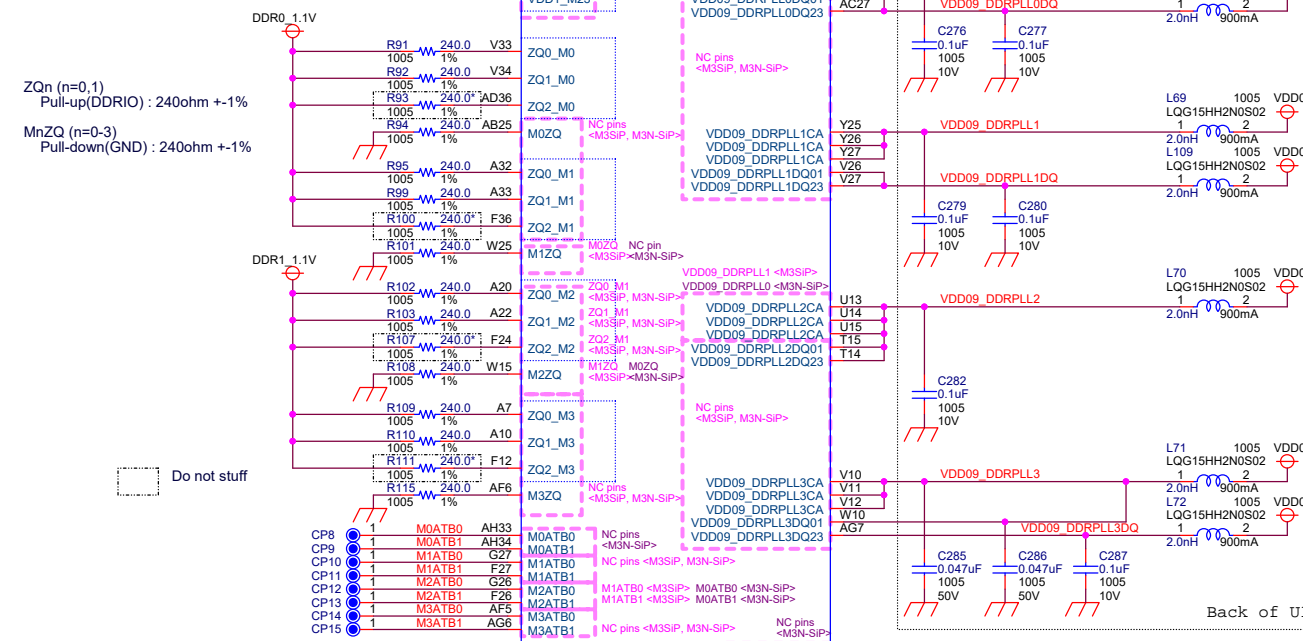Date: Tuesday, December 25, 2018
Sheet 6 of 26

6

Preliminary

Capacitor-Pin Combination DDR0_1.1V(VDDQVA_DDR0)

C612---B34,C34
C613---C32
C614---C36
C615---D28
C616---D34
C617---D37
C618---E30,E32
C619---E34
C620---E36
C621---F28
C622---F32
C623---G28
C624---G30
C625---G34
C626---G36
C627---H36
C628---K28,L28
C629---K36
C630---L30
C631---L34
C632---L36,M36
C633---M34
C634---N29
C635---N36
C636---P30
C637---P34
C638---R30
C639---R34
C640---R35
C641---T30
C642---T35
C643---W35
C644---Y30,AA29
C645---Y33,AA33
C646---Y34,AA34
C647---Y37
C648---AC30
C649---AC34
C650---AC36
C651---AD28
C652---AD34,AD35
C653---AE19
C654---AE29
C655---AE30
C656---AE36
C657---AG24,AH25
C658---AG29,AG30
C659---AG36,AH36
C660---AH37
C661---AJ33
C662---AK29
C663---AK34
C664---AL33
C665---AM34
C666---AN31
=55pcs

Capacitor-Pin Combination DDR0_1.8V(VDD1_M0/M1)

C268---F31
C269---F35
C270---M30
C271---M33
C734---AC29
C735---AC35
C736---AJ30
C740---AJ35
=8pcs

Capacitor-Pin Combination DDR1_1.8V(VDD1_M2/M3)

C272---F8
C273---F10
C274---F19
C275---F23
C737---M7
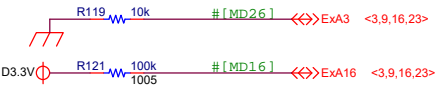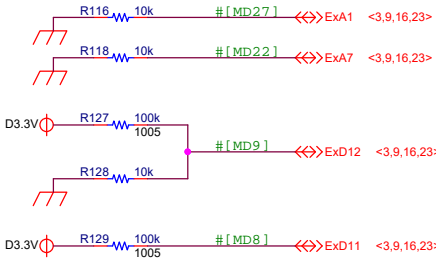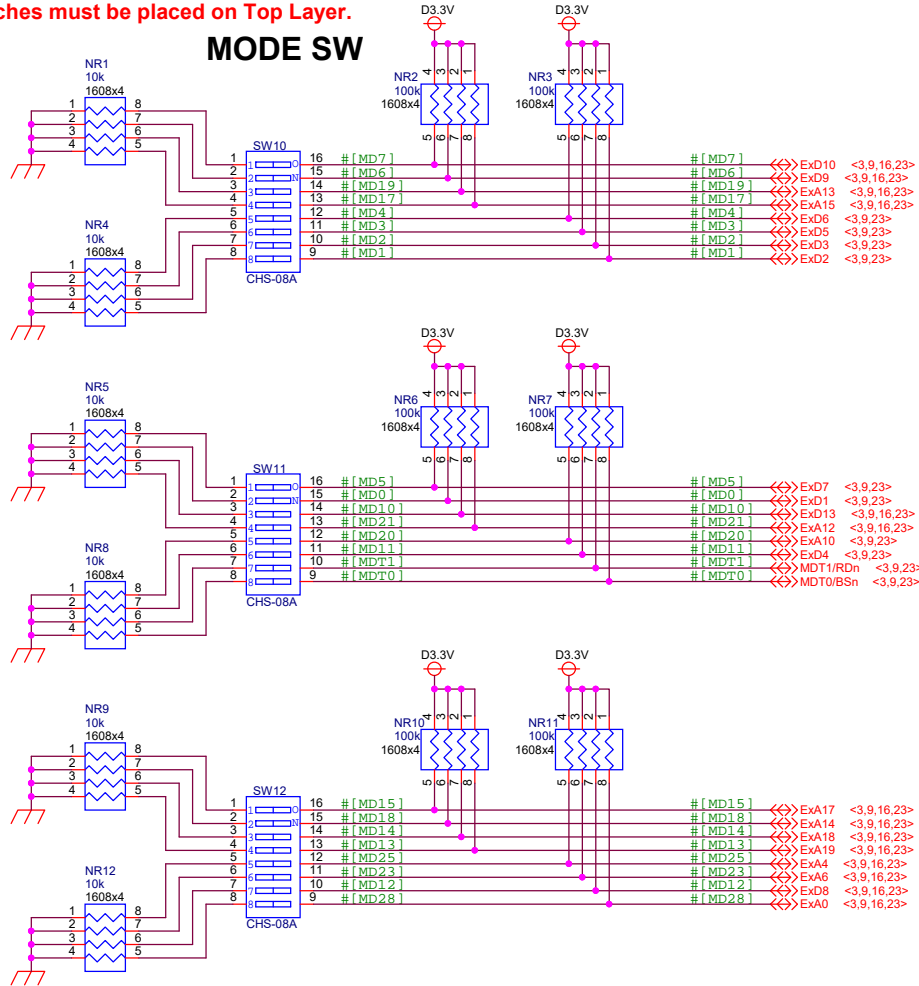C738---M10
C739---M19
C741---M23
=8pcs

Capacitor-Pin Combination DDR1_1.1V(VDDQVA_DDR0)

C667---C6
C668---C8
C669---C10
C670---C18
C671---D5
C672---D8
C673---D10
C674---D13
C675---D16
C676---D22,E22
C677---E6
C678---E8
C679---E10
C680---E12
C681---E18
C682---E24,D25
C683---F13
C684---F16
C685---F20
C686---F25
C687---G4
C688---G8
C689---G10,G11
C690---G13
C691---G16
C692---G18
C693---G22
C694---G24,G25
C695---H4
C696---H6
C697---K4
C698---K6
C699---K11
C700---K13
C701---K16
C702---K18
C703---K24
C704---K25
C705---L4
C706---L5,M6
C707---L7
C708---L10
C709---L13
C710---L16
C711---L18,M18
C712---L20
C713---L22,M22
C714---L25
C715---M12
C716---M24
C717---N13,P13
C718---N18,P18
C719---P10
C720---P16
C721---P20
C722---P22
C723---P25
C724---P4,R5
C725---P7,R6,R7
C726---R10
C727---R11,R12
C728---R18
C729---R20
C730---R22
C731---R24
C732---AD13
C733---AG10
=67pcs

U1E
R-CarH3SiP
R-CarH3SiP_pin_list(rev1.52)(B)

Note: This terminal is connected to the power supply on the SiP.

DDR0_1.1V
DDR1_1.1V
DDR0_1.8V
DDR1_1.8V

[DDR0_1.1V] Back of U1 =55pcs
[DDR1_1.1V] Back of U1 =67pcs
[DDR0_1.8V] Back of U1 =8pcs
[DDR1_1.8V] Back of U1 =8pcs

ZQn (n=0,1) Pull-up(DDRIO) : 240ohm +-1%
MnZQ (n=0-3) Pull-down(GND) : 240ohm +-1%

Do not stuff

Back of U1

R-CarH3 LPDDR_POWER — 7

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R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)

Size	Document Number	Rev
A2	R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)	3.02

Date: Tuesday, December 25, 2018   Sheet 7 of 26

Preliminary

Layout Note:
 Mode switches must be placed on Top Layer.

MODE SW

CONFIDENTIAL

MODE_SW

8

Copyright (c) 2018 Renesas Electronics Corporation.
Title R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size A2 | Document Number R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS) | Rev 3.02
Date: Tuesday, December 25, 2018 | Sheet 8 of 26
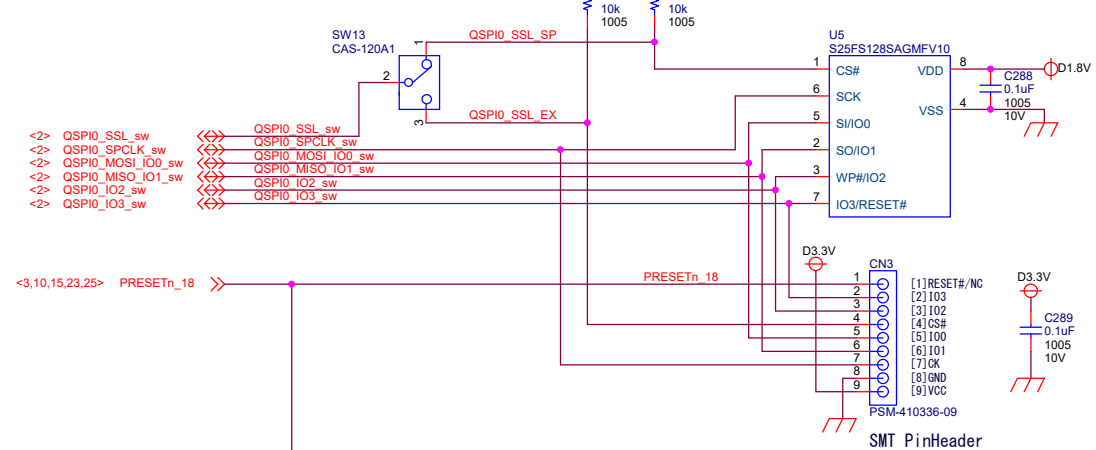
Preliminary

Layout Note:
Following signals need Ground guard.
CLKOUT
QSPI0_SPCLK_18, QSPI0_SPCLK_SP
QSPI1_SPCLK_18, QSPI1_SPCLK_EX

Ex Memory Connector
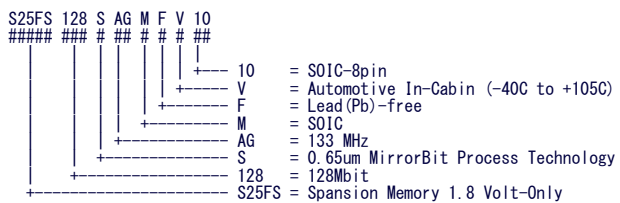**(R0P0400C0001FS)**

CN2

D3.3V

Signal	Pin	
<3,23> WE0n	75	WE0#
<3,23> WE1n	77	WE1#
	79	WE2#
	81	WE3#
<3,23> CS0n	76	CS0#
<3,23> CS1n	80	CS1#/A26
R130 0 1005	82	[EXCS0#]
R131 0 1005	86	[EXCS1#]
	88	[NC]

RD# 85
[IRQ#] 87 L_IRQn R132 0 1005
[EXWAIT#] 90
FRESET# 91
[NC] 92
[BSI#] 78
[CLKOUT] 94
[NC] 89

MDT1/RDn <3,8,23>
IRQ2n/DU_DISP <3,16,23>
EX_WAIT0n/DU_DCLK0 <3,16,23>
PRESETn <3,20,23>
MDT0/BSn <3,8,23>
CLKOUT <3,23>

<3,8,16,23> ExD[0..15]

ExD0	5	D0
ExD1	7	D1
ExD2	9	D2
ExD3	11	D3
ExD4	13	D4
ExD5	15	D5
ExD6	17	D6
ExD7	19	D7
ExD8	21	D8
ExD9	23	D9
ExD10	29	D10
ExD11	31	D11
ExD12	33	D12
ExD13	35	D13
ExD14	37	D14
ExD15	39	D15
	6	D16
	8	D17
	10	D18
	12	D19
	14	D20
	16	D21
	18	D22
	20	D23
	22	D24
	24	D25
	30	D26
	32	D27
	34	D28
	36	D29
	38	D30
	40	D31

A0 41 ExA0
A1 43 ExA1
A2 45 ExA2
A3 47 ExA3
A4 53 ExA4
A5 55 ExA5
A6 57 ExA6
A7 59 ExA7
A8 61 ExA8
A9 63 ExA9
A10 65 ExA10
A11 67 ExA11
A12 69 ExA12
A13 42 ExA13
A14 44 ExA14
A15 46 ExA15
A16 48 ExA16
A17 54 ExA17
A18 56 ExA18
A19 58 ExA19
A20 60 ExA20
A21 62 ExA21 <3>
A22 64 ExA22 <3,20,23>
A23 66 GP/ExA23/DU_VSYNC <3,16,23>
A24 68 GP/ExA24/DU_HSYNC <3,16,23>
A25 70 GP/ExA25/DU_DCLK1 <3,23>

ExA[0..20] <3,8,16,20,23>

ExA20 2k R133 1005
ExA21 2k R134 1005
GP/ExA23/DU_VSYNC 2k R135 1005
GP/ExA24/DU_HSYNC 2k R136 1005
GP/ExA25/DU_DCLK1 2k R137 1005

GND 99
GND 100

52885-1074

QSPI0 Selector
1pin : SPI-FLASH
3pin : EX-SPI-Connector

SPI FLASH (128Mbit/QSPI0)

S25FS128SAGMFV10

D1.8V D1.8V
R138 10k 1005
R139 10k 1005

SW13
CAS-120A1

QSPI0_SSL_SP
QSPI0_SSL_EX

U5
S25FS128SAGMFV10

1 CS#   VDD 8
6 SCK
5 SI/IO0 VSS 4
2 SO/IO1
3 WP#/IO2
7 IO3/RESET#

C288 0.1uF 1005 10V D1.8V

<2> QSPI0_SSL_sw
<2> QSPI0_SPCLK_sw
<2> QSPI0_MOSI_IO0_sw
<2> QSPI0_MISO_IO1_sw
<2> QSPI0_IO2_sw
<2> QSPI0_IO3_sw

QSPI0_SSL_sw
QSPI0_SPCLK_sw
QSPI0_MOSI_IO0_sw
QSPI0_MISO_IO1_sw
QSPI0_IO2_sw
QSPI0_IO3_sw

S25FS128SAGMFV10
S25FS 128 S AG M F V 10
##
10 = SOIC-8pin
V = Automotive In-Cabin (-40C to +105C)
F = Lead (Pb)-free
M = SOIC
AG = 133 MHz
S = 0.65um MirrorBit Process Technology
128 = 128Mbit
S25FS = Spansion Memory 1.8 Volt-Only

<3,10,15,23,25> PRESETn_18

PRESETn_18

CN3
1 [1]RESET#/NC
2 [2]IO3
3 [3]IO2
4 [4]CS#
5 [5]IO0
6 [6]IO1
7 [7]CK
8 [8]GND
9 [9]VCC
PSM-410336-09
SMT PinHeader

D3.3V
C289 0.1uF 1005 10V

EX-SPI Connector (QSPI0)

D1.8V D3.3V
R140 10k 1005

PRESETn_18

CN4
1 [1]RESET#/NC
2 [2]IO3
3 [3]IO2
4 [4]CS#
5 [5]IO0
6 [6]IO1
7 [7]CK
8 [8]GND
9 [9]VCC
PSM-410336-09
SMT PinHeader

<2> QSPI1_IO3_sw
<2> QSPI1_IO2_sw
<2> QSPI1_SSL_sw
<2> QSPI1_MOSI_IO0_sw
<2> QSPI1_MISO_IO1_sw
<2> QSPI1_SPCLK_sw

QSPI1_IO3_sw
QSPI1_IO2_sw
QSPI1_SSL_sw
QSPI1_MOSI_IO0_sw
QSPI1_MISO_IO1_sw
QSPI1_SPCLK_sw

D3.3V
C290 0.1uF 1005 10V

EX-SPI Connector (QSPI1)

TOP VIEW
1pin
2pin 3pin
4pin 5pin
6pin 7pin
8pin 9pin

EX-SPI-Flash-Board generate VIO=1.8V from D3.3V for internal using.

QSPI_FLASH/FL_CN   9

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Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev 3.02
Date: Tuesday, December 25, 2018   Sheet 9 of 26

CONFIDENTIAL

Preliminary

CONFIDENTIAL

PCIE (PCIe-ch0)

PCI_Express(X1)

Top View

CN5
87715-9006

B1 +12V_1	PRSNT1# A1
B2 +12V_2	+12V_4 A2
B3 +12V_3	+12V_5 A3
B4 GND_1	GND_12 A4
B5 SMCLK	JTAG2(TCK) A5	PE0_TCK
B6 SMDAT	JTAG3(TDI) A6	PE0_TDI
B7 GND_2	JTAG4(TDO) A7
B8 +3.3V_1	JTAG5(TMS) A8	PE0_TMS
B9 JTAG1(TRST#)	+3.3V_2 A9
B10 3.3Vaux	+3.3V_3 A10
B11 WAKE#	PERST# A11	PRESETOUTn <3,16,19,20,21,23>
B12 RSVD	GND_13 A12
B13 GND_3	REFCLK+ A13	PCIE0_CN_CLK_P <11>
B14 PET p0	REFCLK- A14	PCIE0_CN_CLK_M <11>
B15 PETn0	GND_14 A15
B16 GND_4	PERp0 A16	PCIE0_RX_P <4>
B17 PRSNT2#_1	PERn0 A17	PCIE0_RX_M <4>
B18 GND_5	GND_15 A18

PE0_TRSTn

D3.3V D12.0V D3.3V D3.3V D12.0V D12.0V D3.3V

R141 1k 1005
R142 1k 1005
R143 1k 1005
R144 0* 3216 Do not stuff
R145 0* 3216 Do not stuff
R146 1k 1005

<4> PCIE0_TX_P
<4> PCIE0_TX_M

D12.0V D3.3V D3.3V

C291 0.1uF 1005 50V
C781 22uF 2012 25V
C782 22uF 2012 25V
C292 0.1uF 1005 10V
C783 22uF 2012 25V
C784 22uF 2012 25V

PE0_TMS R147 4.7k 1005
PE0_TDI R148 4.7k 1005
PE0_TRSTn R149 4.7k 1005
PE0_TCK R150 4.7k 1005

I/O Expander

Slave Address
Read:0x41
Write:0x40

U6 PCA9654EDTR2G

14 SCL	IO0 4	PERST_L
15 SDA	IO1 5	WL_REG_ON
1 AD0	IO2 6	BT_REG_ON
2 AD1	IO3 7	PCIE_CLKREQ_N
3 AD2	IO4 9	PCIE_PME_L
	IO5 10	IO_EX5 CP16
16 VDD	IO6 11	IO_EX6 CP17
	IO7 12	PCIE1_SATA_SEL_18
8 VSS	INT# 13	

<3,11,19,23,26> I2C4_SCL
<3,11,19,23,26> I2C4_SDA

D1.8V
C293 0.1uF 1005 10V

R156 10k 1005
R151 R152 R153 R154 10k 1005
R730 R731 R732 R733 10k 1005

R734 1k* 1005
R735 1k* 1005
R736 1k* 1005
Do not stuff

R705 0 1005 GP5_25/MLB/IOEX_INTn <2,10>

PCIE1_SATA_SEL_18 <11>

BT/WLAN (PCIe-ch1)

#[EXIO_A]
EXIO Connector A
(Top Layer)

CN6 QSH-030-01-L-D-A

MLB_CLK R155 0* 1005 GP5_23/MLB/SOFTSW3 <2>
MLB_SIG R157 0* 1005 GP5_24/MLB_SIG <2,23>
MLB_DAT R158 0* 1005 GP5_25/MLB/IOEX_INTn <2,10>
Do not stuff
MLB signals (3.3V)

PRESETn_J R159 0 1005 PRESETn_18 <3,9,15,23,25>
TRSTn_J R160 0 1005 TRSTn_18 <3>
TDO_J R161 0 1005 TDO_18 <3>
TDI_J R162 0 1005 TDI_18 <3>
TMS_J R163 0 1005 TMS_18 <3>
TCK_J R164 0 1005 TCK_18 <3>
JTAG signals (1.8V)

BCM89359 based module EVB Pin Assign (@2015/01/20)

No.	Pin Name	No.	Pin Name
2	PCIE_PRST_N	1	NC
4	NC	3	NC
6	PCIE_REFCLK_N	5	NC
8	PCIE_REFCLK_P	7	NC
10	PCIE_CLKREQ_N	9	NC
12	GND	11	NC
14	PCIE_TDN	13	NC
16	PCIE_TDP	15	PCIE_PME_L or WL_HOST_WAKE
18	NC	17	WL_REG_ON
20	NC	19	NC
22	PCIE_RDN	21	GPIO_2
24	PCIE_RDP	23	GND
26	GND	25	GPIO_3
28	NC	27	GPIO_5
30	NC	29	GPIO_4
32	NC	31	GPIO_6
34	NC	33	BT_PCM_IN
36	NC	35	BT_PCM_OUT
38	NC	37	BT_PCM_SYNC
40	NC	39	BT_PCM_CLK
42	NC	41	BT_UART_RTS
44	BT_DEV_WAKE	43	BT_UART_CTS
46	BT_HOST_WAKE	45	BT_UART_RXD
48	NC	47	BT_UART_TXD
50	BT_REG_ON	49	NC
52	GND	51	NC
54	NC	53	VDD
56	VIO	55	VDD
58	GND	57	GND
60	NC	59	LPO_IN

-60pin Connector on BT/WLAN EVB
QTH-030-01-L-D-A (Samtec)
-Dimensions
45mm x 35mm

I2S

GP6_20/SSI_SDATA8
GP6_19/SSI_SDATA7
<2,23> GP6_20/SSI_SDATA8
<2,23> GP6_19/SSI_SDATA7

U7 SN74AVC4T245PW
R166 0 1005
R825 2k 1005

1 VCCA	VCCB 16
4 1A1	1B1 13
5 1A2	1B2 12	BT_PCM_OUT
6 2A1	2B1 11	BT_PCM_IN
7 2A2	2B2 10
2 1DIR	1OE 15
3 2DIR	2OE 14
8 GND	GND 9

R165 10k 1005
C295 0.1uF 1005 10V
C294 0.1uF 1005 10V

I2S

GP6_18/SSI_WS78 <2,23>
GP6_17/SSI_SCK78 <2,23>

U8 SN74AVC4T245PW
R826 2k 1005
R827 2k 1005

1 VCCA	VCCB 16
4 1A1	1B1 13
5 1A2	1B2 12	BT_PCM_SYNC
6 2A1	2B1 11	BT_PCM_CLK
7 2A2	2B2 10
2 1DIR	1OE 15
3 2DIR	2OE 14
8 GND	GND 9

R167 10k 1005
C296 0.1uF 1005 10V
C297 0.1uF 1005 10V

SW14 CAS-120A1
#[PCM]
[1]→Master(out)
[3]→Slave(in)

UART

<2> GP5_14/HTX0
<2> GP5_16/HRTS0n
<2> GP5_13/HRX0
<2> GP5_15/HCTS0n

U9 SN74AVC4T245PW
R828 2k 1005
R829 2k 1005

1 VCCA	VCCB 16
4 1A1	1B1 13	BT_UART_TXD
5 1A2	1B2 12	BT_UART_RTS
6 2A1	2B1 11	BT_UART_RXD
7 2A2	2B2 10	BT_UART_CTS
2 1DIR	1OE 15
3 2DIR	2OE 14
8 GND	GND 9

R171 10k 1005
C301 0.1uF 1005 10V
C302 0.1uF 1005 10V

PCIe

[04]NC PERST_L
<11> PCIE1_CN_CLK_M
<11> PCIE1_CN_CLK_P
PCIE_CLKREQ_N
[18]NC
[20]NC
<11> PCIE1_CN_RX_M
<11> PCIE1_CN_RX_P
<11> PCIE1_CN_TX_M
<11> PCIE1_CN_TX_P
[28]NC PRESETn_J
[30]NC TRSTn_J
[32]NC
[34]NC TDO_J
[36]NC TDI_J
TMS_J
TCK_J
[44]BT_DEV_WAKE BT_DEV_WAKE CP26
[46]BT_HOST_WAKE BT_HOST_WAKE CP27
[48]NC
BT_REG_ON
[54]NC
1.8V, 100mA
[60]NC

EXIO_E_NC_5pin CP19 [05]NC
EXIO_E_NC_7pin CP20 [07]NC
MLB_CLK
MLB_SIG
PCIE_PME_L
WL_REG_ON
MLB_DAT
EXIO_E_GPIO_2 CP21 [21]GPIO_2
EXIO_E_GPIO_3 CP22 [25]GPIO_3
EXIO_E_GPIO_5 CP23 [27]GPIO_5
EXIO_E_GPIO_4 CP24 [29]GPIO_4
EXIO_E_GPIO_6 CP25 [31]GPIO_6
BT_PCM_OUT
BT_PCM_IN
BT_PCM_SYNC
BT_PCM_CLK
BT_UART_CTS
BT_UART_RTS
BT_UART_TXD
BT_UART_RXD
EXT_LPO <3>
32.768kHz

MLB signals (3.3V)

R170 0 1608
C300 10uF 2012 16V

D3.3V WLAN3.6V
1200mA
R168 0.005 1% 2012 0.5W
R169 0.005* 1% 2012 0.5W Do not stuff

C298 10uF 2012 16V
C299 100uF 3216 6.3V

Do not stuff

Vout=3.6V
Imax=2A

U10 ADM7172ACP2*

D5.0V
C303 4.7uF* 2012 25V
C304 4.7uF* 2012 25V
C305 1uF* 1005 10V
C306 1000pF* 1005 50V

7 VIN	VOUT 1
8 VIN	VOUT 2
5 EN	SENSE 3
6 GND	SS 4
9 EP	

R172 100k* 1% 1005
R173 4.99k* 1% 1005
R174 49.9k* 1% 1005

Noise Reduction WLAN3.6V

R1 = 100k
R2 = 49.9k
Vout = 1.2V * (1+(R1/R2))
= 3.605V

PCIe ch0/ch1

10

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Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev 3.02
Date: Tuesday, December 25, 2018 Sheet 10 of 26

Default Unit is "mm"

Preliminary

Layout Note:
SATA_TXP/N,SATA_RX_P/N,
PCIE_TX_P/N,PCIE_RX_P/N
Reduce Stub

Serial ATA Drive power supply connector

max 2.0[A]
max 1.2[A]

D12.0V   D5.0V

CN7
4
3
2
1
LC-04A

C307 0.1uF 1005 50V
C742 10uF 3225 25V
C308 0.1uF 1005 50V
C743 10uF 3225 25V

Serial ATA signal connector

D3.3V

C972 0.1uF 1005 10V
C973 0.1uF 1005 10V
C974 0.1uF 1005 10V
C975 0.1uF 1005 10V
C976 0.1uF 1005 10V

Differential Impedance : 90(+/-5)ohm

U97 MAX4888BETI+

Differential Impedance : 100ohm

Differential Impedance : 100ohm

CN8
1 GND
2 TXP
3 TXN
4 GND
5 RXN
6 RXP
7 GND
67491-0020

1pin
7pin

Serial ATA signal connector
Top View

<4> PCIE1_RX_P
<4> PCIE1_RX_M
<4> PCIE1_TX_P
<4> PCIE1_TX_M

2 AIN+
3 AIN-
6 BIN+
7 BIN-

22 AOUTA+
21 AOUTA-
18 BOUTA+
17 BOUTA-

4 AOUTB+
5 AOUTB-
8 BOUTB+
9 BOUTB-

SATA_CN_TX_P
SATA_CN_TX_M

SATA_CN_RX_M
SATA_CN_RX_P

C309 0.01uF 1005 25V
C310 0.01uF 1005 25V

D3.3V
C977 0.1uF 1005 10V

24 SEL
15 SELB

<10> PCIE1_SATA_SEL_18

PCIE1_SATA_SEL_33

U98 HD74LV1GT08A

Level Shift(1.8V--->3.3V)

PCIE1_CN_RX_P <10>
PCIE1_CN_RX_M <10>
PCIE1_CN_TX_P <10>
PCIE1_CN_TX_M <10>

SEL port level
Low : Select SATA
High : Select PCIE1 (Default)

Differential Impedance : 100ohm

D1.8V
BLM18AG601SH1D
L77 1608
600ohm@100MHz

VFG1P8

C311 10uF 2012 16V
C312 1uF 1005 10V
C313 0.1uF 1005 10V
C314 0.1uF 1005 10V
C315 0.1uF 1005 10V
C316 0.1uF 1005 10V
C317 0.1uF 1005 10V

C318 0.1uF 1005 10V
C321 0.1uF 1005 10V
C320 0.1uF 1005 10V

VFG1P8A

R614 1005 1%

C322 1uF 1005 10V
C323 0.1uF 1005 10V

R177 1k* 1005 Do not stuff

R176 1k* 1005 Do not stuff
R178 1k* 1005

I2Cslave address: 1101_000X
Read:H'D1 Write: H'D0

VFG1P8

U11 9FGV0841AKILF

13 VDDIO
21 VDDIO
31 VDDIO
39 VDDIO
47 VDDIO
5 VDDXTAL1.8
6 VDDREF1.8
12 VDDDIG1.8
20 VDD1.8
38 VDD1.8
30 VDDA1.8

15 DIF0
16 DIF0#
18 DIF1
19 DIF1#
23 DIF2
24 DIF2#
26 DIF3
27 DIF3#
32 DIF4
33 DIF4#
35 DIF5
36 DIF5#
41 DIF6
42 DIF6#
44 DIF7
45 DIF7#
14 vOE0#
17 vOE1#
25 vOE2#
28 vOE3#
34 vOE4#
37 vOE5#
43 vOE6#
46 vOE7#

Differential Impedance : 100ohm

PCIE0_CLK_P <4>
PCIE0_CLK_M <4>
PCIE1_CLK_P <4>
PCIE1_CLK_M <4>
PCIE0_CN_CLK_P <10>
PCIE0_CN_CLK_M <10>
PCIE1_CN_CLK_P <10>
PCIE1_CN_CLK_M <10>

USB3S0_CLK_P <4>
USB3S0_CLK_M <4>

D1.8V
R793 1005 10k
R179 1005 10k
R794 1005 10k

VFG1P8A
D1.8V Do not stuff

1 vSS_EN_tri
7 vSADR/REF1.8
48 ^CKPWRGD_PD#
10 SCLK_3.3
11 SDATA_3.3

<3,10,19,23,26> I2C4_SCL
<3,10,19,23,26> I2C4_SDA

X7
NX2016SA[25MHz/20pF/15ppm]

C324 30pF 1005 50V
C325 30pF 1005 50V

3 X1_25
4 X2

GNDXTAL
GNDREF
GNDDIG
GND
GNDA
GND

20pF = C/2 + 4.6pF
C = 30.8pF

DIF0/DIF0#, DIF5/DIF5# and DIF7/DIF7# are disabled outputs.
These pins output Low-level signal.
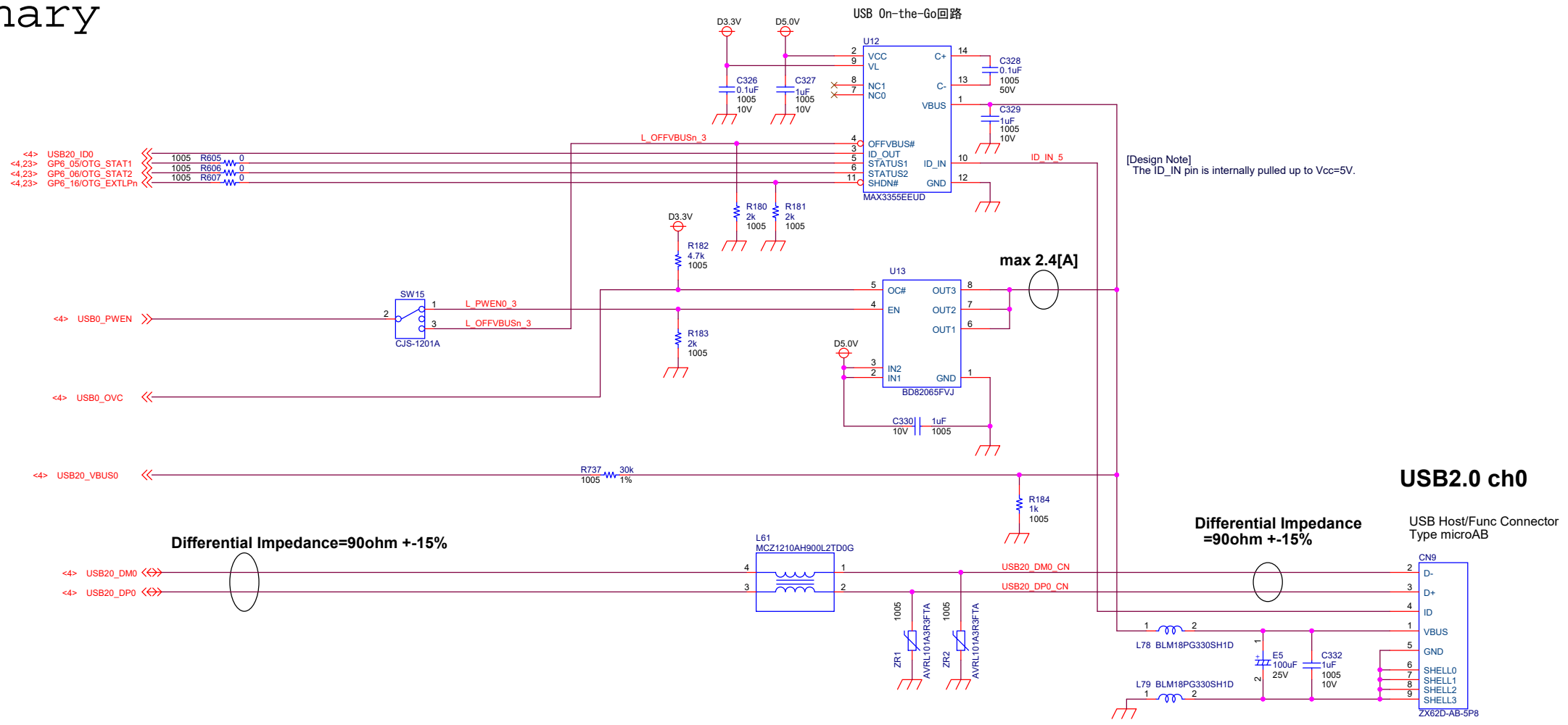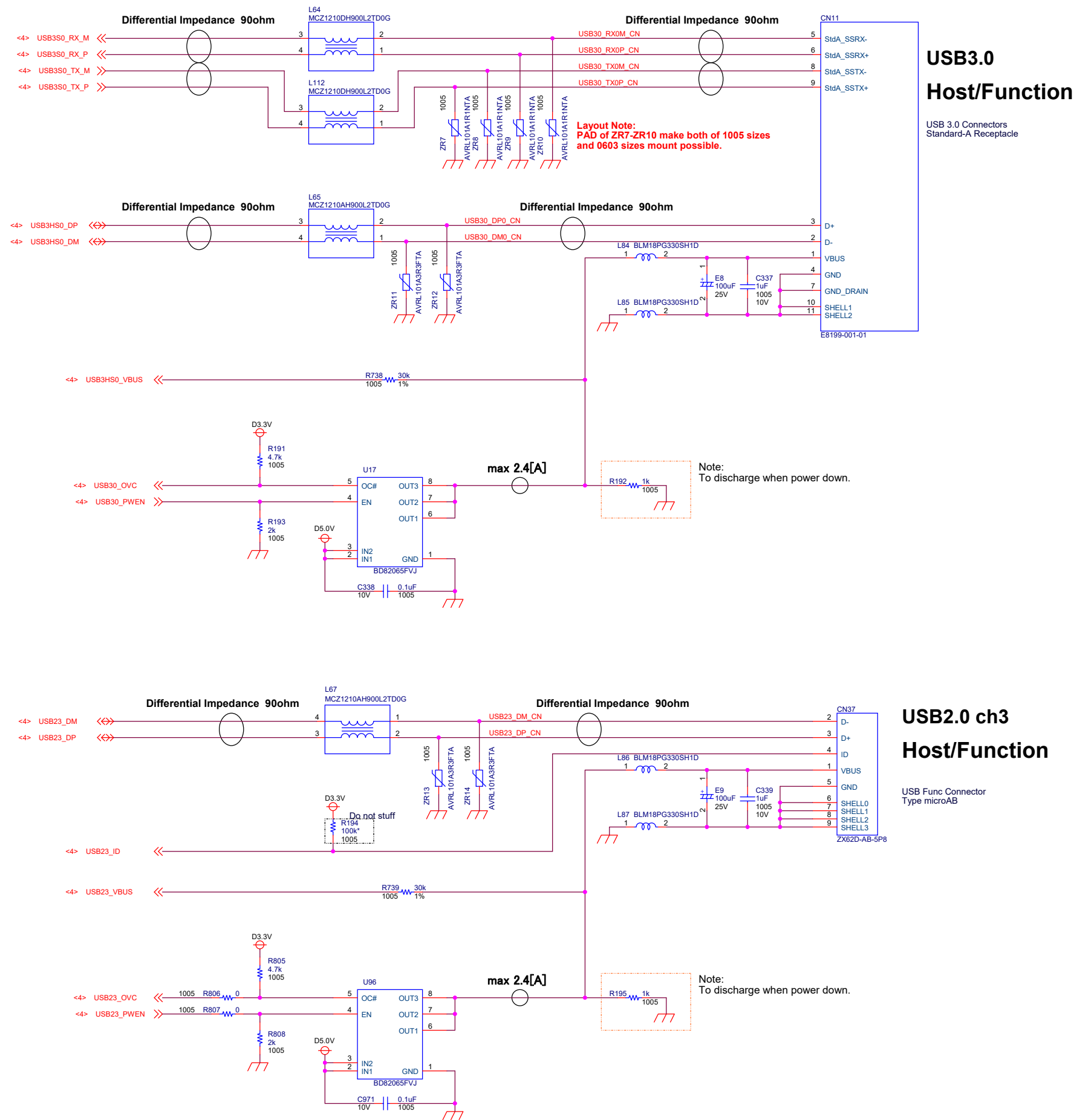
v : prefix indicates internal 120KOhm pull down resistor
^ : prefix indicates internal 120KOhm pull up resistor

Power Management Table

CKPWRGD_PD#	SMBus OE bit	DIFx OEx#	True O/P	Comp. O/P	REF
0	X	X	Low	Low	Hi-Z
1	1	1	Running	Running	Running
1	0	1	Low	Low	Low

SMBus Address Selection Table (I2C Slave address)

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

Select Spread Spectrum Table

vSS_EN_tri	Spread Spectrum
0	Spread Off
M	-0.25%
1	-0.5%

'M' is Mid Voltage = 0.5VDD = 0.9V.
This setting can be controled by software.
Refer to datasheet chapter of "SMBus Table : SS Readback and Control Register"

11

Serial ATA

Default Unit is "mm"

Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev 3.02
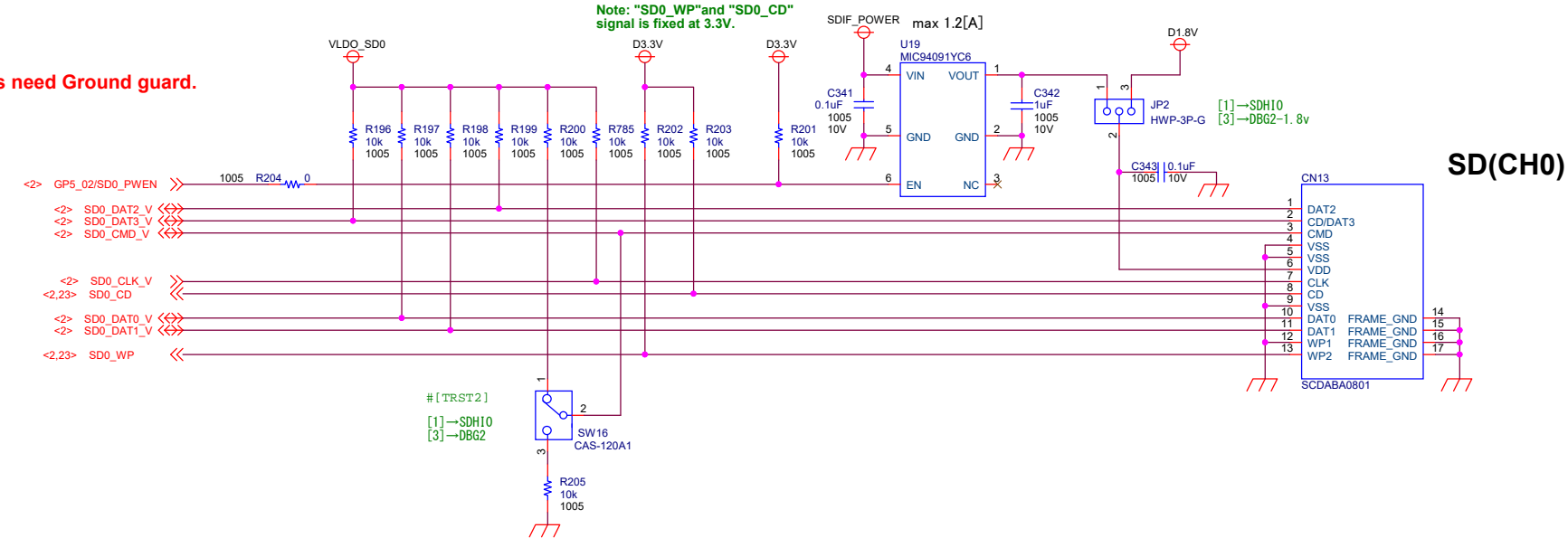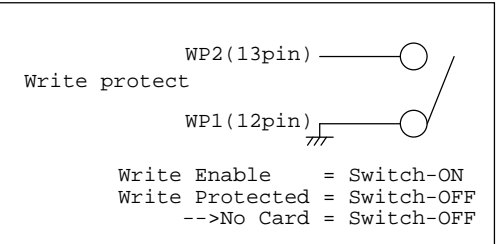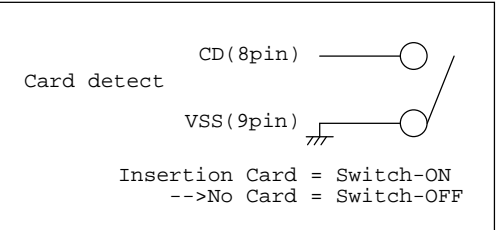Date: Tuesday, December 25, 2018   Sheet 11 of 26

Preliminary

USB On-the-Go回路

USB2.0 ch0

USB2.0 ch1

USB2.0 ch2

[Design Note]
The ID_IN pin is internally pulled up to Vcc=5V.

max 2.4[A]

Differential Impedance=90ohm +-15%
Differential Impedance =90ohm +-15%

USB Host/Func Connector
Type microAB

USB Host Connector
Type A
(Lower Part)

USB Host Connector
Type A
(Upper Part)

Insert USB cable from Here
Board
TOP VIEW

<4> USB20_ID0
<4,23> GP6_05/OTG_STAT1
<4,23> GP6_06/OTG_STAT2
<4,23> GP6_16/OTG_EXTLPn

<4> USB0_PWEN
<4> USB0_OVC
<4> USB20_VBUS0
<4> USB20_DM0
<4> USB20_DP0

<4> USB21_DM1
<4> USB21_DP1
<4> USB1_OVC
<4> USB1_PWEN

<4> USB22_DM2
<4> USB22_DP2
<4,23> USB2_OVC
<4,23> USB2_PWEN

U12 MAX3355EEUD
U13 BD82065FVJ
U15 BD82065FVJ
U16 BD82065FVJ

SW15 CJS-1201A

L61 MCZ1210AH900L2TD0G
L62 MCZ1210AH900L2TD0G
L63 MCZ1210AH900L2TD0G

CN9 ZX62D-AB-5P8
CN10A XM7A-0442-A
CN10B XM7A-0442-A

Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev 3.02
Date: Tuesday, December 25, 2018   Sheet   12   of   26

Preliminary

CONFIDENTIAL

Differential Impedance 90ohm

L64 MCZ1210DH900L2TD0G		

<4> USB3S0_RX_M
<4> USB3S0_RX_P
<4> USB3S0_TX_M
<4> USB3S0_TX_P

USB30_RX0M_CN
USB30_RX0P_CN
USB30_TX0M_CN
USB30_TX0P_CN

L112 MCZ1210DH900L2TD0G

1005 ZR7
AVRL101A1R1NTA ZR8
1005
AVRL101A1R1NTA ZR9
1005
AVRL101A1R1NTA ZR10
1005
AVRL101A1R1NTA

Layout Note:
PAD of ZR7-ZR10 make both of 1005 sizes
and 0603 sizes mount possible.

CN11
StdA_SSRX- 5
StdA_SSRX+ 6
StdA_SSTX- 8
StdA_SSTX+ 9

USB3.0
Host/Function

USB 3.0 Connectors
Standard-A Receptacle

Differential Impedance 90ohm

L65 MCZ1210AH900L2TD0G		

<4> USB3HS0_DP
<4> USB3HS0_DM

USB30_DP0_CN
USB30_DM0_CN

1005 ZR11
AVRL101A3R3FTA
1005 ZR12
AVRL101A3R3FTA

L84 BLM18PG330SH1D

L85 BLM18PG330SH1D

E8 100uF 25V
C337 1uF 1005 10V

D+ 3
D- 2
VBUS 1
GND 4
GND_DRAIN 7
SHELL1 10
SHELL2 11

E8199-001-01

<4> USB3HS0_VBUS
R738 30k 1005 1%

D3.3V
R191 4.7k 1005

<4> USB30_OVC
<4> USB30_PWEN

U17
OC# 5   OUT3 8
EN 4   OUT2 7
         OUT1 6

R193 2k 1005
D5.0V
IN2 3
IN1 2   GND 1
BD82065FVJ

C338 10V   0.1uF 1005

max 2.4[A]

R192 1k 1005

Note:
To discharge when power down.

Differential Impedance 90ohm

L67 MCZ1210AH900L2TD0G		

<4> USB23_DM
<4> USB23_DP

USB23_DM_CN
USB23_DP_CN

1005 ZR13
AVRL101A3R3FTA
1005 ZR14
AVRL101A3R3FTA

L86 BLM18PG330SH1D

L87 BLM18PG330SH1D

E9 100uF 25V
C339 1uF 1005 10V

CN37
D- 2
D+ 3
ID 4
VBUS 1
GND 5
SHELL0 6
SHELL1 7
SHELL2 8
SHELL3 9

ZX62D-AB-5P8

USB2.0 ch3
Host/Function

USB Func Connector
Type microAB

D3.3V
Do not stuff
R194 100k* 1005

<4> USB23_ID

<4> USB23_VBUS
R739 30k 1005 1%

D3.3V
R805 4.7k 1005

<4> USB23_OVC   1005 R806 0
<4> USB23_PWEN   1005 R807 0

U96
OC# 5   OUT3 8
EN 4   OUT2 7
         OUT1 6

R808 2k 1005
D5.0V
IN2 3
IN1 2   GND 1
BD82065FVJ

C971 10V   0.1uF 1005

max 2.4[A]

R195 1k 1005

Note:
To discharge when power down.

USB3.0

13

Title
R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)

Size A2
Document Number
R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev 3.02

Preliminary

Layout Note:
Following signals need Ground guard.
SD0_CLK_V

Note: "SD0_WP"and "SD0_CD"
signal is fixed at 3.3V.

SDIF_POWER   max 1.2[A]

D1.8V

VLDO_SD0   D3.3V   D3.3V
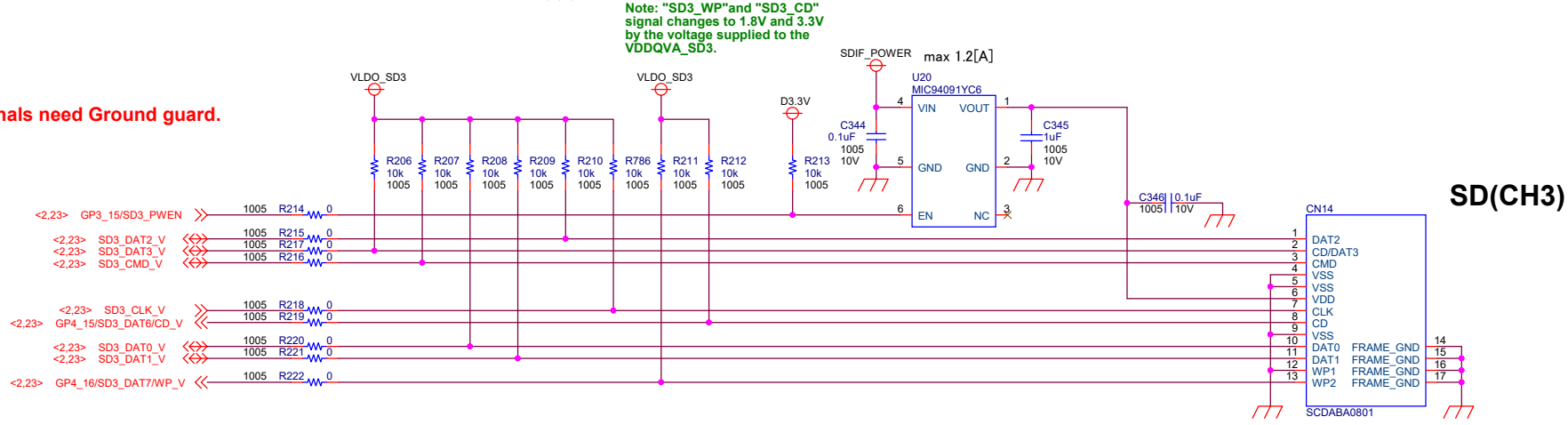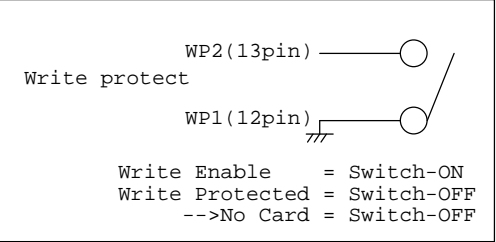
SDHI0 (CLK,CMD,DAT[3:0])
  (1) Matched trace length.
  (2) Single ended impedance = 50ohm

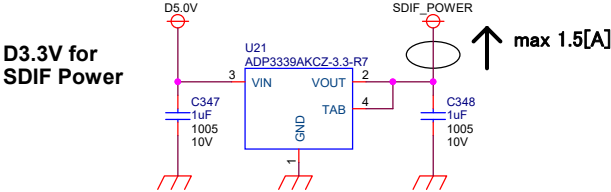U19
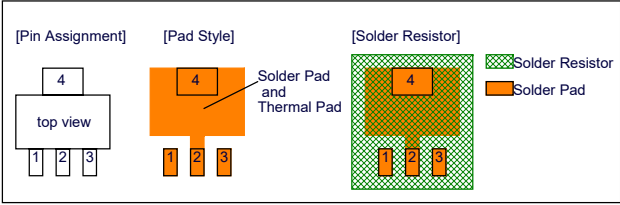MIC94091YC6
4 VIN   VOUT 1
C341
0.1uF
1005
10V
5 GND   GND
6 EN   NC 3

C342
1uF
1005
10V

JP2
HWP-3P-G
[1]→SDHI0
[3]→DBG2-1.8v

C343 0.1uF
1005 10V

SD(CH0)

CN13
1 DAT2
2 CD/DAT3
3 CMD
4 VSS
5 VSS
6 VDD
7 CLK
8 CD
9 VSS
10 DAT0   FRAME_GND 14
11 DAT1   FRAME_GND 15
12 WP1   FRAME_GND 16
13 WP2   FRAME_GND 17
SCDABA0801

R196 R197 R198 R199 R200 R785 R202 R203 R201
10k 10k 10k 10k 10k 10k 10k 10k 10k
1005 1005 1005 1005 1005 1005 1005 1005 1005

<2> GP5_02/SD0_PWEN   1005 R204 0
<2> SD0_DAT2_V
<2> SD0_DAT3_V
<2> SD0_CMD_V
<2> SD0_CLK_V
<2,23> SD0_CD
<2> SD0_DAT0_V
<2> SD0_DAT1_V
<2,23> SD0_WP

#[TRST2]
[1]→SDHI0
[3]→DBG2
SW16
CAS-120A1

R205
10k
1005

Card detect

CD(8pin)
VSS(9pin)

Insertion Card = Switch-ON
-->No Card = Switch-OFF

Write protect

WP2(13pin)
WP1(12pin)

Write Enable   = Switch-ON
Write Protected = Switch-OFF
-->No Card = Switch-OFF

Note: "SD3_WP"and "SD3_CD"
signal changes to 1.8V and 3.3V
by the voltage supplied to the
VDDQVA_SD3.

Layout Note:
Following signals need Ground guard.
SD3_CLK_V

SDIF_POWER   max 1.2[A]

VLDO_SD3   VLDO_SD3   D3.3V

SDHI3 (CLK,CMD,DAT[3:0])
  (1) Matched trace length.
  (2) Single ended impedance = 50ohm

U20
MIC94091YC6
4 VIN   VOUT 1
C344
1uF
1005
10V
5 GND   GND
6 EN   NC

C345
1uF
1005
10V

C346 0.1uF
1005 10V

SD(CH3)

CN14
1 DAT2
2 CD/DAT3
3 CMD
4 VSS
5 VSS
6 VDD
7 CLK
8 CD
9 VSS
10 DAT0   FRAME_GND 14
11 DAT1   FRAME_GND 15
12 WP1   FRAME_GND 16
13 WP2   FRAME_GND 17
SCDABA0801

R206 R207 R208 R209 R210 R786 R211 R212 R213
10k 10k 10k 10k 10k 10k 10k 10k 10k
1005 1005 1005 1005 1005 1005 1005 1005 1005

<2,23> GP3_15/SD3_PWEN   1005 R214 0
<2,23> SD3_DAT2_V   1005 R215 0
<2,23> SD3_DAT3_V   1005 R217 0
<2,23> SD3_CMD_V   1005 R216 0
<2,23> SD3_CLK_V   1005 R218 0
<2,23> GP4_15/SD3_DAT6/CD_V 1005 R219 0
<2,23> SD3_DAT0_V   1005 R220 0
<2,23> SD3_DAT1_V   1005 R221 0
<2,23> GP4_16/SD3_DAT7/WP_V 1005 R222 0

Card detect

CD(8pin)
VSS(9pin)

Insertion Card = Switch-ON
-->No Card = Switch-OFF

Write protect

WP2(13pin)
WP1(12pin)

Write Enable   = Switch-ON
Write Protected = Switch-OFF
-->No Card = Switch-OFF

Layout Note:
Pad Configuration for ADP3339

[Pin Assignment]   [Pad Style]   [Solder Resistor]
4   4   4
top view   Solder Pad   Solder Resistor
                   and   Solder Pad
                   Thermal Pad
1 2 3   1 2 3   1 2 3

D3.3V for
SDIF Power

D5.0V   SDIF_POWER   max 1.5[A]
U21
ADP3339AKCZ-3.3-R7
3 VIN   VOUT 2
C347   C348
1uF   GND TAB 4   1uF
1005   1005
10V   10V

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SDHI0/SDHI3

14

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Title
R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size A2   Document Number   R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)   Rev 3.02
Date: Tuesday, December 25, 2018   Sheet 14 of 26

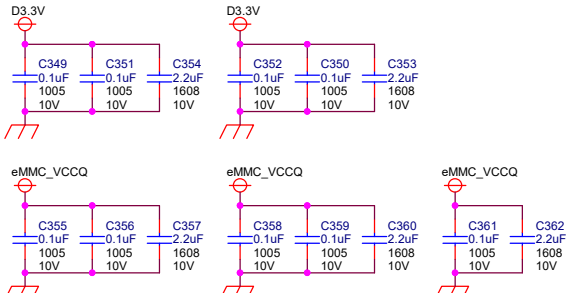# Preliminary

Layout Note:
As short as possible from junction of MMC0_xxx to two Rxxx.

[R-CarH3-SiP side]   [eMMC side]
MMC0_xxx   Rxxx   eMMC_xxx_18
             Rxxx   EX_MMC_xxx   [connector side]

Do not stuff

<2> MMC0_DTA0_V   R225 0 1005 eMMC_D0_18
    R617 0* 1005   EX_MMC_D0_V <23>
<2> MMC0_DTA1_V   R226 0 1005 eMMC_D1_18
    R619 0* 1005   EX_MMC_D1_V <23>
<2> MMC0_DTA2_V   R227 0 1005 eMMC_D2_18
    R620 0* 1005   EX_MMC_D2_V <23>
<2> MMC0_DTA3_V   R228 0 1005 eMMC_D3_18
    R618 0* 1005   EX_MMC_D3_V <23>
<2> MMC0_DTA4_V   R229 0 1005 eMMC_D4_18
    R621 0* 1005   EX_MMC_D4_V <23>
<2> MMC0_DTA5_V   R231 0 1005 eMMC_D5_18
    R622 0* 1005   EX_MMC_D5_V <23>
<2> MMC0_DTA6_V   R230 0 1005 eMMC_D6_18
    R623 0* 1005   EX_MMC_D6_V <23>
<2> MMC0_DTA7_V   R232 0 1005 eMMC_D7_18
    R626 0* 1005   EX_MMC_D7_V <23>
<2> MMC0_CMD_V   R233 0 1005 eMMC_CMD_18
    R627 0* 1005   EX_MMC_CMD_V <23>
<2> MMC0_CLK_V   R234 0 1005 eMMC_CLK_18
    R628 0* 1005   EX_MMC_CLK_V <23>
<2> MMC0_DS_V   R235 0 1005 eMMC_DS_18
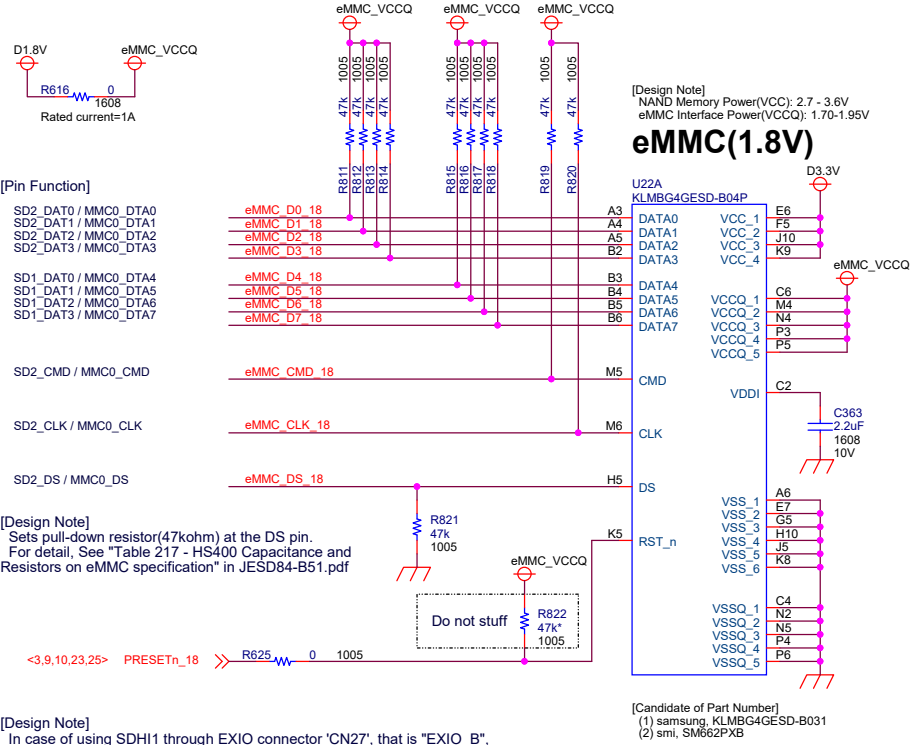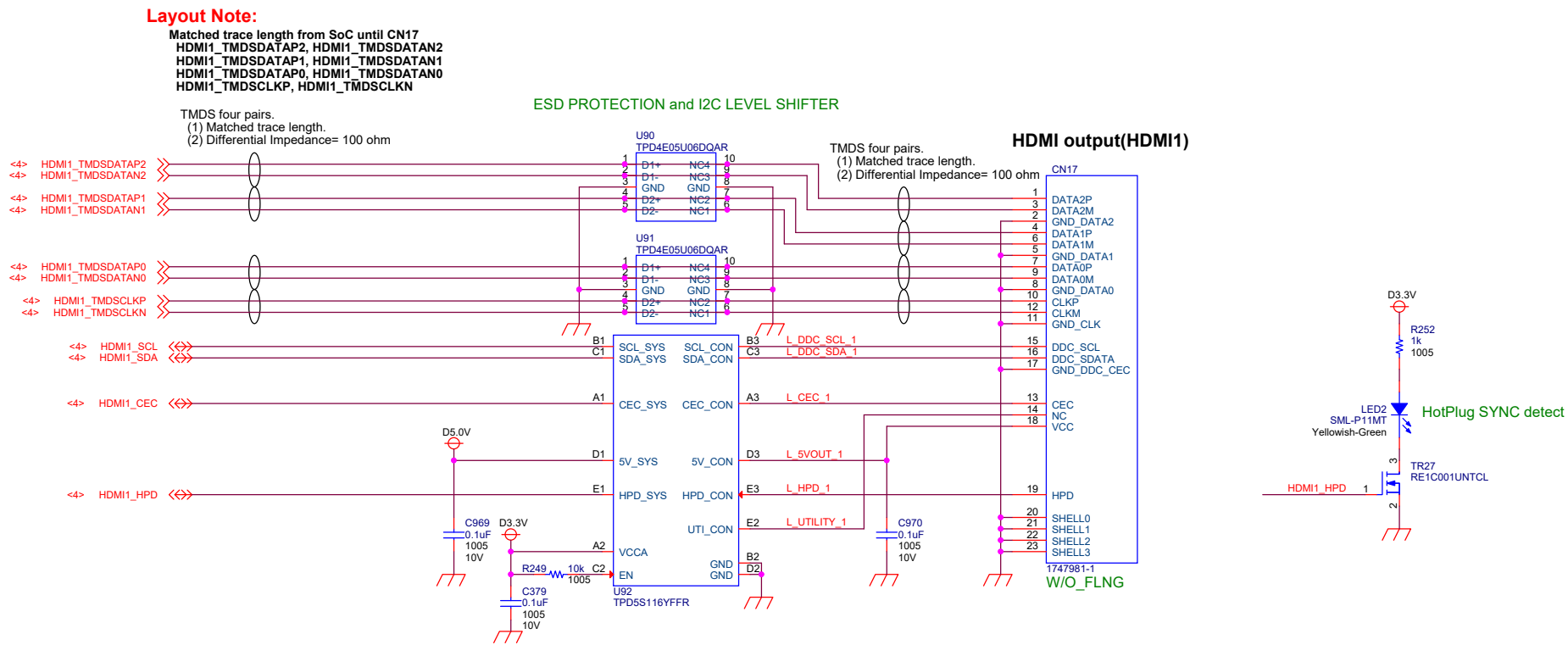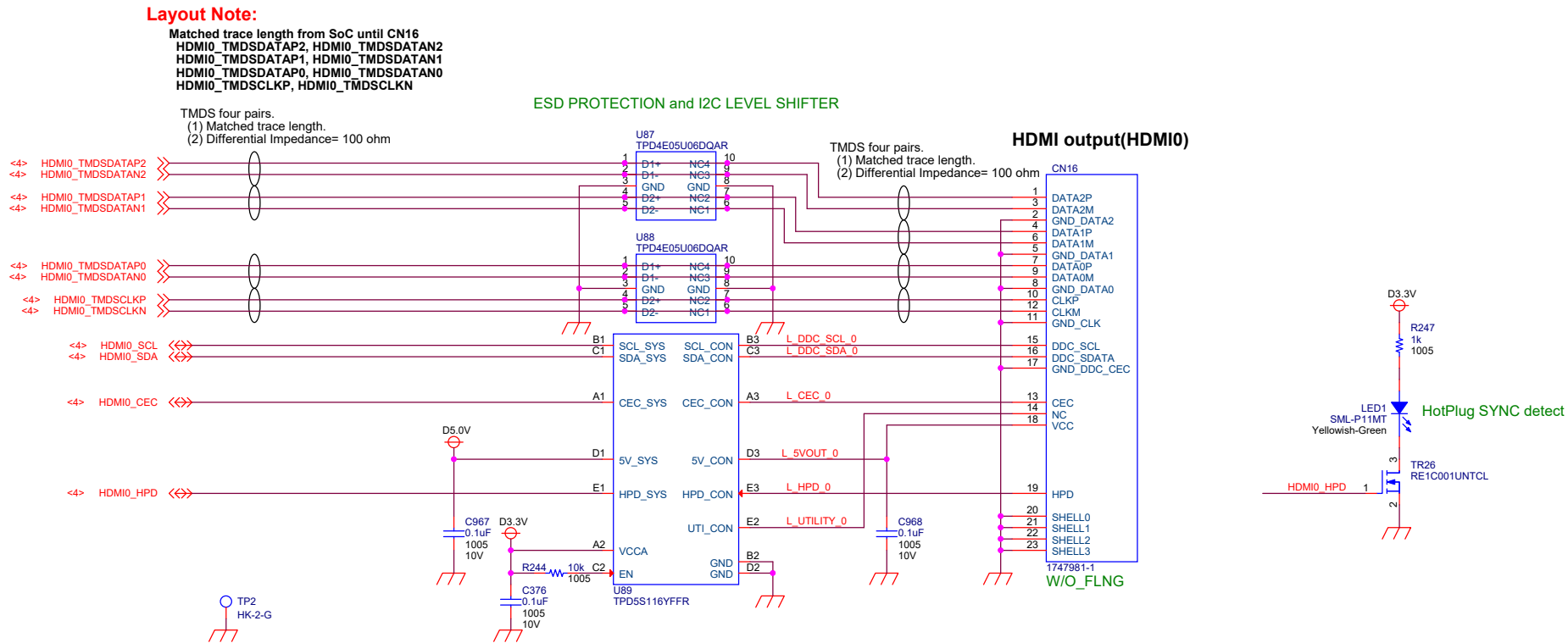   R629 0* 1005   EX_MMC_DS_V <23>

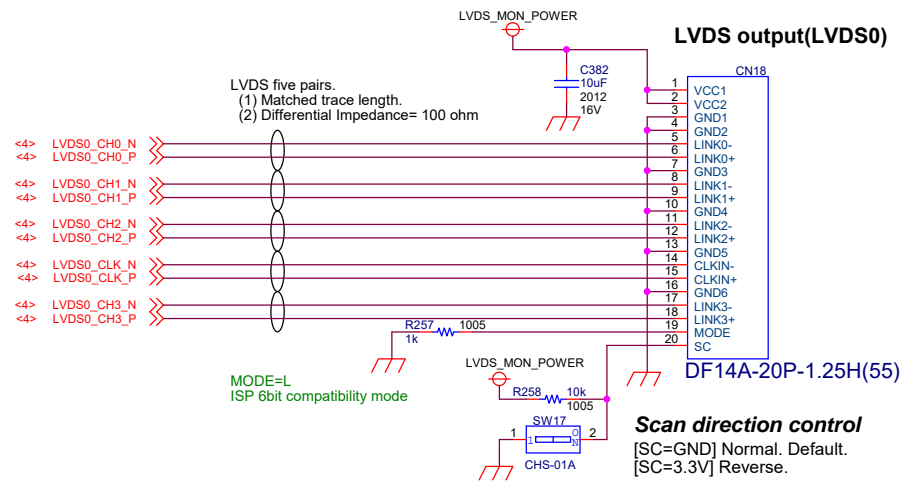**Layout Note:**
Following signals need Ground guard.

MMC0_CLK_V, eMMC_CLK_18, EX_MMC_CLK_V

Layout Note:
(1) Matched Trace Length from R-CarH3-SiP to eMMC. (max 400Mbps/pin)
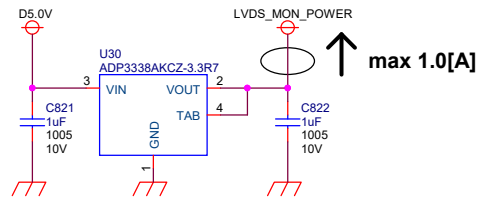(2) Single ended impedance = 50ohm

Group 1
MMC0_DTA[7:0]_V + eMMC_D[7:0]_18
MMC0_CMD_V + eMMC_CMD_18
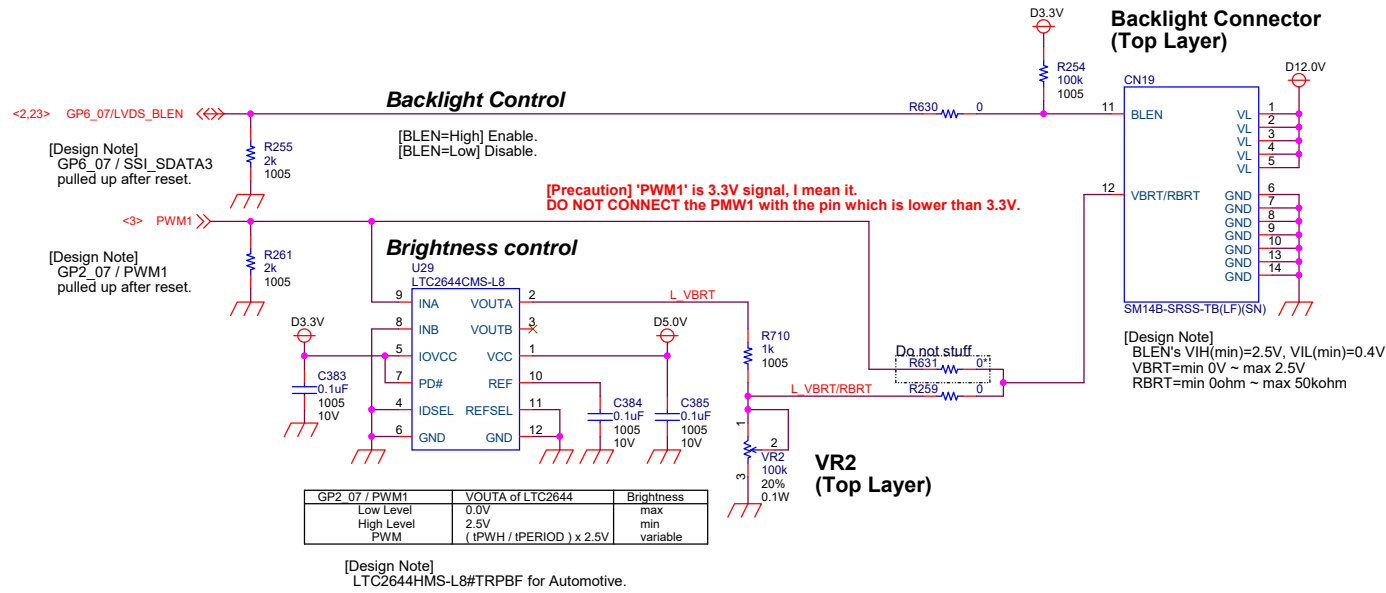MMC0_CLK_V + eMMC_CLK_18
MMC0_DS_V + eMMC_DS_18

D1.8V   eMMC_VCCQ
R616 0 1608
Rated current=1A

[Design Note]
NAND Memory Power(VCC): 2.7 - 3.6V
eMMC Interface Power(VCCQ): 1.70-1.95V

eMMC(1.8V)

eMMC_VCCQ eMMC_VCCQ eMMC_VCCQ
R811 R812 R813 R814 47k 47k 47k 47k 1005
R815 R816 R817 R818 47k 47k 47k 47k 1005
R819 R820 47k 47k 1005

[Pin Function]
SD2_DAT0 / MMC0_DTA0   eMMC_D0_18   A3 DATA0
SD2_DAT1 / MMC0_DTA1   eMMC_D1_18   A4 DATA1
SD2_DAT2 / MMC0_DTA2   eMMC_D2_18   A5 DATA2
SD2_DAT3 / MMC0_DTA3   eMMC_D3_18   B2 DATA3

SD1_DAT0 / MMC0_DTA4   eMMC_D4_18   B3 DATA4
SD1_DAT1 / MMC0_DTA5   eMMC_D5_18   B4 DATA5
SD1_DAT2 / MMC0_DTA6   eMMC_D6_18   B5 DATA6
SD1_DAT3 / MMC0_DTA7   eMMC_D7_18   B6 DATA7

SD2_CMD / MMC0_CMD   eMMC_CMD_18   M5 CMD

SD2_CLK / MMC0_CLK   eMMC_CLK_18   M6 CLK

SD2_DS / MMC0_DS   eMMC_DS_18   H5 DS

[Design Note]
Sets pull-down resistor(47kohm) at the DS pin.
For detail, See "Table 217 - HS400 Capacitance and
Resistors on eMMC specification" in JESD84-B51.pdf

R821 47k 1005

Do not stuff
R822 47k* 1005

<3,9,10,23,25> PRESETn_18   R625 0 1005   K5 RST_n

U22A
KLMBG4GESD-B04P
VCC_1 E6
VCC_2 F5
VCC_3 J10
VCC_4 K9
VCCQ_1 C6
VCCQ_2 M4
VCCQ_3 N4
VCCQ_4 P3
VCCQ_5 P5
VDDI C2
VSS_1 A6
VSS_2 E7
VSS_3 G5
VSS_4 H10
VSS_5 J5
VSS_6 K8
VSSQ_1 C4
VSSQ_2 N2
VSSQ_3 N5
VSSQ_4 P4
VSSQ_5 P6

D3.3V
eMMC_VCCQ

C363 2.2uF 1608 10V

[Candidate of Part Number]
(1) samsung, KLMBG4GESD-B031
(2) smi, SM662PXB

[Design Note]
In case of using SDHI1 through EXIO connector 'CN27', that is "EXIO_B",
DISMOUNT follwoing resistors.
R229, R231, R230, R232(0ohm/1005).
and MOUNT following resistors.
R621, R622, R623, R626(0ohm/1005).

[Design Note]
In case of using SDHI2 through EXIO connector 'CN27', that is "EXIO_B",
DISMOUNT follwoing resistors.
R229, R231, R230, R232(0ohm/1005).
and MOUNT following resistors.
R621, R622, R623, R626(0ohm/1005).

DISMOUNT follwoing resistors
R225, R226, R227, R228, R233, R234, R235(0ohm/1005)
R625(0ohm/1005) for PRESETn_18
and MOUNT following resistors.
R617, R619, R620, R618, R627, R628, R629(0ohm/1005)

and MOUNT following resistors.
R224(47k/1608) to prevent eMMC's CLK-pin floating.
R624(47k/1608) to prevent eMMC's RST_n-pin floatting.

D3.3V
C349 0.1uF 1005 10V
C351 0.1uF 1005 10V
C354 2.2uF 1608 10V

D3.3V
C352 0.1uF 1005 10V
C350 0.1uF 1005 10V
C353 2.2uF 1608 10V

eMMC_VCCQ
C355 0.1uF 1005 10V
C356 0.1uF 1005 10V
C357 2.2uF 1608 10V

eMMC_VCCQ
C358 0.1uF 1005 10V
C359 0.1uF 1005 10V
C360 2.2uF 1608 10V

eMMC_VCCQ
C361 0.1uF 1005 10V
C362 2.2uF 1608 10V

U22B
KLMBG4GESD-B04P

NC   RFU   VSF

MMC0

Preliminary

CONFIDENTIAL

D/A CONVERTER

DU_DR7 DU_DR6 DU_DR5 DU_DR4 DU_DR3 DU_DR2 DU_DR1 DU_DR0

<3,8,9,23> ExD[8..15]

ExD15 48 R9
ExD14 47 R8
ExD13 46 R7
ExD12 45 R6
ExD11 44 R5
ExD10 43 R4
ExD9   42 R3
ExD8   41 R2
       40 R1
       39 R0

DU_DG7 DU_DG6 DU_DG5 DU_DG4 DU_DG3 DU_DG2 DU_DG1 DU_DG0

<3,8,9,23> ExA[12..19]

DU_DGx are not in order.

ExA15 10 G9
ExA14 9   G8
ExA13 8   G7
ExA12 7   G6
ExA19 6   G5
ExA18 5   G4
ExA17 4   G3
ExA16 3   G2
       2   G1
       1   G0

DU_DB7 DU_DB6 DU_DB5 DU_DB4 DU_DB3 DU_DB2 DU_DB1 DU_DB0

<3,8,9,23> ExA[0..7]

ExA7 23 B9
ExA6 22 B8
ExA5 21 B7
ExA4 20 B6
ExA3 19 B5
ExA2 18 B4
ExA1 17 B3
ExA0 16 B2
      15 B1
      14 B0

<3,9,23> IRQ2n/DU_DISP
<3,10,19,20,21,23> PRESETOUTn

12 _SYNC
11 _BLANK
38 _PSAVE

<3,9,23> EX_WAIT0n/DU_DCLK0

24 CLOCK

U24
ADV7123KSTZ140

VAA1 13
VAA2 29
VAA3 30

COMP 35
VREF 36
RSET 37

R238 536

D44 AD1580ARTZ

C371 0.1uF 1005 10V
C372 1uF 1005 10V

R789 1k 1005 1%

V3.3V

C365 0.01uF 1005 25V
C366 0.1uF 1005 10V
C367 0.01uF 1005 25V
C368 0.1uF 1005 10V
C369 0.01uF 1005 25V
C370 0.1uF 1005 10V

IOR   34
_IOR 33

IOG   32
_IOG 31

IOB   28
_IOB 27

GND1 25
GND2 26

Impedance=75ohm

L31 EMI-FIL NFW31SP107X1E4
L32 EMI-FIL NFW31SP107X1E4
L33 EMI-FIL NFW31SP107X1E4

Impedance=75ohm

R239 75.0 1% 1005
R240 75.0 1% 1005
R241 75.0 1% 1005

D19 RB706W-40FH
D20 RB706W-40FH
D21 RB706W-40FH

V3.3V

AnalogRGB(DU)

CN15
1   RED
2   GREEN
3   BLUE
4   RESRV1
5   GND1
6   RGND1
7   GGND1
8   BGND1
9   PLUG
10 GND2
11 SENSE0
12 SENSE1
13 HSYNC
14 VSYNC
15 RESRV2
16 SHELL0
17 SHELL1
D02-M15SAG-23L9E

TP1
HK-2-G

Layout Note:
Following signals need Ground guard.
DU_DOTCLKOUT0_3

<3,9,23> GP/ExA24/DU_HSYNC

D5.0V

U25
1
2
4 HSYNC_5
3
HD74LV1GT08A

<3,9,23> GP/ExA23/DU_VSYNC

D5.0V

U26
1
2
4 VSYNC_5
3
HD74LV1GT08A

D5.0V D5.0V
C373 0.1uF 1005 10V
C374 0.1uF 1005 10V

D3.3V L88 BLM18AG102SH1D V3.3V
C375 10uF 2012 16V

DU_ARGB

16

Preliminary

Layout Note:
Matched trace length from SoC until CN16
HDMI0_TMDSDATAP2, HDMI0_TMDSDATAN2
HDMI0_TMDSDATAP1, HDMI0_TMDSDATAN1
HDMI0_TMDSDATAP0, HDMI0_TMDSDATAN0
HDMI0_TMDSCLKP, HDMI0_TMDSCLKN

TMDS four pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

ESD PROTECTION and I2C LEVEL SHIFTER

U87
TPD4E05U06DQAR

HDMI output(HDMI0)

TMDS four pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

CN16

<4> HDMI0_TMDSDATAP2
<4> HDMI0_TMDSDATAN2

<4> HDMI0_TMDSDATAP1
<4> HDMI0_TMDSDATAN1

<4> HDMI0_TMDSDATAP0
<4> HDMI0_TMDSDATAN0

<4> HDMI0_TMDSCLKP
<4> HDMI0_TMDSCLKN

U88
TPD4E05U06DQAR

DATA2P
DATA2M
GND_DATA2
DATA1P
DATA1M
GND_DATA1
DATA0P
DATA0M
GND_DATA0
CLKP
CLKM
GND_CLK

<4> HDMI0_SCL
<4> HDMI0_SDA

SCL_SYS SCL_CON   L_DDC_SCL_0
SDA_SYS SDA_CON   L_DDC_SDA_0

DDC_SCL
DDC_SDATA
GND_DDC_CEC

D3.3V

R247
1k
1005

<4> HDMI0_CEC

CEC_SYS CEC_CON   L_CEC_0

CEC
NC
VCC

LED1
SML-P11MT
Yellowish-Green

HotPlug SYNC detect

D5.0V

5V_SYS   5V_CON   L_5VOUT_0

<4> HDMI0_HPD

HPD_SYS HPD_CON   L_HPD_0

HPD

TR26
RE1C001UNTCL

HDMI0_HPD

UTI_CON   L_UTILITY_0

C967
0.1uF
1005
10V

D3.3V

C968
0.1uF
1005
10V

SHELL0
SHELL1
SHELL2
SHELL3

1747981-1

R244 10k C2
1005

A2 VCCA

EN   GND
            GND

B2
D2

W/O_FLNG

C376
0.1uF
1005
10V

U89
TPD5S116YFFR

TP2
HK-2-G

Layout Note:
Matched trace length from SoC until CN17
HDMI1_TMDSDATAP2, HDMI1_TMDSDATAN2
HDMI1_TMDSDATAP1, HDMI1_TMDSDATAN1
HDMI1_TMDSDATAP0, HDMI1_TMDSDATAN0
HDMI1_TMDSCLKP, HDMI1_TMDSCLKN

TMDS four pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

ESD PROTECTION and I2C LEVEL SHIFTER

U90
TPD4E05U06DQAR

HDMI output(HDMI1)

TMDS four pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

CN17

<4> HDMI1_TMDSDATAP2
<4> HDMI1_TMDSDATAN2

<4> HDMI1_TMDSDATAP1
<4> HDMI1_TMDSDATAN1

<4> HDMI1_TMDSDATAP0
<4> HDMI1_TMDSDATAN0

<4> HDMI1_TMDSCLKP
<4> HDMI1_TMDSCLKN

U91
TPD4E05U06DQAR

DATA2P
DATA2M
GND_DATA2
DATA1P
DATA1M
GND_DATA1
DATA0P
DATA0M
GND_DATA0
CLKP
CLKM
GND_CLK

<4> HDMI1_SCL
<4> HDMI1_SDA

SCL_SYS SCL_CON   L_DDC_SCL_1
SDA_SYS SDA_CON   L_DDC_SDA_1

DDC_SCL
DDC_SDATA
GND_DDC_CEC

D3.3V

R252
1k
1005

<4> HDMI1_CEC

CEC_SYS CEC_CON   L_CEC_1

CEC
NC
VCC

LED2
SML-P11MT
Yellowish-Green

HotPlug SYNC detect

D5.0V

5V_SYS   5V_CON   L_5VOUT_1

<4> HDMI1_HPD

HPD_SYS HPD_CON   L_HPD_1

HPD

TR27
RE1C001UNTCL

HDMI1_HPD

UTI_CON   L_UTILITY_1

C969
0.1uF
1005
10V

D3.3V

C970
0.1uF
1005
10V

SHELL0
SHELL1
SHELL2
SHELL3

1747981-1

R249 10k C2
1005

A2 VCCA

EN   GND
            GND

B2
D2

W/O_FLNG

C379
0.1uF
1005
10V

U92
TPD5S116YFFR

HDMI_OUT

17

Title
R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)

Size	Document Number	Rev
A2	R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)	3.02

Date: Tuesday, December 25, 2018   Sheet   17   of   26

LVDS output(LVDS0)

LVDS_MON_POWER

C382
10uF
2012
16V

LVDS five pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

CN18

1	VCC1
2	VCC2
3	GND1
4	GND2
5	LINK0-
6	LINK0+
7	GND3
8	LINK1-
9	LINK1+
10	GND4
11	LINK2-
12	LINK2+
13	GND5
14	CLKIN-
15	CLKIN+
16	GND6
17	LINK3-
18	LINK3+
19	MODE
20	SC

<4> LVDS0_CH0_N
<4> LVDS0_CH0_P
<4> LVDS0_CH1_N
<4> LVDS0_CH1_P
<4> LVDS0_CH2_N
<4> LVDS0_CH2_P
<4> LVDS0_CLK_N
<4> LVDS0_CLK_P
<4> LVDS0_CH3_N
<4> LVDS0_CH3_P

R257 1005
1k

DF14A-20P-1.25H(55)

MODE=L
ISP 6bit compatibility mode

LVDS_MON_POWER

R258 10k
1005

SW17
CHS-01A
1 2

Scan direction control
[SC=GND] Normal. Default.
[SC=3.3V] Reverse.

3.3V for LVDS Monitor Power

D5.0V   LVDS_MON_POWER

U30
ADP3338AKCZ-3.3R7
VIN   VOUT
GND   TAB

C821   C822
1uF   1uF
1005   1005
10V   10V

max 1.0[A]

Layout Note:
Pad Configuration for ADP3338

[Pin Assignment]   [Pad Style]   [Solder Resistor]

Solder Pad
and
Thermal Pad

top view

Solder Resistor
Solder Pad

Backlight Connector
(Top Layer)

D3.3V

R254
100k
1005

D12.0V

<2,23> GP6_07/LVDS_BLEN

Backlight Control

R630 0

CN19

11	BLEN
12	VBRT/RBRT

1	VL
2	VL
3	VL
4	VL
5	VL
6	GND
7	GND
8	GND
9	GND
10	GND
13	GND
14	GND

SM14B-SRSS-TB(LF)(SN)

[BLEN=High] Enable.
[BLEN=Low] Disable.

[Design Note]
GP6_07 / SSI_SDATA3
pulled up after reset.

R255
2k
1005

[Precaution] 'PWM1' is 3.3V signal, I mean it.
DO NOT CONNECT the PMW1 with the pin which is lower than 3.3V.

<3> PWM1

[Design Note]
GP2_07 / PWM1
pulled up after reset.

R261
2k
1005

Brightness control

D3.3V

U29
LTC2644CMS-L8

9	INA	VOUTA	2
8	INB	VOUTB	3
5	IOVCC	VCC	1
7	PD#	REF	10
4	IDSEL	REFSEL	11
6	GND	GND	12

L_VBRT

D5.0V

C383   C384   C385
0.1uF   0.1uF   0.1uF
1005   1005   1005
10V   10V   10V

R710
1k
1005

Do not stuff
R631   0*
L_VBRT/RBRT
R259   0

VR2
100k
20%
0.1W

VR2
(Top Layer)

[Design Note]
BLEN's VIH(min)=2.5V, VIL(min)=0.4V
VBRT=min 0V ~ max 2.5V
RBRT=min 0ohm ~ max 50kohm

GP2_07 / PWM1	VOUTA of LTC2644	Brightness
Low Level	0.0V	max
High Level	2.5V	min
PWM	(tPWH / tPERIOD) x 2.5V	variable

[Design Note]
LTC2644HMS-L8#TRPBF for Automotive.

LVDS0

18

Title
R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)

Size	Document Number	Rev
A2	R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)	3.02

Date: Tuesday, December 25, 2018   Sheet 18 of 26

Preliminary

Layout Note:
Connect Dx with NCx under the TPD4E05U06DQAR. See below figure.

Pin1,2   Pin10,9
Pin4,5   Pin7,6

VIDEO DECODER FOR MIPI CSI-2
(channel 0, channel 1)

Layout Note:
Connect the shell of 1747981-1 with ground.
The 1747981-1 has four through holes.

HDMI Input Connector TYPE A(Standard)

TMDS four pairs
Differential Impedance
100ohm +-10%
Matched trace length.

Note:
ESD Protection diode array.

TMDS four pairs
Differential Impedance
100ohm +-10%
Matched trace length.

Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI0_xxxx + CSI0_xxxx

U31
ADV7482WBBCZ

CN20

12	TMDS_CLK-	RXA_CN	RXA_CN
10	TMDS_CLK+	RXA_CP	RXA_CP
11	CK_SHLD		
9	TMDS_DATA0-	RXA_0N	RXA_0N
7	TMDS_DATA0+	RXA_0P	RXA_0P
8	D0_SHLD		
6	TMDS_DATA1-	RXA_1N	RXA_1N
4	TMDS_DATA1+	RXA_1P	RXA_1P
5	D1_SHLD		
3	TMDS_DATA2-	RXA_2N	RXA_2N
1	TMDS_DATA2+	RXA_2P	RXA_2P
2	D2_SHLD		

ADV_CSI0_CLKN <23>
ADV_CSI0_CLKP <23>

ADV_CSI0_DATAN0 <23>
ADV_CSI0_DATAP0 <23>

ADV_CSI0_DATAN1 <23>
ADV_CSI0_DATAP1 <23>

ADV_CSI0_DATAN2 <23>
ADV_CSI0_DATAP2 <23>

ADV_CSI0_DATAN3 <23>
ADV_CSI0_DATAP3 <23>

Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI1_xxxx + CSI1_xxxx

ADV_CSI1_CLKN <23>
ADV_CSI1_CLKP <23>

ADV_CSI1_DATAN0 <23>
ADV_CSI1_DATAP0 <23>

HOTPLUG_DET
DDC_+5V
DDC/CEC_GND
DDC_SDA
DDC_SCL
RESERVED
CEC

1747981-1
Place at Top layer.

SHELL0
SHELL1
SHELL2
SHELL3

HPA_A
DDCA_SDA
DDCA_SCL
CEC_A

R632 1k* 1005
Do not stuff.

CVBS Input Connector

CN21
LPR6520-1501F

Impedance 75ohm

CVBS_AIN8

Layout Note:
Following signals need Ground guard.
CVBS_AIN8(CN21 to U31-pinC10)

R268 24.0 1% 1005
R269 51.0 1% 1005
C823 0.1uF 1005 10V

R266 100k 1005

TP3 HK-2-G

AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
AIN8

DIAG1
DIAG2
DIAG3
DIAG4

L_AIN8

MVDD_A1.8V

C391	C392	C393	C394	C395	C396
0.1uF	0.01uF	0.1uF	0.01uF	0.1uF	0.01uF
1005	1005	1005	1005	1005	1005
10V	25V	10V	25V	10V	25V

MVDD
MVDD
MVDD

CVDD_A1.8V

CVDD

C399	C400
0.1uF	0.01uF
1005	1005
10V	25V

TVDD_A3.3V

TVDD

C402	C403
0.1uF	0.01uF
1005	1005
10V	25V

DVDD_D1.8V

DVDD

C405	C406	C407	C408
0.1uF	0.01uF	0.1uF	0.01uF
1005	1005	1005	1005
10V	25V	10V	25V

AVDD_A1.8V

AVDD

C410	C411
0.1uF	0.01uF
1005	1005
10V	25V

DVDDIO_D3.3V

DVDDIO

C412	C413
0.1uF	0.01uF
1005	1005
10V	25V

PVDD_A1.8V

PVDD

C416	C417
0.1uF	0.01uF
1005	1005
10V	25V

LC filters for ADV7482W

Ref	Part	
L89	BLM18AG102SH1D Rated current=400mA	D1.8V → MVDD_A1.8V
C398	10uF 2012 16V	
L90	BLM18AG102SH1D Rated current=400mA	D1.8V → CVDD_A1.8V
C401	10uF 2012 16V	
L91	BLM18AG102SH1D Rated current=400mA	D3.3V → TVDD_A3.3V
C404	10uF 2012 16V	
L92	BLM18AG102SH1D Rated current=400mA	D1.8V → DVDD_D1.8V
C409	10uF 2012 16V	
L93	BLM18AG102SH1D Rated current=400mA	D1.8V → AVDD_A1.8V
C414	10uF 2012 16V	
L94	BLM18AG102SH1D Rated current=400mA	D3.3V → DVDDIO_D3.3V
C418	10uF 2012 16V	
L95	BLM18AG102SH1D Rated current=400mA	D1.8V → PVDD_A1.8V
C421	10uF 2012 16V	

X8
NX2016SA[28.63636MHz/30pF/15ppm]

XTALN
XTALP

C390 47pF 1005 50V
C397 47pF 1005 50V
L_XTALN
L_XTALP

Layout Note:
Following signals need Ground guard.
GP6_30/INTRQ1, GP6_31/INTRQ2

DVDDIO_D3.3V   DVDDIO_D3.3V

[Design Note]
INTRQ[2:1] are configured as open-drain at the initial state. This setting can be changed.

R272 4.7k 1005
R273 4.7k 1005

RESET#   H8   L_INTRQ1
INTRQ1   F3   L_INTRQ1
INTRQ2   E3   L_INTRQ2

PRESETOUTn <3,10,16,20,21,23>
R635 0 1005 GP6_30/INTRQ1 <4>
R636 0 1005 GP6_31/INTRQ2 <4>

SCLK
SDATA
ALSB

I2C4_SCL <3,10,11,23,26>
I2C4_SDA <3,10,11,23,26>

I2C bus slave address:
ALSB=0: 0xE0 for write, 0xE1 for read.
ALSB=1: 0xE2 for write, 0xE3 for read.

I2S_MCLK
I2S_SCLK
I2S_LRCLK
I2S_SDATA

R637 0 1005 AUDIO_CLKC <2>
R638 0 1005 SSI_SCK4 <2,23>
R639 0 1005 SSI_WS4 <2,23>
R640 0 1005 SSI_SDATA4 <2,23>

[Design Note]
Remove four resistors above in case of using other pin function.
ADV7482W supports 8-channel TDM output mode.

LLC
P0
P1
P2
P3
P4
P5
P6
P7

VREFN   F8
VREFP   G8

C753 0.1uF 1005 10V

DVDDIO_D3.3V

GND (A1, A3, A10, B10)
GND (D5, D6, D7)
GND (E4, E5, E6)
GND (F4, F5, F6, F7)
GND (G5, G6, G7)
GND (H10)
GND (K1, K10)

DNC (A9, ...)

TEST3   D3
TEST2   C5
TEST   G3

R285 4.7k 1005
R288 100k 1005

HDMI_A_5V

R823 47k* 1005
R824 47k 1005
Do not stuff

DDCA_SCL
DDCA_SDA

DVDDIO_D3.3V
R264 27k
D40 RB520SM-30FH

Note: RB520SM-30FH
VF(max)=0.51V@IF=100mA

CEC_A   R633 0 1005   HDMI_CEC

Note:
CEC(Consumer Electric Control Channel)

HPA_A
HDMI_A_5V
R634 0 1005
R271 100k 1005
TR3 RE1C001UNTCL

changed from D5.0V

DVDDIO_D3.3V
TR4 RE1C001UNTCL

Note:
Shorts HPA_A to GND when board powered down.

DVDDIO_D3.3V
changed from D5.0V
R274 1k 1005

LED11 SML-P11MT Yellowish-Green

HPA_A   TR5 RE1C001UNTCL

Note:
HPD A LED

HDMI_A_5V
C388 0.1uF 1005 10V

MIPI CSI-2_VIN

19

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Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)

Size: A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev: 3.02

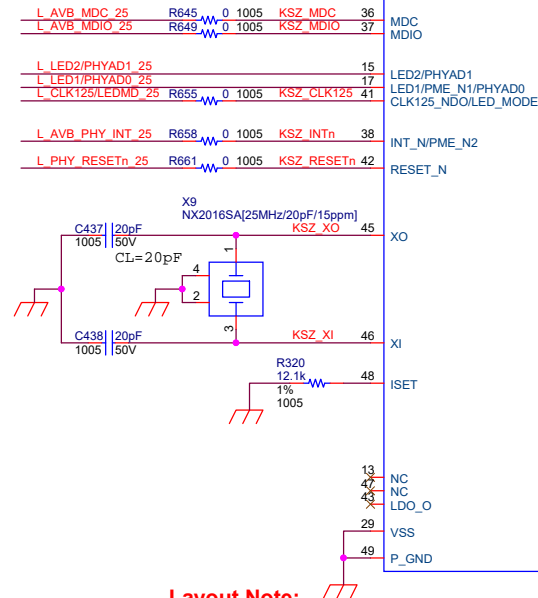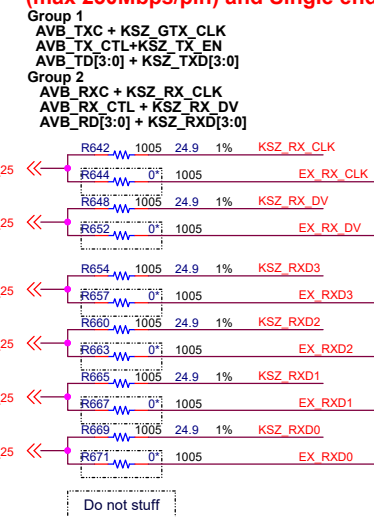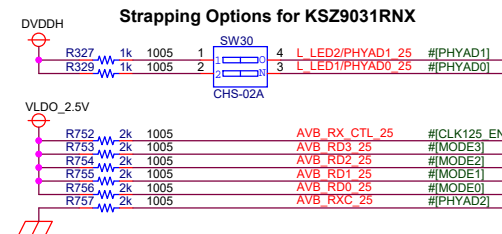Date: Tuesday, December 25, 2018   Sheet 19 of 26

Preliminary

Ethernet AVB GbPHY and PHY Connector

Layout Note:
As short as possible from junction of AVB_xxx to two Rxxx.

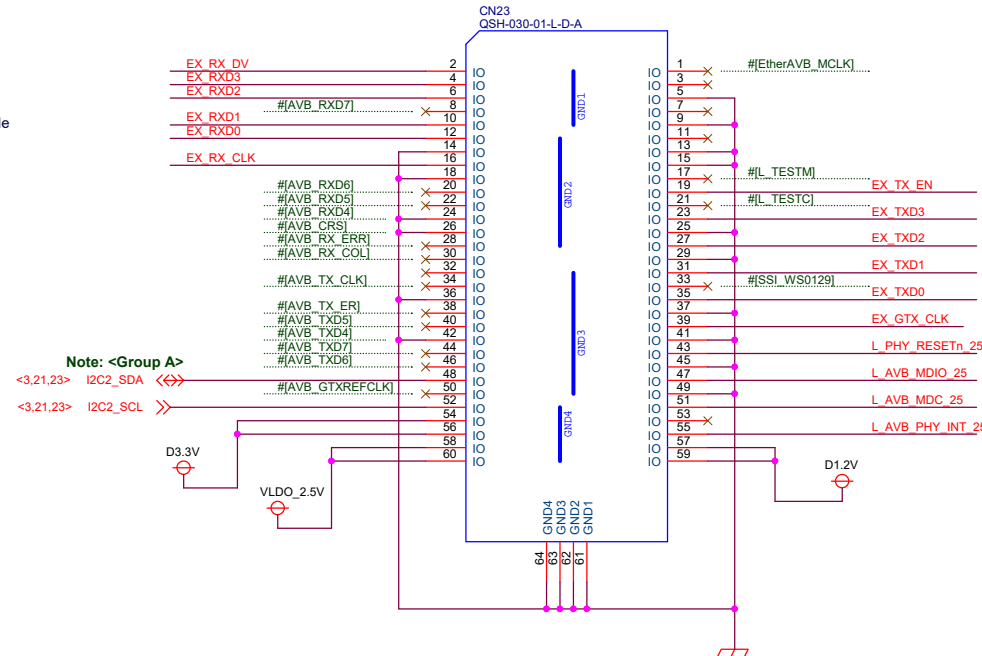[R-CarH3-SiP side] Rxxx KSZ_xxx [KSZ9031 side]
AVB_xxx
Rxxx EX_xxx [connector side]

Layout Note:
Matched Trace Length from R-CarH3-Sip to KSZ9031.
(max 250Mbps/pin) and Single ended impedance 50ohm.
Group 1
 AVB_TXC + KSZ_GTX_CLK
 AVB_TX_CTL+KSZ_TX_EN
 AVB_TD[3:0] + KSZ_TXD[3:0]
Group 2
 AVB_RXC + KSZ_RX_CLK
 AVB_RX_CTL + KSZ_RX_DV
 AVB_RD[3:0] + KSZ_RXD[3:0]

| Gigabit Ethernet Transceiver with RGMII Support | |
U78 KSZ9031RNXVB

Differential Impedance 100ohm

RJ45 with integrated magnetics
CN22 0826-1G1T-23-F

<2> AVB_TXC_25 R641 0 1005 KSZ_GTX_CLK
R643 0* 1005 EX_GTX_CLK
<2> AVB_TX_CTL_25 R647 0* 1005 KSZ_TX_EN
R651 0* 1005 EX_TX_EN
<2> AVB_TD3_25 R653 0 1005 KSZ_TXD3
R656 0* 1005 EX_TXD3
<2> AVB_TD2_25 R659 0 1005 KSZ_TXD2
R662 0* 1005 EX_TXD2
<2> AVB_TD1_25 R664 0 1005 KSZ_TXD1
R666 0* 1005 EX_TXD1
<2> AVB_TD0_25 R668 0 1005 KSZ_TXD0
R670 0* 1005 EX_TXD0

<2> AVB_RXC_25 R642 1005 24.9 1% KSZ_RX_CLK
R644 0* 1005 EX_RX_CLK
<2> AVB_RX_CTL_25 R648 1005 24.9 1% KSZ_RX_DV
R652 0* 1005 EX_RX_DV
<2> AVB_RD3_25 R654 1005 24.9 1% KSZ_RXD3
R657 0* 1005 EX_RXD3
<2> AVB_RD2_25 R660 1005 24.9 1% KSZ_RXD2
R663 0* 1005 EX_RXD2
<2> AVB_RD1_25 R665 1005 24.9 1% KSZ_RXD1
R667 0* 1005 EX_RXD1
<2> AVB_RD0_25 R669 1005 24.9 1% KSZ_RXD0
R671 0* 1005 EX_RXD0

Do not stuff

L_AVB_MDC_25 R645 1005 0 1005 KSZ_MDC 36 MDC
L_AVB_MDIO_25 R649 1005 0 1005 KSZ_MDIO 37 MDIO

L_LED2/PHYAD1_25 15
L_LED1/PHYAD0_25 17
L_CLK125/LEDMD_25 R655 1005 0 1005 KSZ_CLK125 41

L_AVB_PHY_INT_25 R658 0 1005 KSZ_INTn 38 INT_N/PME_N2
L_PHY_RESETn_25 R661 0 1005 KSZ_RESETn 42 RESET_N

24 GTX_CLK
25 TX_EN
22 TXD3
21 TXD2
20 TXD1
19 TXD0
35 RX_CLK/PHYAD2
33 RX_DV/CLK125_EN
27 RXD3/MODE3
28 RXD2/MODE2
31 RXD1/MODE1
32 RXD0/MODE0

LED2/PHYAD1
LED1/PME_N1/PHYAD0
CLK125_NDO/LED_MODE

TXRXP_A TXRXP_A TRD1P
TXRXM_A TXRXM_A TRD1M
TXRXP_B TXRXP_B TRD2P
TXRXM_B TXRXM_B TRD2M
TXRXP_C TXRXP_C TRD3P
TXRXM_C TXRXM_C TRD3M
TXRXP_D TXRXP_D TRD4P
TXRXM_D TXRXM_D TRD4M

AVDDL_PLL 44 AVDDL_PLL
AVDDH 12 AVDDH AVDDH
AVDDL 4 AVDDL AVDDL

TP7 HK-2-G

X9 NX2016SA[25MHz/20pF/15ppm]
KSZ_XO 45 XO
C437 20pF 1005 50V
CL=20pF
C438 20pF 1005 50V
KSZ_XI 46 XI
R320 12.1k 1% 1005 48 ISET

13 NC
47 NC
LDO_O
29 VSS
49 P_GND

11 TRD1P 14 R299 130 1005 D3.3V
10 TRD1M LED1A 13 L_LED1
5 TRD2P LED1K #[Activity(TX,RX)]
4 TRD2M LED2A
3 TRD3P 16 R305 130 1005 D3.3V
2 TRD3M LED2K 15 L_LED2
8 TRD4P #[Link On]
9 TRD4M

12 TRCT1 C824 0.1uF 1005 50V
6 TRCT2 C825 0.1uF 1005 50V
1 TRCT3 C826 0.1uF 1005 50V
7 TRCT4 C827 0.1uF 1005 50V
17 SHIELD0 R646 0 1005
18 SHIELD1 R650 0 1005

C754 0.01uF 1005 25V
C755 0.01uF 1005 25V C756 0.01uF 1005 25V
C757 0.01uF 1005 25V C758 0.01uF 1005 25V

16 DVDDH
34 DVDDH
40 DVDDH
R672 0 VLDO_2.5V
C759 0.1uF 1005 25V C760 0.01uF 1005 25V C761 0.01uF 1005 25V C762 0.1uF 1005 10V C442 10uF 2012 16V

14 DVDDL
18 DVDDL
23 DVDDL
26 DVDDL
30 DVDDL
39 DVDDL
R675 0 D1.2V
C764 0.1uF 1005 25V C765 0.01uF 1005 25V C766 0.01uF 1005 25V C767 0.01uF 1005 25V C768 0.01uF 1005 25V C769 0.1uF 1005 25V C770 0.1uF 1005 10V C451 10uF 2012 16V

Layout Note:
The KSZ9031RNX has Paddle Ground (pin49) at bottom side.
Connect that PAD(pin 49) to the GND.

Strapping Options for KSZ9031RNX
DVDDH
R327 1k 1005 L_LED2/PHYAD1_25 #[PHYAD1]
R329 1k 1005 L_LED1/PHYAD0_25 #[PHYAD0]
SW30 CHS-02A

VLDO_2.5V
R752 2k 1005 AVB_RX_CTL_25 #[CLK125_EN]
R753 2k 1005 AVB_RD3_25 #[MODE3]
R754 2k 1005 AVB_RD2_25 #[MODE2]
R755 2k 1005 AVB_RD1_25 #[MODE1]
R756 2k 1005 AVB_RD0_25 #[MODE0]
R757 2k 1005 AVB_RXC_25 #[PHYAD2]

Layout Note:
Following signals need Ground guard.
AVB_TXCREFCLK, CLK125/LEDMD_25 (125MHz)
AVB_TXC_25, KSZ_GTX_CLK, EX_GTX_CLK (125MHz)
AVB_RXC_25, KSZ_RX_CLK, EX_RX_CLK (125MHz)

Following pin has pull-down resistor at the initial state.
[2.5V-I/O]
AVB_RX_CTL, AVB_RXC, AVB_RD[3:0]
AVB_TX_CTL, AVB_TXC, AVB_TD[3:0]
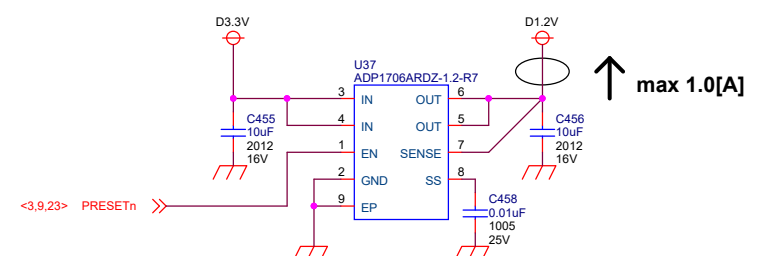[3.3V-I/O]
AVB_TXCREFCLK, AVB_MAGIC, AVB_PHY_INT, AVB_LINK
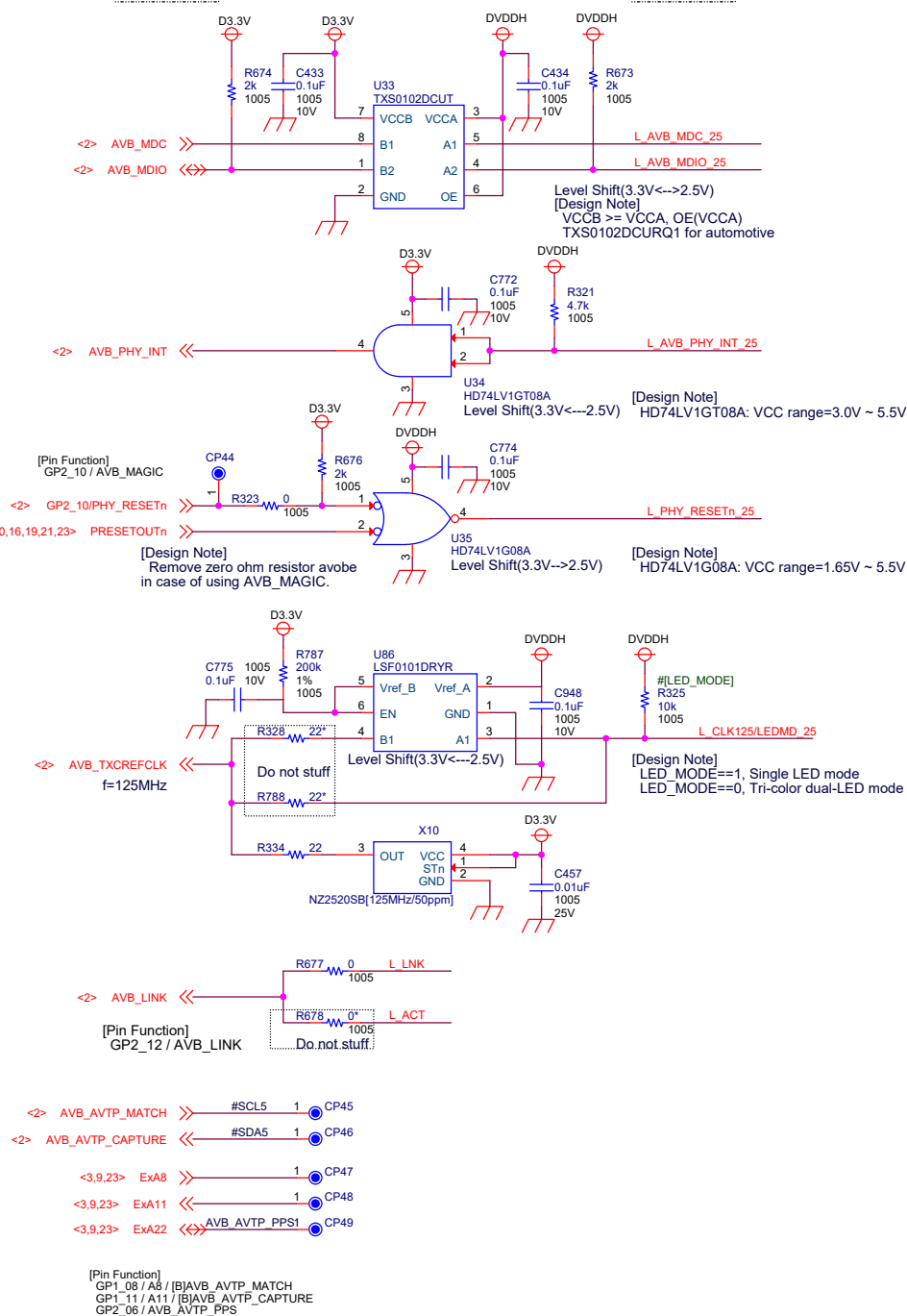
Controls LEDs in the RJ45 connector
D3.3V #[Link On] D3.3V #[Activity(TX,RX)]
R313 10k 1005 L_LED2 R314 10k 1005 L_LED1
L_LNK TR6 RE1C001UNTCL L_ACT TR7 RE1C001UNTCL
TR8 RE1C001UNTCL TR9 RE1C001UNTCL
L_LED2/PHYAD1_25 L_LED1/PHYAD0_25
R318 10k 1005 R319 10k 1005

LC filters for KSZ9031RNX
L96 BLM18AG102SH1D Rated current=400mA
D1.2V AVDDL_PLL VLDO_2.5V
C444 10uF 2012 16V C763 0.1uF 1005 10V C950 1000pF 1005 50V C951 0.1uF 1005 10V
L97 BLM18AG102SH1D Rated current=400mA
D3.3V AVDDH
C453 10uF 2012 16V C771 0.1uF 1005 10V
L98 BLM18AG102SH1D Rated current=400mA
D1.2V AVDDL
C454 10uF 2012 16V C773 0.1uF 1005 10V

Local Regulator for KSZ9031RNX, PHY Connector
D3.3V D1.2V
U37 ADP1706ARDZ-1.2-R7
3 IN OUT 6
2 IN OUT 5
1 EN SENSE 7
4 GND SS 8
EP
C455 10uF 2012 16V C456 10uF 2012 16V
<3,9,23> PRESETn C458 0.01uF 1005 25V

max 1.0[A]

Layout Note:
The ADP1706 has EXPOSED PAD(pin9) at bottom side.
Connect that EXPOSED PAD(pin 9) to the GND.

D3.3V C433 0.1uF 1005 10V
R674 2k 1005
U33 TXS0102DCUT
7 VCCB VCCA 3
8 B1 A1 5
1 B2 A2 4
2 GND OE 6
DVDDH R673 2k 1005 C434 0.1uF 1005 10V
L_AVB_MDC_25
L_AVB_MDIO_25
<2> AVB_MDC
<2> AVB_MDIO
Level Shift(3.3V<-->2.5V)
[Design Note] VCCB >= VCCA, OE(VCCA) TXS0102DCURQ1 for automotive

D3.3V C772 0.1uF 1005 10V R321 4.7k 1005
U34 HD74LV1GT08A Level Shift(3.3V<-->2.5V)
<2> AVB_PHY_INT L_AVB_PHY_INT_25
[Design Note] HD74LV1GT08A: VCC range=3.0V ~ 5.5V

[Pin Function] GP2_10 / AVB_MAGIC
CP44 D3.3V R676 2k 1005 DVDDH C774 0.1uF 1005 10V
<2> GP2_10/PHY_RESETn R323 1005
<3,10,16,19,21,23> PRESETOUTn
U35 HD74LV1G08A Level Shift(3.3V-->2.5V)
L_PHY_RESETn_25
[Design Note] Remove zero ohm resistor avobe in case of using AVB_MAGIC.
[Design Note] HD74LV1G08A: VCC range=1.65V ~ 5.5V

D3.3V R787 200k 1% 1005
C775 0.1uF 10V
U86 LSF0101DRYR
4 Vref_B Vref_A 5
6 EN GND 1
2 B1 A1 3
R328 22* DVDDH DVDDH C948 0.1uF 1005 10V R325 10k 1005 #[LED_MODE]
L_CLK125/LEDMD_25
Do not stuff R788 22*
Level Shift(3.3V<-->2.5V)
<2> AVB_TXCREFCLK f=125MHz
[Design Note] LED_MODE==1, Single LED mode LED_MODE==0, Tri-color dual-LED mode

R334 22 X10 NZ2520SB[125MHz/50ppm]
3 OUT VCC 4 D3.3V
STn 2
1 GND
C457 0.01uF 1005 25V

R677 1005 L_LNK
<2> AVB_LINK R678 0* L_ACT
[Pin Function] GP2_12 / AVB_LINK Do.not.stuff.

<2> AVB_AVTP_MATCH #SCL5 1 CP45
<2> AVB_AVTP_CAPTURE #SDA5 1 CP46
<3,9,23> ExA8 1 CP47
<3,9,23> ExA11 1 CP48
<3,9,23> ExA22 AVB_AVTP_PPS1 1 CP49
[Pin Function]
GP1_08 / A8 / [B]AVB_AVTP_MATCH
GP1_11 / A11 / [B]AVB_AVTP_CAPTURE
GP2_06 / AVB_AVTP_PPS

Ethernet AVB PHY Connector
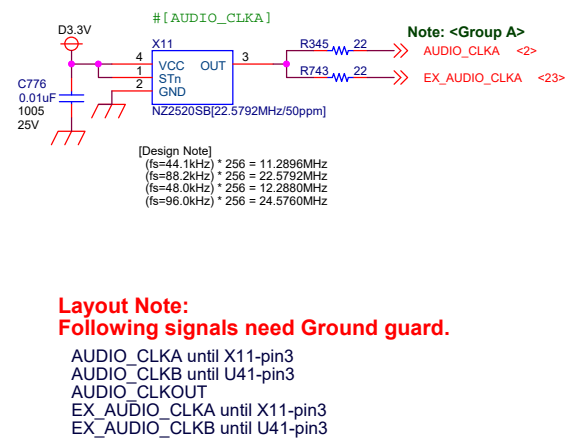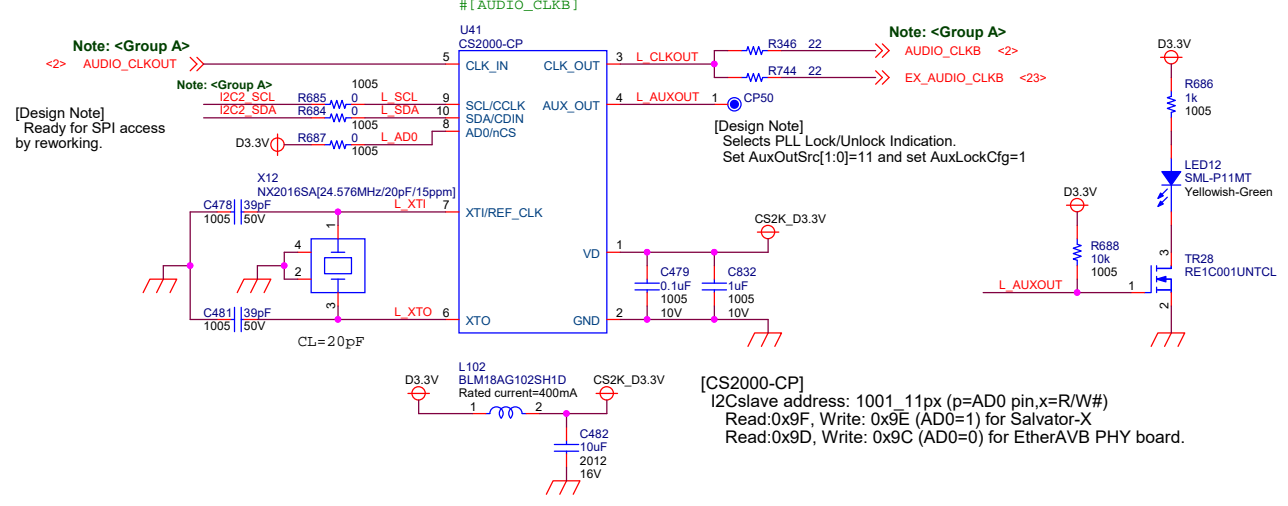CN23 QSH-030-01-L-D-A

EX_RX_DV 2 IO IO 1 #[EtherAVB_MCLK]
EX_RXD3 4 IO IO 3
EX_RXD2 6 IO IO 5
#[AVB_RXD7] 8 IO IO 7
EX_RXD1 10 IO IO 9
EX_RXD0 12 IO IO 11
14 IO IO 13
EX_RX_CLK 16 IO IO 15
18 IO IO 17 #[L_TESTM]
#[AVB_RXD6] 20 IO IO 19 #[L_TESTC] EX_TX_EN
#[AVB_RXD5] 22 IO IO 21 EX_TXD3
#[AVB_RXD4] 24 IO IO 23 EX_TXD2
#[AVB_CRS] 26 IO IO 25 EX_TXD1
#[AVB_RX_ERR] 28 IO IO 27 EX_TXD0
#[AVB_RX_COL] 30 IO IO 29
#[AVB_TX_CLK] 32 IO IO 31 #[SSI_WS0129]
34 IO IO 33
#[AVB_TX_ER] 36 IO IO 35
#[AVB_TXD5] 38 IO IO 37
#[AVB_TXD4] 40 IO IO 39 EX_GTX_CLK
#[AVB_TXD3] 42 IO IO 41 L_PHY_RESETn_25
#[AVB_TXD6] 44 IO IO 43 L_AVB_MDIO_25
46 IO IO 45 L_AVB_MDC_25
Note: <Group A> 48 IO IO 47
<3,21,23> I2C2_SDA #[AVB_GTXREFCLK] 50 IO IO 49 L_AVB_PHY_INT_25
<3,21,23> I2C2_SCL 52 IO IO 51
54 IO IO 53
D3.3V 56 IO IO 55
58 IO IO 57
60 IO IO 59 D1.2V
VLDO_2.5V
GND4 GND3 GND2 GND1
64 63 62 61

EtherAVB(GbPHY,PHY_CN) 20

Preliminary

AUDIO (SSI0/1) I/F

LINE OUT

Layout Note:
Following signals need Ground guard.
AUDIO_CLKOUT3
L_OUT_R, AKM_OUT_R until CN39
L_OUT_L, AKM_OUT_L until CN39
L_RIN1, AKM_IN_R until CN40
L_LIN1, AKM_IN_L until CN40

Note: <Group A>
<2,23> AUDIO_CLKOUT3

U38
AK4613VQ

[Design Note]
Master/Slave# mode selection.
M/S=0: AK4613 becomes Slave mode.
M/S=1: AK4613 becomes Master mode.

R337 10k 1005
R680 0 1005

_AUDIO_GND

<2,23> SSI_SCK0129
<2,23> SSI_WS0129
L_M/Sn

[Design Note]
DAC output selection when power down.
High=DAC outputs are Hi-Z.
Low =DAC outputs are VCOM voltage.

R341 10k 1005
R682 0 1005

Do not stuff.

<2,23> SSI_SDATA0

TP8 HK-2-G

L_DVMPD

<3,10,16,19,20,23> PRESETOUTn

<2,23> SSI_SDATA1
R683 0 1005

Note: <Group A>
<3,20,23> I2C2_SCL
<3,20,23> I2C2_SDA

I2Cslave address: 0010_000x (CAD[1:0]=0)
Read:0x21, Write: 0x20

Microphone Amplifier
(20dB fixed gain)

U82 MAX9813LEKA+T
R340 2k 1005
C828 0.1uF 1005 10V
C829 0.1uF 1005 10V
C461 0.1uF 1005 10V
AKM_IN_R

MIC Input

U83 MAX9813LEKA+T
R343 2k 1005
C830 0.1uF 1005 10V
C831 0.1uF 1005 10V
C464 0.1uF 1005 10V
AKM_IN_L

CN40 SJ-3523-SMT

[Design Note]
By all means use any cables incorporating resistor,
in case of connecting as Line Input.

Layout Note:
One Point Ground

_AUDIO_GND

C465 10uF 2012 16V
C466 0.1uF 1005 10V
C469 10uF 2012 16V
C470 0.1uF 1005 10V
C473 10uF 2012 16V
C474 0.1uF 1005 10V

C467 0.1uF 1005 10V
C468 10uF 2012 16V
L99 BLM18AG102SH1D Rated current=400mA
C471 0.1uF 1005 10V
C472 10uF 2012 16V
L100 BLM18AG102SH1D Rated current=400mA
C475 0.1uF 1005 10V
C476 2.2uF 1608 10V

CN39 SJ-3523-SMT

E17 22uF 6.3V
R679 10k 1005
E18 22uF 6.3V
R681 10k 1005

Audio Clock for 44.1kHz, 88.2kHz

#[AUDIO_CLKA]
X11
C776 0.01uF 1005 25V
NZ2520SB[22.5792MHz/50ppm]
R345 22
R743 22

Note: <Group A>
AUDIO_CLKA <2>
EX_AUDIO_CLKA <23>

[Design Note]
(fs=44.1kHz) * 256 = 11.2896MHz
(fs=88.2kHz) * 256 = 22.5792MHz
(fs=48.0kHz) * 256 = 12.2880MHz
(fs=96.0kHz) * 256 = 24.5760MHz

Layout Note:
Following signals need Ground guard.
AUDIO_CLKA until X11-pin3
AUDIO_CLKB until U41-pin3
AUDIO_CLKOUT
EX_AUDIO_CLKA until X11-pin3
EX_AUDIO_CLKB until U41-pin3

Audio Clock for 48kHz, 96kHz, and for EtherAVB

#[AUDIO_CLKB]
U41 CS2000-CP

<2> AUDIO_CLKOUT

Note: <Group A>
I2C2_SCL R685 0 L_SCL 1005
I2C2_SDA R684 0 L_SDA 1005
R687 0 L_AD0 1005

[Design Note]
Ready for SPI access
by reworking.

X12 NX2016SA[24.576MHz/20pF/15ppm]
C478 39pF 1005 50V
C481 39pF 1005 50V
CL=20pF

R346 22
R744 22

Note: <Group A>
AUDIO_CLKB <2>
EX_AUDIO_CLKB <23>

CP50

[Design Note]
Selects PLL Lock/Unlock Indication.
Set AuxOutSrc[1:0]=11 and set AuxLockCfg=1

CS2K_D3.3V
C479 0.1uF 1005 10V
C832 1uF 1005 10V

L102 BLM18AG102SH1D Rated current=400mA
CS2K_D3.3V
C482 10uF 2012 16V

[CS2000-CP]
I2Cslave address: 1001_11px (p=AD0 pin,x=R/W#)
Read:0x9F, Write: 0x9E (AD0=1) for Salvator-X
Read:0x9D, Write: 0x9C (AD0=0) for EtherAVB PHY board.

R686 1k 1005
LED12 SML-P11MT Yellowish-Green
R688 10k 1005
TR28 RE1C001UNTCL
L_AUXOUT

TOP VIEW
Board Edge
Board
Left MIC
Right AOUT
Over 12mm

AUDIO(AK4613VQ)   21

Title: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Size A2
Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)
Rev 3.02
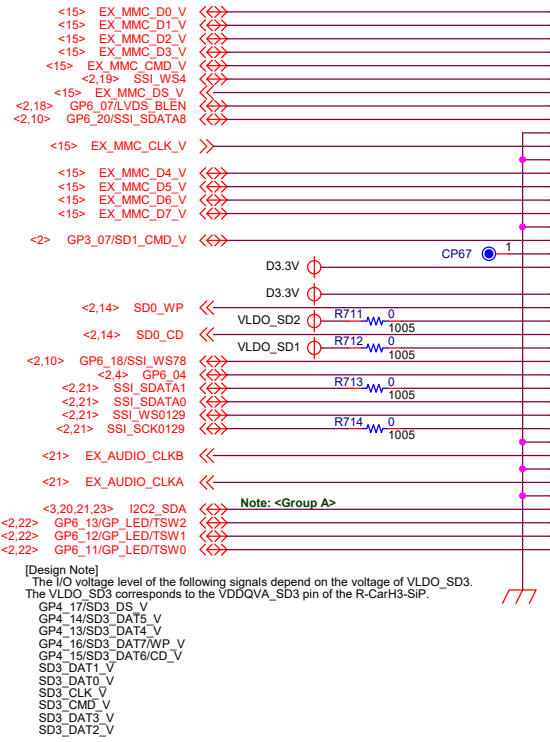Date: Tuesday, December 25, 2018   Sheet 21 of 26

Preliminary

Debug Serial-0
(SCIF2_A, group A)

D3.3V

R350
10k
1005

Serial-USB Bridge
(USB Bus-Powered)
U42

Note: <Group A>
<2> SCIF2_TXD

Note: <Group A>
<2> SCIF2_RXD

D3.3V
C483 1005
0.1uF 10V

U43
HD74LV1GT08A

RXD   REGIN
TXD   VBUS
CTS   DM
RTS   DP
DSR
DTR   NC1
       NC2
SUSPEND NC3
SUSPEND# NC4
       NC5
DCD   NC6
RI   NC7
       NC8
       NC9
RST   NC10
       NC11
R351
4.7k
1005
GND   VDD
ExPAD
CP2102

CP2102_D3.3V_0

C485
0.1uF
1005
10V

USB microAB(Func)
CN25
D-
D+
ID
VBUS
GND
SHELL0
SHELL1
SHELL2
SHELL3
ZX62D-AB-5P8

C833
1uF
1005
10V

DEBUG SERIAL-0

[Design Note]
Following pins can be left unconnected when not used.
(1) CTS, RTS, DSR, DTR, DCR, RI, SUPEND, SUPEND#

[Design Note]
The RST pin has two functions.
(1) Open-drain output of internal POR.
(2) Vdd monitor.

[Design Note]
The VDD pin outputs internal
3.3V voltage regulator.

Debug Serial-1
(SCIF1/HSCIF1_A, group A)

D3.3V

R352
10k
1005

Serial-USB Bridge
(USB Bus-Powered)
U44

Note: <Group A>
<2,23> GP5_06/TX1/HTX1

R689 0 1005 L_TX1/HTX1

[Design Note]
Remove a resistor above
in case of using as GPIO.

Note: <Group A>
<2,23> GP5_05/RX1/HRX1

R690 0 1005 L_RX1/HRX1

D3.3V
C486 1005
0.1uF 10V

[Design Note]
Remove a resistor above
in case of using as GPIO.

<2,23> GP5_08/RTS1n/HRTS1n

R691 0 1005 L_RTS1n/HRTS1n

[Design Note]
Remove a resistor above
in case of using as GPIO.

U45
HD74LV1GT08A

RXD   REGIN
TXD   VBUS
CTS   DM
RTS   DP
DSR
DTR   NC1
       NC2
SUSPEND NC3
SUSPEND# NC4
       NC5
DCD   NC6
RI   NC7
       NC8
       NC9
RST   NC10
       NC11
R355
4.7k
1005
GND   VDD
ExPAD
CP2102

CP2102_D3.3V_1

C488
0.1uF
1005
10V

D3.3V
C489 1005
0.1uF 10V

<2,23> GP5_07/CTS1n/HCTS1n

R692 0 1005 L_CTS1n/HCTS1n

[Design Note]
Remove a resistor above
in case of using as GPIO.

U46
HD74LV1GT08A

USB microAB(Func)
CN26
D-
D+
ID
VBUS
GND
SHELL0
SHELL1
SHELL2
SHELL3
ZX62D-AB-5P8

C834
1uF
1005
10V

DEBUG SERIAL-1

[Design Note]
Following pins can be left unconnected when not used.
(1) CTS, RTS, DSR, DTR, DCR, RI, SUPEND, SUPEND#

[Design Note]
The RST pin has two functions.
(1) Open-drain output of internal POR.
(2) Vdd monitor.

[Design Note]
The VDD pin outputs internal
3.3V voltage regulator.

GPLED / Tact Switch

General Purpose LEDs or Tactile Switches
Following LEDs and Switches are connected to GPIO of R-CarH3-SiP

D3.3V
R358
1k
1005

SW20 B3U-1100PM
R364
1005
2k

C490
0.1uF
1005
10V

D37
DZ2S033M0L

D3.3V
R359
1k
1005

LED4
SML-P11MT
Yellowish-Green

TR10
RE1C001UNTCL

<2,23> GP6_11/GP_LED/TSW0
R695 0 1005 L_LED/TSW0

D3.3V
R360
1k
1005

SW21 B3U-1100PM
R365
1005
2k

C491
0.1uF
1005
10V

D38
DZ2S033M0L

D3.3V
R361
1k
1005

LED5
SML-P11MT
Yellowish-Green

TR11
RE1C001UNTCL

<2,23> GP6_12/GP_LED/TSW1
R694 0 1005 L_LED/TSW1

D3.3V
R362
1k
1005

SW22 B3U-1100PM
R366
1005
2k

C492
0.1uF
1005
10V

D39
DZ2S033M0L

D3.3V
R363
1k
1005

LED6
SML-P11MT
Yellowish-Green

TR12
RE1C001UNTCL

<2,23> GP6_13/GP_LED/TSW2
R693 0 1005 L_LED/TSW2

GP6_11/GP_LED/TSW0 1 CP51
GP6_12/GP_LED/TSW1 1 CP52
GP6_13/GP_LED/TSW2 1 CP53
1 CP54

DEBUG_SCIF/LED/TactSW   **22**

Preliminary

EXIO Connector A: BT/WLAN connector.
EXIO Connector B: SSI connector.
EXIO Connector C: MIPI CSI-2 connector.
EXIO Connector D: LBSC connector (Not for NOR Flash board)

Layout Note:
Following signals need Ground guard.
GP3_06/SD1_CLK_V, SD3_CLK_V, EX_MMC_CLK_V,
AUDIO_CLKOUT3,
EX_AUDIO_CLKA, EX_AUDIO_CLKB

Layout Note:
Following signals need Ground guard.
CLKOUT, EX_WAIT0n/DU_DCLK0(VI4_CLK), CS1n(VI5_CLK)
WE0n(CAN_CLK)

#[EXIO_B]
EXIO Connector B (SSI)
(Bottom Layer, Lower Right side of R-CarH3-SiP)

#[EXIO_D]
EXIO Connector D (LBSC)
(Bottom Layer, Upper Right side of R-CarH3-SiP)

#[EXIO_C]
EXIO Connector C (MIPI CSI-2)
(Bottom Layer, Upper Left side of R-CarH3-SiP)

Layout Note:
Following signals need Ground guard.
GP6_30, GP6_31

Differential Impedance
100ohm +-10%

Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI0_xxxx + CSI0_xxxx

Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI1_xxxx + CSI1_xxxx

Layout Note:
The PI3PCIE3212ZBE has Center Ground (pin21) at bottom side.
Connect that PAD(pin 21) to the GND.

Layout Note:
The PI3PCIE3212ZBE has Center Ground (pin21) at bottom side.
Connect that PAD(pin 21) to the GND.

[Design Note]
The PI3PCIE3212ZBE is not an automotive product.

[Design Note]
SW=ON: Selects channel-B(ADV7482W) side.
SW=OFF: Selects channel-C(EXIO CN) side.

Layout Note:
Place TestIC at bottom layer

Do not stuff

EXIO_CN/MIPI_SW   **23**

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Title	R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)	
Size A2	Document Number R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS)	Rev 3.02
Date: Tuesday, December 25, 2018	Sheet 23 of 26	

CONFIDENTIAL

Preliminary

It is impossible to supply DC5.0V and DC3.3V through CN30 and CN36.

It is prohibited to supply more than DC12.0V .

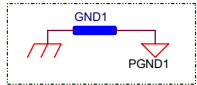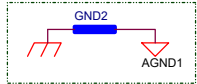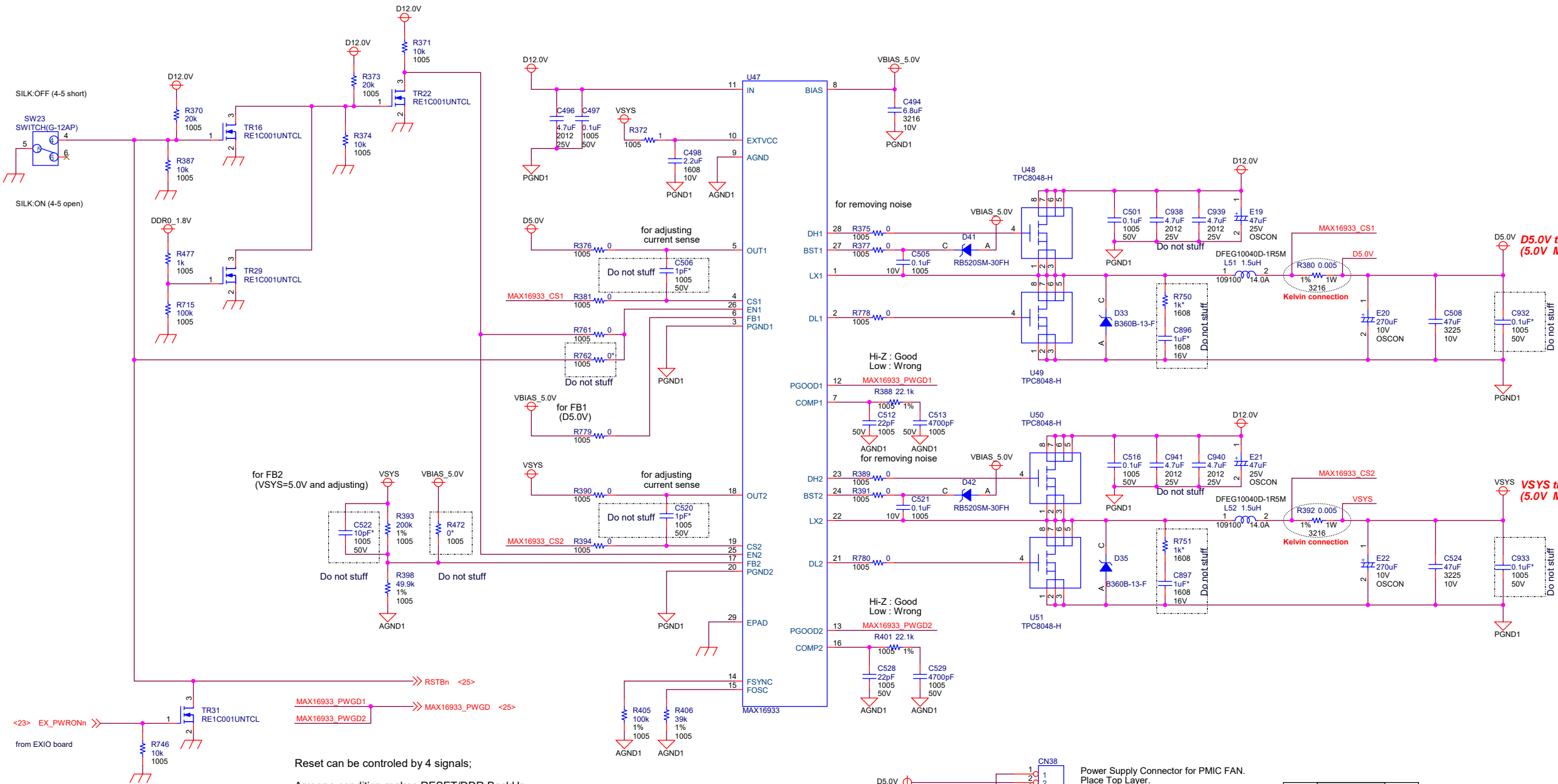LED8,LED9 and LED14 are Yellowish Green LEDs indicate Power Good.
LED8 turns on after detecting DC12.0V.
LED9 turns on after detecting D5.0V and VSYS.
LED14 turns on during DDR Back Up.

One Point Ground is more than "0.6mm VIA x 2"
Connect each other under the Exposed Pad by Layout tool.

GND1 — PGND1

One Point Ground is more than "0.6mm VIA x 2"
Connect each other under the Exposed Pad by Layout tool.

GND2 — AGND1

Legacy connector — CN30, 53259-0429, GND/GND/12V/12V

D43 TCH20A15 — Rated Current=10Ax2

Rated Current=5.5A/pin[AWG.#18]

AC Adapter — CN36, PJ-063AH

L103 BLM18KG260TZ1 Rated Current=6.0A 1608
L105 BLM18KG260TZ1 Rated current=6.0A 1608
L107 BLM18KG260TZ1 Rated current=6.0A 1608

L104 NFM31HK223R1H3 Rated Current=10A 3216
L106 NFM31HK223R1H3 Rated Current=10A 3216

max 18.0[A]

D12.0V

E12 470uF 25V
C493 0.1uF 50V 1005

VR = 1.9V
Vce = 0.3V
Ir = (12V-1.9V-0.3V)/6.8k = 1.44mA
Wr = (12V-1.9V-0.3V) * 1.44mA = 14.12mW
1005size: 63mW (max)

R758 6.8k 1005 1%   R759 6.8k 1005 1%   R760 6.8k 1005 1%

LED8 SML-P11MT Yellowish-Green — **12V LED**
LED9 SML-P11MT Yellowish-Green — **5V LED**
LED14 SML-P11MT Yellowish-Green — **Back up LED**

VBIAS_5.0V

TR13 RE1C001UNTCL   TR30 RE1C001UNTCL

R508 47k 1005

MAX16933_PWGD1 Power GOOD(D5.0V/VSYS)

<7,25> BKUP_CTRL_11

SILK:OFF (4-5 short)
SW23 SWITCH(G-12AP)
SILK:ON (4-5 open)

D12.0V R370 20k 1005   R387 10k 1005
TR16 RE1C001UNTCL

D12.0V R373 20k 1005   R374 10k 1005
TR22 RE1C001UNTCL

D12.0V R371 10k 1005

DDR0_1.8V R477 1k 1005   R715 100k 1005
TR29 RE1C001UNTCL

D12.0V C496 4.7uF 2012 25V C497 0.1uF 1005 50V
R372 1005
C498 2.2uF 1608 10V

D5.0V R376 1005 0
for adjusting current sense
C506 1pF* 1005 50V Do not stuff

MAX16933_CS1 R381 1005
R761 1005 0
R762 1005 0* Do not stuff

VBIAS_5.0V for FB1 (D5.0V)
R779 1005

for FB2 (VSYS=5.0V and adjusting)
VSYS VBIAS_5.0V
C522 10pF* 1005 50V   R393 200k 1% 1005   R472 0* 1005
R398 49.9k 1% 1005
Do not stuff   Do not stuff

VSYS R390 1005
for adjusting current sense
C520 1pF* 1005 50V Do not stuff

MAX16933_CS2 R394 1005

U47 MAX16933
11 IN
8 BIAS
10 EXTVCC
9 AGND
5 OUT1
4 CS1
26 EN1
6 FB1
3 PGND1
7 COMP1
12 PGOOD1
18 OUT2
19 CS2
25 EN2
17 FB2
20 PGND2
13 PGOOD2
16 COMP2
14 FSYNC
15 FOSC
29 EPAD

VBIAS_5.0V C494 6.8uF 3216 10V

for removing noise
DH1 28 R375 1005 0
BST1 27 R377 1005 0
C505 0.1uF 1005 10V
D41 RB520SM-30FH
LX1 1
DL1 R778 1005
VBIAS_5.0V

U48 TPC8048-H
C501 0.1uF 1005 50V C938 4.7uF 2012 25V C939 4.7uF 2012 25V E19 47uF 25V OSCON
Do not stuff
MAX16933_CS1

R750 1k* 1608   C896 1uF* 1608 16V
Do not stuff
D33 B360B-13-F

U49 TPC8048-H

Hi-Z : Good
Low : Wrong

DFEG10040D-1R5M L51 1.5uH 109100 14.0A
R380 0.005 1% 1W 3216
Kelvin connection

D5.0V **D5.0V trace width is 10mm (5.0V MAX 10A)**
E20 270uF 10V OSCON   C508 47uF 3225 10V   C932 0.1uF 1005 50V Do not stuff

COMP1 R388 22.1k 1005 1%
C512 22pF 1005 50V C513 4700pF 1005 50V
for removing noise

DH2 23 R388 1005 0
BST2 24 R391 1005 0
C521 0.1uF 1005 10V
D42 RB520SM-30FH
LX2 22
DL2 21 R780 1005

U50 TPC8048-H
VBIAS_5.0V
C516 0.1uF 1005 50V C941 4.7uF 2012 25V C940 4.7uF 2012 25V E21 47uF 25V OSCON
Do not stuff
MAX16933_CS2

R751 1k* 1608   C897 1uF* 1608 16V
Do not stuff
D35 B360B-13-F

U51 TPC8048-H

Hi-Z : Good
Low : Wrong

DFEG10040D-1R5M L52 1.5uH 109100 14.0A
R392 0.005 1% 1W 3216
Kelvin connection

VSYS **VSYS trace width is 10mm (5.0V MAX 10A)**
E22 270uF 10V OSCON   C524 47uF 3225 10V   C933 0.1uF 1005 50V Do not stuff

PGOOD2 13 R401 22.1k 1005 1%
COMP2 16
C528 22pF 1005 50V C529 4700pF 1005 50V

R405 100k 1% 1005   R406 39k 1% 1005

RSTBn <25>
MAX16933_PWGD1   MAX16933_PWGD <25>
MAX16933_PWGD2

<23> EX_PWRONn
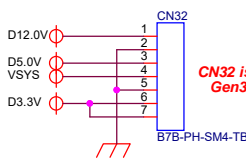TR31 RE1C001UNTCL
R746 10k 1005
from EXIO board

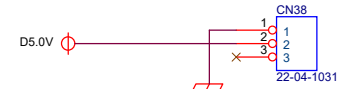Reset can be controled by 4 signals;

Any one condition makes RESET/DDR BackUp
  SW23(ACC Switch):RSTBn= Low
  EXIO(SYSCON)   : EX_PWRONn=High
  PowerGood D5.0V: MAX16933_PWGD1=Low
  PowerGood VSYS: MAX16933_PWGD2 =Low

All conditions make POWER ON
  SW23(ACC Switch):RSTBn= High
  EXIO(SYSCON)   : EX_PWRONn=Low
  PowerGood D5.0V: MAX16933_PWGD1=High
  PowerGood VSYS: MAX16933_PWGD2 =High

Power Supply Connector for I/O board.
CN32 B7B-PH-SM4-TB
D12.0V / D5.0V / VSYS / D3.3V
CN32 is ONLY for Gen3 extension board.

D12.0V trace width is 2mm
D5.0V trace width is 2mm
VSYS trace width is 2mm
D3.3V trace width is 4mm

CN38 22-04-1031 Power Supply Connector for PMIC FAN. Place Top Layer.
D5.0V

CN34 22-04-1031 Power Supply Connector for CPU FAN. Place Top Layer.
D12.0V R411 0 Do not stuff. R412 0*
D5.0V

3pin 2pin 1pin
FAN Connector - Top View

C508/C524 : Automotive type is available soon
Power circuit might be changed depending on evaluation.

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Size A2 Document Number: R-CarH3-SiP/M3-SiP System Evaluation Board (Salvator-XS) Rev 3.02
Date: Tuesday, December 25, 2018   Sheet 24 of 26

Power 5V/VSYS

24

Preliminary

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RSTB
Low : Reset or DDR back-up (need to set)
High : Active (awake reset)

RSTBMODE(Low=Level, Hi=Pulse)

Do not Stuff

thermistor

Reset Switch

RSTB : Internal pull-up(100k V3P3) with schmid.
MRB: Internal pull-up(100k V3P3)
SYNC : Internal pull-down(100k)

OCP = 0.28V

BOOST :Internal pull-down(100k)

BKUP_REQB Internal pull-down(100k)

Do not stuff

I2Cslave address: 0110_000x
Read:0x61, Write: 0x60

BD9571MWF-M

I2C EEPROM for PMIC

U57 BR24T01FVM-W

I2Cslave address: 1010_000x
Read:0xA1, Write: 0xA0

[Design Note]
WP=GND means writeable.
VCC range=1.7V ~ 5.5V

SYSTEM Reset LED

VSYS=5.0V trace width is 10mm
D5.0V trace width is 10mm

One Point Ground (But number of via need to consider).
Connect each other by Layout tool.

2in1 FET

DVFS : DCDC controler

DVFS0.8V trace width is 16mm (TYP 0.82V MAX 16A) (TBD)

for Current-Sense Amplifier (U58)

Kelvin connection

SPM6545VT-R15M-D
L110   0.15uH
7065   22.0A

Do not stuff

C533-C537,C543 and C942-C945 are temporal to BD9571MVW 3rd cut.
From 3rd cut, these would be 47uF(GCM32ER70J476KE19)

PMIC_VSSSENSE

FB_DVFS/REMOTE_M_DVFS Layout Note:
these are led from the neiborhood of SoC ball in pairs.

2in1 FET

VD09: DCDC controler

VDD0.8V trace width is 8mm (TYP 0.82V MAX 8A) (TBD)

for Current-Sense Amplifier (U59)

Kelvin connection

SPM5030VT-R15M-D
L111   0.15uH
5550   14.5A

Do not stuff

FB_VD09 Layout Note: this is led from the neiborhood of SoC ball.

DDR0C-DDR1C: LDO

DDR0: DCDC

TFM201610ALMAR24MTAA
L55 0.24uH

Do not stuff.

DDR0_1.8V/DDR1_1.8V
(1.8V MAX 250mA(peak 600mA))

DDR0_1.1V trace width is 4mm
(1.1V MAX 4A)
DDR0_1.1V (1.028V-1.333V)

FB_DDR0 Layout Note:
The blanch point is led from the neiborhood of DDR.

DDR1: DCDC

TFM201610ALMAR24MTAA
L56 0.24uH

Do not stuff.

DDR1_1.1V trace width is 4mm
(1.1V MAX 4A)
DDR1_1.1V (1.028V-1.333V)

FB_DDR1 Layout Note:
The blanch point is led from the neiborhood of DDR.

VD18: DCDC

TFM201610ALMAR33MTAA
L57 0.33uH

Do not stuff.

D1.8V trace width is 3mm
(1.8V MAX 3A)

VD33: DCDC

TFM201610ALMAR33MTAA
L58 0.33uH

Do not stuff.

D3.3V trace width is 3mm
(3.3V MAX 3A)

VD25: LDO

VLDO2.5V
(2.5V MAX 300mA)

SD0-SD3: LDO

VLDO_SD0/VLDO_SD1/VLDO_SD2/VLDO_SD3
(1.8V/3.3V MAX 170mA)

TOP VIEW of BD9571MWV-M

Exposed PAD

BD9571MWF-M

U67 Layout Note:
BD9571MWV-M has a exposed pad at bottom side.
CONNECT to MASTER GND.

C540/C542 : Automotive type is available soon
Power circuit might be changed depending on evaluation.

Power PMIC

Preliminary

Current-Sense Amplifiers with ADC for DVFS0.8V

DVFS_RSP
Note: PMIC side DVFS_RSP
U58 MAX9611AUB+
JP3 HWP-2-G
Note: SoC side DVFS0.8V
DVFS0.8V

RS+ SCL 6 → I2C4_SCL <3,10,11,19,23>
RS- SDA 7 → I2C4_SDA <3,10,11,19,23>
SET A1 8 D3.3V
VCC A0 9
GND OUT 1

D3.3V
C569 4.7uF 2012 25V
C570 0.1uF 1005 10V

I2Cslave address: 1111_111x
Read:0xFF, Write: 0xFE

Current-Sense Amplifiers with ADC for VDD0.8V

VDD_RSP
Note: PMIC side VDD_RSP
U59 MAX9611AUB+
JP4 HWP-2-G
Note: SoC side VDD0.8V
VDD0.8V

RS+ SCL 6 I2C4_SCL
RS- SDA 7 I2C4_SDA
SET A1 8 D3.3V
VCC A0 9
GND OUT 1

D3.3V
C574 4.7uF 2012 25V
C575 0.1uF 1005 10V

I2Cslave address: 1111_100x
Read:0xF9, Write: 0xF8

GND
TH3 TH4
AGND1 PGND1

GND
TH5 TP9 HW-1-G
AGND2 PGND2

Holes to fix a board.

EH1 HOLE_E_4.0
EH2 HOLE_E_4.0
EH3 HOLE_E_4.0
EH4 HOLE_E_4.0
EH5 HOLE_E_4.0
EH6 HOLE_E_4.0
EH7 HOLE_E_4.0
EH8 HOLE_E_4.0

D3.3V   For EMI.
C913 0.1uF 1005 10V
C914 0.1uF 1005 10V
C915 0.1uF 1005 10V
C916 0.1uF 1005 10V
C917 0.1uF 1005 10V
C918 0.1uF 1005 10V
C919 0.1uF 1005 10V
C920 0.1uF 1005 10V
C921 0.1uF 1005 10V
C922 0.1uF 1005 10V
C923 0.1uF 1005 10V

D1.8V
C927 0.1uF 1005 10V
For EMI.

D1.8V
C928 47uF 3225 6.3V
For auxiliary power supply

D12.0V   For EMI.
C901 0.1uF 1005 50V
C902 0.1uF 1005 50V
C903 0.1uF 1005 50V
C904 0.1uF 1005 50V
C905 0.1uF 1005 50V

D5.0V
C907 0.1uF 1005 10V
C906 0.1uF 1005 10V
C908 0.1uF 1005 10V
C909 0.1uF 1005 10V
C910 0.1uF 1005 10V
C911 0.1uF 1005 10V
C912 0.1uF 1005 10V

Power PMIC2

26