Preliminary

R-CarH3-SiP System Evaluation Board "Salvator-X"

RTP0RC7795SIPB0010S

Rev.0.20

Preliminary

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1

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 1 of 25	

Preliminary

Layout Note:
Following signals need Ground guard.

AUDIO_CLKA
AUDIO_CLKB
AUDIO_CLKC

AUDIO_CLKOUT
AUDIO_CLKOUT3
SCIF_CLK, SCIF_CLK until X1-pin3

SD0_CLK_V,SD0_CLK_SOC
SD3_CLK_V,SD3_CLK_SOC
MMC0_CLK_V,MMC0_CLK_SOC

AVB_TXCREFCLK
AVB_TXC_25
AVB_RXC_25

QSPI0_SPCLK_18, QSPI0_SPCLK_sw
QSPI1_SPCLK_18, QSPI1_SPCLK_sw

VTHSENSE0_18 until TH1
VTHREF0_18 until TH2

U1A

SRU(3.3V)

<21> AUDIO_CLKA — AB38 AUDIO_CLKA_A
<21> AUDIO_CLKB — A34 GP5_12/HSCK0/AUDIO_CLKB_A
<19> AUDIO_CLKC — C39 GP5_21/MSIOF0_SS2/AUDIO_CLKC_A
<21> AUDIO_CLKOUT — G37 GP5_18/MSIOF0_SYNC/AUDIO_CLKOUT_A
<21,23> AUDIO_CLKOUT3 — B39 GP5_19/MSIOF0_SS1/AUDIO_CLKOUT3_A

SSI(3.3V)

<21,23> SSI_SCK0129 — M39 SSI_SCK0129
<21,23> SSI_WS0129 — J37 SSI_WS0129
<21,23> SSI_SDATA0 — K37 SSI_SDATA0
<21,23> SSI_SDATA1 — L37 SSI_SDATA1_A

<19,23> SSI_SCK4 — P39 GP6_08/SSI_SCK4
<19,23> SSI_WS4 — T37 GP6_09/SSI_WS4
<19,23> SSI_SDATA4 — P38 GP6_10/SSI_SDATA4

SCIF(3.3V)

D3.3V — C1 0.1uF 1005 10V
D3.3V — X1 (4 VCC, 1 STn, 2 GND, 3 OUT) NZ2520SB[14.7456MHz/50ppm]
SERIES_TERM R1 0 SCIF_CLK — AB39 GP6_23/AUDIO_CLKB_B/SCIF_CLK_A

<22> SCIF2_TXD — F38 GP5_10/TX2_A
<22> SCIF2_RXD — F39 GP5_11/RX2_A

<22,23> GP5_05/RX1/HRX1 — E39 GP5_05/RX1_A/HRX1_A
<22,23> GP5_06/TX1/HTX1 — E38 GP5_06/TX1_A/HTX1_A
<22,23> GP5_07/CTS1#/HCTS1n — H38 GP5_07/CTS1#/HCTS1#_A
<22,23> GP5_08/RTS1n/HRTS1n — H39 GP5_08/RTS1#/TANS/HRTS1#_A

SDHI0/DBG2(3.3V/1.8V)

Note: "SD0_WP"and "SD0_CD" signal is fixed at 3.3V.

SDHI0 (CLK,CMD,DAT[3:0])
(1) Matched trace length.

<14,23> SD0_WP — D29 SD0_WP
<14,23> SD0_CD — D30 SD0_CD
<14> SD0_DAT3_V — D31 SD0_DAT3/ASEBRK2
<14> SD0_DAT2_V — D32 SD0_DAT2/TDI2
<14> SD0_DAT1_V — C31 SD0_DAT1/TMS2
<14> SD0_DAT0_V — B31 SD0_DAT0/TCK2
<14> SD0_CMD_V — A31 SD0_CMD/TRST2_N
<14> SD0_CLK_V — R3 1005 22 SD0_CLK_SOC — A30 SD0_CLK/TDO2

3.3V
3.3V
3.3V/1.8V

SDHI3(3.3V/1.8V)

Note: "SD3_WP"and "SD3_CD" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD3.

SDHI3 (CLK,CMD,DAT[3:0])
(1) Matched trace length.

<14,23> GP4_16/SD3_DAT7/WP_V — D20 GP4_16/SD3_DAT7/SD3_WP
<14,23> GP4_15/SD3_DAT6/CD_V — D21 GP4_15/SD3_DAT6/SD3_CD
<14,23> SD3_DAT3_V — A21 GP4_12/SD3_DAT3
<14,23> SD3_DAT2_V — C23 GP4_11/SD3_DAT2
<14,23> SD3_DAT1_V — B23 GP4_10/SD3_DAT1
<14,23> SD3_DAT0_V — A23 GP4_09/SD3_DAT0
<14,23> SD3_CMD_V — C20 GP4_08/SD3_CMD
<14,23> SD3_CLK_V — R8 1005 22 SD3_CLK_SOC — A24 GP4_07/SD3_CLK

3.3V/1.8V

MMC(3.3V/1.8V)_[SDHI1,2]

MMC (CLK,CMD,DAT[7:0])
(1) Matched trace length.

<15> MMC0_DTA7_V — D27 GP3_11/SD1_DAT3/SD2_DAT7
<15> MMC0_DTA6_V — C27 GP3_10/SD1_DAT2/SD2_DAT6
<15> MMC0_DTA5_V — B27 GP3_09/SD1_DAT1/SD2_DAT5
<15> MMC0_DTA4_V — A27 GP3_08/SD1_DAT0/SD2_DAT4
<15> MMC0_DTA3_V — D23 GP4_05/SD2_DAT3
<15> MMC0_DTA2_V — D24 GP4_04/SD2_DAT2
<15> MMC0_DTA1_V — C25 GP4_03/SD2_DAT1
<15> MMC0_DTA0_V — D26 GP4_02/SD2_DAT0
<15> MMC0_CMD_V — A25 GP4_01/SD2_CMD
<15> MMC0_CLK_V — R9 1005 22 MMC0_CLK_SOC — A26 GP4_00/SD2_CLK
<15> MMC0_DS_V — B25 GP4_06/SD2_DS

3.3V/1.8V

GPIO

GPIO_Unused(1.8V/3.3V)

Note: "SD3_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD3.

<23> GP4_13/SD3_DAT4_V — B21 GP4_13/SD3_DAT4
<23> GP4_14/SD3_DAT5_V — C21 GP4_14/SD3_DAT5
<23> GP4_17/SD3_DS_V — C22 GP4_17/SD3_DS

GPIO_Unused(1.8V/3.3V)

Note: "SD1_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD1.

<23> GP3_06/SD1_CLK_V — A28 GP3_06/SD1_CLK
<23> GP3_07/SD1_CMD_V — A29 GP3_07/SD1_CMD

GPIO_Unused(3.3V)

<23> GP6_04 — M37 GP6_04/SSI_SDATA2_A
<23> GP6_21 — V36 GP6_21/SSI_SDATA9_A

R763 10k 1005 GP4_13/SD3_DAT4_V
R764 10k 1005 GP4_14/SD3_DAT5_V
R765 10k 1005 GP4_17/SD3_DS_V
R766 10k 1005 GP3_06/SD1_CLK_V
R767 10k 1005 GP3_07/SD1_CMD_V

GPIO_PU

<10,23> GP6_17/SSI_SCK78 — U39 GP6_17/SSI_SCK78
<10,23> GP6_18/SSI_WS78 — U37 GP6_18/SSI_WS78
<10,23> GP6_19/SSI_SDATA7 — V39 GP6_19/SSI_SDATA7
<10,23> GP6_20/SSI_SDATA8 — V37 GP6_20/SSI_SDATA8

D3.3V — R15 10k 1005
<10> GP5_13/HRX0 — D39 GP5_13/HRX0
<10> GP5_14/HTX0 — D38 GP5_14/HTX0
<10> GP5_15/HCTS0n — C38 GP5_15/HCTS0#
<10> GP5_16/HRTS0n — G38 GP5_16/HRTS0#
<10,23> GP5_24/MLB_SIG — J39 GP5_24/MLB_SIG
<10> GP5_25/MLB/IOEX_INTn — J38 GP5_25/MLB_DAT

R-CarH3SiP
H3SIP_BGA_r0096_005

EtherAVB

2.5V
AVB_RX_CTL — A16 — AVB_RX_CTL_25 <20>
AVB_RXC — B19 — AVB_RXC_25 <20>
AVB_RD0 — A13 — AVB_RD0_25 <20>
AVB_RD1 — B13 — AVB_RD1_25 <20>
AVB_RD2 — A14 — AVB_RD2_25 <20>
AVB_RD3 — B14 — AVB_RD3_25 <20>

R724~R729:Close to U1(H3SiP)

2.5V
AVB_TX_CTL — A8 R724 1005 24.9 1% — AVB_TX_CTL_25 <20>
AVB_TXC — A19 R725 1005 24.9 1% — AVB_TXC_25 <20>
AVB_TD0 — A18 R726 1005 24.9 1% — AVB_TD0_25 <20>
AVB_TD1 — B18 R727 1005 24.9 1% — AVB_TD1_25 <20>
AVB_TD2 — A17 R728 1005 24.9 1% — AVB_TD2_25 <20>
AVB_TD3 — B17 R729 1005 24.9 1% — AVB_TD3_25 <20>

3.3V
AVB_TXCREFCLK — A12 — AVB_TXCREFCLK <20>
AVB_MDIO — A9 — AVB_MDIO <20>
AVB_MDC — A15 — AVB_MDC <20>
GP2_10/AVB_MAGIC — B15 — GP2_10/PHY_RESETn <20>
AVB_PHY_INT — B16 — AVB_PHY_INT <20>
AVB_LINK — B9 — AVB_LINK <20>
AVB_AVTP_MATCH_A(wired or SCL5) — B11 — AVB_AVTP_MATCH <20>
AVB_AVTP_CAPTURE_A(wired or SDA5) — A11 — AVB_AVTP_CAPTURE <20>

QSPI(1.8V)

QSPI0_SPCLK — W3 — QSPI0_SPCLK_18
QSPI0_SSL — Y3 — QSPI0_SSL_18
QSPI0_MOSI/IO0 — AC5 — QSPI0_MOSI_IO0_18
QSPI0_MISO/IO1 — AB4 — QSPI0_MISO_IO1_18
QSPI0_IO2 — Y6 — QSPI0_IO2_18
QSPI0_IO3 — AB6 — QSPI0_IO3_18

QSPI1_SPCLK — V3 — QSPI1_SPCLK_18
QSPI1_SSL — V5 — QSPI1_SSL_18
QSPI1_MOSI/IO0 — AC7 — QSPI1_MOSI_IO0_18
QSPI1_MISO/IO1 — AE5 — QSPI1_MISO_IO1_18
QSPI1_IO2 — AE4 — QSPI1_IO2_18
QSPI1_IO3 — AC3 — QSPI1_IO3_18

RPC_INT# — Y7
RPC_WP# — V6
RPC_RESET# — V7

Do not stuff.
R604 0* 1005

D1.8V — R2 10k 1005 — SW3 CHS-01A

QSPI0_SPCLK_FLASH — W4
QSPI0_SSL_FLASH — AA3
QSPI0_MOSI_IO0_FLASH — AB5
QSPI0_MISO_IO1_FLASH — AC4
QSPI0_IO2_FLASH — AA6
QSPI0_IO3_FLASH — AC6

QSPI1_SPCLK_FLASH — V4
QSPI1_SSL_FLASH — W5
QSPI1_MOSI_IO0_FLASH — AB7
QSPI1_MISO_IO1_FLASH — AD5
QSPI1_IO2_FLASH — AD4
QSPI1_IO3_FLASH — AB3

RPC_INT_N_FLASH — AA7
RPC_WP_N_FLASH — W6
RPC_RESET_N_FLASH — W7
RSTO_N_FLASH — Y4

Do not stuff
D1.8V — R4 10k 1005
D1.8V — R5 10k* 1005
D1.8V — R6 10k 1005
D1.8V — R7 10k 1005

SW1 CHS-06A
QSPI1_SSL_18 — QSPI1_SSL_sw <9>
QSPI1_SPCLK_18 — QSPI1_SPCLK_sw <9>
QSPI0_SPCLK_18 — QSPI0_SPCLK_sw <9>
QSPI0_IO2_18 — QSPI0_IO2_sw <9>
QSPI0_MOSI_IO0_18 — QSPI0_MOSI_IO0_sw <9>
QSPI0_MISO_IO1_18 — QSPI0_MISO_IO1_sw <9>

SW2 CHS-06A
QSPI0_SSL_18 — QSPI0_SSL_sw <9>
QSPI1_MOSI_IO0_18 — QSPI1_MOSI_IO0_sw <9>
QSPI0_IO3_18 — QSPI0_IO3_sw <9>
QSPI1_IO3_18 — QSPI1_IO3_sw <9>
QSPI1_MISO_IO1_18 — QSPI1_MISO_IO1_sw <9>
QSPI1_IO2_18 — QSPI1_IO2_sw <9>

LVDS_bklight_Cnt

GP6_07/SSI_SDATA3 — N37 — GP6_07/LVDS_BLEN <18,23>

SoftSW

D3.3V — R10 100k 1005
GP5_17/MSIOF0_SCK — A38 GP5_17/SOFTSW0
GP5_20/MSIOF0_TXD — A37 GP5_20/SOFTSW1
GP5_22/MSIOF0_RXD — B37 GP5_22/SOFTSW2
GP5_23/MLB_CLK — AA39 — GP5_23/MLB/SOFTSW3 <10>

GP5_17/SOFTSW0 — CP1 MSIOF_SCK
GP5_20/SOFTSW1 — CP2 MSIOF_TXD
GP5_22/SOFTSW2 — CP3 MSIOF_RXD
AUDIO_CLKOUT — CP4 MSIOF_SYNC

SW4 CHS-04A
GP5_17/SOFTSW0 — R11 2k 1005
GP5_20/SOFTSW1 — R12 2k 1005
GP5_22/SOFTSW2 — R13 2k 1005
GP5_23/MLB/SOFTSW3 — R14 2k 1005

LED/TactSW

GP6_11/SSI_SCK5 — R39 — GP6_11/GP_LED/TSW0 <22,23>
GP6_12/SSI_WS5 — R37 — GP6_12/GP_LED/TSW1 <22,23>
GP6_13/SSI_SDATA5 — P37 — GP6_13/GP_LED/TSW2 <22,23>

T.SENSE(1.8V)

Matched trace length.
Trace like as differential pair.

VTHSENSE0 — AF4 VTHSENSE0_18 — C2 0.1uF 1005 10V — TH1 VTHSENSE
VTHREF0 — AG4 VTHREF0_18 — C3 0.1uF 1005 10V — TH2 VTHREF

After tying the GND side of both Cx and Cx, tie to the internal GND plane.

(3.3V) SDHI_PW

GP5_02/TX0 — B35 — GP5_02/SD0_PWEN <14>
GP5_01/RX0 — A35 — GP5_01/SD0_PWSEL <25>
GP3_15/SD1_WP(wired or SDA0) — B29 — GP3_15/SD3_PWEN <14,23>
GP3_14/SD1_CD(wired or SCL0) — C29 — GP3_14/SD3_PWSEL <23,25>
GP5_03/CTS0# — F37 — GP5_03/SD1_PWSEL <25>
GP5_09/SCK2 — L39 — GP5_09/SD2_PWSEL <25>

R-CarH3 SDHI/QSPI

2

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 2 of 25	

CONFIDENTIAL

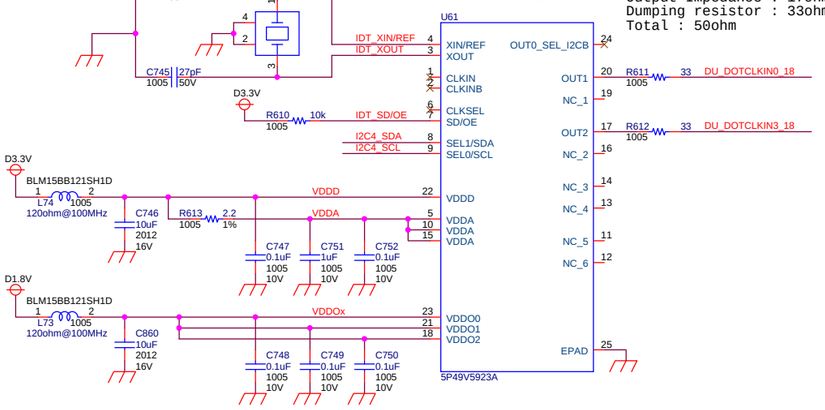
Preliminary

I2Cslave address: 1101_010X
Read:H'D5 Write: H'D4

Versaclock5 5P49V5923A

CL = 20pF(typ.)

Output Impedance : 17ohm
Dumping resistor : 33ohm
Total : 50ohm



Note.
1. Set OEn bit to output clock.
2. I2C is 3.3V signal.
3. C752(0.10uF) is for pin 5

Versaclock5 have Internal Pull-down Resistor(100k-300k)
CLKIN
CLKINB
SEL1/SDA
SEL0/SCL
OUT0_SEL_I2CB --> 0 = Use I2C (Default)
CLKSEL --> 0 = XIN/REF, XOUT (Default)
1 = CLKIN, CLKINB
SD/OE --> = OE and active low

Layout Note:
Following signals need Ground guard.

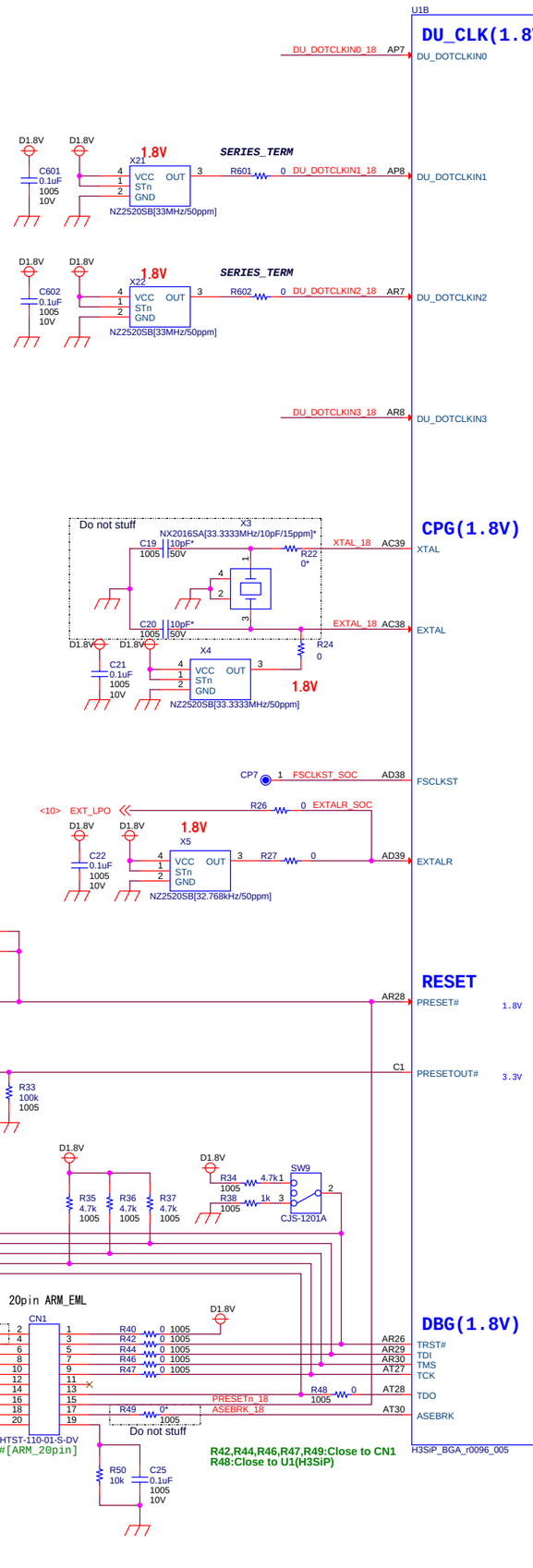
DU_DOTCLKIN0_18
DU_DOTCLKIN0_18 until U61-pin20
DU_DOTCLKIN1_18
DU_DOTCLKIN1_18 until X21-pin3
DU_DOTCLKIN2_18
DU_DOTCLKIN2_18 until X22-pin3
DU_DOTCLKIN3_18
DU_DOTCLKIN3_18 until U61-pin17
XTAL_18, EXTAL_18 until X4-pin3
EXT_LPO
EXTALR_SOC, EXTALR_SOC until X5-pin3,

CLKOUT_SOC,CLKOUT

TCK_18

WE0n [CAN_CLK(40MHz)]

Be carefull !!
See Pin Assignment.



CONFIDENTIAL

R-CarH3 DU/LBSC

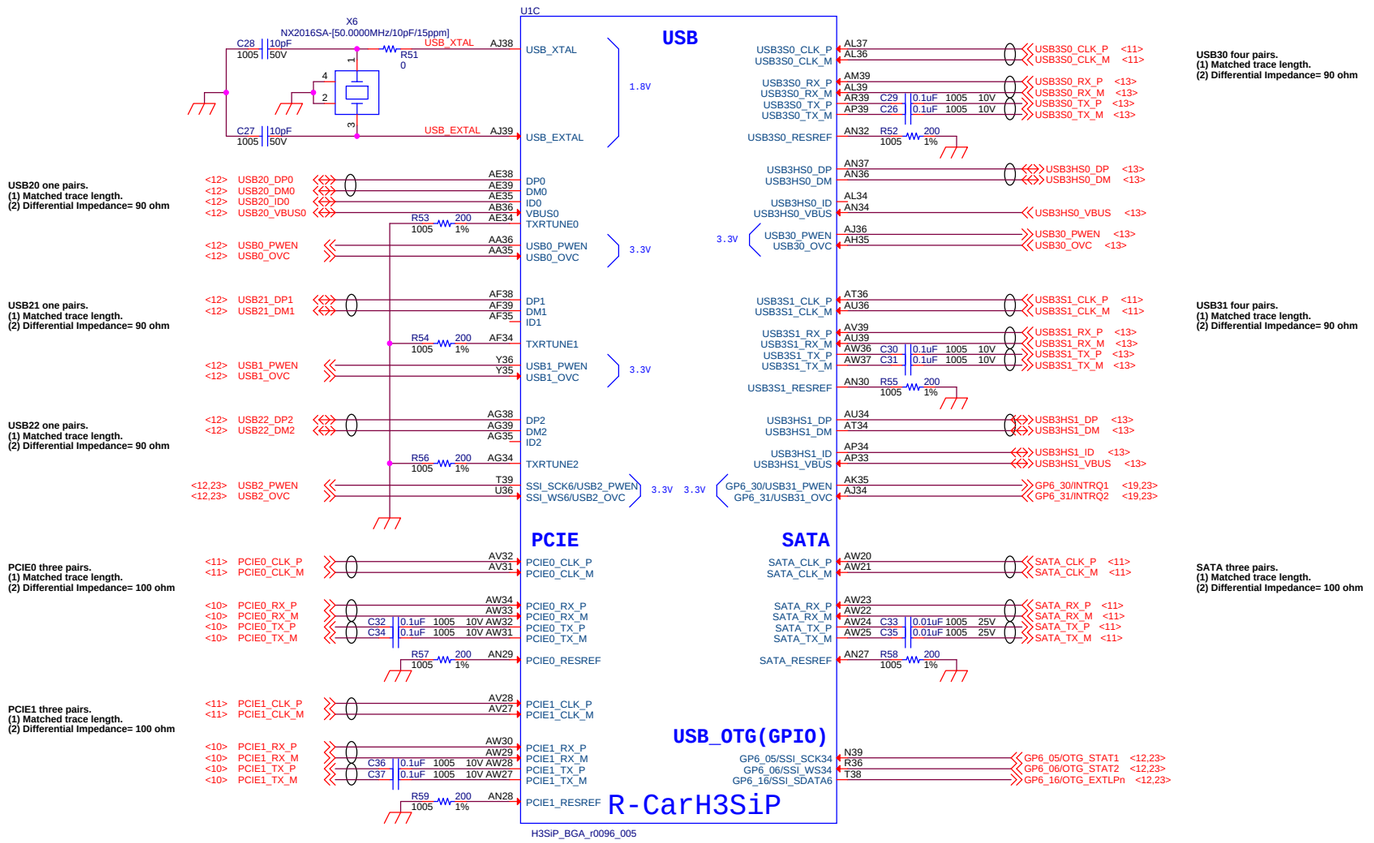
3

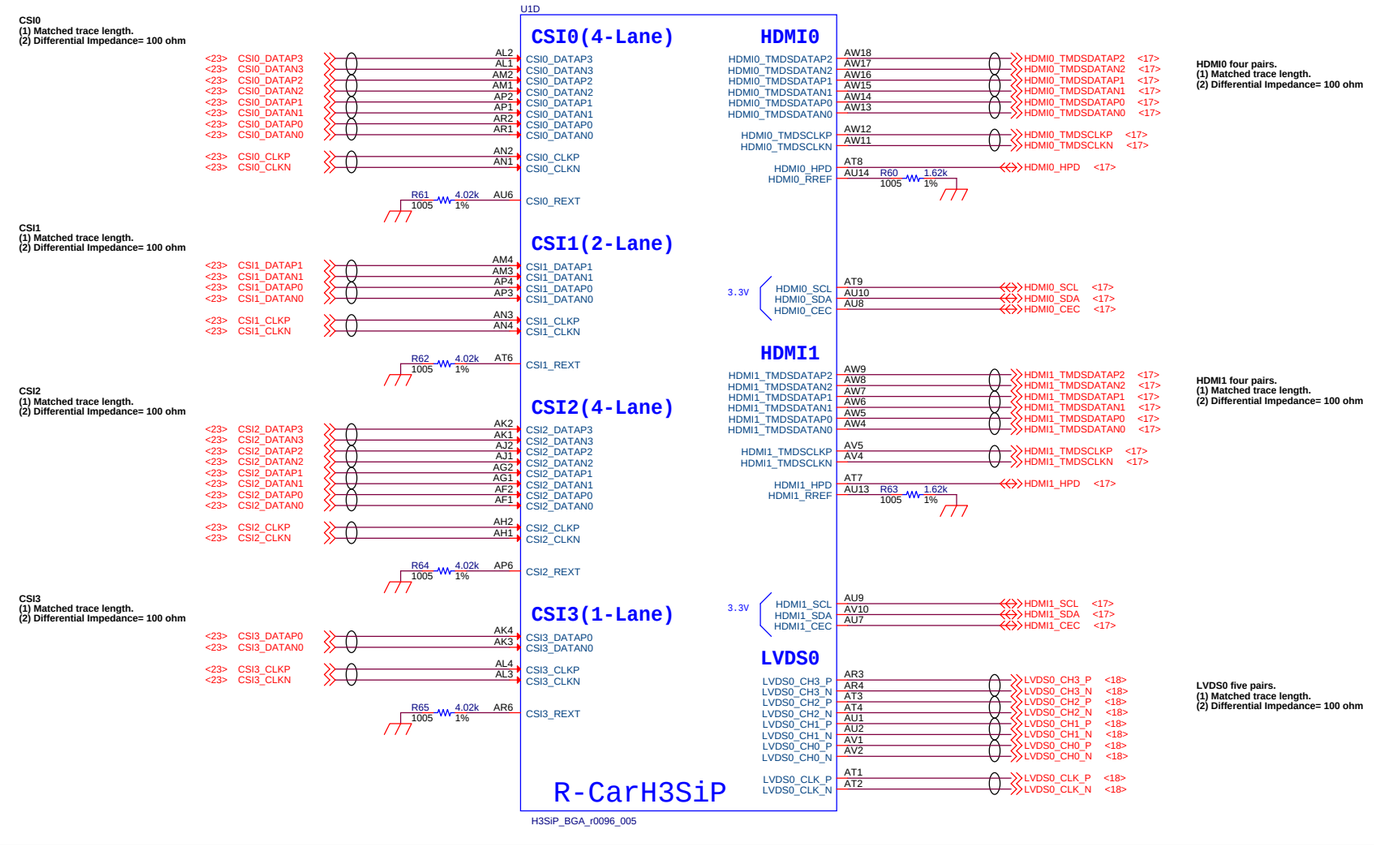
Title	R-CarH3-SiP System Evaluation Board (Salvator-X)
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X) Rev 0.20
Date: Thursday, May 28, 2015	Sheet 3 of 25

Preliminary

Layout Note:
Following signals need Ground guard.

USB_XTAL, USB_EXTAL
GP6_30/INTRQ1 [AUDIO_CLKOUT2_B(50MHz)]
GP6_31/INTRQ2 [AUDIO_CLKOUT3_B(50MHz)]





TXRTUNEn (n=0,1,2)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
USB3Sn_RESREF (n=0,1)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
PCIEn_RESREF (n=0,1)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
SATA_RESREF
Pull-down(GND) : 200ohm +-1% 100ppm/°C
CSIn_REXT (n=0-3)
Pull-down(GND) : 4.02kohm
HDMIn_RREF (n=0,1)
Pull-down(GND) : 1620ohm +-1%

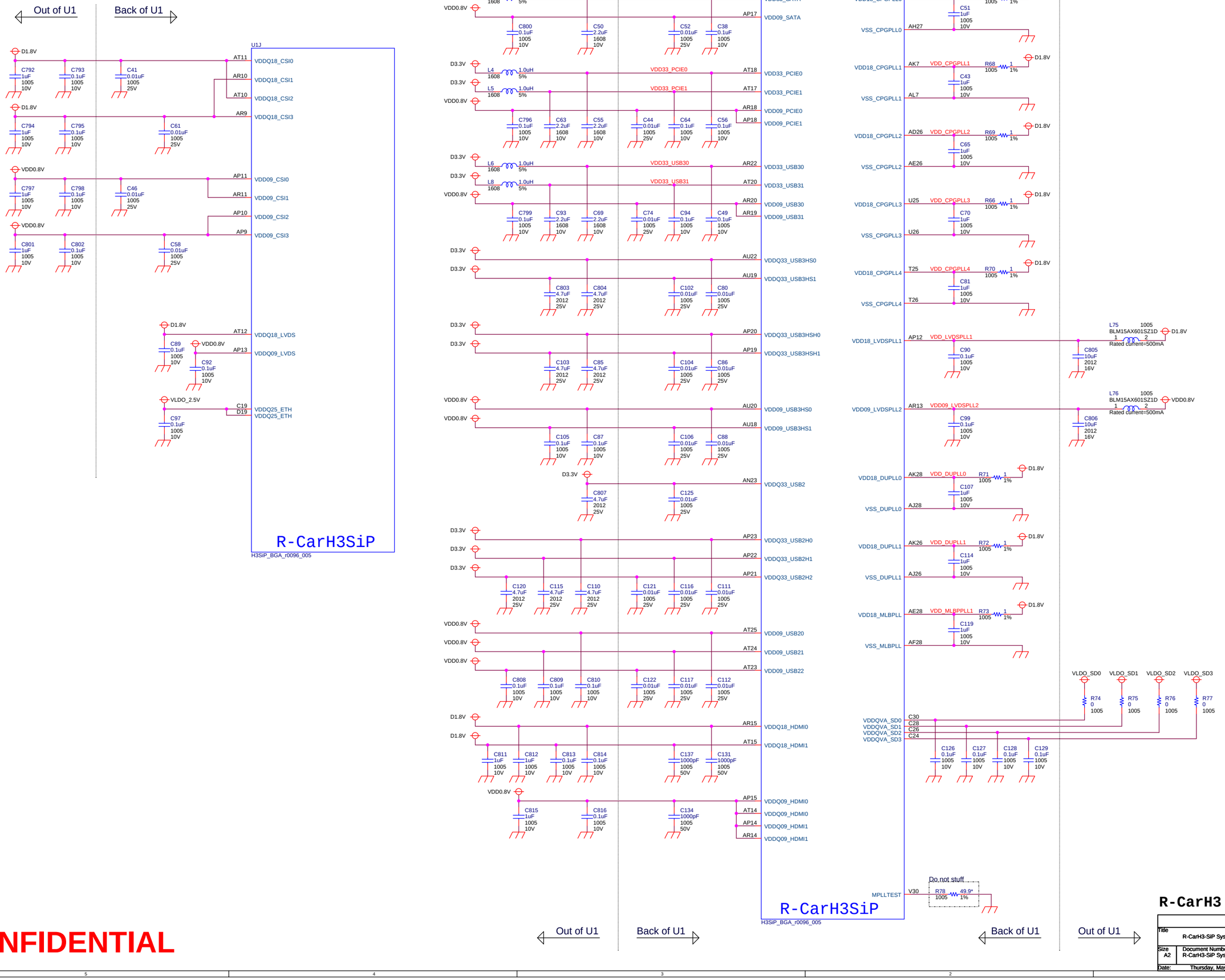
CONFIDENTIAL

R-CarH3 USB/HDMI

4

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 4 of 25	

Preliminary



CONFIDENTIAL

R-CarH3 POWER1

5

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 5 of 25	

Preliminary

Capacitor-Pin Combination
D3.3V(VDDQ33)
C142---J33
C143---L26
C144---N27
C145---N33
C146---T33
C147---U28,U29
C148---W28,W29
C149---AD25,AE24
C150---AH5
C151---AJ27
C152---AJ5
C153---AK24
C154---AM7
C604---AN25
C605---AN5
C606---AP24
C607---AR16
=17pcs

Capacitor-Pin Combination
D1.8V(VDDQ18)
C157---Y5,AA5
C158---AD3,AE2,AE3
C159---AD6,AE6
C160---AF26,AF27,AG26
C608---AH6
C609---AJ10
C610---AN26
C611---AP16
=8pcs

Capacitor-Pin Combination
VDD0.8V(VDD)
C162---M3
C163---N5
C879---R3
C165---U6
C880---W27

C167---AA28
C881---AD11
C874-+
C875-+
C876-+
C877-+
C882---AF13
C883---AF15
C171---AF17,AG18
C172---AF19
C173---AF21
C174---AG20
C175---AG22,AG23
C884---AH11

C177---AJ18
C885---AJ22
C886---AK11
C180---AK23
C887---AN10
C888---AN12
C889---AN14
C890---AN16
C891---AN18
C892---AN20
C893---AN22
=28-2+4=30pcs

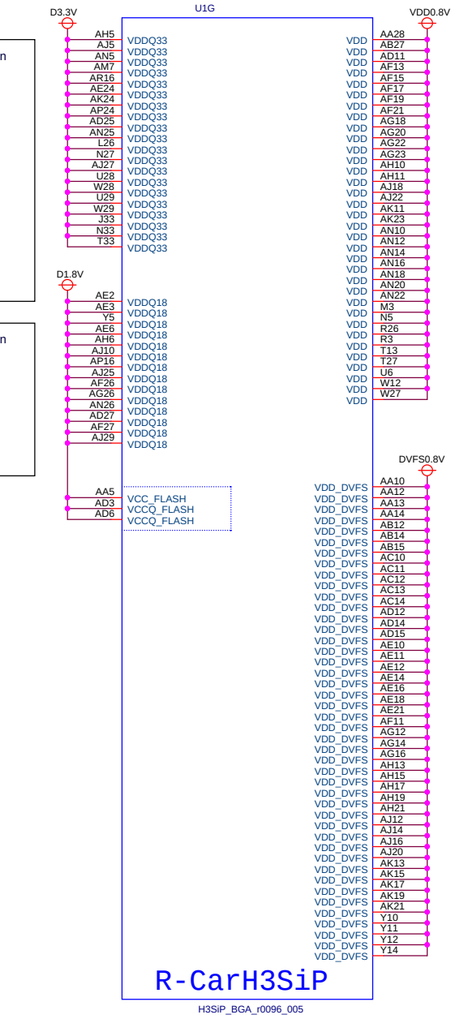
Capacitor-Pin Combination
DVFS0.8V(VDD_DVFS)
C863---Y10,Y11,AA10
C861-+
C864---Y12,AA12
C865---Y14
C862-+
C878-+
C866---AA13,AA14
C867---AB12,AC12
C195---AB14,AB15
C868---AC10,AC11
C869---AC13,AC14,AD14,AD15,AE14
C198---AD12,AE11,AE12,AF11
C870---AE10
C200---AE16
C201---AE18
C871---AE21
C203---AG12
C204---AG14
C205---AG16
C206---AH13,AJ14
C872---AH15
C873---AH17,AJ16
C209---AH19
C210---AH21
C211---AJ12,AK13
C212---AJ20
C213---AK15
C214---AK17
C215---AK19
C216---AK21
=27+3=30pcs

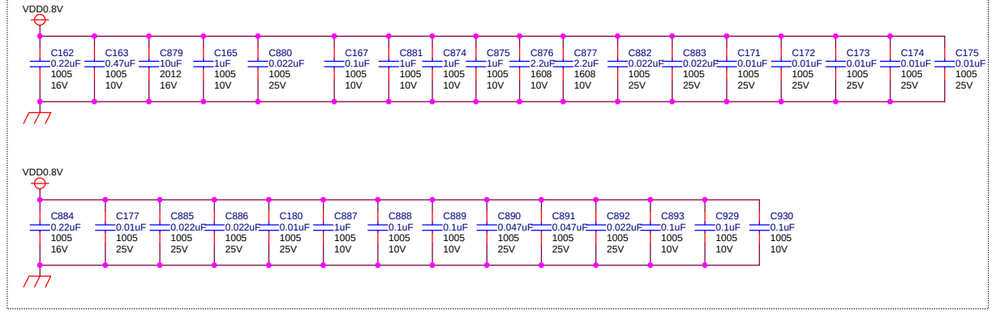
[VDD]
Back of U1
=30pcs

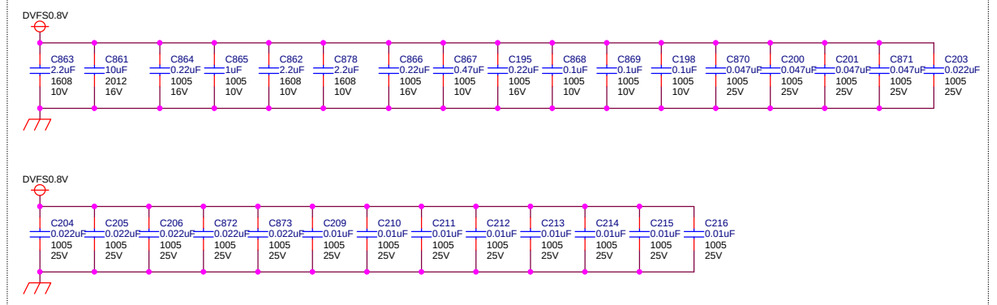
[VDD_DVFS]
Back of U1
=30pcs

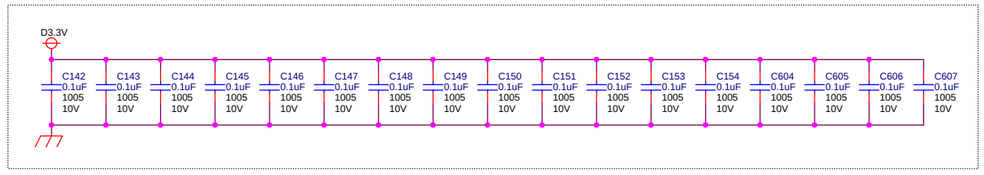
[VDDQ33]
Back of U1
=17pcs

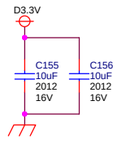
[VDDQ18]
Back of U1
=8pcs

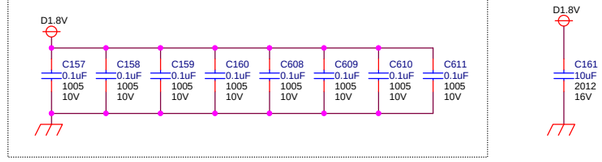


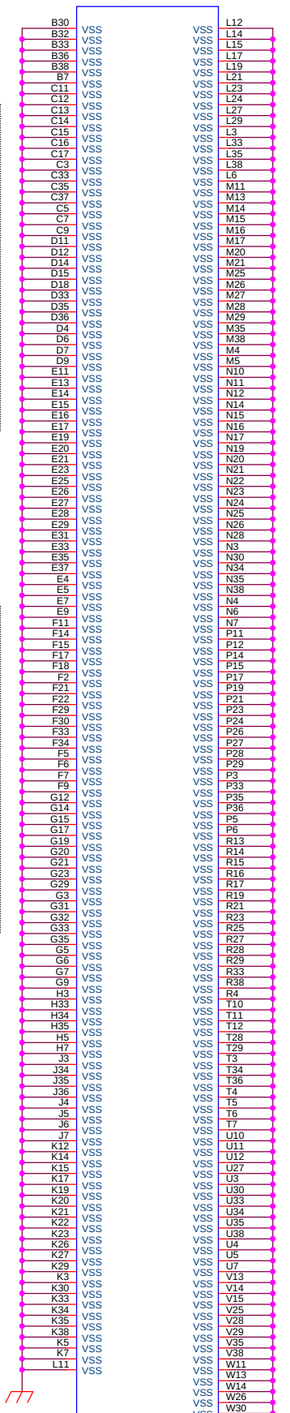


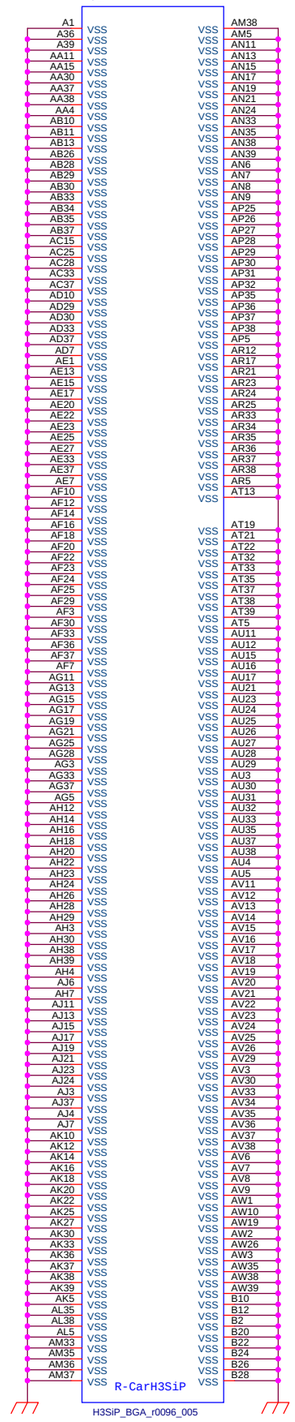


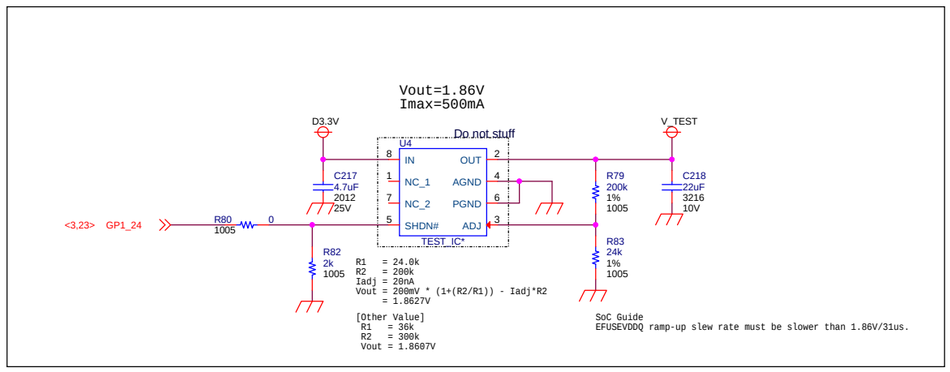


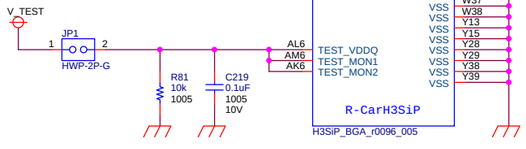




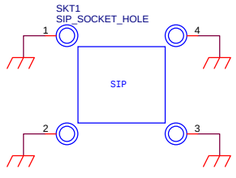








R-CarH3_Sip socket hole is connected to GND.



CONFIDENTIAL

R-CarH3 POWER2

6

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 6 of 25	

Preliminary

Capacitor-Pin Combination
DDR0_1.1V(VDDQVA_DDR0)
C612---B34,C34
C613---C32
C614---C36
C615---D28
C616---D34
C617---D37
C618---E30,E32
C619---E34
C620---E36
C621---F28
C622---F32
C623---G28
C624---G30
C625---G34
C626---G36
C627---H36
C628---K28,L28
C629---K36
C630---L30
C631---L34
C632---L36,M36
C633---M34
C634---N29
C635---N36
C636---P30
C637---P34
C638---R30
C639---R34
C640---R35
C641---T30
C642---T35
C643---W35
C644---Y30,AA29
C645---Y33,AA33
C646---Y34,AA34
C647---Y37
C648---AC30
C649---AC34
C650---AC36
C651---AD28
C652---AD34,AD35
C653---AE19
C654---AE29
C655---AE30
C656---AE36
C657---AG24,AH25
C658---AG29,AG30
C659---AG36,AH36
C660---AH37
C661---AJ33
C662---AK29
C663---AK34
C664---AL33
C665---AM34
C666---AN31
=55pcs

Capacitor-Pin Combination
DDR0_1.8V(VDD1_M0/M1)
C268---F31
C269---F35
C270---M30
C271---M33
C734---AC29
C735---AC35
C736---AJ30
C740---AJ35
=8pcs

Capacitor-Pin Combination
DDR1_1.8V(VDD1_M2/M3)
C272---F8
C273---F10
C274---F19
C275---F23
C737---M7
C738---M10
C739---M19
C741---M23
=8pcs

Capacitor-Pin Combination
DDR1_1.1V(VDDQVA_DDR0)
C667---C6
C668---C8
C669---C10
C670---C18
C671---D5
C672---D8
C673---D10
C674---D13
C675---D16
C676---D22,E22
C677---E6
C678---E8
C679---E10
C680---E12
C681---E18
C682---E24,D25
C683---F13
C684---F16
C685---F20
C686---F25
C687---G4
C688---G8
C689---G10,G11
C690---G13
C691---G16
C692---G18
C693---G22
C694---G24,G25
C695---H4
C696---H6
C697---K4
C698---K6
C699---K11
C700---K13
C701---K16
C702---K18
C703---K24
C704---K25
C705---L4
C706---L5,M6
C707---L7
C708---L10
C709---L13
C710---L16
C711---L18,M18
C712---L20
C713---L22,M22
C714---L25
C715---M12
C716---M24
C717---N13,P13
C718---N18,P18
C719---P10
C720---P16
C721---P20
C722---P22
C723---P25
C724---P4,R5
C725---P7,R6,R7
C726---R10
C727---R11,R12
C728---R18
C729---R20
C730---R22
C731---R24
C732---AD13
C733---AG10
=67pcs

ZQn (n=0,1)
Pull-up(DDRIO) : 240ohm +-1%

MnZQ (n=0-3)
Pull-down(GND) : 240ohm +-1%

Do not stuff

Do not stuff

Note: This terminal is connected to the power supply on the SIP.

Back of U1

H3SiP_BGA_r0096_005

DDR0_1.1V

[DDR0_1.1V]
Back of U1
=55pcs

DDR1_1.1V

[DDR1_1.1V]
Back of U1
=67pcs

DDR0_1.8V

[DDR0_1.8V]
Back of U1
=8pcs

DDR1_1.8V

[DDR1_1.8V]
Back of U1
=8pcs

CONFIDENTIAL

R-CarH3 LPDDR_POWER

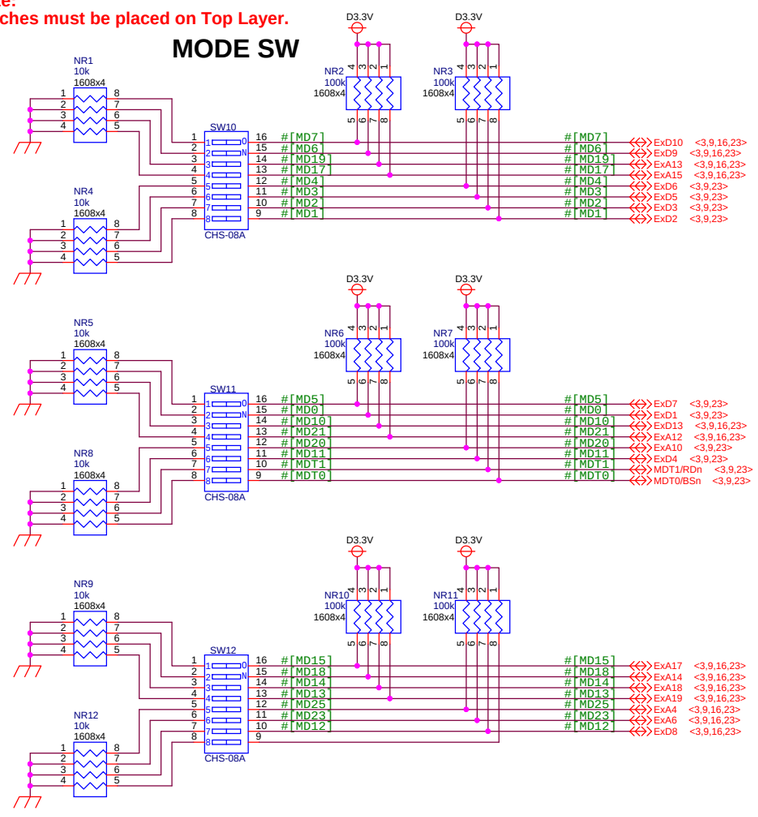
7

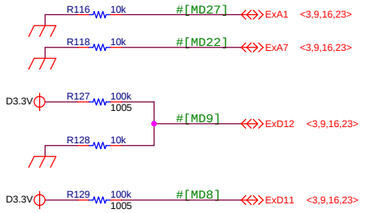
Title	R-CarH3-SiP System Evaluation Board (Salvator-X)
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X) Rev 0.20
Date: Thursday, May 28, 2015	Sheet 7 of 25

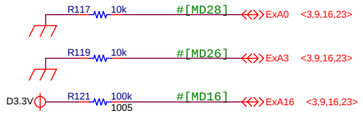
Preliminary

Layout Note:
Mode switches must be placed on Top Layer.

MODE SW







[Design Note]
It is not necessary to setup MD24.

CONFIDENTIAL

MODE_SW

8

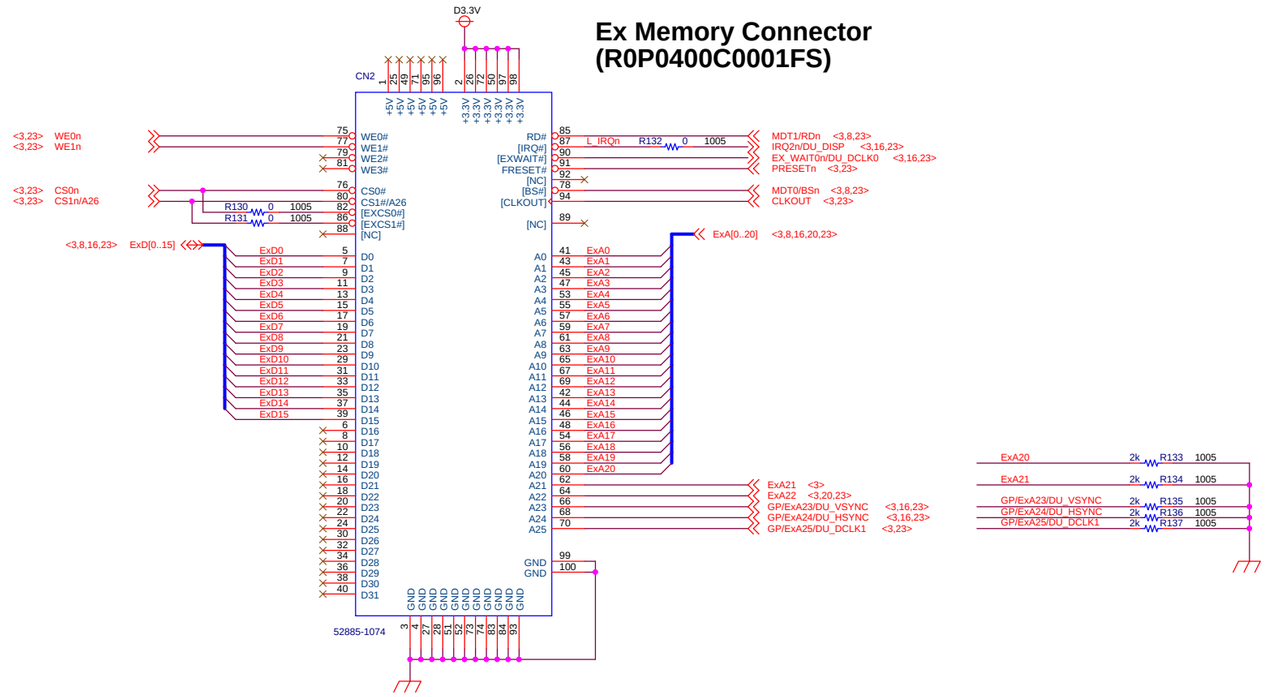
Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 8 of 25	

Preliminary

Layout Note:
Following signals need Ground guard.

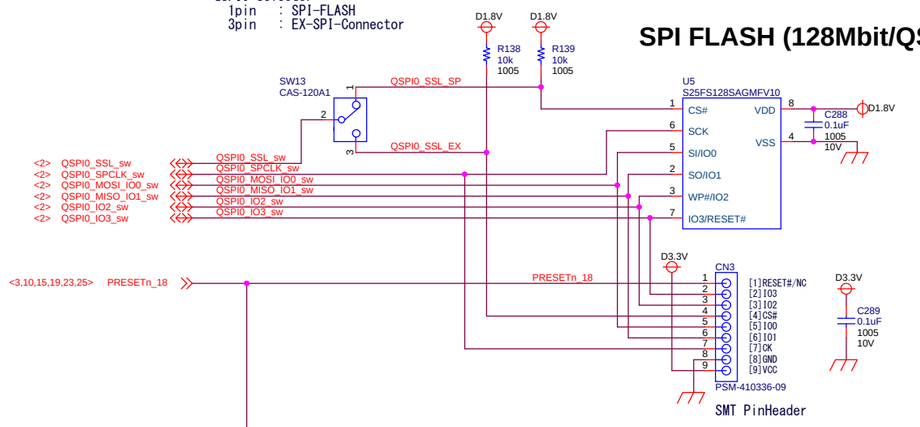
CLKOUT
QSPI0_SPCLK_18, QSPI0_SPCLK_SP
QSPI1_SPCLK_18, QSPI1_SPCLK_EX

Ex Memory Connector (R0P0400C0001FS)



QSPI0 Selector
1pin : SPI-FLASH
3pin : EX-SPI-Connector

SPI FLASH (128Mbit/QSPI0)

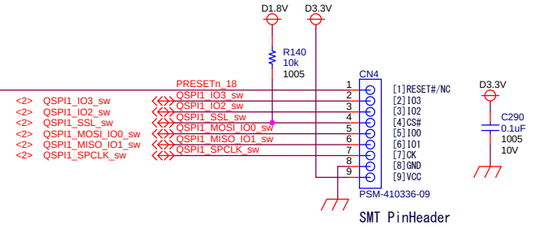


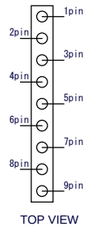
S25FS128SAGMFV10

S25FS 128 S AG M F V 10
##

- 10 = SOIC-8pin
- V = Automotive In-Cabin (-40C to +105C)
- F = Lead(Pb)-free
- M = SOIC
- AG = 133 MHz
- S = 0.65um MirrorBit Process Technology
- 128 = 128Mbit
- S25FS = Spansion Memory 1.8 Volt-Only

EX-SPI Connector (QSPI0)





EX-SPI Connector (QSPI1)

EX-SPI-Flash-Board generate VIO=1.8V from D3.3V for internal using.

QSPI_FLASH/FL_CN

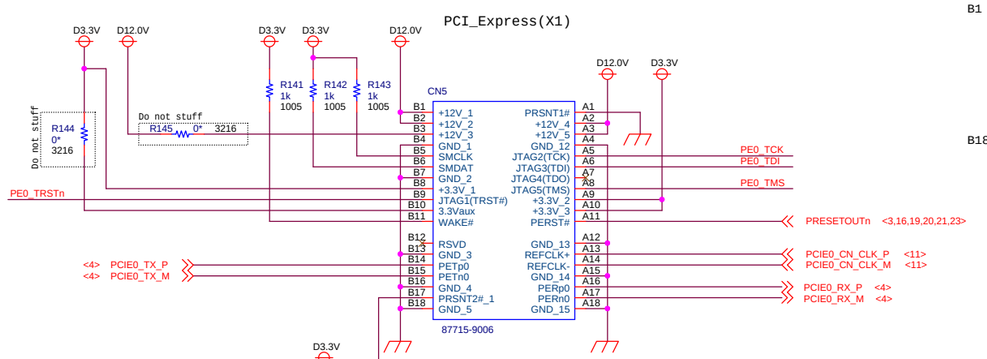
9

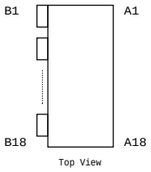
Title: R-CarH3-SiP System Evaluation Board (Salvator-X)			
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)		Rev: 0.20
Date: Thursday, May 28, 2015	Sheet 9 of 25		

CONFIDENTIAL

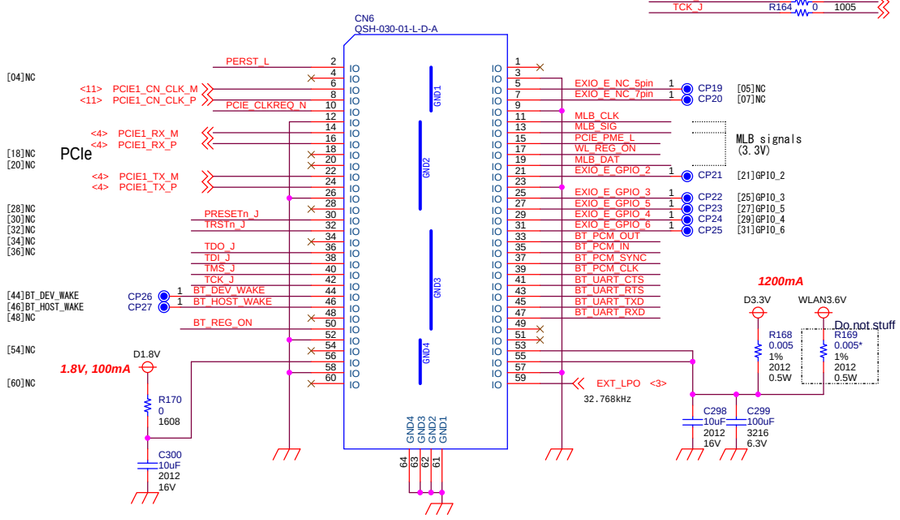
Preliminary

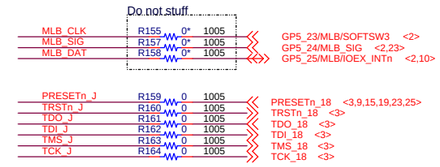
PCIE (PCIe-ch0)





BT/WLAN (PCIe-ch1)



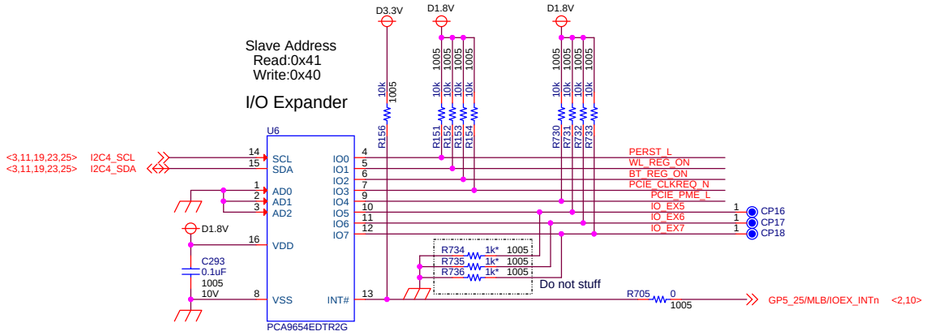


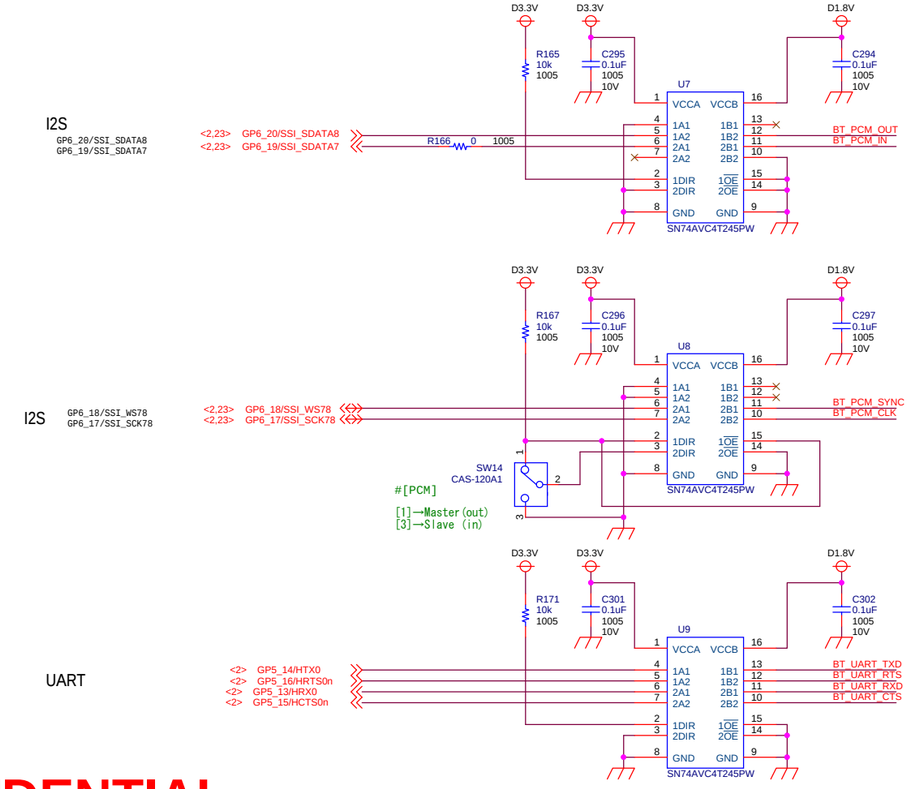
BCM89359 based module EVB Pin Assign (@2015/01/20)

No.	Pin Name	No.	Pin Name
2	PCIE_PRST_N	1	NC
4	NC	3	GND
6	PCIE_REFCLK_N	5	NC
8	PCIE_REFCLK_P	7	NC
10	PCIE_CLKREQ_N	9	GND
12	GND	11	NC
14	PCIE_TDN	13	NC
16	PCIE_TDP	15	PCIE_PME_L or WL_HOST_WAKE
18	NC	17	WL_REG_ON
20	NC	19	NC
22	PCIE_RDN	21	GPIO_2
24	PCIE_RDP	23	GND
26	GND	25	GPIO_3
28	NC	27	GPIO_5
30	NC	29	GPIO_4
32	NC	31	GPIO_6
34	NC	33	BT_PCM_IN
36	NC	35	BT_PCM_OUT
38	NC	37	BT_PCM_SYNC
40	NC	39	BT_PCM_CLK
42	NC	41	BT_UART_RTS
44	BT_DEV_WAKE	43	BT_UART_CTS
46	BT_HOST_WAKE	45	BT_UART_RXD
48	NC	47	BT_UART_TXD
50	BT_REG_ON	49	NC
52	GND	51	NC
54	NC	53	VDD
56	VIO	55	VDD
58	GND	57	GND
60	NC	59	LPO_IN

-60pin Connector on BT/WLAN EVB
OTH-030-01-L-D-A (Samtec)

-Dimensions
45mm x 35mm





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Default Unit is "mm"

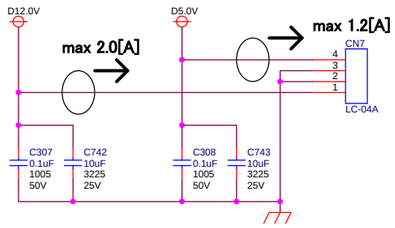
10

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X) Rev 0.20
Date: Thursday, May 28, 2015	Sheet 10 of 25

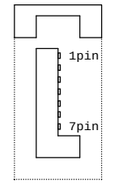
PCIe ch0/ch1

Preliminary

Serial ATA Drive power supply connector

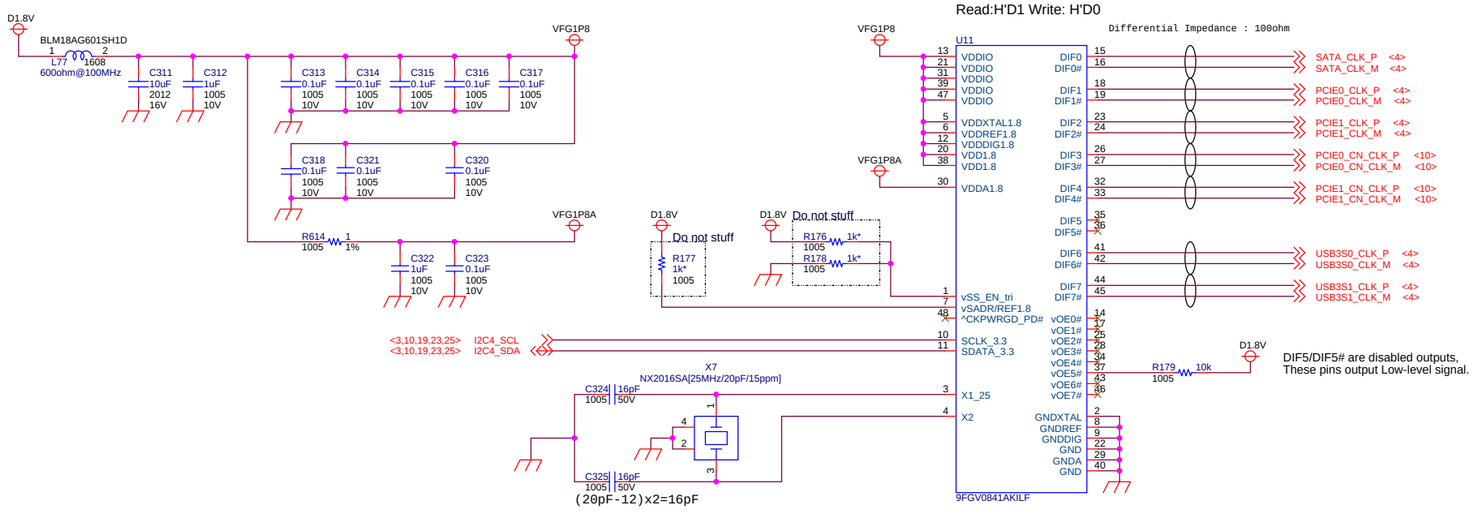


Serial ATA signal connector



Serial ATA signal connector
Top View

I2Cslave address: 1101_000X
Read:H'D1 Write: H'D0



v : prefix indicates internal 120KOhm pull down resistor
^ : prefix indicates internal 120KOhm pull up resistor

Power Management Table

CKPWRGD_PD#	SMBus OE bit	DIFx			REF
		OEx#	True O/P	Comp. O/P	
0	X	X	Low	Low	Hi-Z
1	1	0	Running	Running	Running
1	0	1	Low	Low	Low

SMBus Address Selection Table (I2C Slave address)

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

Select Spread Spectrum Table

vSS_EN_tri	Spread Spectrum
0	Spread Off
M	-0.25%
1	-0.5%

'M' is Mid Voltage = 0.5VDD = 0.9V.
This setting can be controled by software.
Refer to datasheet chapter of "SMBus Table : SS Readback and Control Register"

CONFIDENTIAL

Default Unit is "mm"

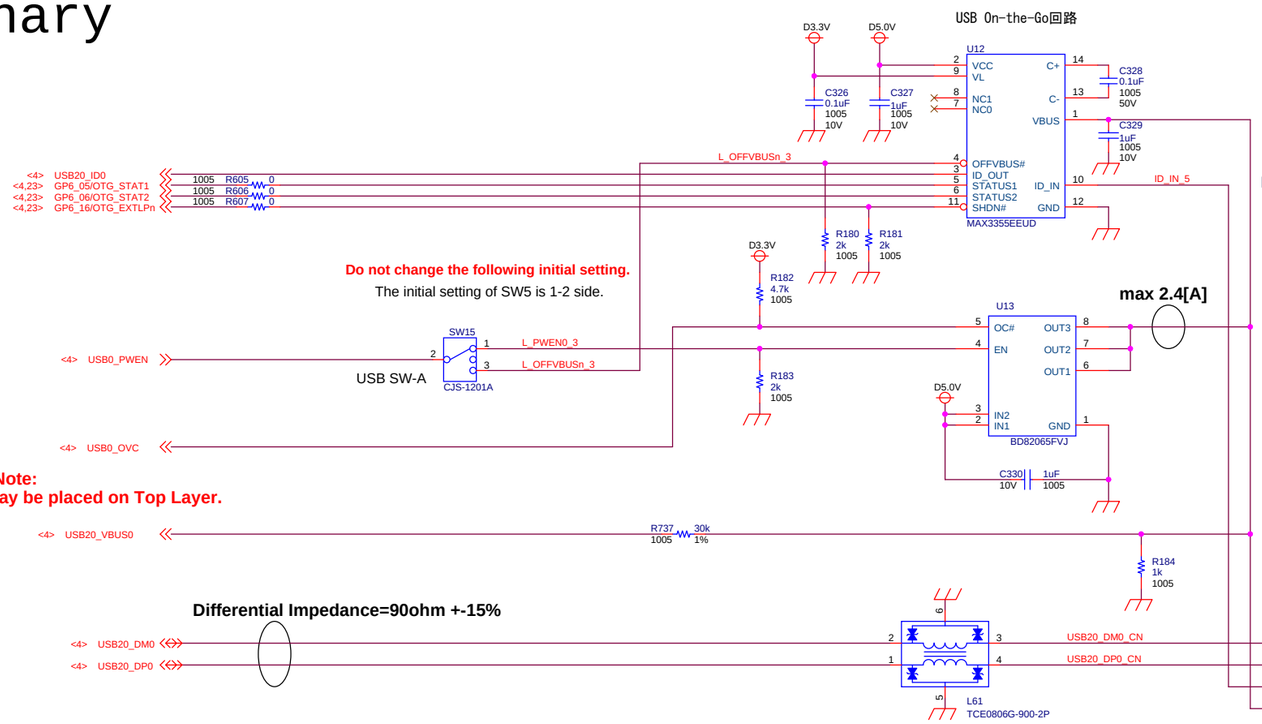
Serial ATA

11

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 11 of 25	

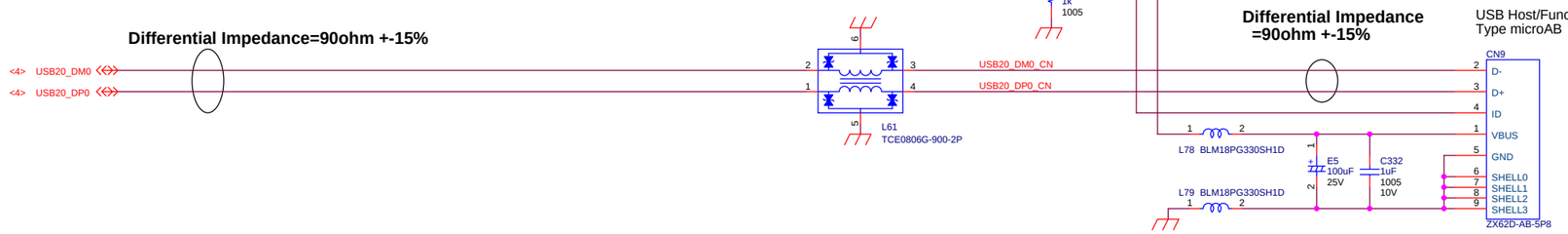
Preliminary

USB 0n-the-Go回路

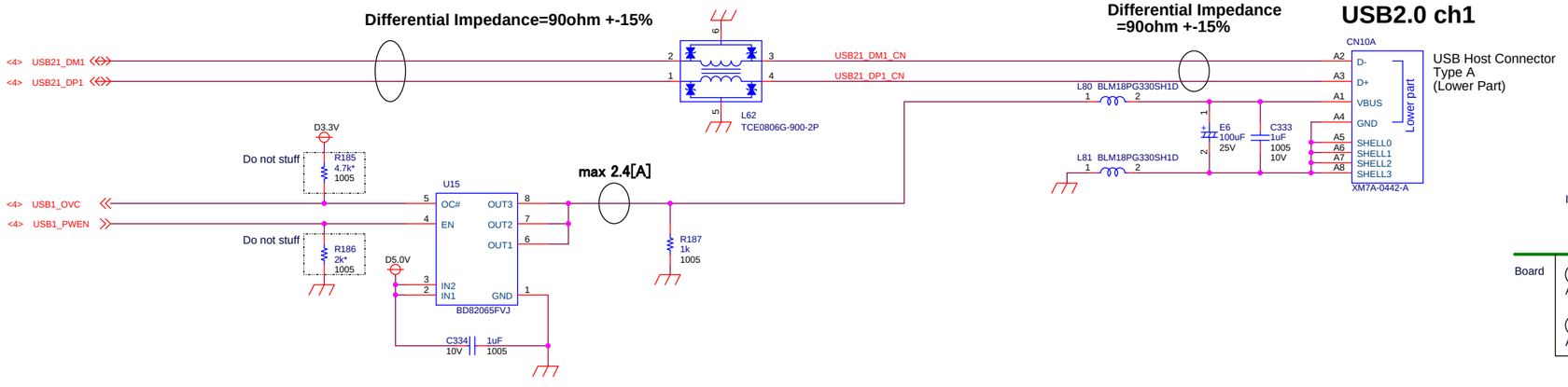


[Design Note]
The ID_IN pin is internally pulled up to Vcc=5V.

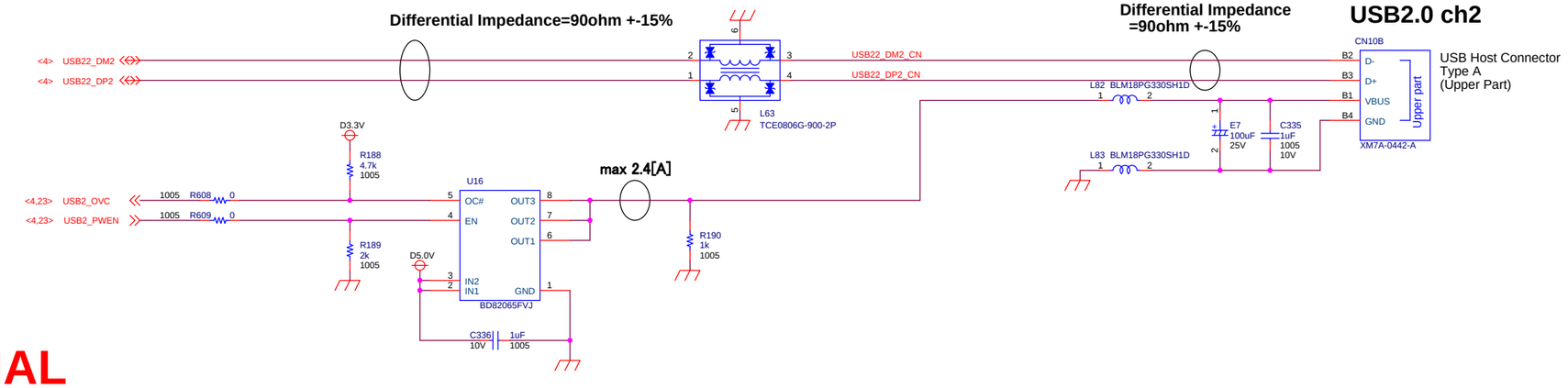
USB2.0 ch0



USB2.0 ch1



USB2.0 ch2



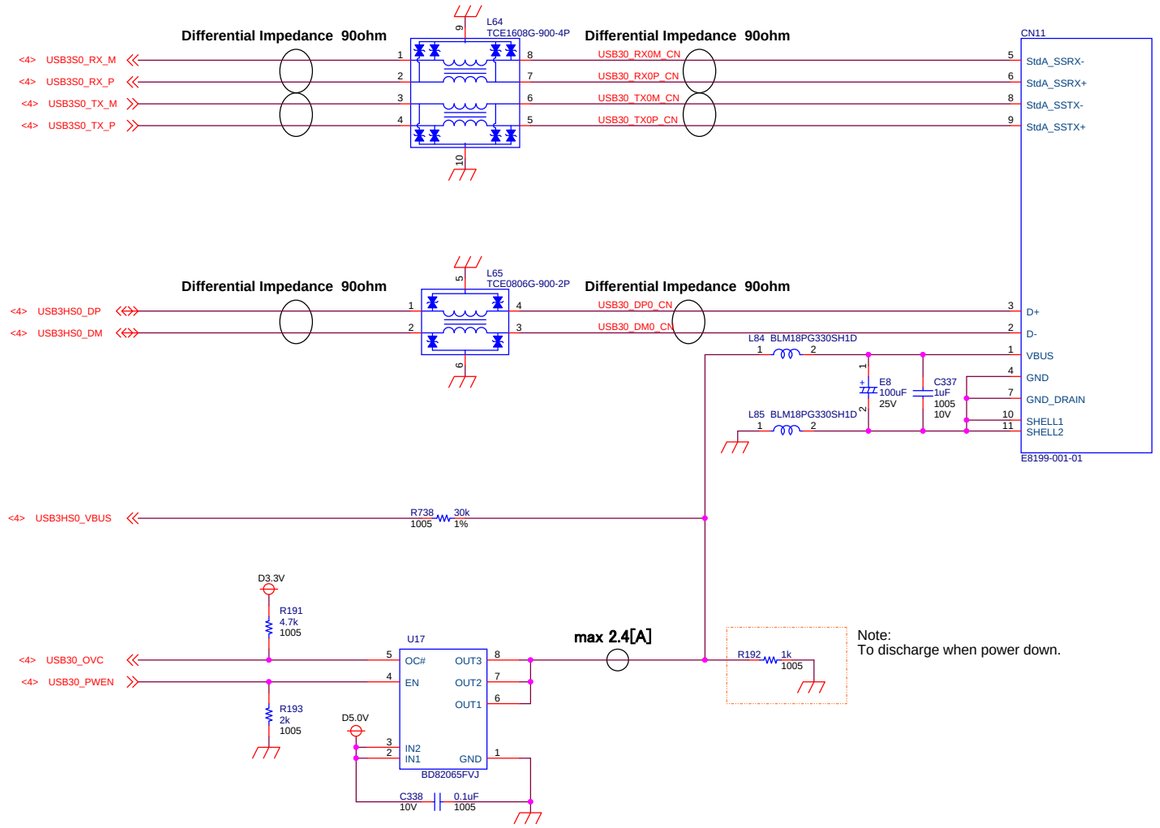
CONFIDENTIAL

USB2.0

12

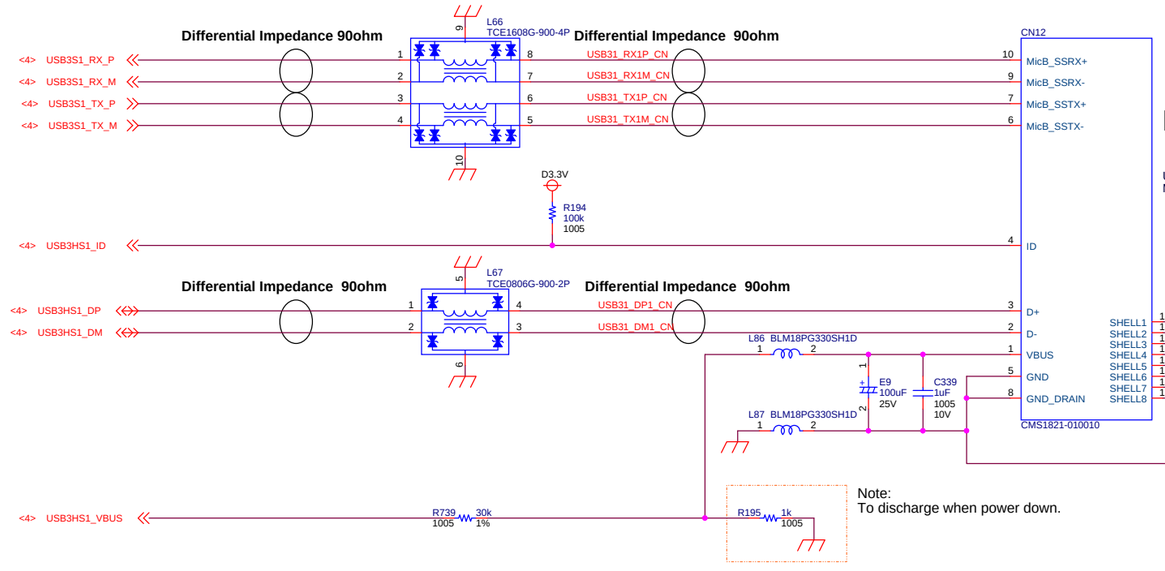
Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.20
Date: Thursday, May 28, 2015	Sheet 12 of 25	

Preliminary



Host/Function

USB 3.0 Connectors
Standard-A Receptacle



Function Only

USB 3.0 Connectors
Micro-B Receptacle

USB3.0

13

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 13 of 25	

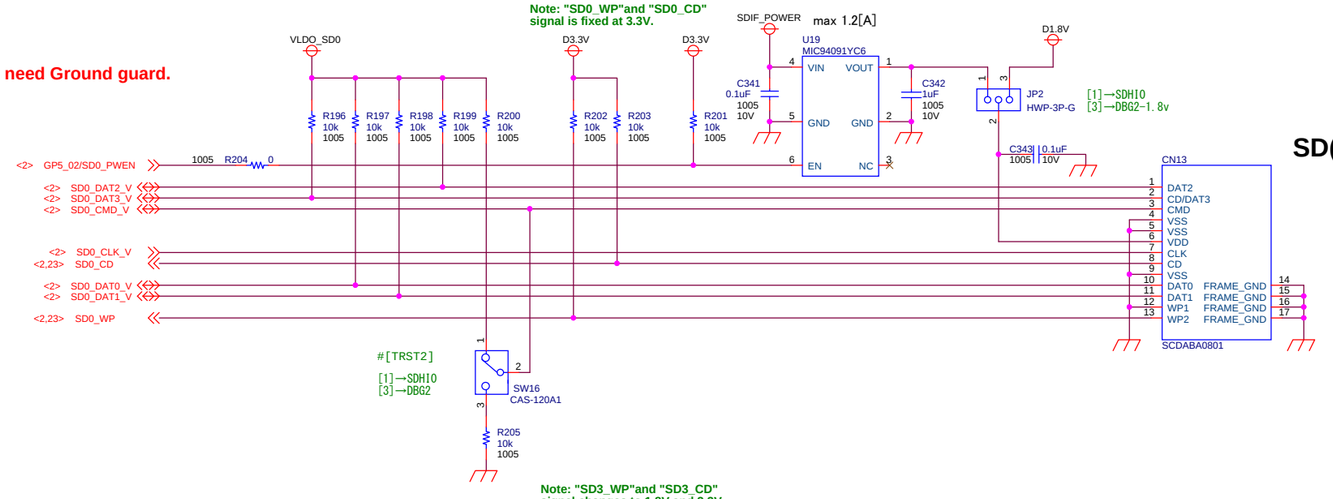
CONFIDENTIAL

Preliminary

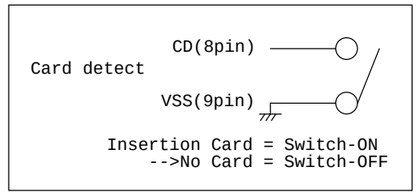
Layout Note:
Following signals need Ground guard.

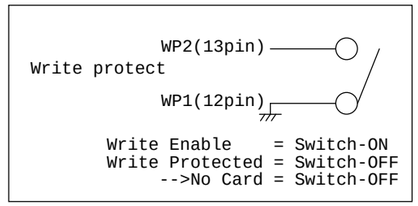
SD0_CLK_V

Note: "SD0_WP"and "SD0_CD" signal is fixed at 3.3V.



SD(CH0)

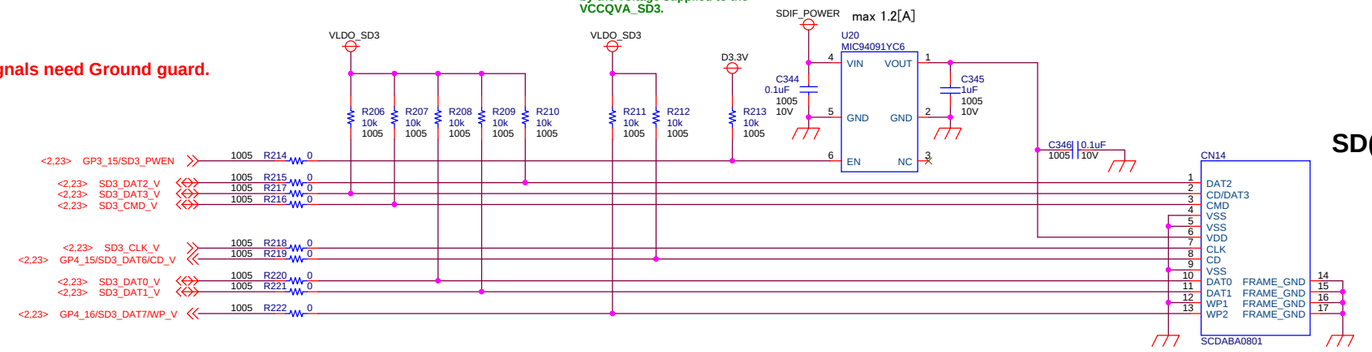




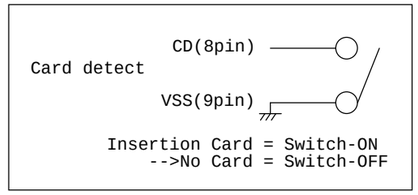
Layout Note:
Following signals need Ground guard.

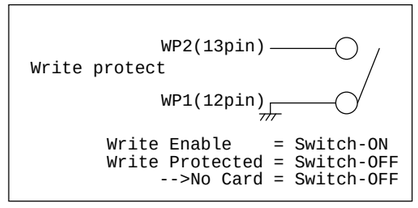
SD3_CLK_V

Note: "SD3_WP"and "SD3_CD" signal changes to 1.8V and 3.3V by the voltage supplied to the VCCQVA_SD3.

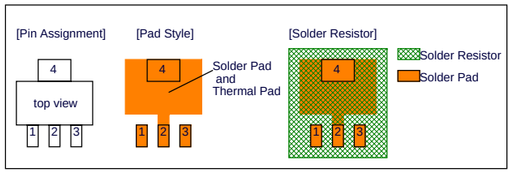


SD(CH3)

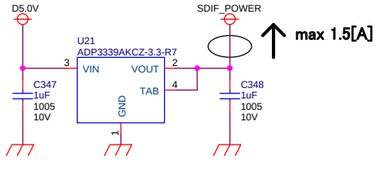




Layout Note:
Pad Configuration for ADP3339



D3.3V for SDIF Power



CONFIDENTIAL

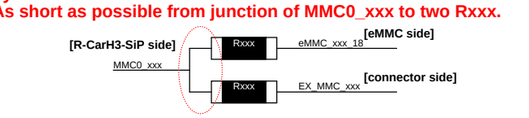
SDHI0/SDHI3

14

Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.20
Date: Thursday, May 28, 2015	Sheet 14 of 25	

Preliminary

Layout Note:
As short as possible from junction of MMC0_xxx to two Rxxx.



Do not stuff

<2> MMC0_DTA0_V	R225 0 1005 eMMC_D0_18	R617 0* 1005	EX_MMC_D0_V <23>
<2> MMC0_DTA1_V	R226 0 1005 eMMC_D1_18	R619 0* 1005	EX_MMC_D1_V <23>
<2> MMC0_DTA2_V	R227 0 1005 eMMC_D2_18	R620 0* 1005	EX_MMC_D2_V <23>
<2> MMC0_DTA3_V	R228 0 1005 eMMC_D3_18	R618 0* 1005	EX_MMC_D3_V <23>
<2> MMC0_DTA4_V	R229 0 1005 eMMC_D4_18	R621 0* 1005	EX_MMC_D4_V <23>
<2> MMC0_DTA5_V	R231 0 1005 eMMC_D5_18	R622 0* 1005	EX_MMC_D5_V <23>
<2> MMC0_DTA6_V	R230 0 1005 eMMC_D6_18	R623 0* 1005	EX_MMC_D6_V <23>
<2> MMC0_DTA7_V	R232 0 1005 eMMC_D7_18	R626 0* 1005	EX_MMC_D7_V <23>
<2> MMC0_CMD_V	R233 0 1005 eMMC_CMD_18	R627 0* 1005	EX_MMC_CMD_V <23>
<2> MMC0_CLK_V	R234 0 1005 eMMC_CLK_18	R628 0* 1005	EX_MMC_CLK_V <23>
<2> MMC0_DS_V	R235 0 1005 eMMC_DS_18	R629 0* 1005	EX_MMC_DS_V <23>

Layout Note:
Following signals need Ground guard.

MMC0_CLK_V, eMMC_CLK_18, EX_MMC_CLK_V

Layout Note:
Matched Trace Length from R-CarH3-SiP to eMMC. max 400Mbps/pin

Group 1
- MMC0_DTA[7:0]_V + eMMC_D[7:0]_18
- MMC0_CMD_V + eMMC_CMD_18
- MMC0_CLK_V + eMMC_CLK_18
- MMC0_DS_V + eMMC_DS_18

D1.8V — R616 0 — eMMC_VCCQ

Rated current=1A

eMMC_VCCQ — NR14 47k 1608x4 (4 3 2 1 / 5 6 7 8)

eMMC_VCCQ — NR15 47k 1608x4 (4 3 2 1 / 5 6 7 8)

eMMC_VCCQ — R223 47k — R224 47k* Do not stuff

[Design Note]
NAND Memory Power(VCC): 2.7 - 3.6V
eMMC Interface Power(VCCQ): 1.70-1.95V

eMMC(1.8V)

[Pin Function]

U22A
KLMBG4GESD-B031

SD2_DAT0 / MMC0_DTA0	eMMC_D0_18	A3	DATA0	VCC_1 E6
SD2_DAT1 / MMC0_DTA1	eMMC_D1_18	A4	DATA1	VCC_2 F5
SD2_DAT2 / MMC0_DTA2	eMMC_D2_18	A5	DATA2	VCC_3 J10
SD2_DAT3 / MMC0_DTA3	eMMC_D3_18	B2	DATA3	VCC_4 K9
SD1_DAT0 / MMC0_DTA4	eMMC_D4_18	B3	DATA4	
SD1_DAT1 / MMC0_DTA5	eMMC_D5_18	B4	DATA5	VCCQ_1 C6
SD1_DAT2 / MMC0_DTA6	eMMC_D6_18	B5	DATA6	VCCQ_2 M4
SD1_DAT3 / MMC0_DTA7	eMMC_D7_18	B6	DATA7	VCCQ_3 N4
				VCCQ_4 P3
				VCCQ_5 P5
SD2_CMD / MMC0_CMD	eMMC_CMD_18	M5	CMD	
				VDDI C2
SD2_CLK / MMC0_CLK	eMMC_CLK_18	M6	CLK	
SD2_DS / MMC0_DS	eMMC_DS_18	H5	DS	
				VSS_1 A6
				VSS_2 E7
				VSS_3 G5
				VSS_4 H10
				VSS_5 J5
		K5	RST_n	VSS_6 K8
				VSSQ_1 C4
				VSSQ_2 N2
				VSSQ_3 N5
				VSSQ_4 P4
				VSSQ_5 P6

D3.3V — C363 2.2uF 1608 10V

[Design Note]
Sets pull-down resistor(47kohm) at the DS pin.
For detail, See "Table 217 - HS400 Capacitance and Resistors on eMMC specification" in JESD84-B51.pdf

R236 47k

eMMC_VCCQ — Do not stuff — R624 47k*

<3,9,10,19,23,25> PRESETn_18 — R625 0 1005

[Design Note]
In case of using SDHI1 through EXIO connector 'CN27', that is "EXIO_B",

DISMOUNT follwoing resistors.
R229, R231, R230, R232(0ohm/1005).
and MOUNT following resistors.
R621, R622, R623, R626(0ohm/1005).

[Design Note]
In case of using SDHI2 through EXIO connector 'CN27', that is "EXIO_B",

DISMOUNT follwoing resistors.
R229, R231, R230, R232(0ohm/1005).
and MOUNT following resistors.
R621, R622, R623, R626(0ohm/1005).

DISMOUNT follwoing resistors
R225, R226, R227, R228, R233, R234, R235(0ohm/1005)
R625(0ohm/1005) for PRESETn_18
and MOUNT following resistors.
R617, R619, R620, R618, R627, R628, R629(0ohm/1005)

and MOUNT following resistors.
R224(47k/1608) to prevent eMMC's CLK-pin floating.
R624(47k/1608) to prevent eMMC's RST_n-pin floatting.

[Candidate of Part Number]
(1) samsung, KLMBG4GESD-B031
(2) micron, MTFC16GAKAECN-AIT
(3) smi, under development.

D3.3V — C349 0.1uF 1005 10V — C351 0.1uF 1005 10V — C354 2.2uF 1608 10V

D3.3V — C352 0.1uF 1005 10V — C350 0.1uF 1005 10V — C353 2.2uF 1608 10V

eMMC_VCCQ — C355 0.1uF 1005 10V — C356 0.1uF 1005 10V — C357 2.2uF 1608 10V

eMMC_VCCQ — C358 0.1uF 1005 10V — C359 0.1uF 1005 10V — C360 2.2uF 1608 10V

eMMC_VCCQ — C361 0.1uF 1005 10V — C362 2.2uF 1608 10V

U22B
KLMBG4GESD-B031

NC

A1	NC_1	NC_66	K1		
A2	NC_2	NC_67	K2		
A3	NC_3	NC_68	K3		
A9	NC_4	NC_69	K12		
A10	NC_5	NC_70	K13		
A11	NC_6	NC_71	K14		
A12	NC_7				
A13	NC_8	NC_72	L1		
A14	NC_9	NC_73	L2		
		NC_74	L3		
B1	NC_10	NC_75	L12		
B2	NC_11	NC_76	L13		
B8	NC_12	NC_77	L14		
B9	NC_13				
B10	NC_14	NC_78	M1		
B11	NC_15	NC_79	M2		
B12	NC_16	NC_80	M3		
B13	NC_17	NC_81	M7		
B14	NC_18	NC_82	M8		
		NC_83	M9		
C1	NC_19	NC_84	M10		
C2	NC_20	NC_85	M11		
C5	NC_21	NC_86	M12		
C7	NC_22	NC_87	M13		
C8	NC_23	NC_88	M14		
C9	NC_24				
C10	NC_25	NC_89	N1		
C11	NC_26	NC_90	N3		
C12	NC_27	NC_91	N6		
C13	NC_28	NC_92	N7		
C14	NC_29	NC_93	N8		
		NC_94	N9		
D1	NC_30	NC_95	N10		
D2	NC_31	NC_96	N11		
D3	NC_32	NC_97	N12		
D4	NC_33	NC_98	N13		
D12	NC_34	NC_99	N14		
D13	NC_35				
D14	NC_36	NC_100	P1		
		NC_101	P2		
E1		NC_102	P8		
E2	NC_37	NC_103	P9		
E3	NC_38	NC_104	P11		
E12	NC_39	NC_105	P12		
E13	NC_40	NC_106	P13		
E14	NC_41	NC_107	P14		
	NC_42				

RFU

F1			
F2	NC_43	RFU_1	A7
F3	NC_44	RFU_2	E5
F12	NC_45	RFU_3	E8
F13	NC_46	RFU_4	G3
F14	NC_47	RFU_5	G10
	NC_48	RFU_6	K6
G1		RFU_7	K7
G2	NC_49	RFU_8	K10
G12	NC_50	RFU_9	P7
G13	NC_51	RFU_10	P10
G14	NC_52		
	NC_53		

VSF

H1			
H2	NC_54	VSF_1	E9
H3	NC_55	VSF_2	E10
H12	NC_56	VSF_3	F10
H13	NC_57		
H14	NC_58		
	NC_59		
J1			
J2	NC_60		
J3	NC_61		
J12	NC_62		
J13	NC_63		
J14	NC_64		
	NC_65		

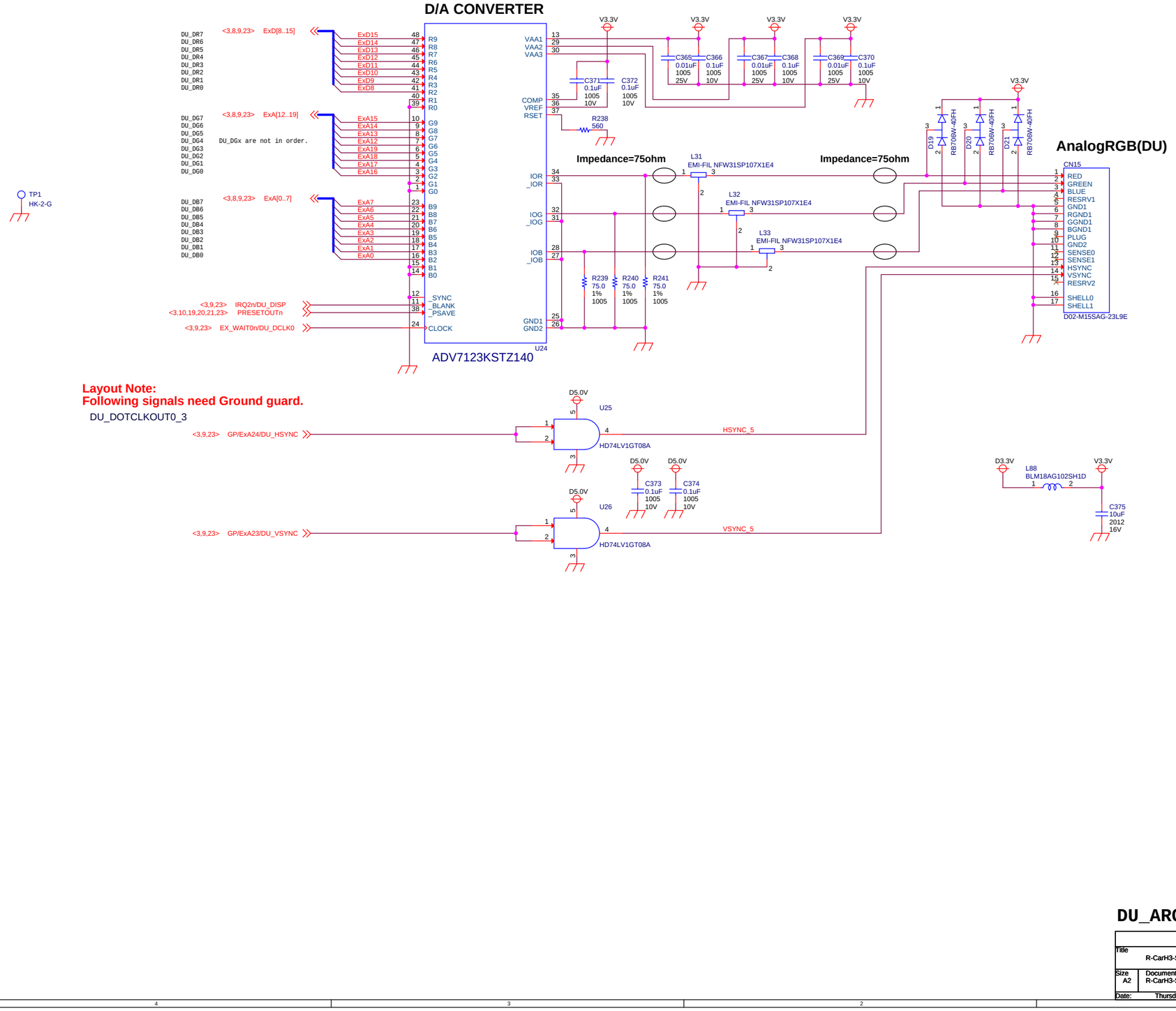
MMC0

15

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 15 of 25	

CONFIDENTIAL

Preliminary



CONFIDENTIAL

DU_ARGB

16

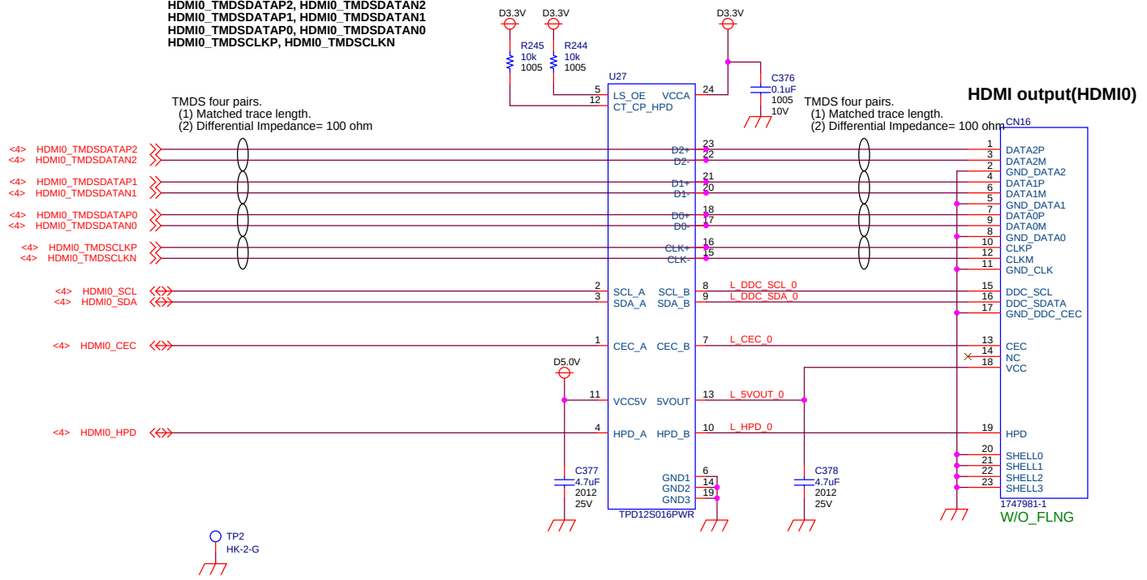
Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.20
Date: Thursday, May 28, 2015	Sheet 16 of 25	

Preliminary

Layout Note:

Matched trace length from SoC until CN16
HDMI0_TMDSDATAP2, HDMI0_TMDSDATAN2
HDMI0_TMDSDATAP1, HDMI0_TMDSDATAN1
HDMI0_TMDSDATAP0, HDMI0_TMDSDATAN0
HDMI0_TMDSCLKP, HDMI0_TMDSCLKN

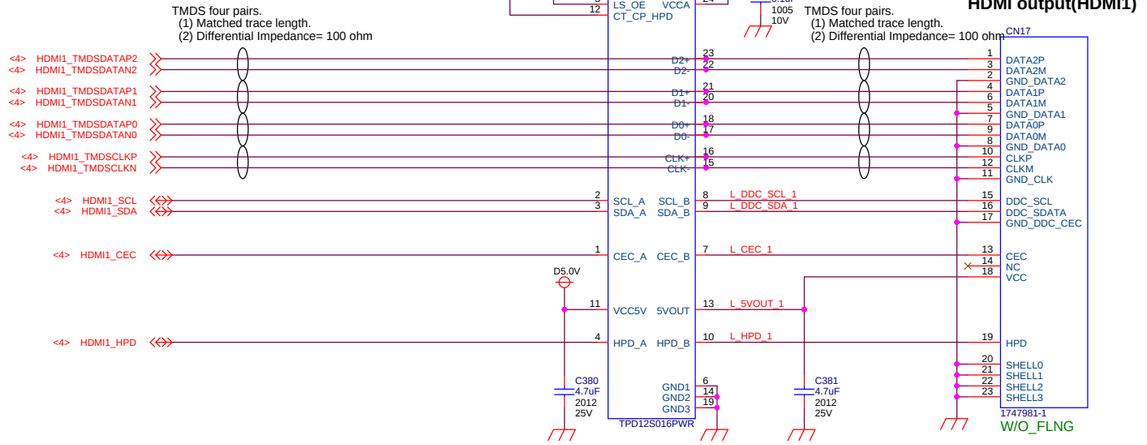
HDMI COMPANION CHIP
WITH ESD PROTECTION, I2C LEVEL SHIFTER



Layout Note:

Matched trace length from SoC until CN17
HDMI1_TMDSDATAP2, HDMI1_TMDSDATAN2
HDMI1_TMDSDATAP1, HDMI1_TMDSDATAN1
HDMI1_TMDSDATAP0, HDMI1_TMDSDATAN0
HDMI1_TMDSCLKP, HDMI1_TMDSCLKN

HDMI COMPANION CHIP
WITH ESD PROTECTION, I2C LEVEL SHIFTER



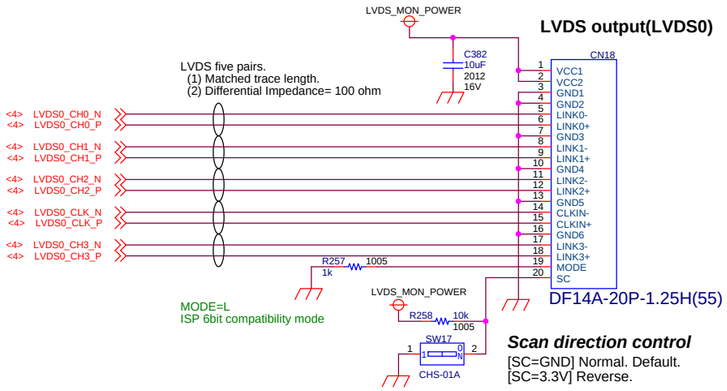
CONFIDENTIAL

HDMI_OUT

17

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 17 of 25	

Preliminary

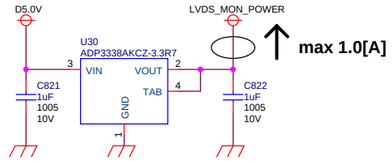


LVDS output(LVDS0)

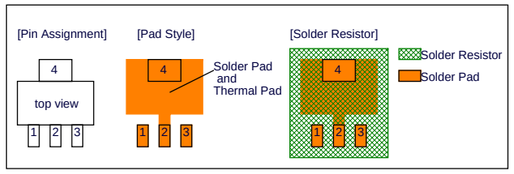
Scan direction control

[SC=GND] Normal. Default.
[SC=3.3V] Reverse.

3.3V for LVDS Monitor Power



Layout Note: Pad Configuration for ADP3338



Backlight Connector (Top Layer)

VR2 (Top Layer)

GP2_07 / PWM1 / A21	VOUTA of LTC2644	Brightness
Low Level	0.0V	max
High Level	2.5V	min
PWM	(tPWH / tPERIOD) x 2.5V	variable

CONFIDENTIAL

LVDS0

18

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 18 of 25	

Preliminary

VIDEO DECODER FOR MIPI CSI-2 (channel 0, channel 1)

Layout Note:
Connect the shell of 1747981-1 with ground.
The 1747981-1 has four through holes.

HDMI Input Connector TYPE A(Standard)

CN20 — 1747981-1 — Place at Top layer.

Layout Note:
Connect INx with OUTx under the RCLAMP0524. See below figure.

Pin1,4 Pin10,7 Pin2,5 Pin9,6

TMDS four pairs Differential Impedance 100ohm +-10% Matched trace length.

Note: ESD Protection diode array.

D22, D23, D25 — RCLAMP0524PATCT

HDMI_A_5V — C388 0.1uF 1005 10V

HPA_A — R632 1k 1005

DDCA_SDA, DDCA_SCL, CEC_A

TP3 HK-2-G

R266 100k 1005

TMDS four pairs Differential Impedance 100ohm +-10% Matched trace length.

U31 ADV7482WBBCZ

RXA_CN, RXA_CP, RXA_0N, RXA_0P, RXA_1N, RXA_1P, RXA_2N, RXA_2P, HPA_A, HDMI_CEC, DDCA_SDA, DDCA_SCL → DDC_SDA, DDC_SCL

Differential Impedance 100ohm +-10% Matched trace length from ADV7482 to R-CarH3-SiP ADV_CSI0_xxxx + CSI0_xxxx

CLKAN, CLKAP, DA0N, DA0P, DA1N, DA1P, DA2N, DA2P, DA3N, DA3P → ADV_CSI0_CLKN, ADV_CSI0_CLKP, ADV_CSI0_DATAN0, ADV_CSI0_DATAP0, ADV_CSI0_DATAN1, ADV_CSI0_DATAP1, ADV_CSI0_DATAN2, ADV_CSI0_DATAP2, ADV_CSI0_DATAN3, ADV_CSI0_DATAP3 <23>

Differential Impedance 100ohm +-10% Matched trace length from ADV7482 to R-CarH3-SiP ADV_CSI1_xxxx + CSI1_xxxx

CLKBN, CLKBP, DB0N, DB0P → ADV_CSI1_CLKN, ADV_CSI1_CLKP, ADV_CSI1_DATAN0, ADV_CSI1_DATAP0 <23>

HPD RX_5V, CEC

AIN1–AIN8, DIAG1–DIAG4

CVBS Input Connector

CN21 LPR6520-1501F — Impedance 75ohm

Layout Note:
Following signals need Ground guard.
CVBS_AIN8(CN21 to U31-pinC10)

CVBS_AIN8 — R268 24.0 1% 1005 — C823 0.1uF 1005 10V — L_AIN8 — R269 51.0 1% 1005

X8 NX2016SA[28.63636MHz/30pF/15ppm]

XTALN — J9 L_XTALN — C390 47pF 1005 50V

XTALP — J10 L_XTALP — C397 47pF 1005 50V

Layout Note:
Following signals need Ground guard.
GP6_30/INTRQ1, GP6_31/INTRQ2

DVDDIO_D3.3V — R272 4.7k 1005, R273 4.7k 1005

[Design Note] INTRQ[2:1] are configured as open-drain at the initial state. This setting can be changed.

RESET# — H8 — PRESETOUTn <3,10,16,20,21,23>

INTRQ1 — F3 L_INTRQ1 — R635 0 1005 — GP6_30/INTRQ1 <4,23>

INTRQ2 — E3 L_INTRQ2 — R636 0 1005 — GP6_31/INTRQ2 <4,23>

SCLK — J8 — I2C4_SCL <3,10,11,23,25>

SDATA — K8 — I2C4_SDA <3,10,11,23,25>

ALSB — K9

I2C bus slave address:
ALSB==0: 0xE0 for write, 0xE1 for read.
ALSB==1: 0xE2 for write, 0xE3 for read.

I2S_MCLK — C4 — R637 0 1005 — AUDIO_CLKC <2>
I2S_SCLK — B2 — R638 0 1005 — SSI_SCK4 <2,23>
I2S_LRCLK — C3 — R639 0 1005 — SSI_WS4 <2,23>
I2S_SDATA — A2 — R640 0 1005 — SSI_SDATA4 <2,23>

[Design Note] Remove four resistors above in case of using other pin function. ADV7482W supports 8-channel TDM output mode.

LLC, P0–P7

VREFN — F8 — C753 0.1uF 1005 10V — G8 — VREFP

DVDDIO_D3.3V — R285 4.7k 1005 — TEST3 D3

TEST2 C5

TEST — G3 — R288 100k 1005

DNC A9, B6, B7, C7, D7, E7, K7

Load switch for ADV7482W

D1.8V — max 1.2[A] — D1.8V_PERI

U80 MIC94091YC6 — VIN, VOUT, GND, GND, EN, NC

C898 0.1uF 1005 10V — C899 1uF 1005 10V

<3,9,10,15,23,25> PRESETn_18

LC filters for ADV7482W

L89 BLM18AG102SH1D Rated current=400mA — D1.8V_PERI — C398 10uF 2012 16V — MVDD_A1.8V

L90 BLM18AG102SH1D Rated current=400mA — D1.8V_PERI — C401 10uF 2012 16V — CVDD_A1.8V

L91 BLM18AG102SH1D Rated current=400mA — D3.3V — C404 10uF 2012 16V — TVDD_A3.3V

L92 BLM18AG102SH1D Rated current=400mA — D1.8V_PERI — C409 10uF 2012 16V — DVDD_D1.8V

L93 BLM18AG102SH1D Rated current=400mA — D1.8V_PERI — C414 10uF 2012 16V — AVDD_A1.8V

L94 BLM18AG102SH1D Rated current=400mA — D3.3V — C418 10uF 2012 16V — DVDDIO_D3.3V

L95 BLM18AG102SH1D Rated current=400mA — D1.8V_PERI — C421 10uF 2012 16V — PVDD_A1.8V

MVDD_A1.8V — C391 C392 C393 C394 C395 C396 — B1, J3, K2 MVDD

CVDD_A1.8V — B3 CVDD — C399 C400

TVDD_A3.3V — C6 TVDD — C402 C403

DVDD_D1.8V — D4, G4 DVDD — C405 C406 C407 C408

AVDD_A1.8V — E7 AVDD — C410 C411

DVDDIO_D3.3V — H3 DVDDIO — C412 C413

PVDD_A1.8V — H9 PVDD — C416 C417

A1, A3, A10, B10, D5–D7, E4–E6, F4–F7, G5–G7, H10, K1, K10 GND

HDMI_A_5V — Do not stuff — R262 47k* — R263 47k — DDCA_SCL, DDCA_SDA

DVDDIO_D3.3V — R264 27k — D40 RB520SM-30FH

Note: RB520SM-30FH
VF(max)=0.51V@IF=100mA

CEC_A — R633 0 1005 — HDMI_CEC

Note:
CEC(Consumer Electric Control Channel)

HPA_A — R634 0 1005

HDMI_A_5V — R271 100k 1005

TR3 RE1C001UNTCL

changed from D5.0V

DVDDIO_D3.3V — TR4 RE1C001UNTCL

Note:
Shorts HPA_A to GND when board powered down.

DVDDIO_D3.3V — *changed from D5.0V* — R274 1k 1005 — LED11 SML-P11MT Yellowish-Green

HPA_A — TR5 RE1C001UNTCL

Note:
HPD A LED

CONFIDENTIAL

MIPI CSI-2_VIN

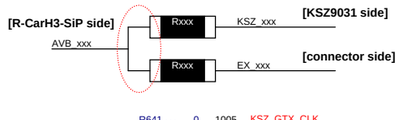
19

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)		Rev 0.20
Date: Thursday, May 28, 2015		Sheet 19 of 25	

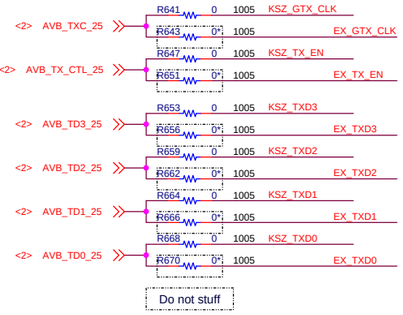
Preliminary

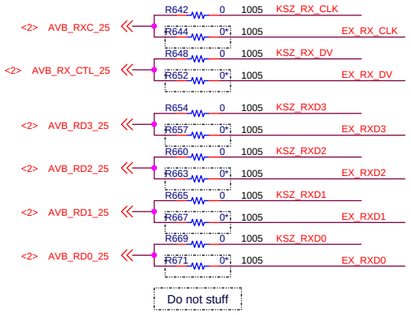
Ethernet AVB GbPHY and PHY Connector

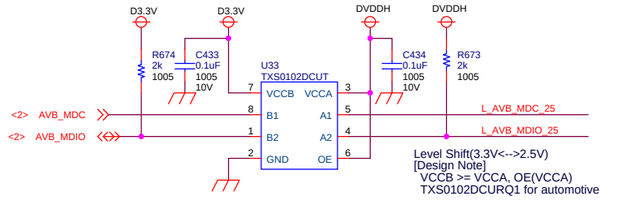
Layout Note:
As short as possible from junction of AVB_xxx to two Rxxx.

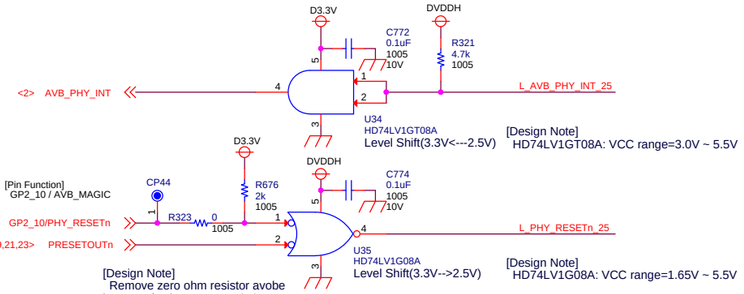


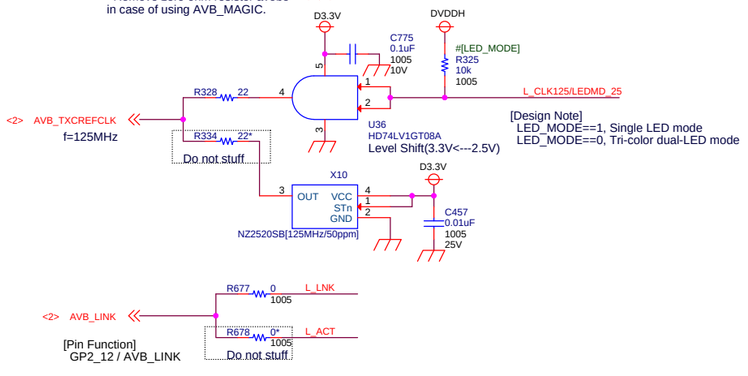
Layout Note:
Matched Trace Length from R-CarH3-Sip to KSZ9031.
(max 250Mbps/pin)
Group 1
AVB_TXC + KSZ_GTX_CLK
AVB_TX_CTL+KSZ_TX_EN
AVB_TD[3:0] + KSZ_TXD[3:0]
Group 2
AVB_RXC + KSZ_RX_CLK
AVB_RX_CTL + KSZ_RX_DV
AVB_RD[3:0] + KSZ_RXD[3:0]

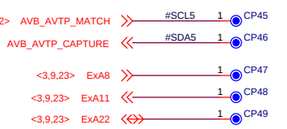






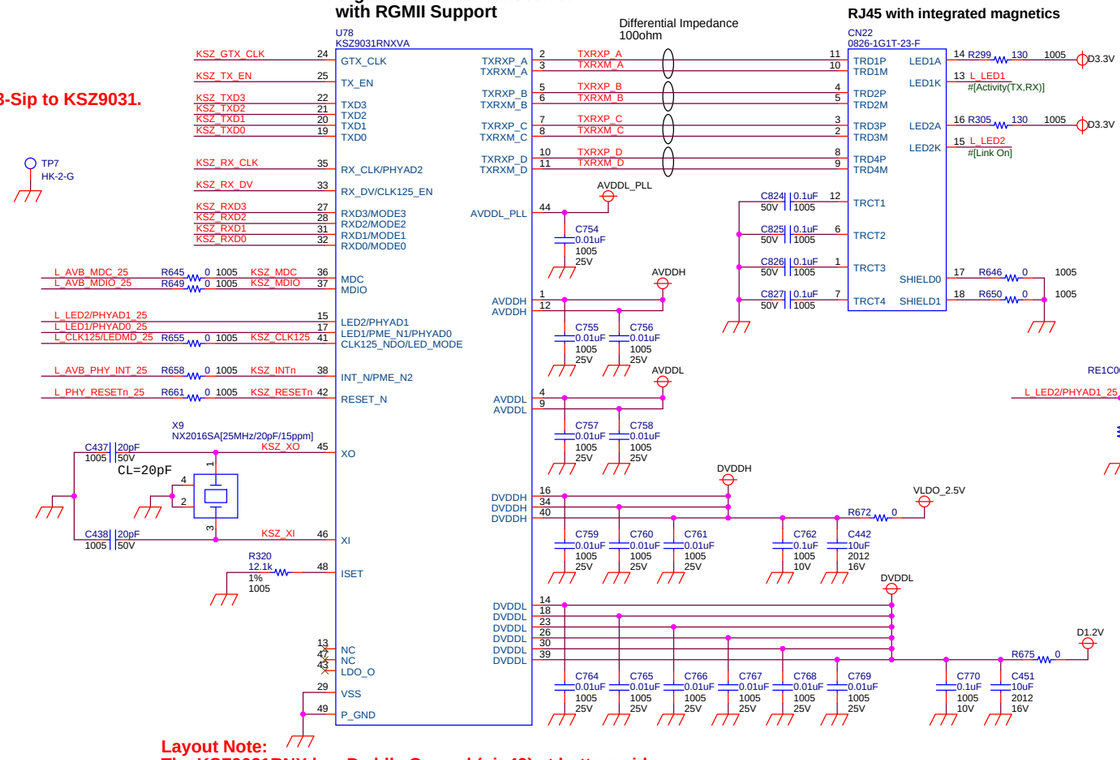






[Pin Function]
GP1_08 / A8 / [B]AVB_AVTP_MATCH
GP1_11 / A11 / [B]AVB_AVTP_CAPTURE
GP2_06 / A22 / AVB_AVTP_PPS

Gigabit Ethernet Transceiver with RGMII Support

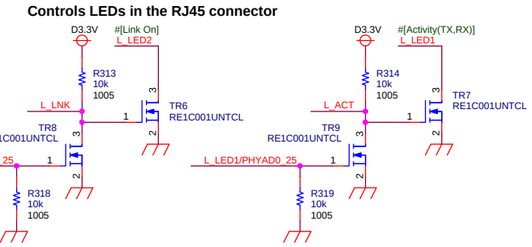


Layout Note:
The KSZ9031RNX has Paddle Ground (pin49) at bottom side.
Connect that PAD(pin 49) to the GND.

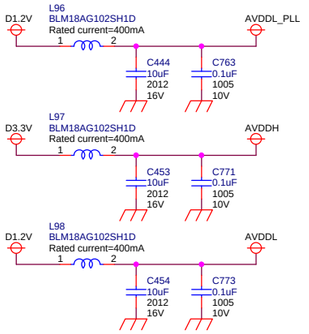
Layout Note:
Following signals need Ground guard.
AVB_TXCREFCLK, CLK125/LEDMD_25 (125MHz)
AVB_TXC_25, KSZ_GTX_CLK, EX_GTX_CLK (125MHz)
AVB_RXC_25, KSZ_RX_CLK, EX_RX_CLK (125MHz)

Following pin has pull-down resistor at the initial state.
[2.5V-I/O]
AVB_RX_CTL, AVB_RXC, AVB_RD[3:0]
AVB_TX_CTL, AVB_TXC, AVB_TD[3:0]
[3.3V-I/O]
AVB_TXCREFCLK, AVB_MAGIC, AVB_PHY_INT, AVB_LINK

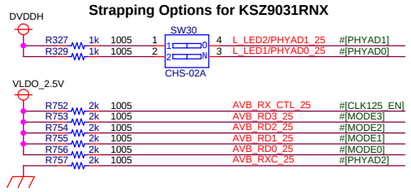
Controls LEDs in the RJ45 connector



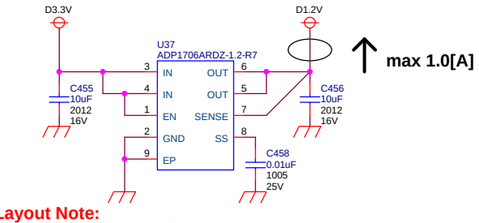
LC filters for KSZ9031RNX



Strapping Options for KSZ9031RNX

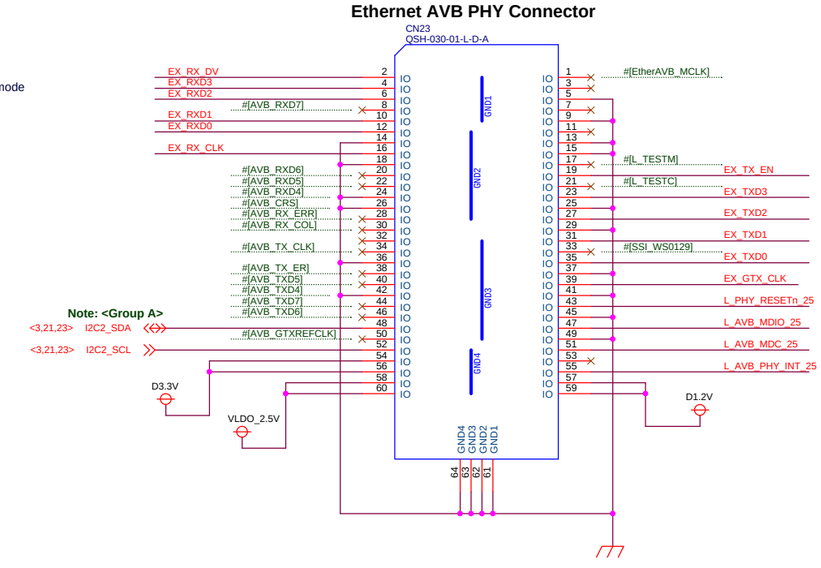


Local Regulator for KSZ9031RNX, PHY Connector



Layout Note:
The ADP1706 has EXPOSED PAD(pin9) at bottom side.
Connect that EXPOSED PAD(pin 9) to the GND.

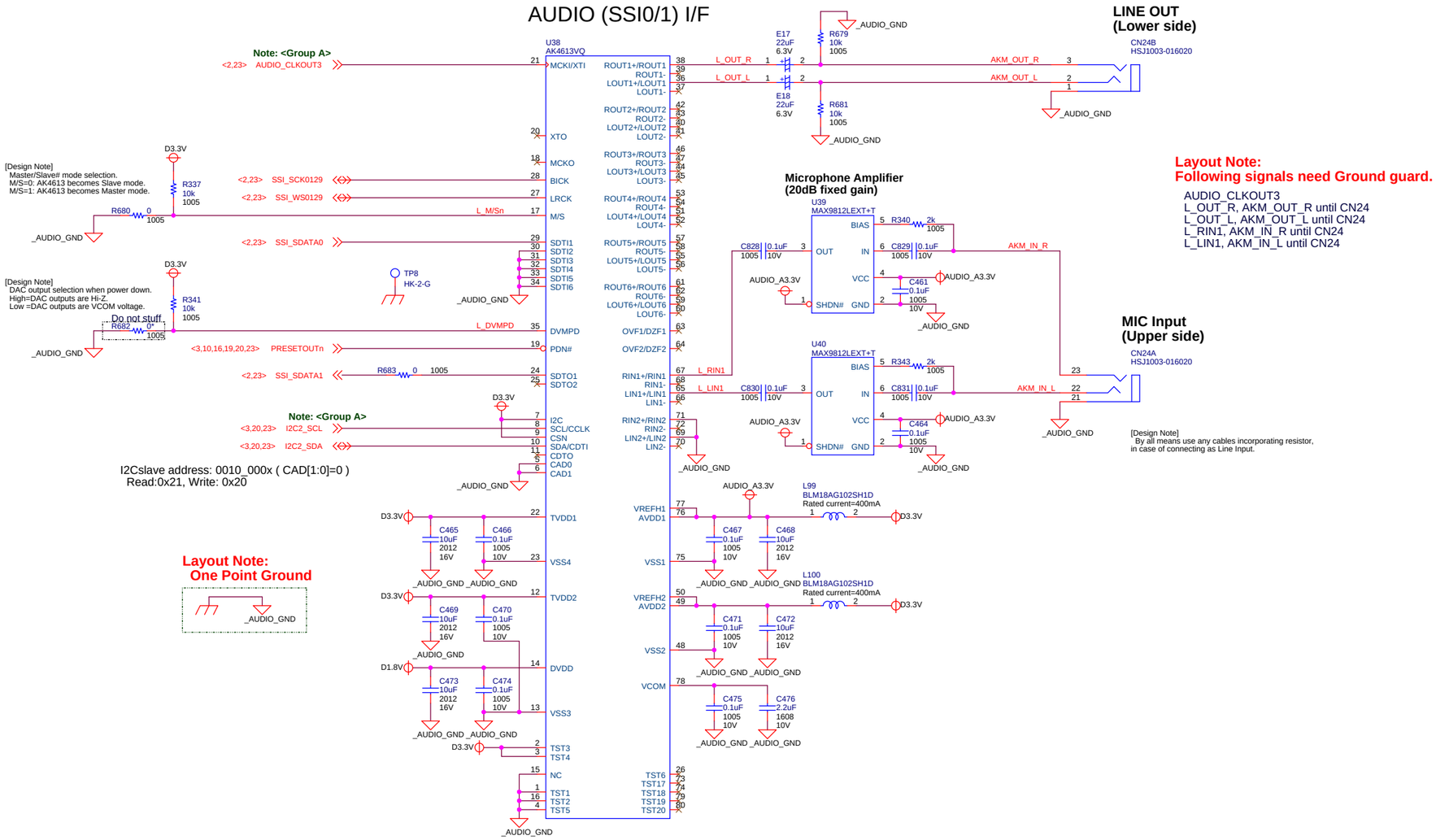
Ethernet AVB PHY Connector



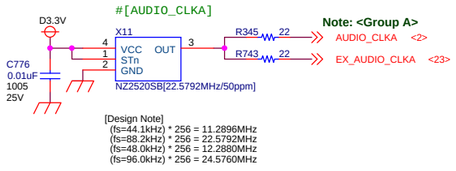
Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 20 of 25	

Preliminary

AUDIO (SSI0/1) I/F



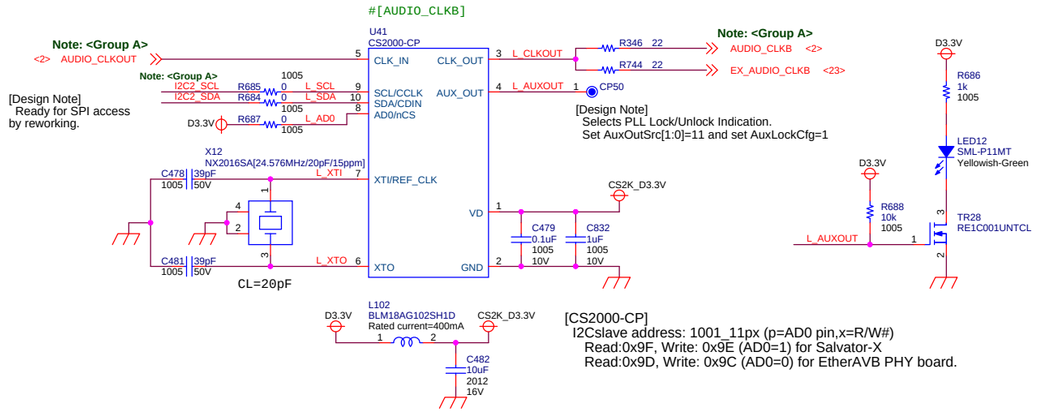
Audio Clock for 44.1kHz, 88.2kHz



Layout Note:
Following signals need Ground guard.

AUDIO_CLKA until X11-pin3
AUDIO_CLKB until U41-pin3
AUDIO_CLKOUT
EX_AUDIO_CLKA until X11-pin3
EX_AUDIO_CLKB until U41-pin3

Audio Clock for 48kHz, 96kHz, and for EtherAVB



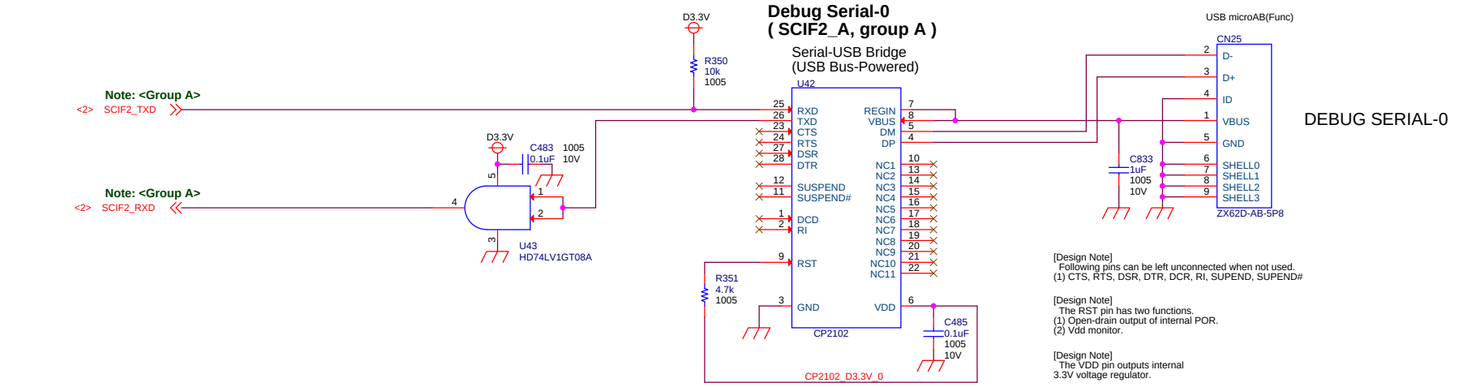
CONFIDENTIAL

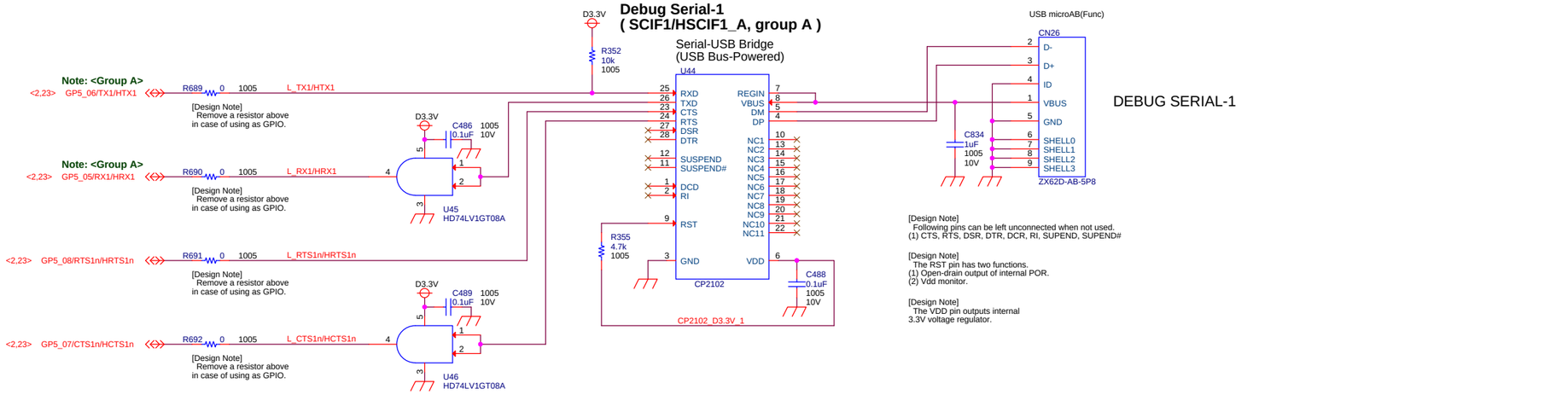
AUDIO(AK4613VQ)

21

Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.20
Date: Thursday, May 28, 2015	Sheet 21 of 25	

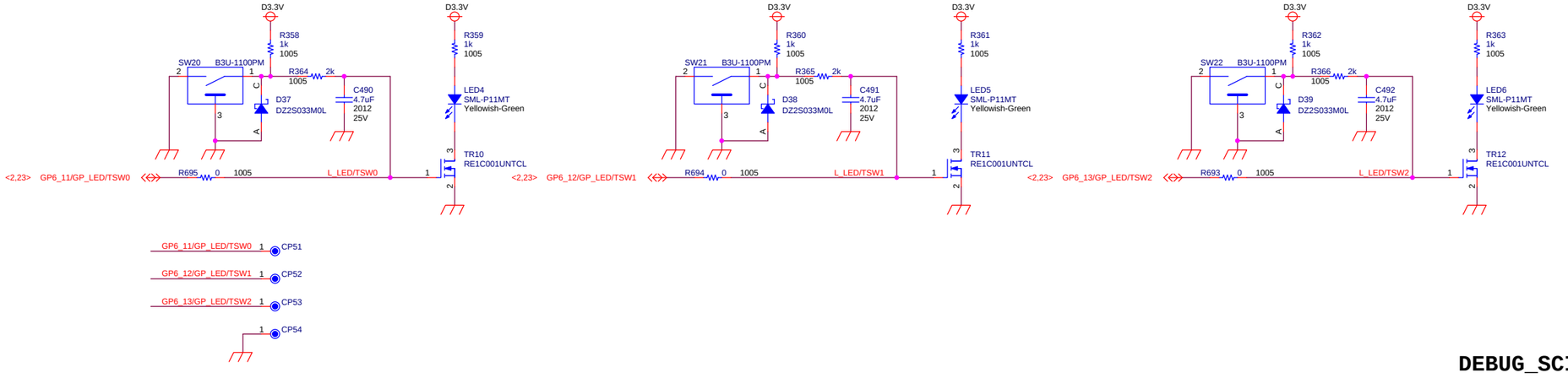
Preliminary





GPLED / Tact Switch

General Purpose LEDs or Tactile Switches
Following LEDs and Switches are connected to GPIO of R-CarH3-SiP



CONFIDENTIAL

DEBUG_SCIF/LED/TactSW 22

Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.20
Date: Thursday, May 28, 2015	Sheet 22 of 25	

Preliminary

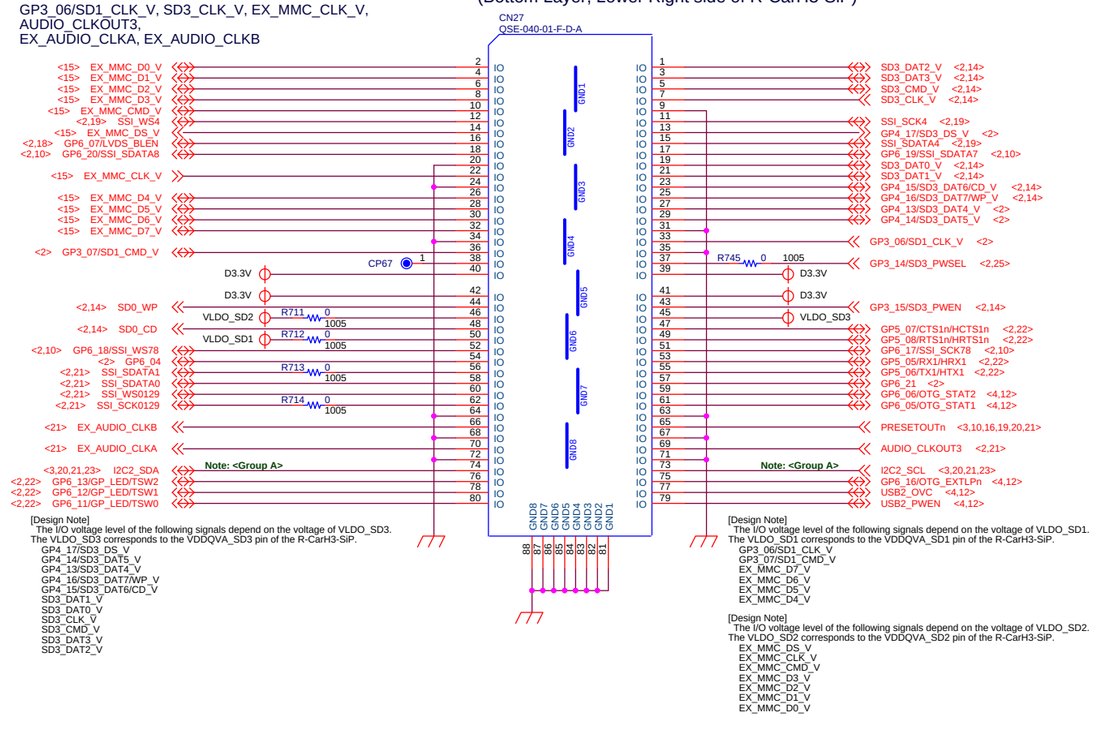
EXIO Connector A: BT/WLAN connector.
EXIO Connector B: SSI connector.
EXIO Connector C: MIPI CSI-2 connector.
EXIO Connector D: LBSC connector (Not for NOR Flash board)

Layout Note:
Following signals need Ground guard.

GP3_06/SD1_CLK_V, SD3_CLK_V, EX_MMC_CLK_V, AUDIO_CLKOUT3, EX_AUDIO_CLKA, EX_AUDIO_CLKB

#[EXIO_B]

EXIO Connector B (SSI)
(Bottom Layer, Lower Right side of R-CarH3-SiP)



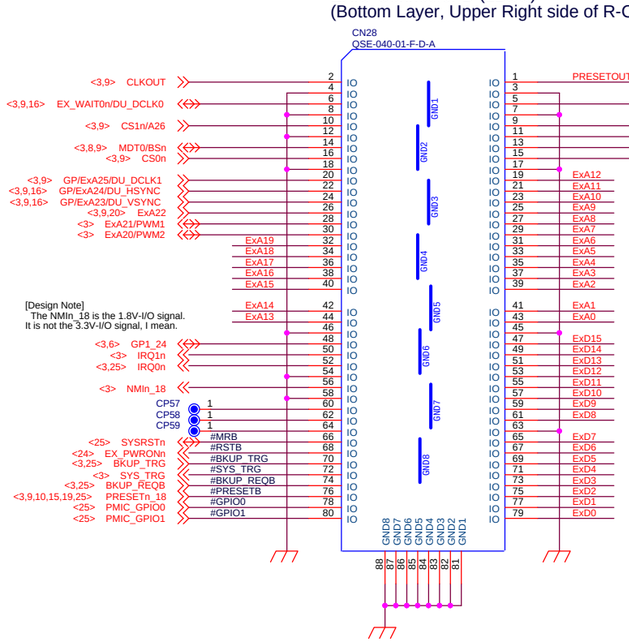
[Design Note]
The I/O voltage level of the following signals depend on the voltage of VLDO_SD3.
The VLDO_SD3 corresponds to the VDDQVA_SD3 pin of the R-CarH3-SiP.
GP4_17/SD3_DS_V
GP4_14/SD3_DAT5_V
GP4_13/SD3_DAT4_V
GP4_16/SD3_DAT7/WP_V
GP4_15/SD3_DAT6/CD_V
SD3_DAT1_V
SD3_DAT0_V
SD3_CLK_V
SD3_CMD_V
SD3_DAT3_V
SD3_DAT2_V

[Design Note]
The I/O voltage level of the following signals depend on the voltage of VLDO_SD1.
The VLDO_SD1 corresponds to the VDDQVA_SD1 pin of the R-CarH3-SiP.
GP3_06/SD1_CLK_V
GP3_07/SD1_CMD_V
EX_MMC_D7_V
EX_MMC_D6_V
EX_MMC_DS_V
EX_MMC_D4_V

[Design Note]
The I/O voltage level of the following signals depend on the voltage of VLDO_SD2.
The VLDO_SD2 corresponds to the VDDQVA_SD2 pin of the R-CarH3-SiP.
EX_MMC_DS_V
EX_MMC_CLK_V
EX_MMC_CMD_V
EX_MMC_D3_V
EX_MMC_D2_V
EX_MMC_D1_V
EX_MMC_D0_V

#[EXIO_D]

EXIO Connector D (LBSC)
(Bottom Layer, Upper Right side of R-CarH3-SiP)



Layout Note:
Following signals need Ground guard.

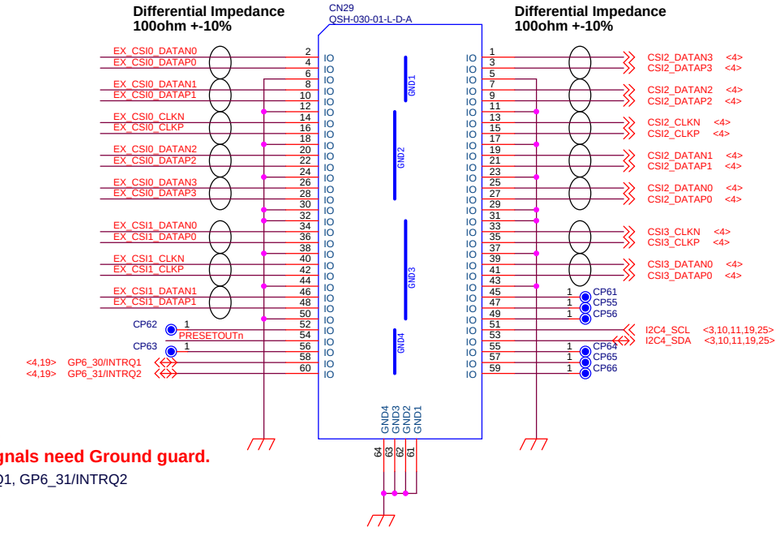
CLKOUT, EX_WAIT0n/DU_DCLK0(VI4_CLK), CS1n/A26(VI5_CLK)
WE0n(CAN_CLK)

<3,8,9,16,20> ExA[0..19]
ExA19 ExA18 ExA17 ExA16 ExA15 ExA14 ExA13 ExA12 ExA11 ExA10 ExA9 ExA8 ExA7 ExA6 ExA5 ExA4 ExA3 ExA2 ExA1 ExA0

<3,8,9,16> ExD[0..15]
ExD15 ExD14 ExD13 ExD12 ExD11 ExD10 ExD9 ExD8 ExD7 ExD6 ExD5 ExD4 ExD3 ExD2 ExD1 ExD0

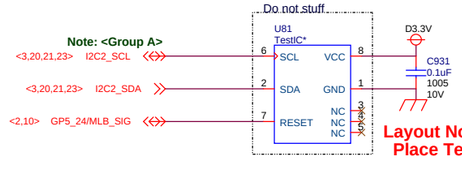
#[EXIO_C]

EXIO Connector C (MIPI CSI-2)
(Bottom Layer, Upper Left side of R-CarH3-SiP)



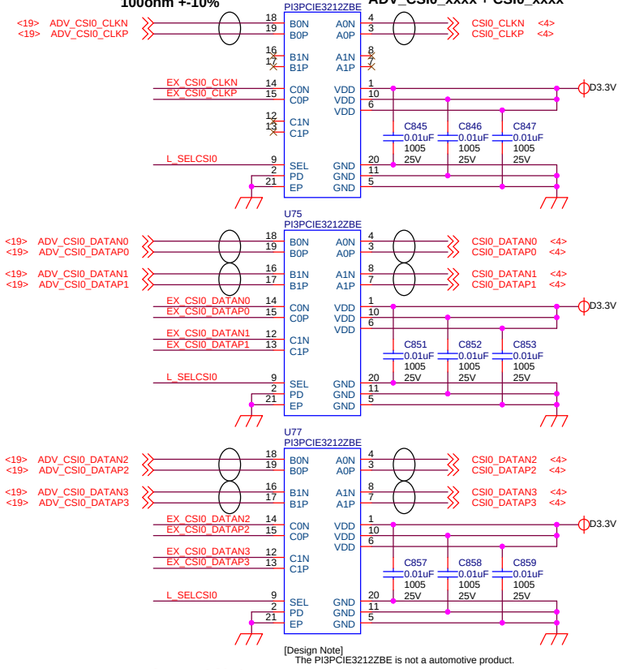
Layout Note:
Following signals need Ground guard.

GP6_30/INTRQ1, GP6_31/INTRQ2



Layout Note:
Place TestIC at bottom layer

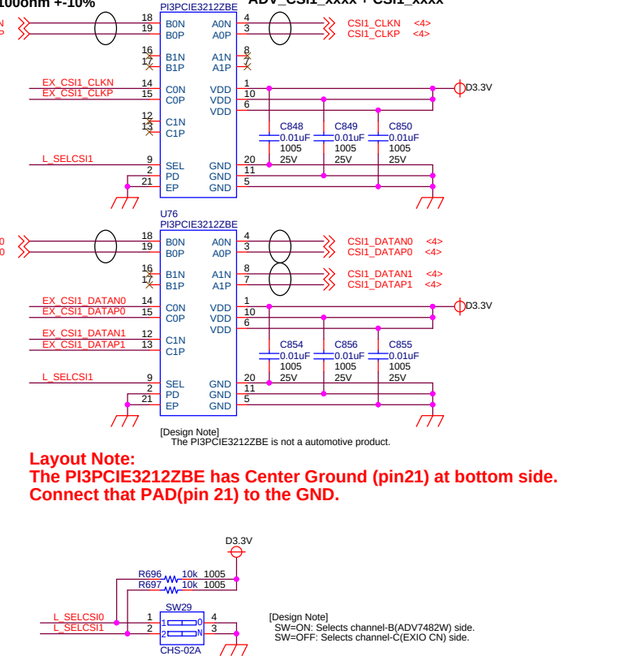
Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI0_xxxx + CSI0_xxxx



[Design Note]
The PI3PCIE3212ZBE is not a automotive product.

Layout Note:
The PI3PCIE3212ZBE has Center Ground (pin21) at bottom side.
Connect that PAD(pin 21) to the GND.

Differential Impedance
100ohm +-10%
Matched trace length from ADV7482 to R-CarH3-SiP
ADV_CSI1_xxxx + CSI1_xxxx



[Design Note]
The PI3PCIE3212ZBE is not a automotive product.

Layout Note:
The PI3PCIE3212ZBE has Center Ground (pin21) at bottom side.
Connect that PAD(pin 21) to the GND.

[Design Note]
SW=ON: Selects channel-B(ADV7482W) side.
SW=OFF: Selects channel-C(EXIO CN) side.

CONFIDENTIAL

EXIO_CN/MIPI_SW

23

Title: R-CarH3-SiP System Evaluation Board (Salvator-X)		
Size: A2	Document Number: R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev: 0.20
Date: Thursday, May 28, 2015	Sheet 23 of 25	

Preliminary

It is impossible to supply DC5.0V and DC3.3V through CN30 and CN36.

It is prohibited to supply more than DC12.0V .

Legacy connector

CN30 53259-0429 (GND, GND, 12V, 12V)

D43 TCH20A15

Rated Current=10Ax2

Rated Current=5.5A/pin[AWG.#18]

L103 BLM18KG260TZ1 Rated current=6.0A 1608

L104 NFM31HK223R1H3 Rated Current=10A 3216

L105 BLM18KG260TZ1 Rated current=6.0A 1608

L106 NFM31HK223R1H3 Rated Current=10A 3216

L107 BLM18KG260TZ1 Rated current=6.0A 1608

max 18.0[A]

E12 470uF 25V

C493 0.1uF 50V 1005

AC Adapter

CN36 PJ-063BH

LED8,LED9 and LED14 are Yellowish Green LEDs indicate Power Good.
LED8 turns on after detecting DC12.0V.
LED9 turns on after detecting D5.0V and VSYS.
LED14 turns on during DDR Back Up.

R758 6.8k 1005 1%
R759 6.8k 1005 1%
R760 6.8k 1005 1%

VR = 1.9V
Vce = 0.3V
Ir = (12V-1.9V-0.3V)/6.8k = 1.44mA
Wr = (12V-1.9V-0.3V) * 1.44mA = 14.12mW
1005size: 63mW (max)

LED8 SML-P11MT Yellowish-Green — 12V LED
LED9 SML-P11MT Yellowish-Green — 5V LED
LED14 SML-P11MT Yellowish-Green — Back up LED

VBIAS_5.0V
R508 47k 1005
TR13 RE1C001UNTCL
TR30 RE1C001UNTCL

MAX16933_PWGD1
Power GOOD(D5.0V/VSYS)

<7,25> BKUP_CTRL_11

TH3 TH4 AGND1 PGND1

PGND1 — One Point Ground is more than "0.6mm VIA x 2" Connect each other under the Exposed Pad by Layout tool.

R466 0* 1005, R467 0* 1005 PGND1 — Extra One Point Ground. Connect each other by Layout tool. Do not Stuff.

AGND1 — One Point Ground is more than "0.6mm VIA x 2" Connect each other under the Exposed Pad by Layout tool.

R468 0* 1005, R469 0* 1005 AGND1 — Extra One Point Ground. Connect each other by Layout tool. Do not Stuff.

For EMI.

D12.0V: C901 C902 C903 C904 C905 0.1uF 1005 50V

D5.0V: C907 C906 C908 C909 C910 C911 C912 0.1uF 1005 10V

SILK:OFF (4-5 short)

SW23 SWITCH(G-12AP)

SILK:ON (4-5 open)

R370 20k 1005, TR16 RE1C001UNTCL, R387 10k 1005

R373 20k 1005, R371 10k 1005, TR22 RE1C001UNTCL, R374 10k 1005

DDR0_1.8V: R477 1k 1005, TR29 RE1C001UNTCL, R715 100k 1005

C496 4.7uF 2012 25V, C497 0.1uF 1005 50V, PGND1

VSYS — R372 1 1005 — C498 2.2uF 1608 10V — PGND1, AGND1

U47 BIAS IN EXTVCC AGND

VBIAS_5.0V — C494 6.8uF 3216 10V — PGND1

for adjusting current sense

R376 0 1005 — C506 1pF* 1005 50V (Do not stuff) — OUT1

MAX16933_CS1 — R381 0 1005 — CS1

R761 0 1005, R762 0* 1005 (Do not stuff) — EN1, FB1, PGND1

VBIAS_5.0V — for FB1 (D5.0V)

PGND1

for FB2 (VSYS=5.0V and adjusting)

C522 10pF* 1005 50V, R393 0* 1005, R472 0 1005, R398 1k* 1005 (Do not stuff)

for adjusting current sense

R390 0 1005 — C520 1pF* 1005 50V (Do not stuff) — OUT2

MAX16933_CS2 — R394 0 1005 — CS2

FB2, PGND2

PGND1 — EPAD

FSYNC, FOSC

R405 100k 1% 1005, R406 39k 1% 1005 AGND1

MAX16933

RSTBn <25>

<23> EX_PWRONn — TR31 RE1C001UNTCL — R746 10k 1005 — from EXIO board

MAX16933_PWGD1, MAX16933_PWGD2 — MAX16933_PWGD <25>

Reset can be controled by 4 signals;

Any one condition makes RESET/DDR BackUp
SW23(ACC Switch):RSTBn= Low
EXIO(SYSCON) : EX_PWRONn=High
PowerGood D5.0V: MAX16933_PWGD1=Low
PowerGood VSYS: MAX16933_PWGD2 =Low

All conditions make POWER ON
SW23(ACC Switch):RSTBn= High
EXIO(SYSCON) : EX_PWRONn=Low
PowerGood D5.0V: MAX16933_PWGD1=High
PowerGood VSYS: MAX16933_PWGD2 =High

for removing noise

U48 TPC8048-HTE12LQ

DH1, BST1, LX1, DL1

R375 0 1005, R377 0 1005, C505 0.1uF 1005 10V

VBIAS_5.0V — D41 RB520SM-30FH

D12.0V — E19 47uF 25V OSCON, C501 0.1uF 1005 50V — PGND1

U49 TPC8048-HTE12LQ

D33 B360B-13-F, C896 1uF* 1608 16V (Do not stuff)

R750 1k* 1608

DFEG10040D-1R5M L51 1.5uH 109100 14.0A

MAX16933_CS1 — R380 0.005 1% 1W 3216 — Kelvin connection

D5.0V — E20 270uF 10V OSCON, C508 47uF 3225 10V — PGND1

D5.0V trace width is 10mm (5.0V MAX 10A)

Hi-Z : Good
Low : Wrong

PGOOD1 — MAX16933_PWGD1 — R388 22.1k 1005 1%

COMP1 — C512 22pF 1005 50V — AGND1 — C513 4700pF 1005 50V — AGND1

for removing noise

U50 TPC8048-HTE12LQ

DH2, BST2, LX2, DL2

R389 0 1005, R391 0 1005, C521 0.1uF 1005 10V

VBIAS_5.0V — D42 RB520SM-30FH

D12.0V — E21 47uF 25V OSCON, C516 0.1uF 1005 50V — PGND1

U51 TPC8048-HTE12LQ

D35 B360B-13-F, C897 1uF* 1608 16V (Do not stuff)

R751 1k* 1608

DFEG10040D-1R5M L52 1.5uH 109100 14.0A

MAX16933_CS2 — R392 0.005 1% 1W 3216 — Kelvin connection

VSYS — E22 270uF 10V OSCON, C524 47uF 3225 10V — PGND1

VSYS trace width is 10mm (5.0V MAX 10A)

Hi-Z : Good
Low : Wrong

PGOOD2 — MAX16933_PWGD2 — R401 14k 1005 1%

COMP2 — C528 33pF 1005 50V — AGND1 — C529 4700pF 1005 50V — AGND1

C508/C524 : Automotive type is available soon

Power Supply Connector for I/O board.

CN32 B7B-PH-SM4-TB

D12.0V, D5.0V, VSYS, D3.3V

CN32 is ONLY for Gen3 extension board.

D12.0V trace width is 2mm
D5.0V trace width is 2mm
VSYS trace width is 2mm
D3.3V trace width is 4mm

Power Supply Connector for CPU FAN.
Place Top Layer.

D12.0V — R411 0 — D5.0V — Do not stuff. R412 0* — CN34 22-04-1031

3pin 2pin 1pin
CPU FAN Connector - Top View

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Power 5V/VSYS

24

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)	
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X)	Rev 0.20
Date: Thursday, May 28, 2015	Sheet 24 of 25	

Preliminary

RSTB
Low : Reset or DDR back-up (need to set)
High : Active (awake reset)

Reset Switch

RSTBMODE(Low=Level, Hi=Pulse)

Do not Stuff

thermistor

U70 HD74LV1GT08A

U72B BD9571MWV-M

RSTB : Internal pull-up(100k V3P3) with schmid.
MRB: Internal pull-up(100k V3P3)
SYNC : Internal pull-down(100k)
AVS0/AVS1 : Internal pull-down(100k)
BOOST :Internal pull-down(100k)
BKUP_REQB Internal pull-down(100k)

Do not stuff

Do not stuff

SW28 CHS-01A

I2Cslave address: 0110_000x
Read:0x61, Write: 0x60

I2C EEPROM for PMIC

U57 BR24T01FVM-W

I2Cslave address: 1010_000x
Read:0xA1, Write: 0xA0

[Design Note]
WP=GND means writeable.
VCC range=1.7V ~ 5.5V

Current-Sense Amplifiers with ADC for DVFS0.8V

U58 MAX9611AUB+

I2Cslave address: 1111_111x
Read:0xFF, Write: 0xFE

Current-Sense Amplifiers with ADC for VDD0.8V

U59 MAX9611AUB+

I2Cslave address: 1111_100x
Read:0xF9, Write: 0xF8

SYSTEM Reset LED

SML-P11MT LED15

TR20 RE1C001UNTCL

TR21 RE1C001UNTCL

For EMI.

For EMI.

For auxiliary power supply

TOP VIEW of BD9571MWV-M

Exposed PAD

U67 Layout Note:
BD9571MWV-M has a exposed pad at bottom side.
CONNECT to MASTER GND.

VSYS=5.0V trace width is 10mm

D5.0V trace width is 10mm

GND

One Point Ground (But number of via need to consider).
Connect each other by Layout tool.

Extra One Point Ground.
Connect each other by Layout tool.
Do not Stuff.

DVFS : DCDC controler

for Current-Sense Amplifier (U58)

DDFCUL0630-H-R12M

DVFS0.8V trace width is 16mm
(0.8V MAX 16A)
0.500V - 1.200V (25mV step)

For test circuit. Layout solder side.

FB_DVFS/REMOTE_M_DVFS Layout Note:
these are led from the neiborhood of SoC ball in pairs.

VD09: DCDC controler

for Current-Sense Amplifier (U59)

SPM3020T-R15M-LR

VDD0.8V trace width is 8mm
(0.8V MAX 8A)
0.500V - 1.200V (25mV step)

For test circuit. Layout solder side.

FB_VD09 Layout Note: this is led from the neiborhood of SoC ball.

DDR0C-DDR1C: LDO

DDR0_1.8V/DDR1_1.8V
(1.8V MAX 170mA)

DDR0: DCDC

DDR0_1.1V trace width is 4mm
(1.8V MAX 4A)

FB_DDR0 Layout Note:
The blanch point is led from the neiborhood of DDR.

DDR1: DCDC

DDR1_1.1V trace width is 4mm
(1.8V MAX 4A)

FB_DDR1 Layout Note:
The blanch point is led from the neiborhood of DDR.

VD18: DCDC

D1.8V trace width is 3mm
(1.8V MAX 3A)
1.625V - 2.000V (25mV step)

VD33: DCDC

D3.3V trace width is 3mm
(3.3V MAX 3A)
2.800V - 3.800V (100mV step)

VD25: LDO

VLDO2.5V
(2.5V MAX 300mA)
2.150V - 2.900V (50mV step)

SD0-SD3: LDO

VLDO_SD0/VLDO_SD1/VLDO_SD2/VLDO_SD3
(1.8V/3.3V MAX 170mA)

C540/C542 : Automotive type is available soon

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Power PMIC

25

Title	R-CarH3-SiP System Evaluation Board (Salvator-X)
Size A2	Document Number R-CarH3-SiP System Evaluation Board (Salvator-X) Rev 0.20
Date: Thursday, May 28, 2015	Sheet 25 of 25