Firmware Update for NIM EASIROC Module

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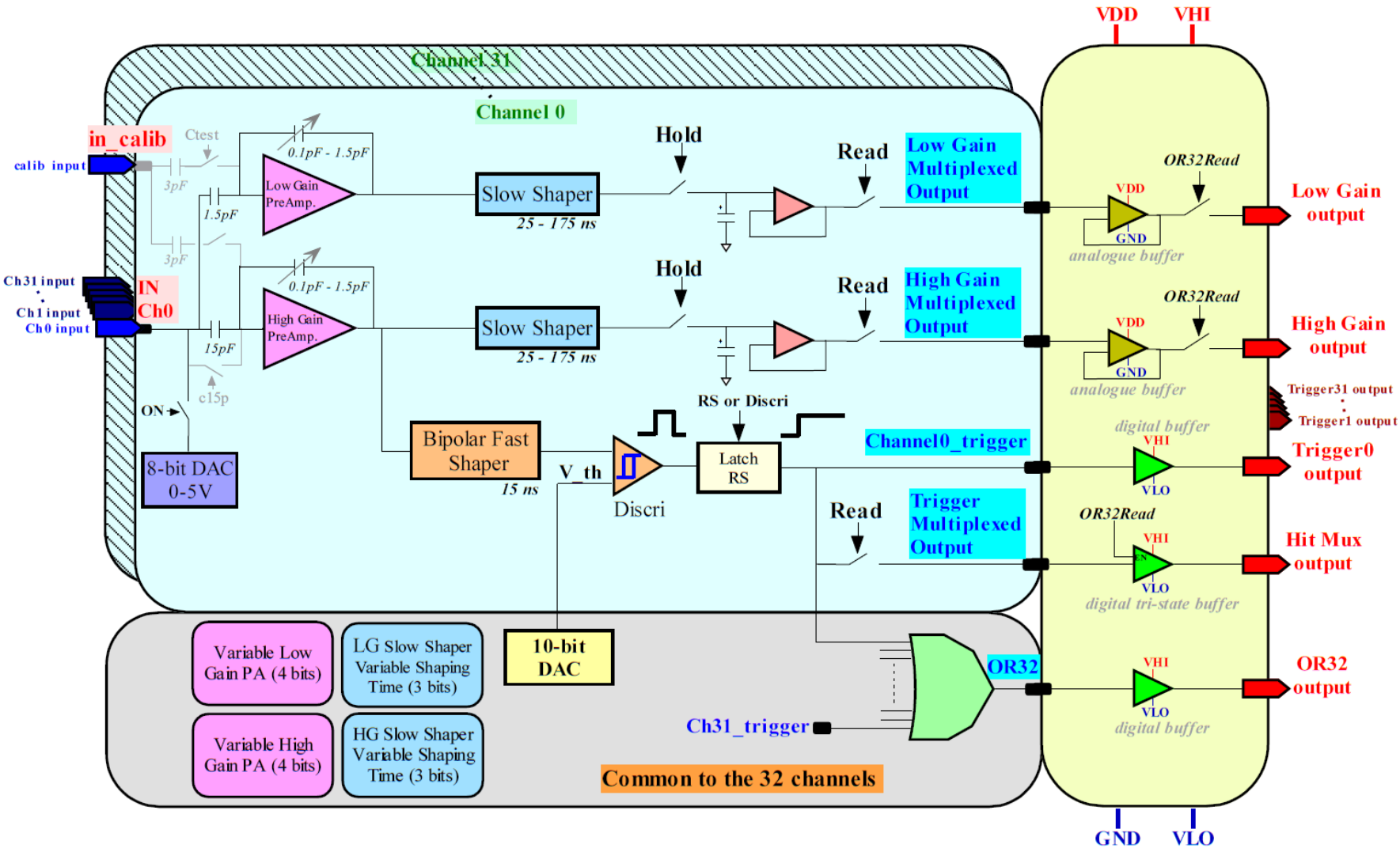

Fig. 1 EASIROC schematic.[1]

Register Name	bits	Register description	Default Value
EN_input_dac	1	Enable 32 input 8-bit DACs	1 (DACs ON)
8-bit DAC reference	1	8-bit input DAC Voltage Reference (1 = external 4,5V , 0 = internal 2,5V)	1 (External Ref)
Input 8-bit DAC	288	Input 8-bit DAC Data from channel 0 to 31 – (DAC0…DAC7 + DAC OFF)	32 x 0000 0000 0
Low Gain PA bias	1	Low Gain PreAmp bias (weak bias = 1 , high bias = 0)	1 (weak bias)
High Gain PreAmplifier PP	1	Disable High Gain preamp power pulsing mode (force ON)	1 (PA ON)
EN_High_Gain_PA	1	Enable High Gain preamp	1 (PA Enabled)
Low Gain PreAmplifier PP	1	Disable Low Gain preamp power pulsing mode (force ON)	1 (PA ON)
EN_Low_Gain_PA	1	Enable Low Gain preamp	1 (PA Enabled)
Capacitor HG PA Comp	4	High gain preamp compensation capacitances commands (0…3)	0000
Capacitor HG PA Fdbck	4	High gain preamp feedback capacitances commands (0…3) [active low]	0000
Capacitor LG PA Fdbck	4	Low gain preamp feedback capacitances commands (3…0) [active low]	0000
Capacitor LG PA Comp	4	Low gain preamp compensation capacitances commands (3…0)	0000
DisablePA & In_calib_EN	64	Disable charge preamp + Enable calibration capacitor (from channel 0 to 31)	32 x 00
Low Gain Slow Shaper PP	1	Disable low gain slow shaper power pulsing mode (force ON)	1 (SS ON)
EN_Low_Gain_Slow Shaper	1	Enable Low Gain Slow Shaper	1 (SS Enabled)
Time Constant LG Shaper	3	Low gain shaper time constant commands (2…0)	000
High Gain Slow Shaper PP	1	Disable high gain slow shaper power pulsing mode (force ON)	1 (SS ON)
EN_High_Gain_Slow Shaper	1	Enable high gain Slow Shaper	1 (SS Enabled)
Time Constant HG Shaper	3	High gain shaper time constant commands (2…0)	000
Fast Shapers Follower PP	1	Disable fast shaper follower power pulsing mode (force ON)	1 (FSb follower ON)
EN_Fast Shaper	1	Enable fast shaper	1 (FSb Enabled)
Fast Shaper PP	1	Disable fast shaper power pulsing mode (force ON)	1 (FSb ON)
T&H (Widlar SCA) PP	1	Disable Track & Hold power pulsing mode (force ON)	1 (T&H ON)
EN_T&H (Widlar SCA)	1	Enable Track & Hold	1 (T&H Enabled)
T&H bias(Widlar)	1	Track & Hold bias (weak bias = 1 , high bias = 0)	1 (weak bias)
EN_discri	1	Enable Discriminator	1 (Discri Enabled)
Discriminator PP	1	Disable trigger discriminator power pulsing mode (force ON)	1 (Discri ON)
RS_or_discri	1	Select latched (RS : 1) or direct output (trigger : 0)	1 (RS)
Discriminator Mask	32	Allows to Mask Discriminator (channel 0 to 31) [active low]	32 x 1 (no mask)
DAC code	10	10-bit DAC (LSB-MSB)	00 0000 0000
DAC slope	1	DAC slope (fine = 1 , coarse = 0)	1 (fine)
DAC PP	1	Disable DAC power pulsing mode (force ON)	1 (DAC ON)
EN_DAC	1	Enable DAC	1 (DAC Enabled)
BandGap PP	1	Disable BandGap power pulsing mode (force ON)	1 (BandGap ON)
EN_BandGap	1	Enable BandGap	1 (BandGap Enabled)
High Gain OTAq PP	1	Disable High Gain OTA power pulsing mode (force ON)	0
Low Gain OTAq PP	1	Disable Low Gain OTA power pulsing mode (force ON)	0
Probe OTAq PP	1	Disable Probe OTA power pulsing mode (force ON)	0
LVDS receivers PP	1	Disable LVDS receivers power pulsing mode (force ON)	0
EN_High Gain OTAq	1	Enable High Gain OTA	0 (HG path Disabled)
EN_Low Gain OTAq	1	Enable Low Gain OTA	0 (LG path Disabled)
EN_Probe OTAq	1	Enable Probe OTA	0 (Probe Disabled)
EN_LVDS receivers	1	Enable LVDS receivers	0 (LVDS rec Disabled)
EN_out_dig	1	Enable digital multiplexed output (Hit mux out)	0 (digital out disabled)
EN_OR32	1	Enable digital OR32 output [active low]	0 (OR32 enabled)
EN_32 triggers	1	Enable 32 channels triggers outputs [active low]	0 (Triggers enabled)
NC	4		0000
TOTAL	**456**		

Fig. 2 Slow control parameters.[1]

2 NIM EASIROC Module

The NIM EASIROC module has been developed by KEK and Open-It for the purpose of ....

2.1 EASIROC chips

Two EASIROCs are mounted on the board, so that 64 channels of MPPC are able to be measured in total. Outputs from the EASIROCs' slow shaper are connected to four ADCs, and then transferred to an FPGA. Discriminators' outputs from EASIROC are directly connected to the FPGA, and to LVDS outputs on the back-panel.

2.2 FPGA

An FPGA is used to control signals from EASRIOC and from/to front-panel inputs/outputs, that is a product of Xilinx, Artix-7 series; XC7A100T-2FGG676C.

2.3 Interface

On the front-panel are 6 digital signal inputs, 5 digital outputs, and 5 analog outputs. Also, there are 64 channels inputs for MPPC and an Ethernet connector for data acquisition and other firmware controls. On the back-panel are LVDS outputs for each MPPC channel, +6V AC power supply, and NIM power supply.

2.3.1 Digital inputs

2.3.2 Digital outputs

2.3.3 Analog outputs

2.4 LED

There are four LEDs on the front-panel (Dialight 568-0721-111), flashing with double colors, green or red. They are able to be controlled in the firmware, and still be adjustable and optimized.

2.5 Jumper pins

Three jumper pins are on the board.

- JP1 ...
- JP2 ...
- JP3 ...

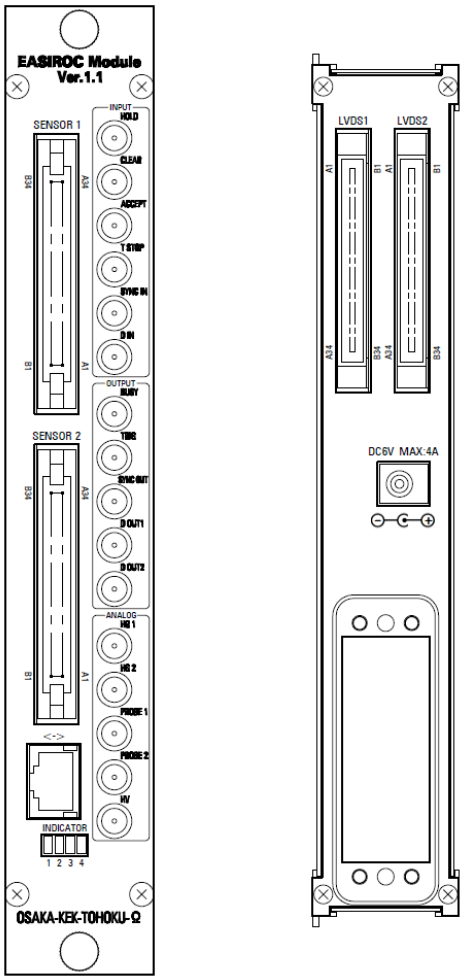

Fig. 3 The front and back overview of NIM EASIROC Module.

3 Firmware

3.1 Inherited functions from VME EASIROC module

Many functions were already implemented in the VME EASIROC module's firmware [5], such as controlling data acquisition, "slow control", and the trigger manager.

3.1.1 ADC

This module controls pedestal suppressions, too.

3.1.2 Multi-hit TDC

3.1.3 Scaler

1. Scalar timer

3.1.4 Clock manager

Using the external 50 MHz clock signal, clock signals with different frequencies to be used in the firmware;

- 3 MHz, used for controlling AD9220.
- 6 MHz, used for "slow control" and ADC module.
- 25 MHz, used for SiTCP.
- 66 MHz, used for controlling SPI FLASH memory.
- 125 MHz, used for TDC operation and Scaler.
- 250 MHz, with different phases of 0°, 90°, 180° and 270°, used for TDC sampling.

3.1.5 Reset manager

3.1.6 Trigger manager

Trigger manger module receives front-panel signals such as "HOLD", "CLEAR", "ACCEPT", and "T STOP", and distributes trigger, busy, or clear signals for other modules. As receiving "HOLD" signal, it sends trigger signals for EASIROC to hold the electric charge of the slow shaper. "CLEAR" signal leads to fast clear signals for other firmware modules. Receiving "ACCEPT" signal, a trigger is sent to global gather module and data transmit via SiTCP is started. "T STOP" signal corresponds to the common stop for TDC and scaler. While data acquisition, "HOLD", "T STOP", and "ACCEPT" signals have to be sent to the NIM EASIROC module in this oder for each event. The timing difference between "HOLD" and "ACCEPT" must be larger than 2 μs to wait for all the ADC values are stored in the firmware.

3.1.7 Discriminator's OR signal

3.1.8 SiTCP

1. SiTCP library
2. RBCP distributor

3.1.9 "Slow control"

3.1.10 Direct control

Hold signal (pin: holdb), reset of PreAmp charge (pin: reset_pa), reset of latched trigger if used (pin: raz_chn), and acquisition window (pin: val_evt) are controlled by this module. Besides, power pulsing mode (pin: pwr_on), register selection of either "probe" or "slow control" (pin: select), load of slow control (pin: load_sc), selected register reset (pin: rstb_sr), and read register reset (pin: tstb_read) are controlled.

3.1.11 Status register

Users could select the mode;

- DAQ mode ... This mode enables taking data.
- ADC on/off ... "On" mode enables taking ADC data, and "off" disables.
- TDC on/off ... "On" mode enables taking TDC data, and "off" disables.
- Scaler on/off ... "On" mode enables taking Scaler data, and "off" disables.

3.1.12 Read register

Users can select the channel whose signal after slow shaper is probed from "HG" output on the front-panel through this module as "read register."

3.1.13 Read register selector

This module selects connections of read register inputs to EASIROC (pin: clk_read, srin_read, and rstb_read). While taking data with DAQ mode, read register pins are connected to ADC module. While not taking data, that is out from DAQ mode, read register pins are connected to Global read register module.

3.1.14 Version

3.1.15 Data transfer

1. Global gatherer
2. Global sender

3.1.16 SPI FLASH programmer

3.2 Unique functions to NIM EASIROC module

3.2.1 MPPC's HV control

90 V boost DC/DC converter with APD current monitor (LT3482EUD[2]) is able to provide bias voltage to MPPCs with up to 90 V output, as being combined with a 16-bit digital-to-analog converter (DAC8411 TEXAS INSTRUMENTS[3]) which sends a reference current. The following four pins control the bias voltage;

1. bias voltage supplier's shutdown/enable ("HV_EN") ... this is always set as "enable" as the NIM module is powered on, but it would be possible to set "shutdown" by sending the shutdown signal through RBCP bus.
2. serial input to 16 bits DAC ("SDI_DAC") ... Users send 16 bits DAC input value to the firmware with the upper 8 bits and lower 8 bits separately in order through RBCP bus.
3. control clock signal for 16 bits DAC ("SCK_DAC") ... As the control clock signal, 25 MHz is used.
4. enable signal for 16 bits DAC ("CS_DAC") ... As starting to send the serial DAC input value, this enable pin is set only while one clock period.

3.2.2 Monitor ADC

An ADC, AD7795[4], is mounted on the NIM EASIROC module for the purpose to monitor the values of MPPC's bias voltage, bias current, 8-bit InputDAC, and temperature. It is possible for users to select a mode of theme, and also a channel or all channels of the chips as for InputDAC. The monitor ADC's output is provided as the serial signal and interpreted in the firmware due to the calibration's coefficients. The resisters corresponds to the data sent by users. Users send 8 bits data and this module correspondingly sends the register values to the monitor ADC, such as selecting readout channels, reading the current configuration, reading the monitor ADC data, selecting ADC mode, and sending reset as follows;

3.2.3 LED control

This module controls four LEDs on the front-panel. For each LED, there are two inputs; one turns on "green" and the other turns on "red", and the LED is tuened off when none of them is on. At present, these are controlled as follows:

Data sent by users	Register	Remark
0 - 10	0x10001{data}	Communication Register (8 bits) is set for the write operation mode and the following 16 bits are written into Configuration Register. Configuration Register sets bias voltage generator disabled, bipolar coding enabled, the gain value as 1, ADC input range as 2.5 V, the external reference, and unbuffered mode. And also select the active analogue input channel.
248	0x080003	Communication Register (8 bits) is set for the write operation mode and the following 16 bits are written into Mode Register. The reaout mode is set as the normal (single) readout, not the continuous readout. Mode Register sets the continuous convesion mode (default), the internal 64 kHz clock for the operation of AD7795, 125 Hz filter updata rate.
240	0x58	Comunication Register is set for the read operation mode. The following register is Data Register and allow the access to the result of conversion.
254	0x50	Comunication Register is set for the read operation mode. The following register is Configuration Register and allow the access to the current configuration.
255	0xFF	ADC is reset.

Table 1 Function in the firmware for the monitor ADC's register

- LED1 ... While power is supplied for the NIM module, the LED is turned on. "Green" is on while TCP connection ("Tcp_Open_Ack") is running, and "red" is on while TCP connection is not running.
- LED2 ... Busy signal turns "red" light on.
- LED3 ... Trigger signal (the OR signal of two "OR32") turns "green" light on.
- LED4 ... When the MPPC bias voltage is higher than 5 V, "green" is on.

3.2.4 Trigger width adjuster

Users can adjust the width of trigger signal for selectable logic module from 40 ns up to 800 ns, by 8ns step. The leading edge of the width-adjusted trigger signal is synchronized with the raw trigger signal from EASIROC, but the trailing edge is not synchronized with the raw trigger but synchronized with 125 MHz internal clock signal. Therefore, the trigger timing is synchronized with raw trigger, but instead the trigger width of the adjusted trigger signal is not fixed but fluctuates with around ± 4 ns. This adjusted triggers are used in "selectable logic" module and then probed out to the front-panel "TRIG" output, but TDC and scaler modules use the triggers with its raw width.

3.2.5 Selectable logic

Using the width-adjusted trigger, users can select pattern triggers by three register values, such as pattern, threshold for the number of hits, and the channel number used for AND logic. The following the list of pattern triggers.

- One channel ... The selected one of 64 channels is probed out. The number of hits and the AND logic do not affect the output with this pattern.
- OR signal of a chip ... The OR signal of 32 channels in the selected chip is probed out. If the threshold is set, the output would be "on" only if the number of hits in the selected chip is more than the threshold or equal. The AND logic does not affect the output with this pattern.
- OR signal of all 64 channels ... The OR signal of all 64 channels is probed out. If the threshold is set, the output would be "on" only if the number of hits in 64 channels is is more than the

threshold or equal.
- (OR signal of chip 1) AND (OR signal of chip 2) ... If the threshold is set, both of the numbers of hits in each chip are required to be more than the threshold or equal. The AND logic does not affect the output with this pattern.
- (OR of channel 0 to 15) AND (OR of channel 16 to 31) AND (OR of channel 32 to 47) AND (OR of channel 48 to 63) ... If the threshold is set, all of four numbers of hits in each group are required to be more than the threshold or equal. The AND logic does not affect the output with this pattern.
- AND signal of the selected channels in a chip, or within all 64 channels ... Users can select the channels which are used in the AND logic. The threshold of the number of hits does not affect the output in these patterns.
- (selected AND logic in chip 1) OR (selected AND logic in chip 2) ... Users can select the channels which are used in the AND logic. The threshold of the number of hits does not affect the output in these patterns.

3.2.6 Test charge injection

This module controls the direct input for EASIROC when the pin "In_calib_EN" is on. The module is operated by the same clock as TDC module that is 125 MHz, and when the count becomes equal to 32768 the voltage is biased during one period, 8 ns, into the calibration pin of the both chips, which is converted into electric charge by 3 pF capacitors for both of low gain and high gain pre-amplifiers. The count in this module is reset when the reset signal ("PWR_RST") is provided by a reset generator ("TPS3103K33") every 130 ms. In order to use this test charge injection, the corresponding register in slow control ("DisablePA & In_calib_EN") have to be set for a channel. Operating more than one channel at the same time should not be recommended for the precise calibration.

3.2.7 Clock signal output

The clock signal is probed out from the front-panel NIM output of the module by the user's selection as follows;

- OFF (low level, by default),
- ON (high level),
- Clock signal, with the frequency of 1 Hz, 10Ḣz, 100Ḣz, 1k̇Hz, 10k̇Hz, 100k̇Hz, 3Ṁ Hz.

4 Control software

4.1 Date acquisition

4.2 EASIROC "slow control"

4.3 Other modules' controller

4.4 Register

1. DefaultRegisterValue.yml ... Definition of the default values of all slow control bits.
2. RegisterAttribute.yml ... Definition of the bit structure for each parameter of slow control, the number of bits, bits order to be sent, and which of high or low to be active.
3. RegisterValue.yml ... Some parameters which user would like to overwrite the default value.
4. RegisterValueAlias.yml ... Definition of alias parameters which would be used as register values.
5. Calibration.yml ... Coefficients for converting the monitor ADC's outputs to the voltage, current, or temperature, and for converting the input value of the internal bias voltage to the corresponding DAC value.

5 Performance Test

5.1 List of performance tests

5.1.1 Calibration

1. Internal bias power supply ... LT3482EUD is used as an internal bias power supply, which provides MPPCs with bias voltage in the range from 0 V to 90 V, in response to 16-bit input. Setting the jumper pin(JP3) to be short-circuited, its voltage is probed out from the front panel output, and possible to be measured with multi-meter. The measured voltage is calibrated with the 16-bit input.
2. Monitor ADC ... AD7795BRUZ is mounted on this module as the monitor ADC, and able to measure bias voltage, bias current, 8-bit input DAC, and temperature. The bias voltage and 8-bit input DAC are directly measured by multi-meter and the corresponding value of the monitor ADC is calibrated.

5.1.2 Slow control test

EASIROC's parameters as follows(Fig.2) are controlled by "Slow control" through RBCP bus. As a performance test of the updated firmware and the whole EASIROC model, not of the chip itself, it is confirmed whether each "slow control" parameter behaves as expected to the user's input value.

5.1.3 New functions test

Some new functions as follows are implemented into EASIROC firmware for the first time.

1. Clock signal output
2. Pattern trigger
3. Trigger width adjuster

These functions' behaviors are confirmed so that they are correct as expected and controlled, and do not disturb other functions especially for data acquisition.

5.1.4 Performance test with test pulse

After that each component of the updated firmware correctly behaves is confirmed, the performance as an EASIROC module is measured with the test pulse inputs to MPPC input pins. Here is the list of the measurements. Almost all of the measurements is done with the setup as Fig. 4.

1. Data transfer time
2. ADC's behavior to input charge
3. MHTDC's time resolution
4. Scaler's behavior
5. Tolerance for high event rate
6. Multi-hit separation

Table **??** shows the specification of the modules used for the measurement.

Table 2 The modules for the measurement with test pulse injection.

Module	Specification
Function Generator	
Gate & Delay	
TTL-NIM	
FAN IN/OUT	
ATTENUATOR	

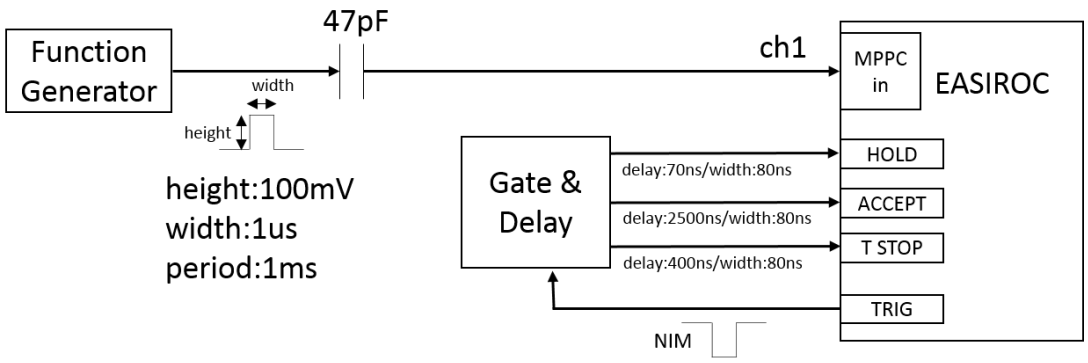

Fig. 4 Setup for the performance test with test pulse.

5.1.5 Performance test with 32-channel arrayed MPPC

Table 3 The modules for the measurement with 32-channel arrayed MPPC

Module	Specification
32-channel arrayed MPPC	
LED	
Clock module	
Gate generator	

5.1.6 Chip fault test with calibration input

5.2 Calibration of bias voltage control for MPPC.

The NIM EASIROC module contains bias voltage supplier, which is able to provide voltage up to around 90 V in accordance with DAC value input. This bias voltage is in common for all the channels of MPPCs, and it would be possible to probe the value from the front-panel output when the jumper pin ("JP3") is short cut. The bias voltage is measured by a multi-meter, whose specification is written in Tab. 4. The bias voltage is measured to the input 16-bit DAC value as Fig. 5, and the linearity is observed up to 92 V and the voltage is saturated.

Table 4 Multi-meter's specifications

Specification	Remarks
aaa	aaa
aaa	aaa

5.3 Calibration of the monitor ADC.

5.4 Feedback capacitor of preamplifier controlled by slow control

The input signal from MPPCs are transfered into the EASIROC chip and fist arrived at the preamplifier with high gain or low gain. The value of gain is able to be controlled by changing the feedback capacity via slow control. As decreasing the feedback capacity, the gain is increased and it is confirmed that the gain is correctly controlled as Fig. 6. Note that the waveforms in the figure are not the whole waveform after the preamplifier, but just around the peak of the waveform.

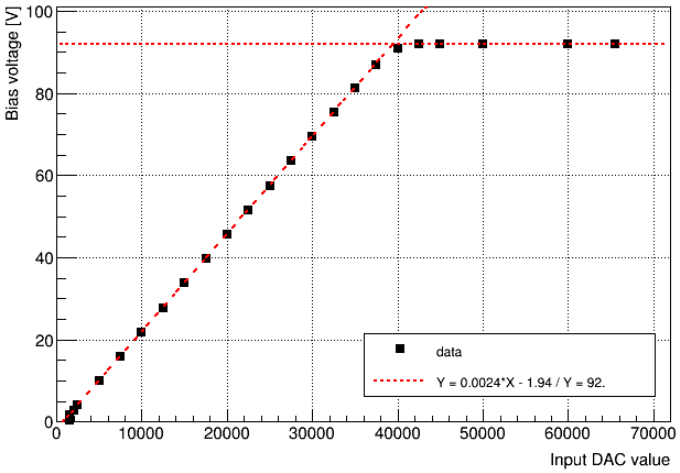

Fig. 5 The bias voltage to the input DAC value.

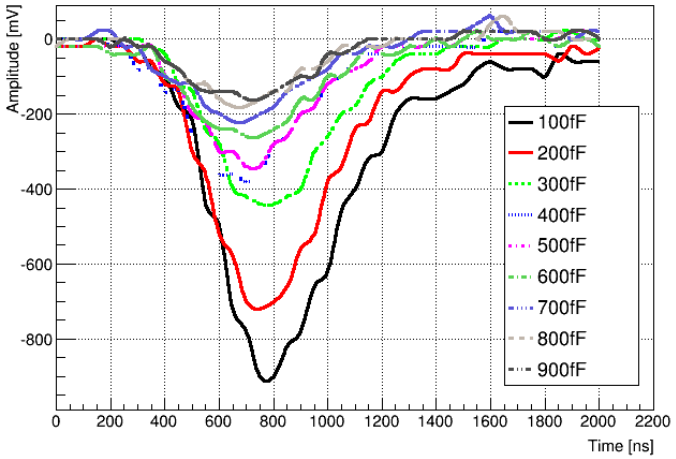

Fig. 6 The front-panel signals for the high gain preamplifier in EASIROC with different feedback capacitors.

5.5 Hold timing control

5.6 Data transfer time

Changing the delay time from the "HOLD" trigger to the "ACCEPT" signal, the distribution of the ADC values is measured.

5.7 ADC's behavior to input charge

The setup of this measurement is shown in Fig. 4. The distribution of ADC values are fitted with a gauss function, and the mean value of the gauss function is determined to be the average ADC value for the setup, and the sigma of the that is to be the statistic error for the ADC value. The ADC values are plotted as functions of input charge from the capacitor in Fig. 10. Shapers in EASIROC with different feedback capacitances behave differently to the input charges; Both of the feedback capacitors of the "high gain shaper" and that of the "low gain shaper" are set as 200 fF. The "high gain shaper" is more

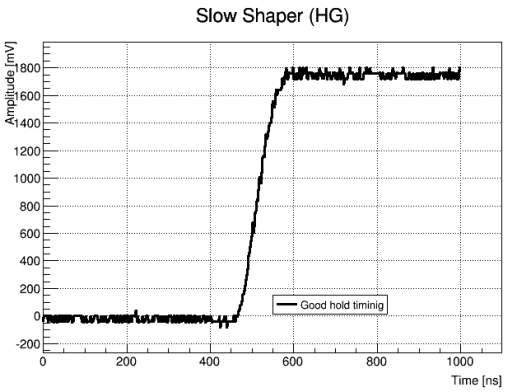

Fig. 7 The signal of the slow shaper after high gain preamplifier.

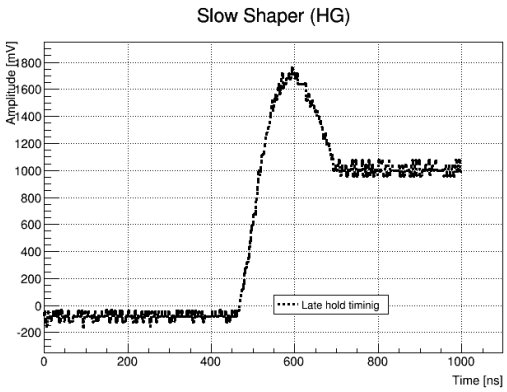

Fig. 8 The signal of the slow shaper after high gain preamplifier.

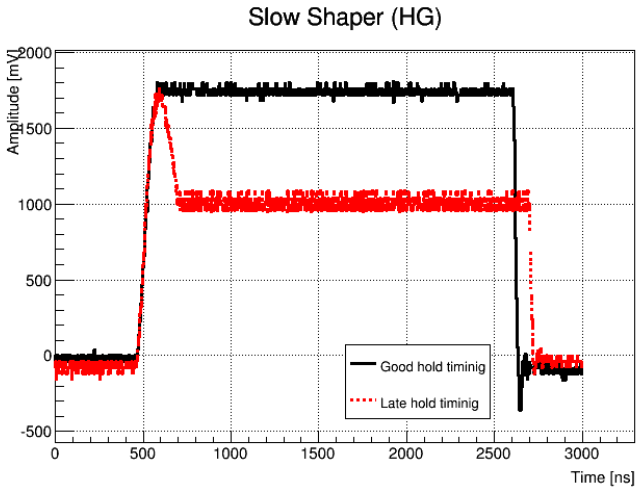

Fig. 9 The signal of the slow shaper after high gain preamplifier.

sensitive to small value of charge, whereas the "low gain shaper" is more sensitive to relatively large value of charge. Both of them are finally saturated at a constant value.

5.8 MHTDC's time resolution measurement

Figure 4 shows the setup for the MHTDC's time resolution measurement. This TDC value means the time difference from the timing of discriminator's signal to the timing of "T STOP" signal, therefore the time resolution includes the following components;

- the precision of discriminator signal's timing by the chip,
- that of delayed signal by "Gate and Delay" module,
- the accuracy of the MHTDC module in the firmware,
- the fluctuation of arrival timing of signals in the EASIROC module.

The precision of the function generator needs not to be considered because the "TRIG" front-panel output is synchronized with the discriminator signal.

Figure 11 shows the distribution of TDC values for about 55 million events, and the gauss function fitting the distribution. As the σ of the gauss function, the time resolution of the EASIROC module is measured to be 0.53 ns.

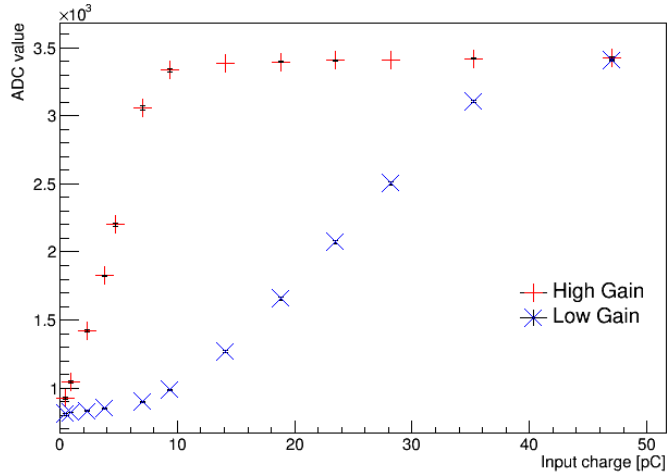

Fig. 10 ADC value of "high gain slow shaper" and "low gain slow shaper" to the input charge.

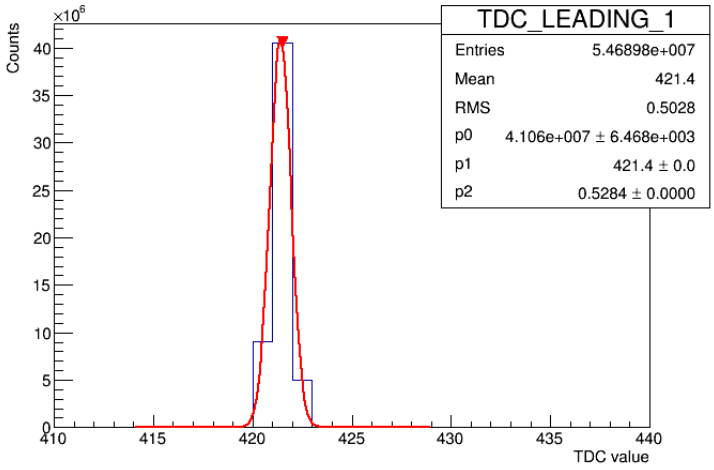

Fig. 11 Distribution of MHTDC value with test pulse.

5.9 Scaler test with test pulse

Figure **??** shows the setup for the performance test of the scaler function in firmware. In this test measurement, one of the front-panel NIM inputs is directly connected to the input for scaler module in the firmware, and the scaler counts are measured to the frequency of the input pulse. The trigger rate for readout is fixed to be 1 kHz. The result is plotted in the Fig. 12. Scaler counts are consistent with the frequency of the input pulse by the accuracy of 0.5% up to 100 kHz, 2% up to 2 MHz. Howeve, the scaler counts saturate at 4095 because the value is the maximum countable number for each event.

5.10 Tolerance for high event rate.

5.11 Multi-hit separation

In order to measure the ability of MHTDC to separate multi-hits, double pulses are used as inputs for the EASIROC module with the setup as Fig. 13. The data acquisition triggers are synchronized with

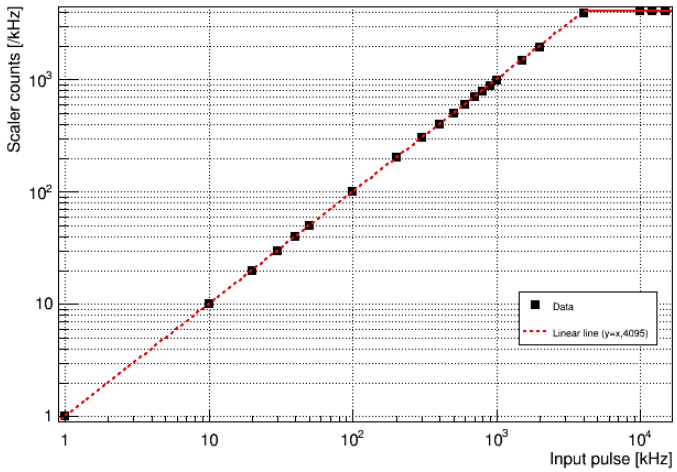

Fig. 12 Scaler counts plotted to the frequency of the input pulse.

the input pulse by the function generator. The ability of multi-hit separation as the MHTDC module in the firmware was already measured and it was confirmed that the limitation of multi-hit separation was 7 ns as the width between the trailing edge of the first pulse and the leading edge of the second pulse[5]. Therefore, the ability as the EASIROC module only needs to be measured.

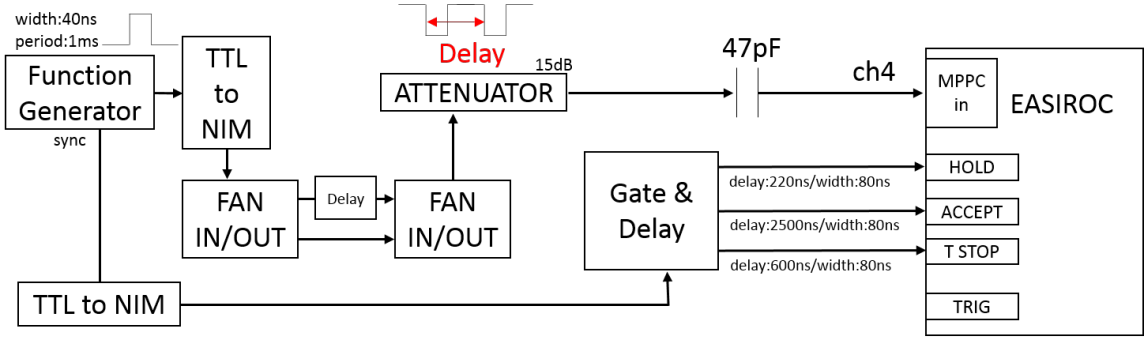

Fig. 13 Setup for multi-hit measurement.

Figure **??** is the waveform of the input to a channel of the front-panel MPPC input of the EASIROC module. Given the shaping time of "fast shaper" with 15 ns, the delay time is decreased down to about 60 ns. The MHTDC distributions for the two discriminator signals are in Fig. 15. The time width between the trailing edge of the first signal and the leading edge of the second signal is 16 ns, and it is confirmed that there is no missing edges with this time margin. Due to the negative pulses existing, the measurement with even smaller time margin could not be done.

5.12 Module performance test with signal from 32ch MPPC array

In order to confirm that the EASIROC module is able to acquire data from MPPC's signal, and to control the bias voltage for MPPCs, the following performance is measured with 32ch MPPC array and light injection from LED.

1. Photon counting performance
2. MPPC's gain linearity

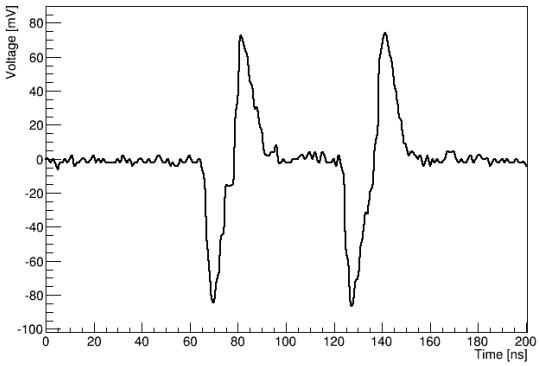

Fig. 14 The double-pulse input.

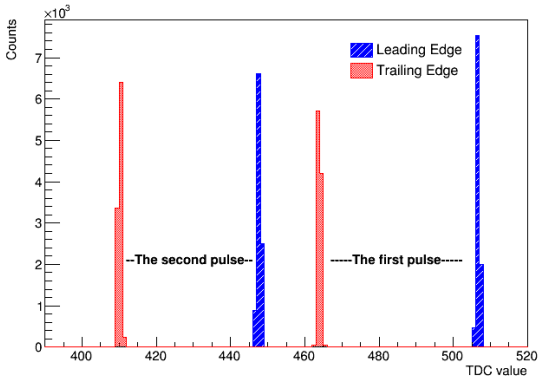

Fig. 15 Distribution of MHTDC value with double test pulses separated by 60ns.

Figure 16 shows an example of the distribution of the MPPC's signal, and the gauss functions fitting the peak for each number of photo electrons from 0 to 4. The trigger signal here is synchronized with the 1-kHz clock signal controlling LED's light injection. The MPPC's gain is measured as the difference of ADC values between 1 p.e. and 2 p.e., and it is confirmed that the gain is controlled by the InputDAC value of EASIROC. Figure 17 shows the gain changes linearly in accordance with the overvoltage.

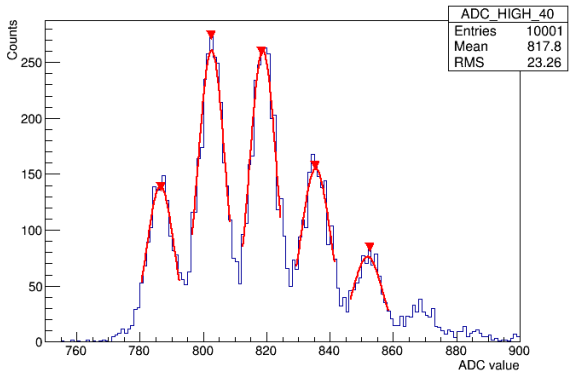

Fig. 16 MPPC's signal distribution with the overvoltage of about 2 V, and gauss functions fitting the peaks of 0 p.e., 1 p.e., 2 p.e., 3 p.e. and 4 p.e.

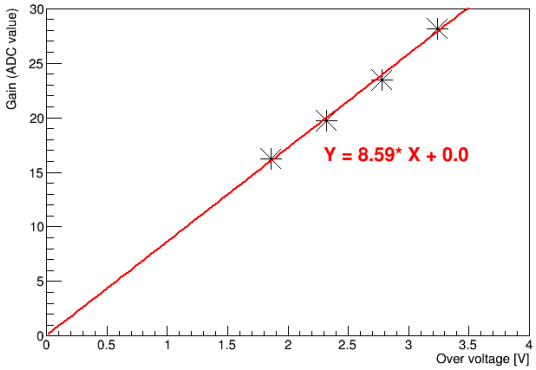

Fig. 17 MPPC's gain distribution to the overvoltage.

Furthermore, it is confirmed that the EASIROC module is able to control many MPPC channels at the same time. Figure 18 shows the ADC distribution for MPPC signals. 32-channel arrayed MPPC is connected to one of two chips on the EASIROC module, which corresponds to channel 32 to 63, and the other chip is open. The MPPCs are operated at the overvoltage of about 2 V, and it is observed that there are several peaks of photo electrons from 1 p.e. to 4 p.e. (or 5 p.e.). Note that in Fig. 18 the pedestal position is adjusted at 750 for the purpose to make the figure easy to be compared between channels. The gains are increased a bit as close to the edge channel within the chip with the MPPC signals, and this is because a 3-m long flat cable is used for the connection between 32-channel arrayed MPPC and EASIROC and is more sensitive to the noise as close to the edge of the cable.

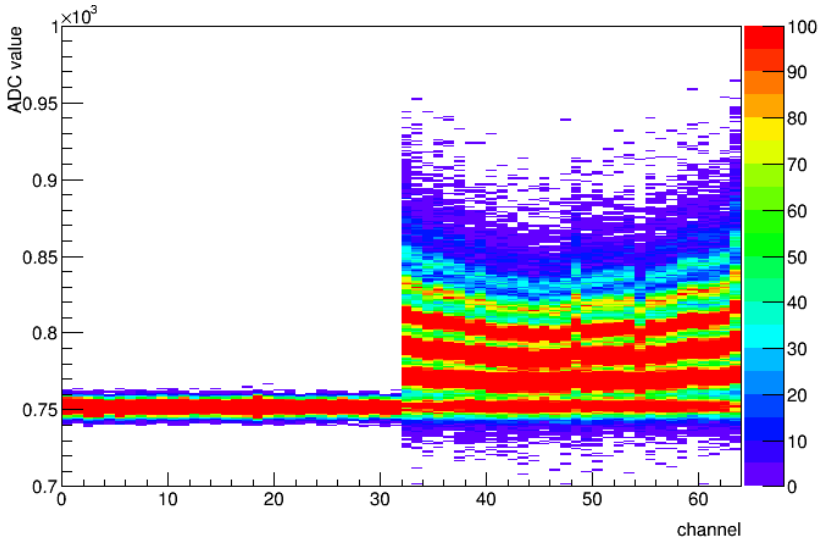

Fig. 18 MPPC's signal distribution with the overvoltage of about 2 V for all the channels on a chip of two, corresponding to channel 32 to 63.

5.13 InputDAC behavior check test with calibration input.

EASIROC has a function to inject the calibration charge ("in_calib"), and both of high and low gains are provided with the same constant charge. This calibration charge would be used for checking the behavior of InputDAC. The ADC distributions when the calibration charge is injected with the InputDAC value of 400 and 100 are shown in Fig. 19 and Fig. 20. When the InputDAC value is supposed to be broken, the ADC distribution is always as if DAC being turned off (Fig. 20) regardless of the InputDAC value. At the same time the analog memory value in EASIROC is observed unstably, so that it is sometimes corresponding value to the input charge and other times small constant value.

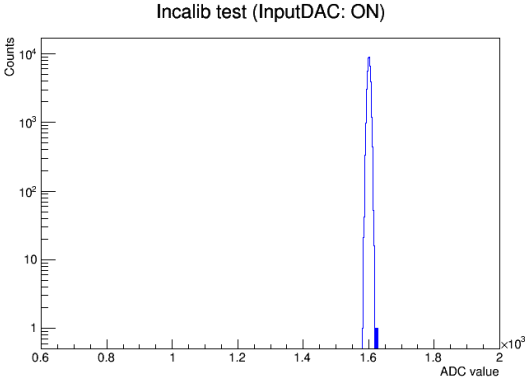

Fig. 19 ADC distribution for the calibration charge ("Incalib") with the InputDAC 400 (ON).

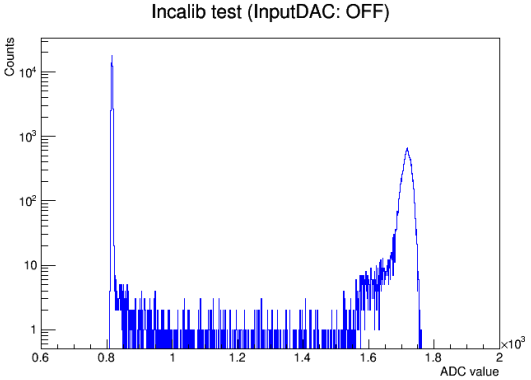

Fig. 20 ADC distribution with the calibration charge ("Incalib") with the InputDAC 100 (OFF).

A Troubles in developing the firmware

A.1 meta-stable

References

[1] EASIROC DATASHEET Version:5 April 2011

[2] LT3482 data sheet, Linear Technology.

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[5] 塩崎健弘. Development of a MPPC multi-channel readout system for the Σp scattering experiment. Master thesis. 東北大学大学院理学研究科, 物理学専攻, 2014