Status Report #15

2020. Feb 20 (Thu)

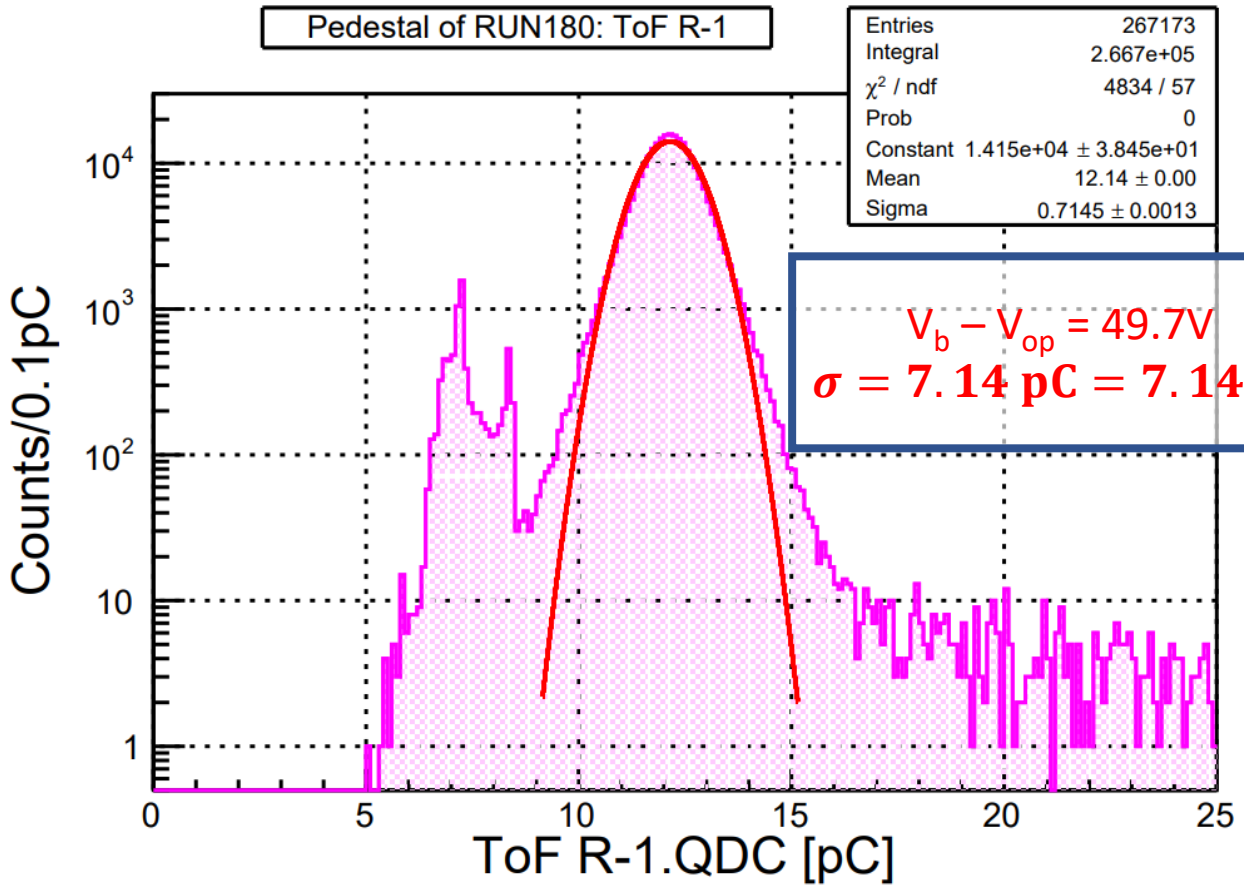
B4 FUJIWARA Tomomasa

This week

- ToF: Beam time data analysis
- ToF: Cosmic
- New circuit design

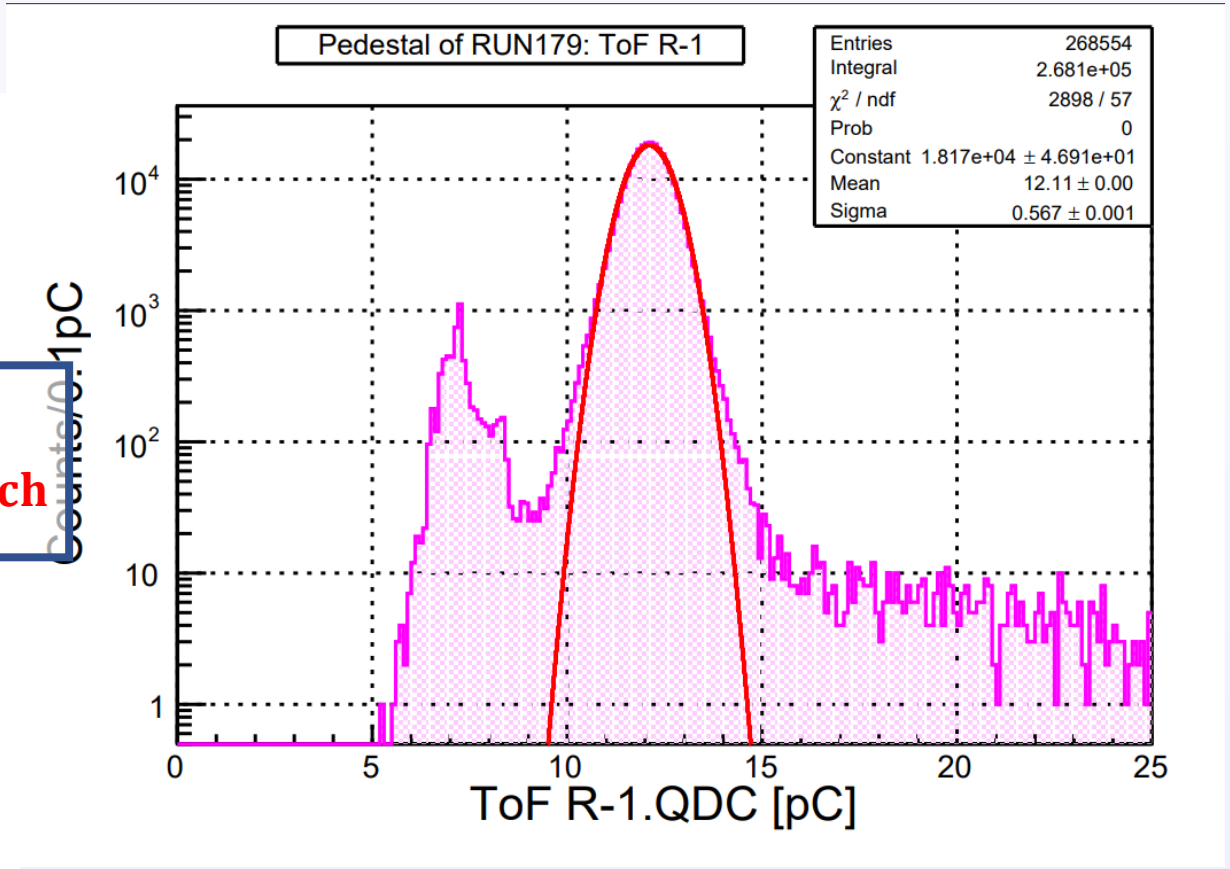
Beam time data analysis

- Checked pedestal distribution in high voltage region



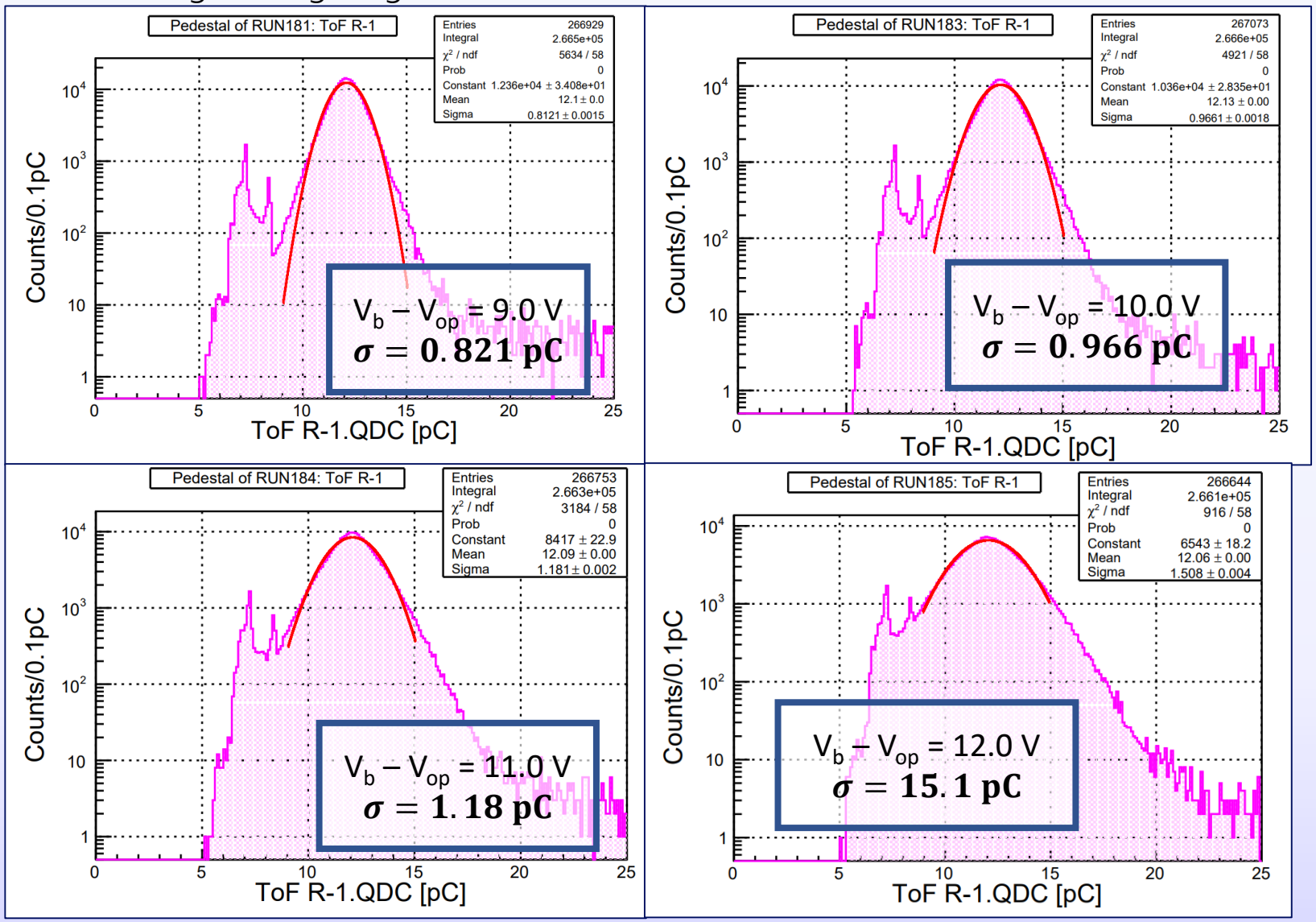
$V_b - V_{op} = 49.7V$

$\sigma = 7.14\ pC = 7.14\ ch$



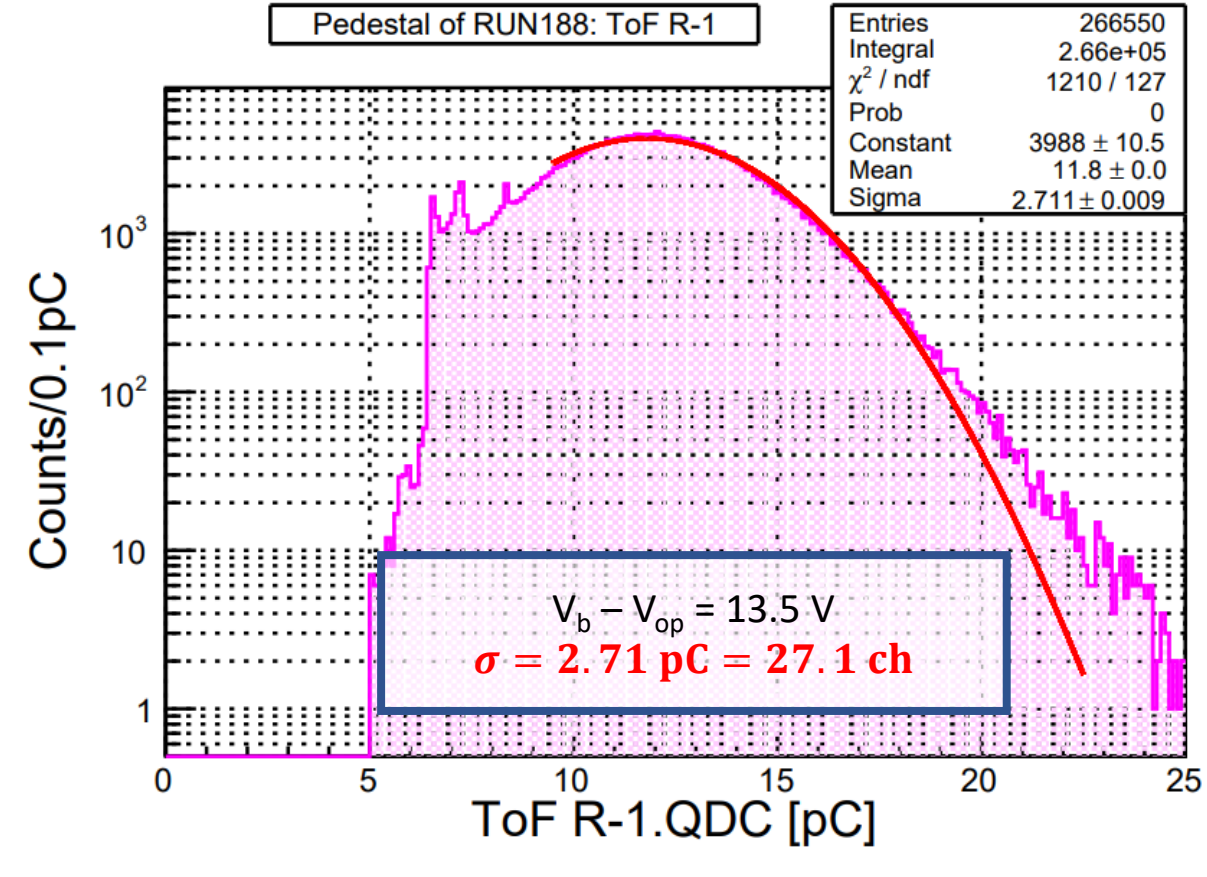
Beam time data analysis

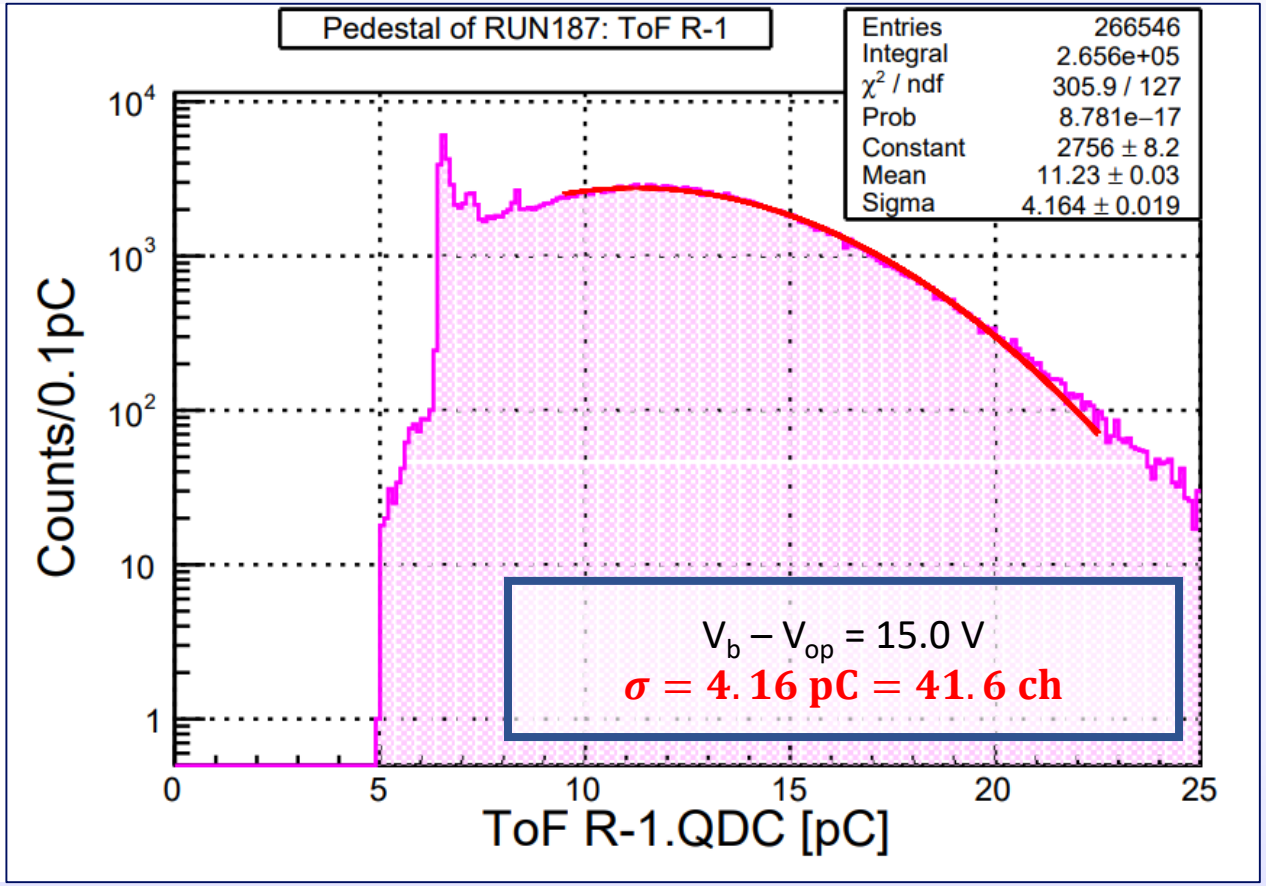
- Checked pedestal distribution in high voltage region



Beam time data analysis

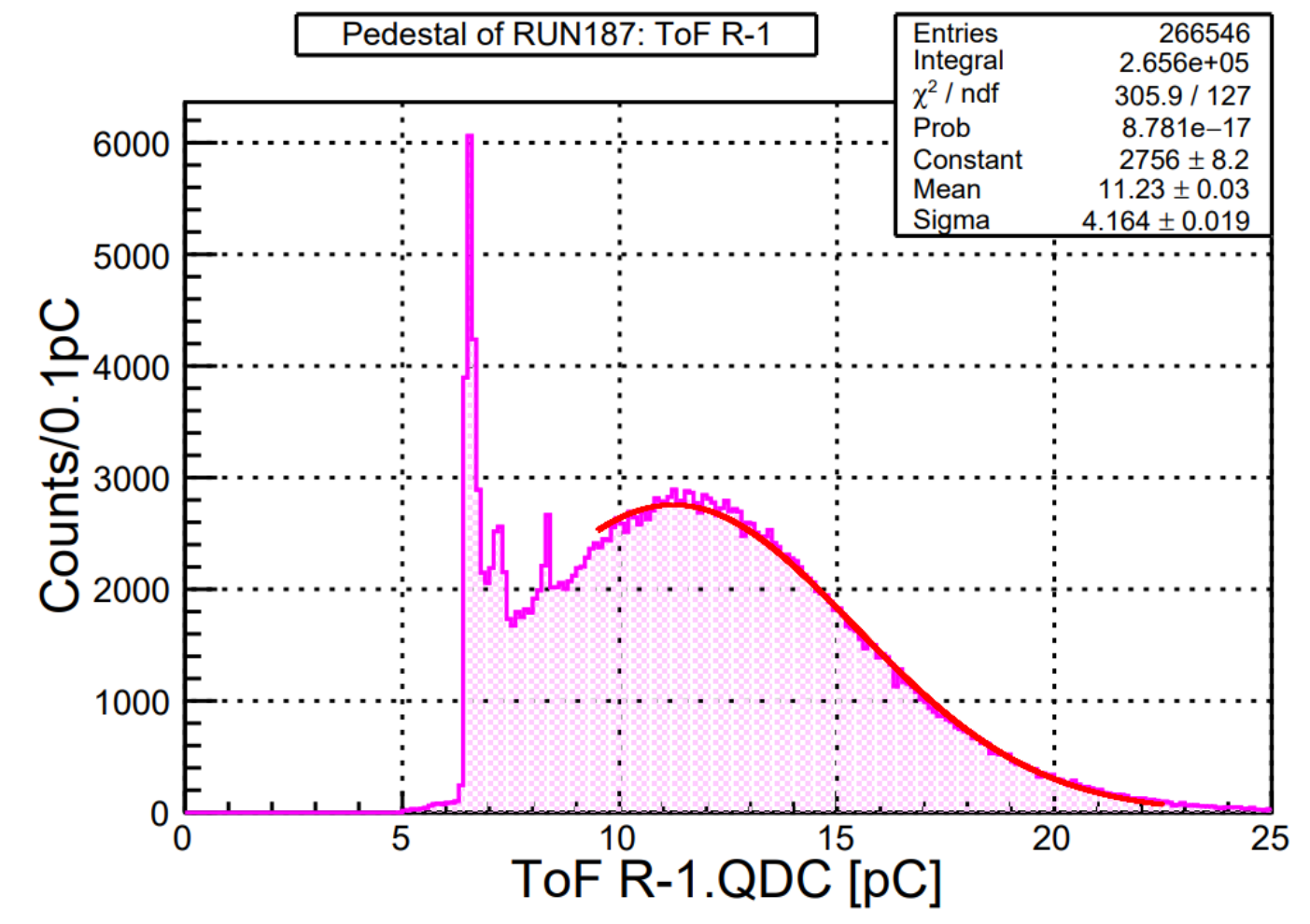
- In 53.2V (+13.5V) & 56.7 V (+15.0V)

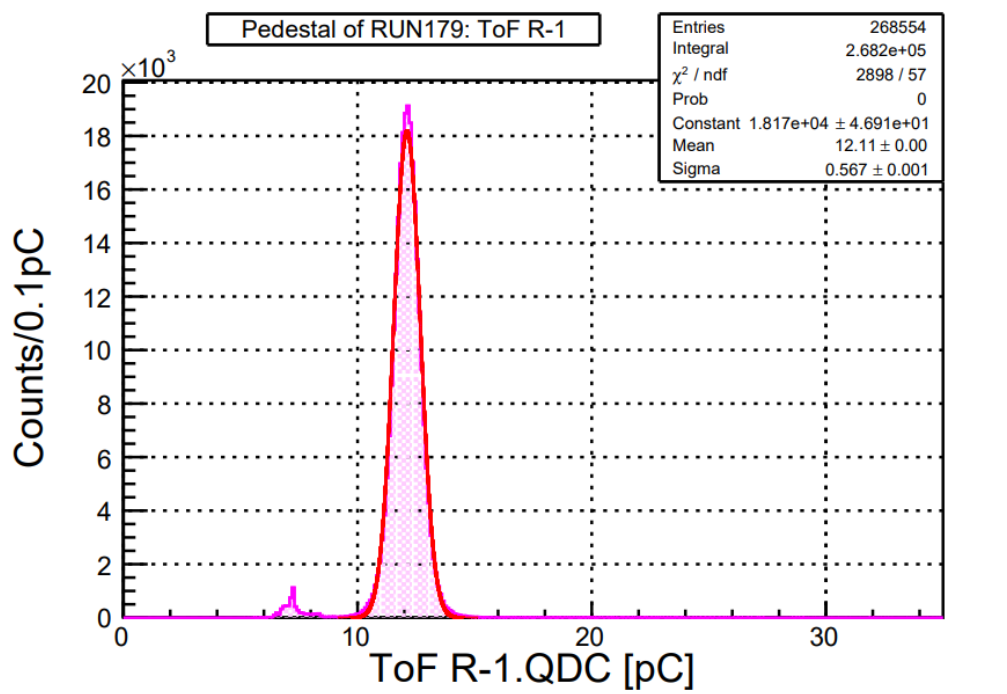


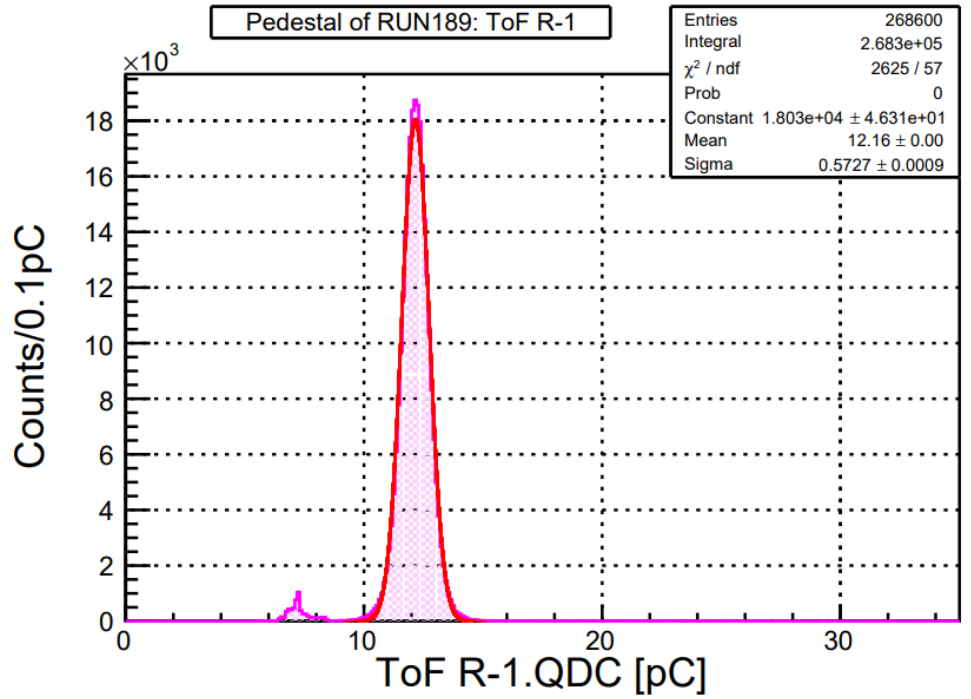


Beam time data analysis

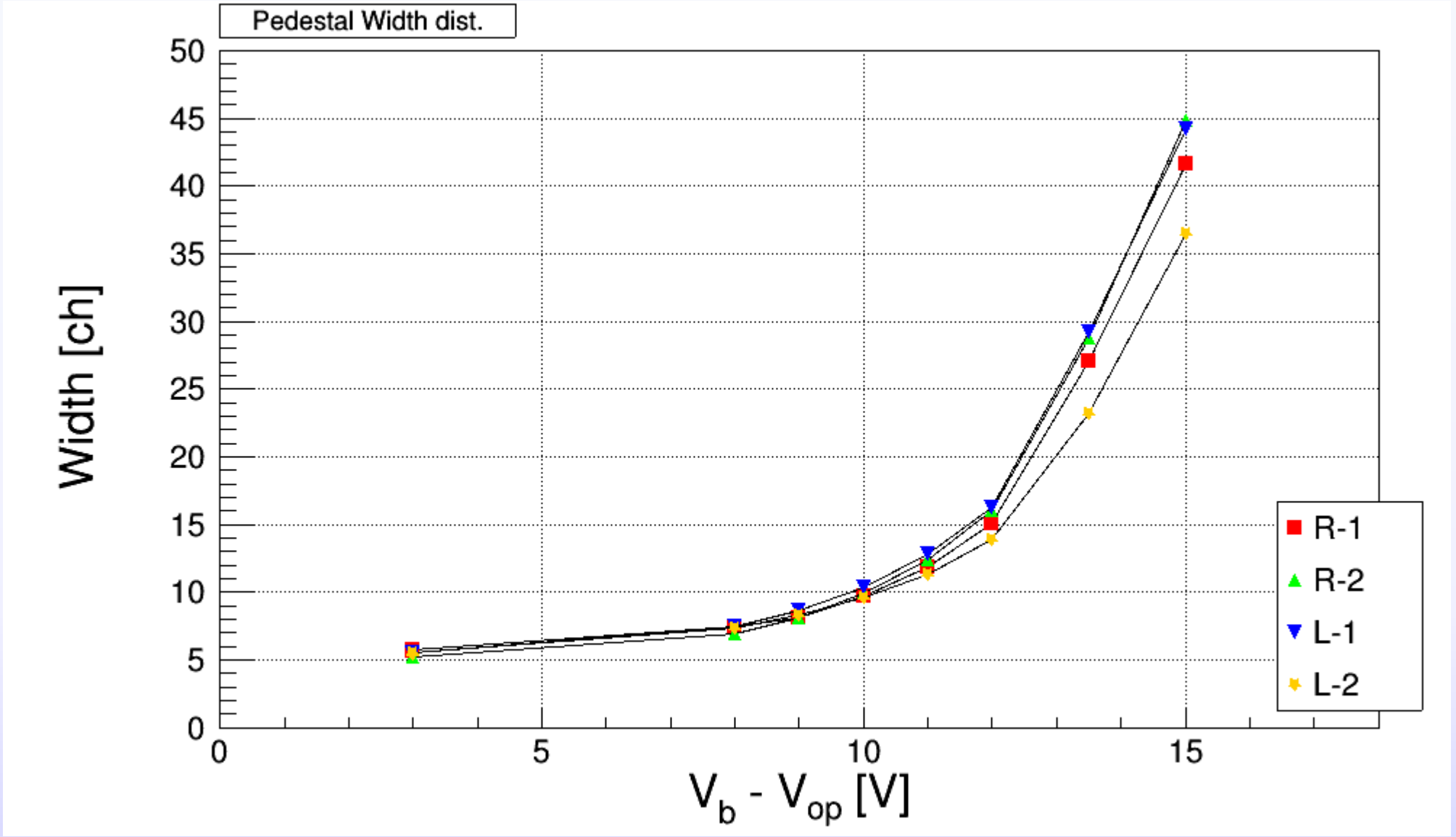
- In 56.7V (Linear scale)





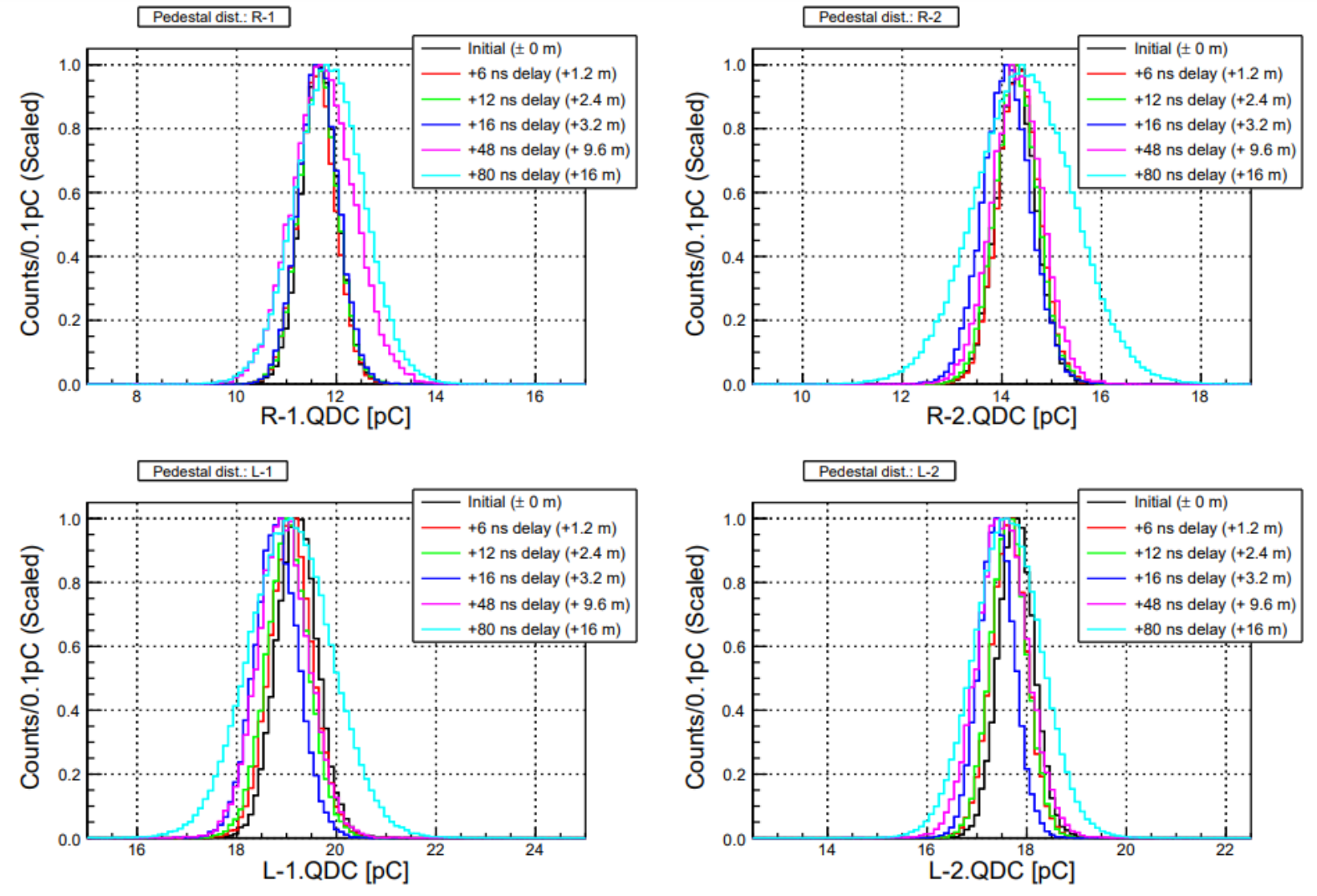


Beam time data analysis: Pedestal



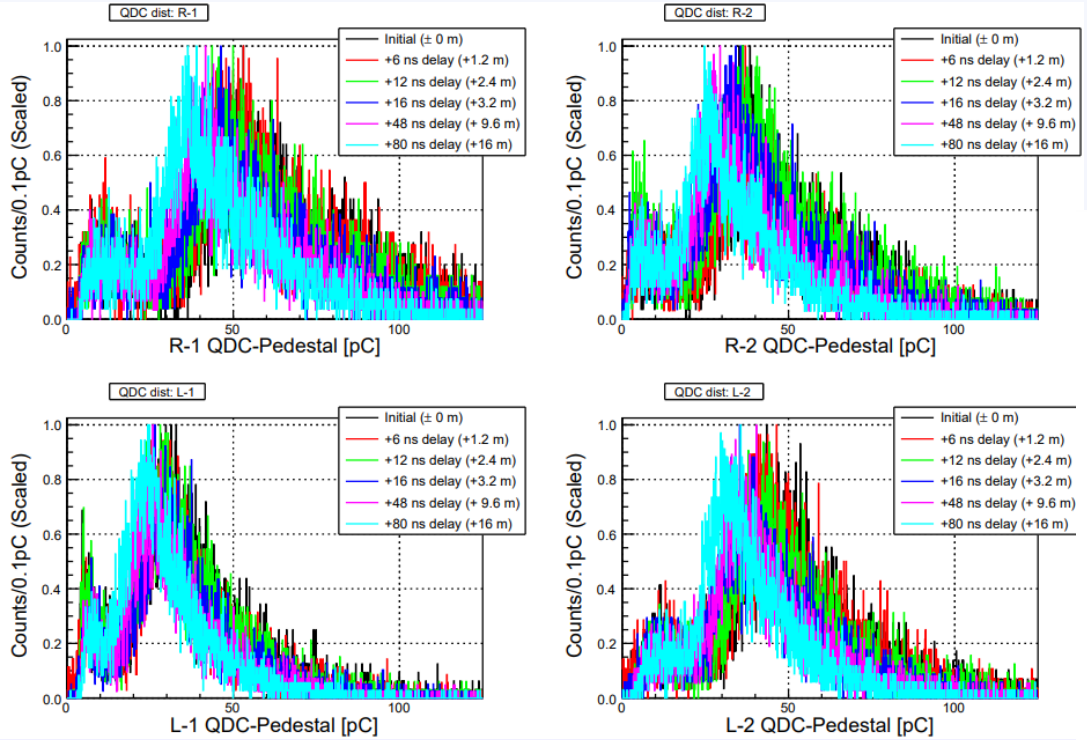
ToF: Cosmic-ray –check cable length dependence-

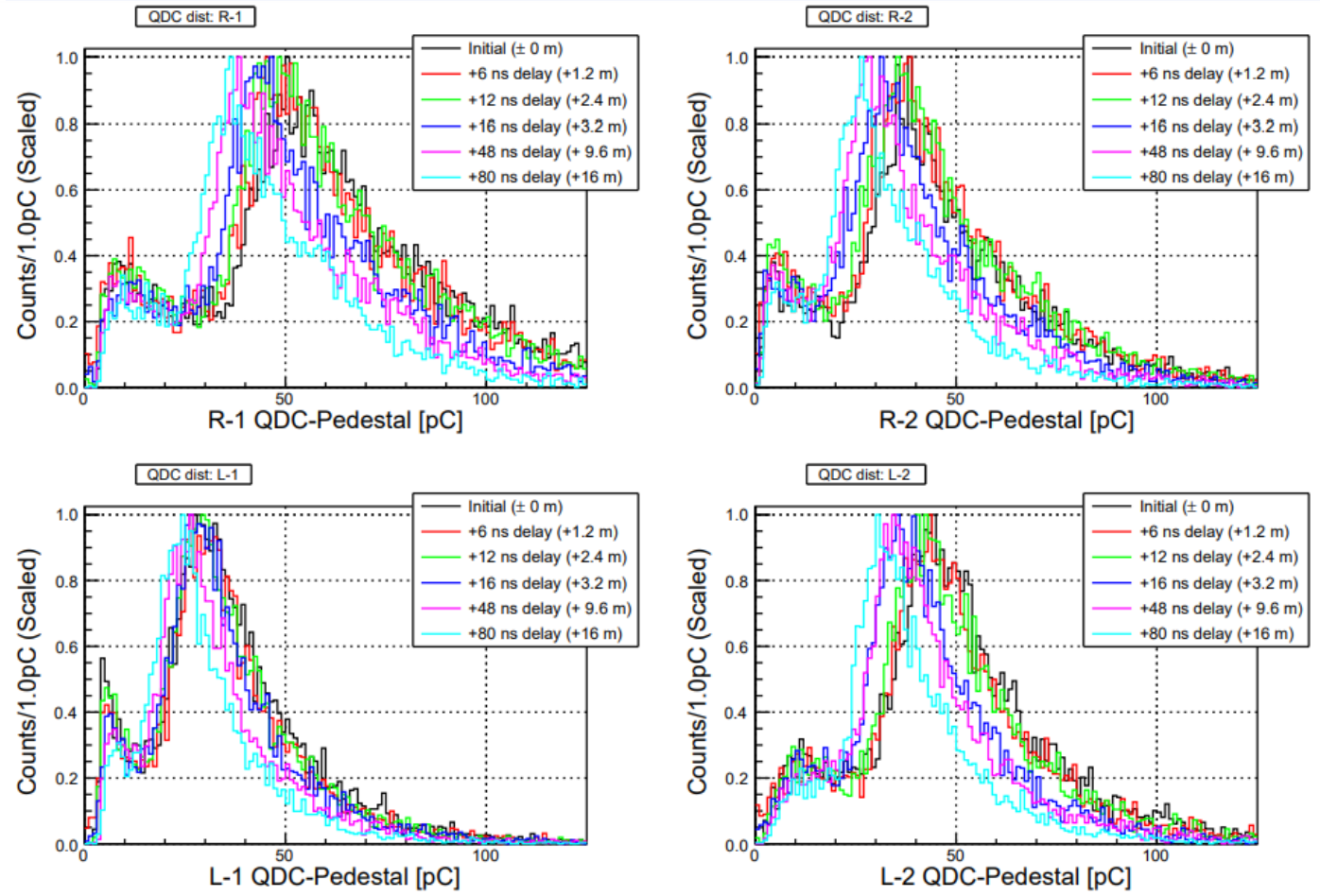
- Pedestal distribution
- Scaled peak = 1



ToF: Cosmic-ray –check cable length dependence-

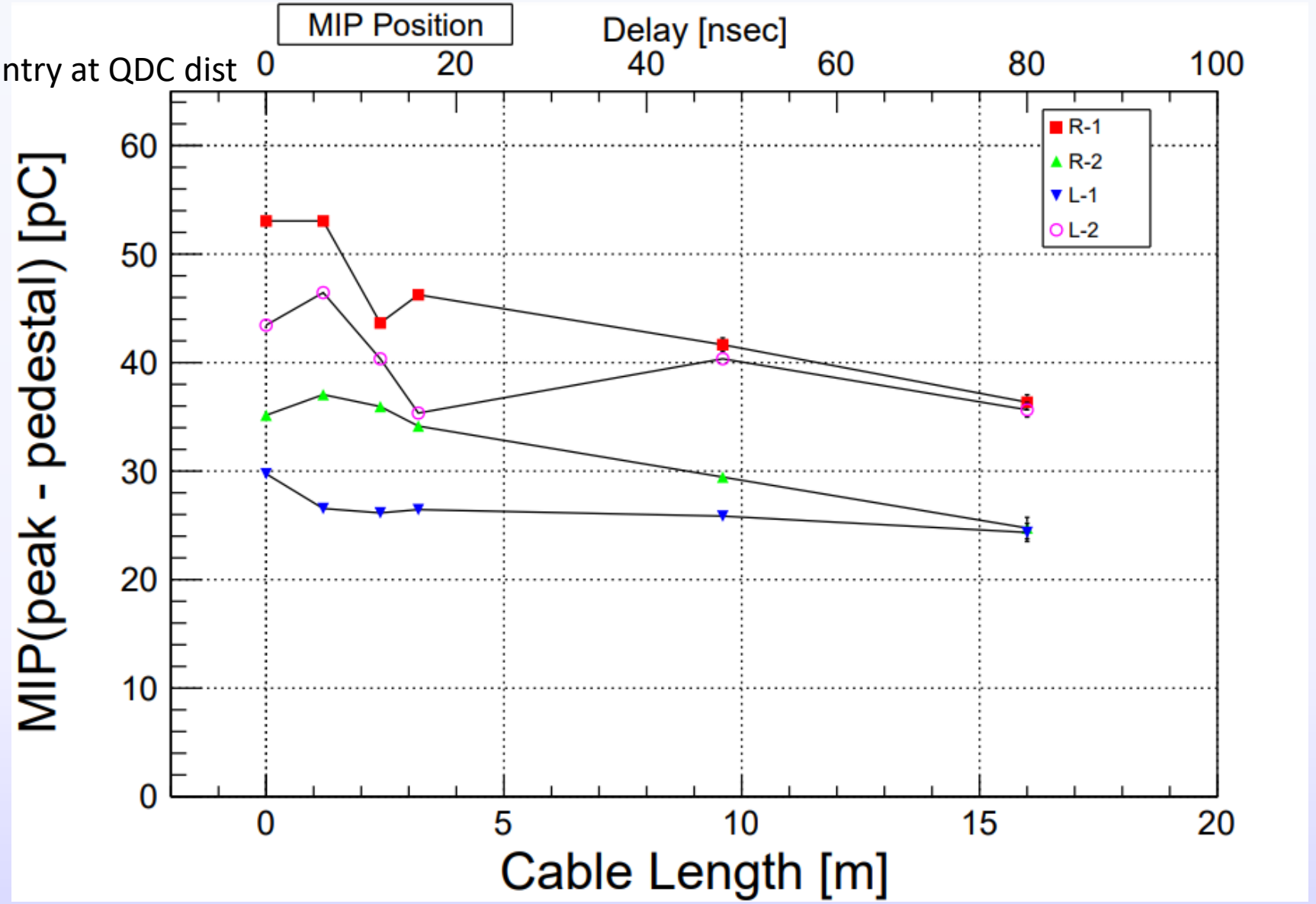
- QDC dist. (Calibrated by pedestal = 0)



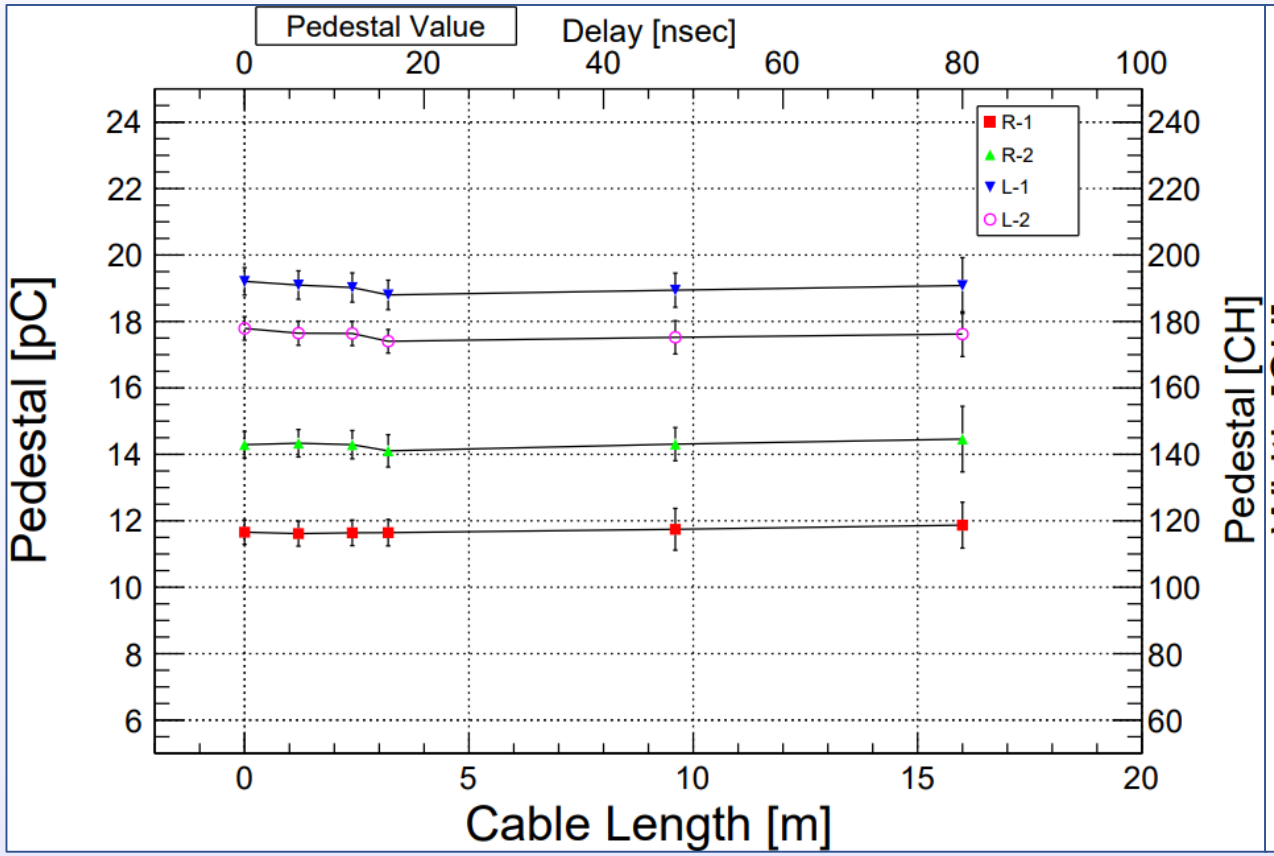


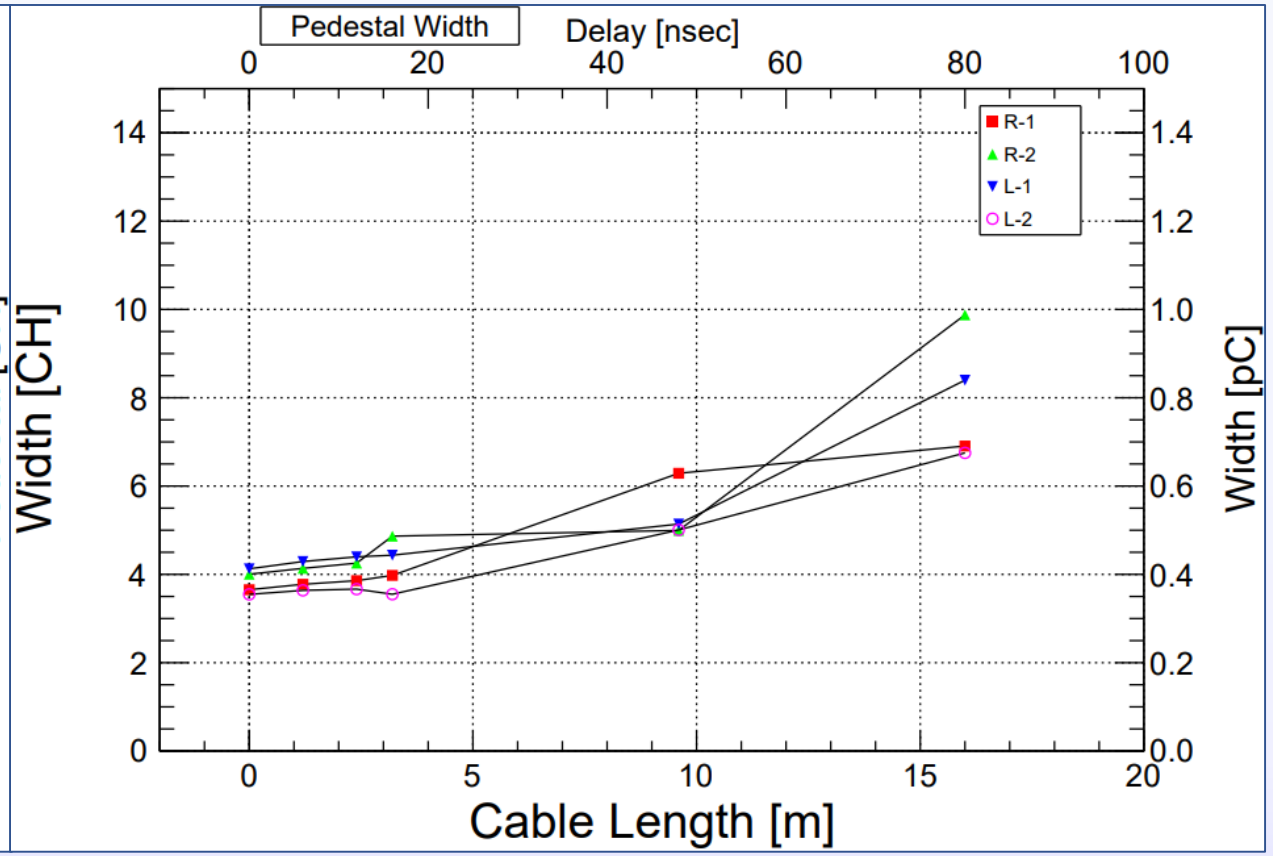
ToF: Cosmic-ray –check cable length dependence-

MIP: Center value with Maximum entry at QDC dist
Slightly decreased MIP value



ToF: Cosmic-ray –check cable length dependence-





ToF: Cosmic-ray –check cable length dependence-

- Check additional cable length dependence of Timing resolution:

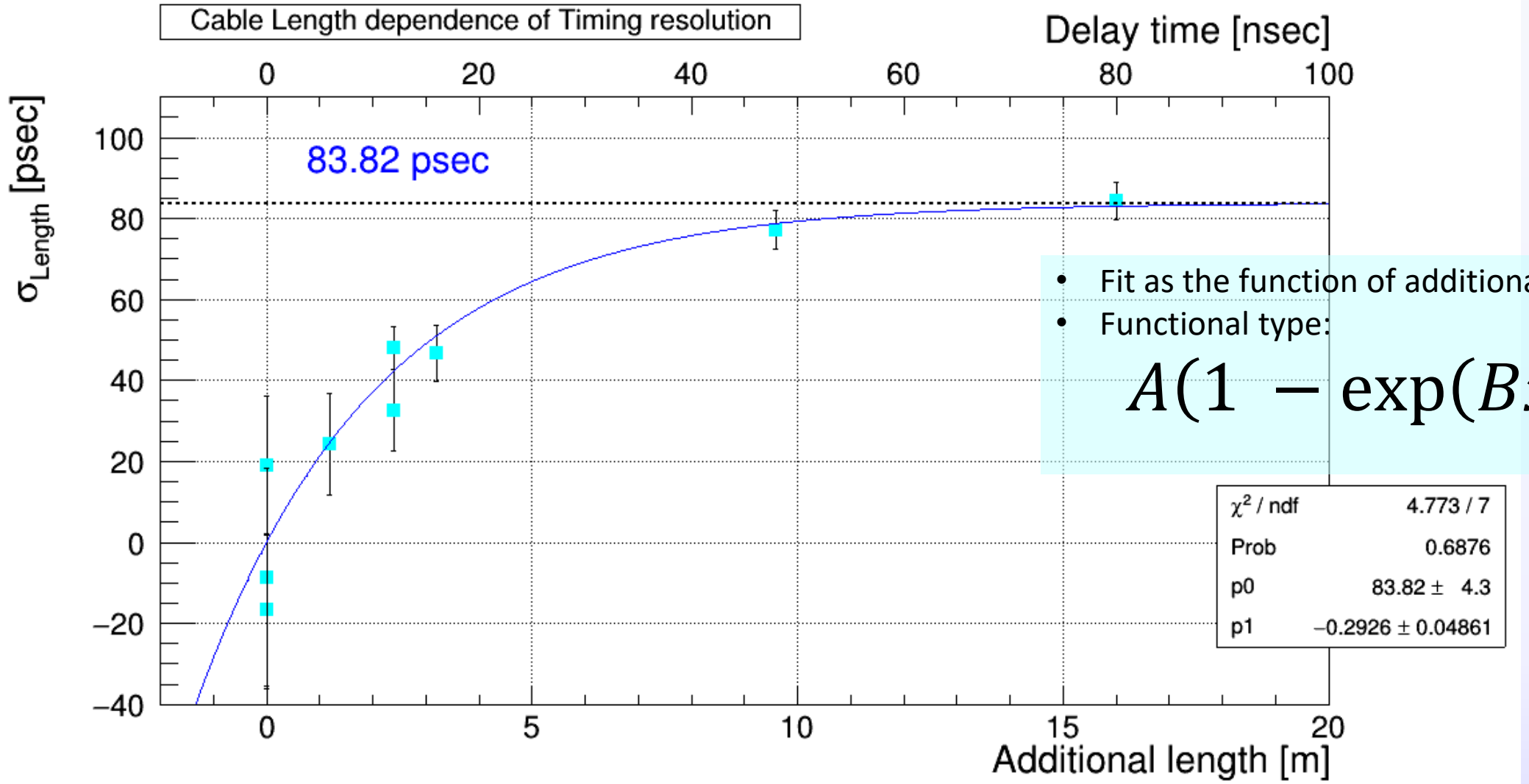
$$\sigma_{Length}^2 \equiv \sigma_{L=l}^2 - \sigma_{L=0}^2$$

- Reference value: $\sigma_{L=0}$ → defined by average of $\sigma_{L:initial}$ at V_b - V_{op} = +3.0V (V_b = 44.7V)
- Error of σ_{Length}: derived from propagation of error,

$$\epsilon_{Length} \equiv \sqrt{\left(\frac{\partial \sigma_{Length}}{\partial \sigma_{L=l}}\right)^2 \epsilon_{L=l}^2 + \left(\frac{\partial \sigma_{Length}}{\partial \sigma_{L=0}}\right)^2 \epsilon_{L=0}^2}$$

$$= \frac{\sigma_{L=l}^2}{\sigma_{Length}^2} \epsilon_{L=l}^2 + \frac{\sigma_{L=0}^2}{\sigma_{Length}^2} \epsilon_{L=0}^2$$

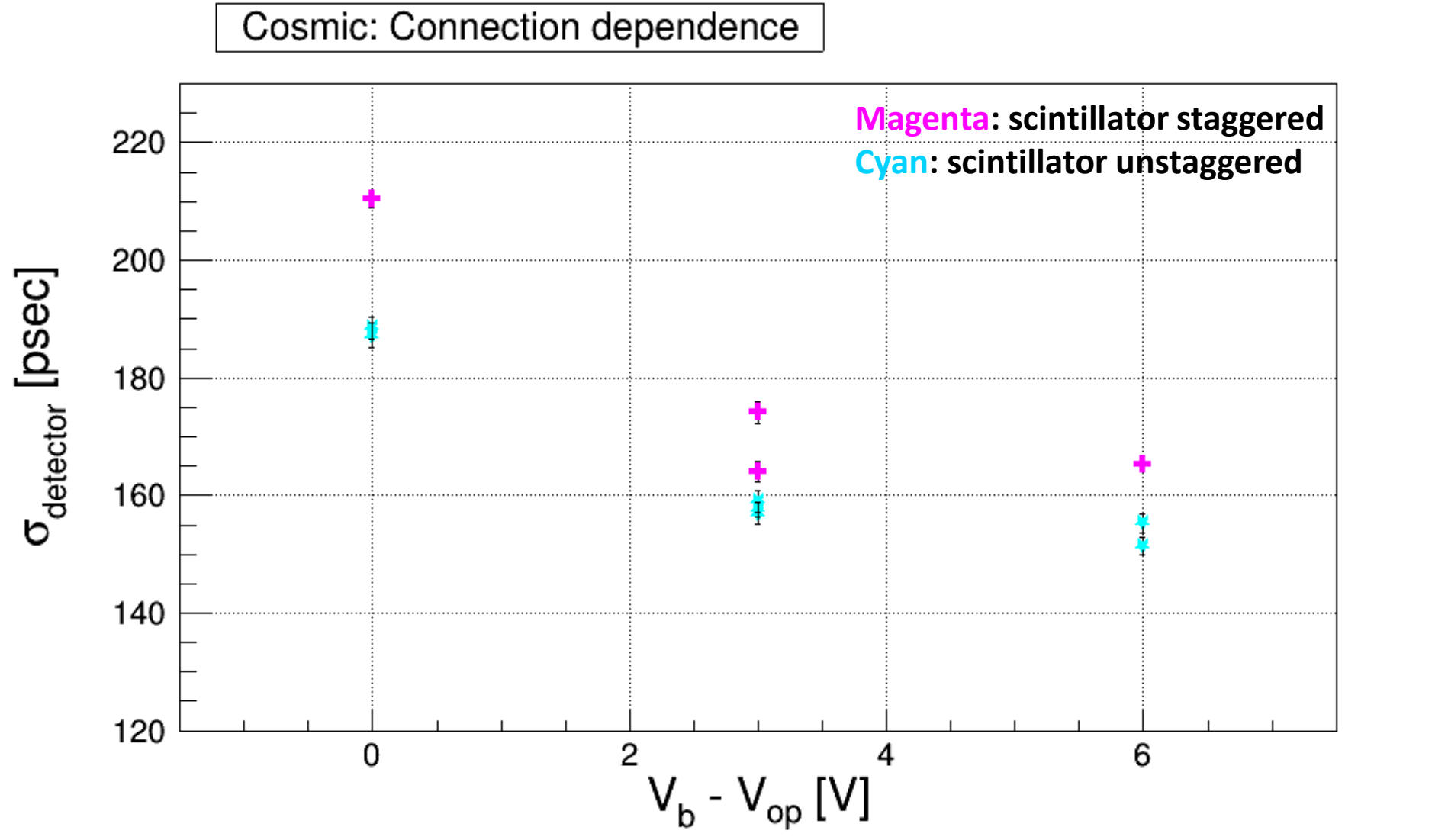
ToF: Cosmic-ray –check cable length dependence-



- Fit as the function of additional cable length
- Functional type:

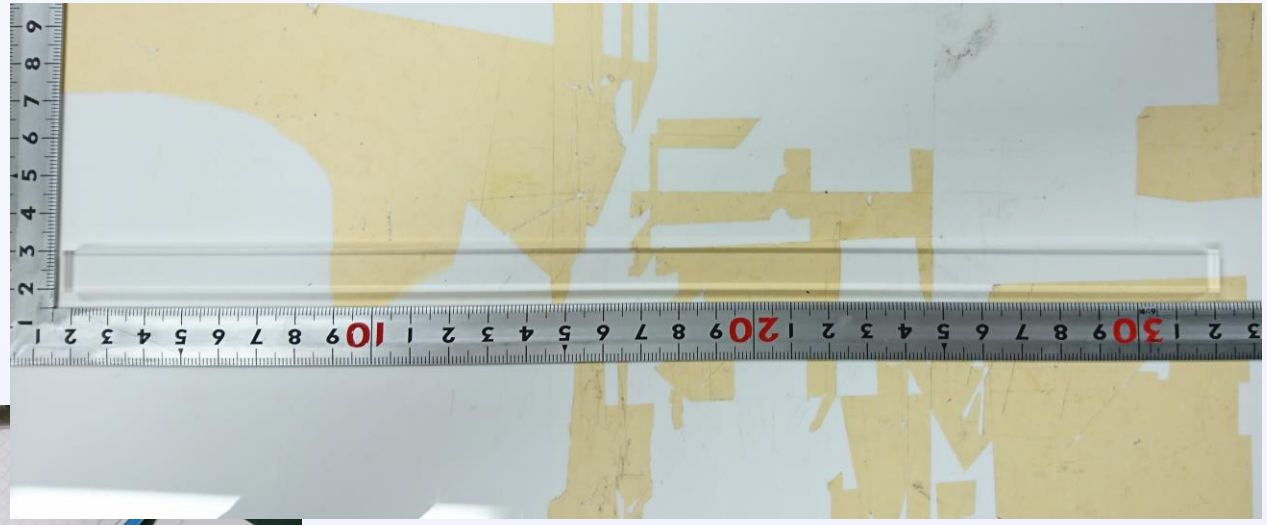
$$A(1 - \exp(Bx))$$

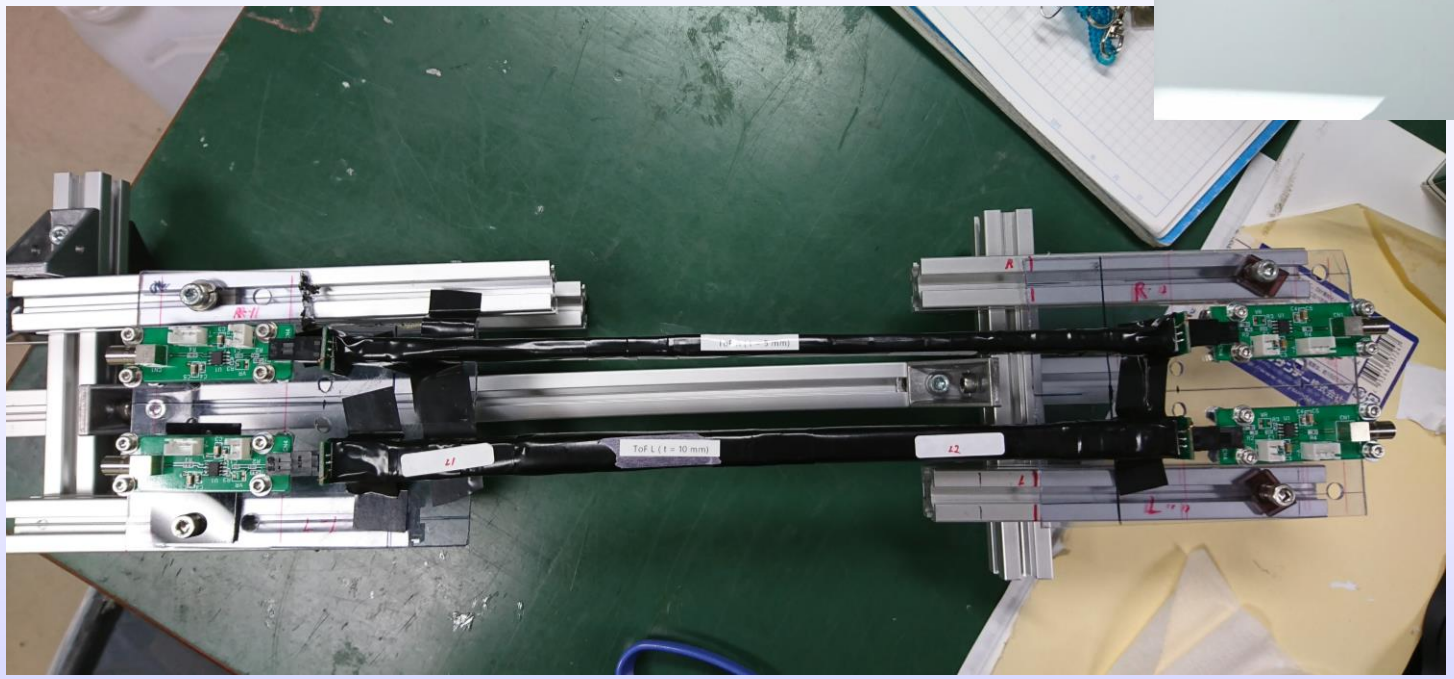
ToF: Cosmic-ray –Connection dependence-



New Scintillator: t = 5mm

Started data taking with different thickness scintillator: $5^{t} \times 11^{w} \times 300^{h}$ mm





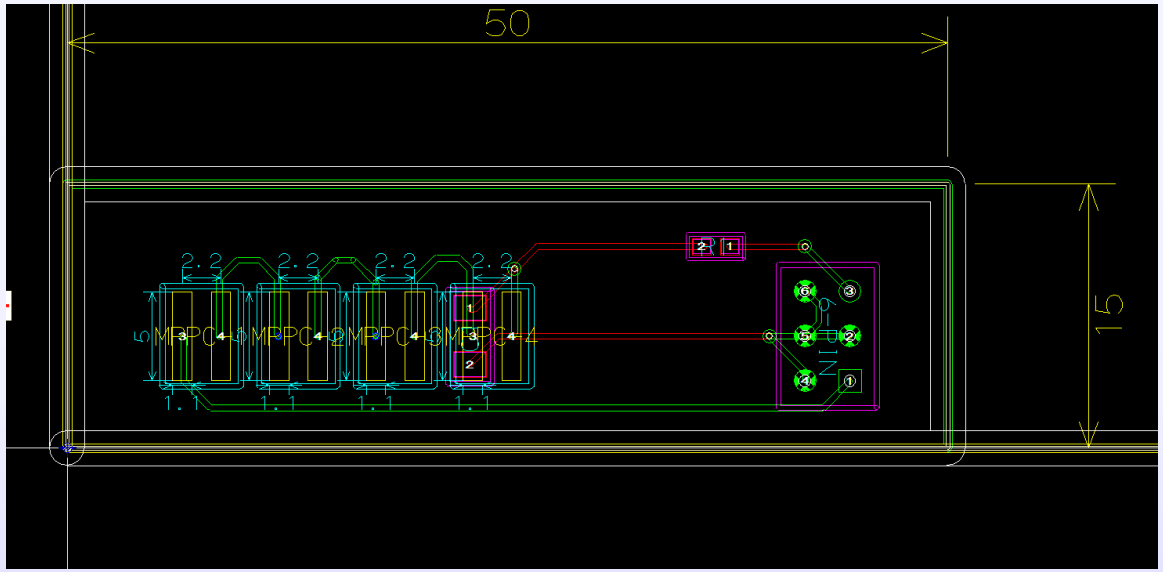
New Circuit design for ToF (MPPC)

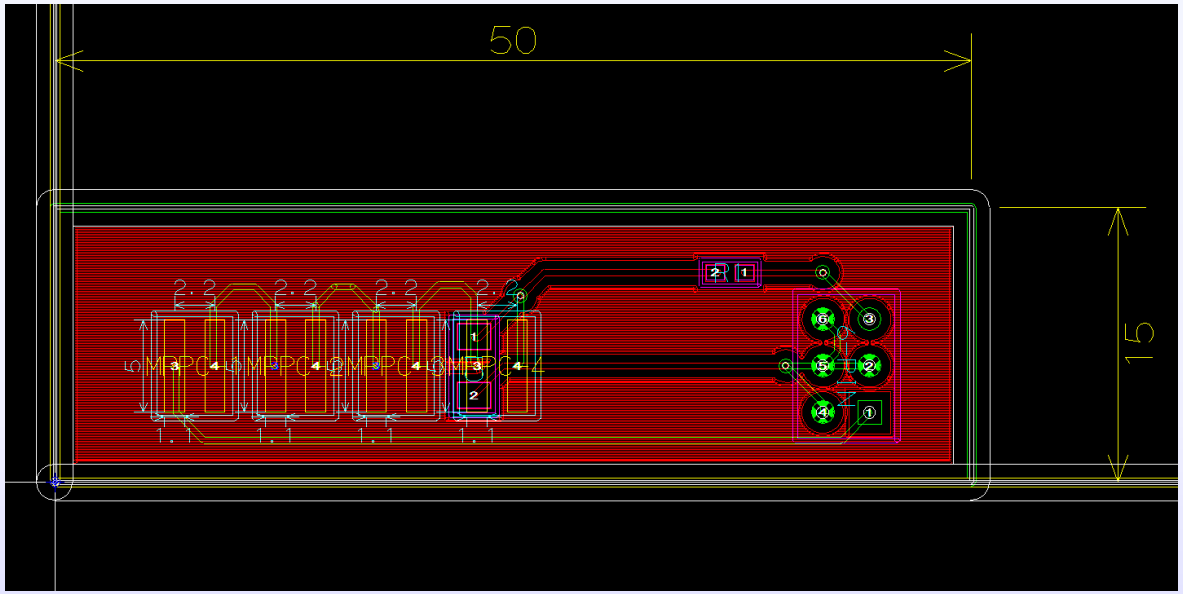
✓ Future plan: Study about readout method

1. Series connection: 直列
2. Parallel connection: 並列

✓ Task: Design for PCB of each type.

✓ Now: Making Series ver.





To do next

- Design new circuit: ~Tomorrow (or next week??)
- Scintillator Thickness & width study (Bias & Length) by cosmic-ray

- **Prepare for second presentation of B4 thesis**

From my presentation of B4 thesis mid-term presentation

ToFL

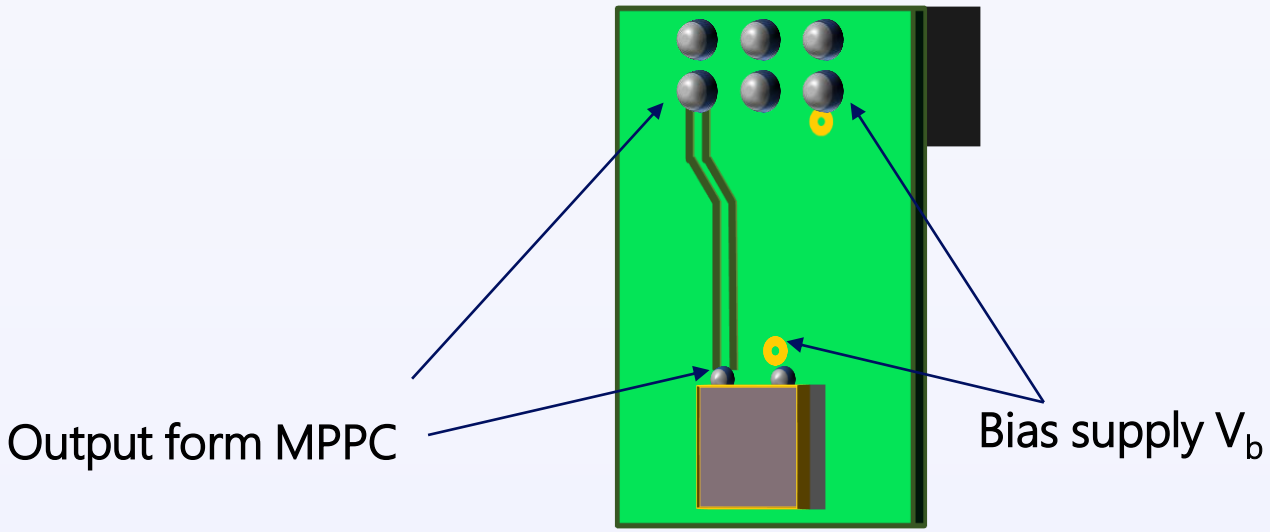
余談

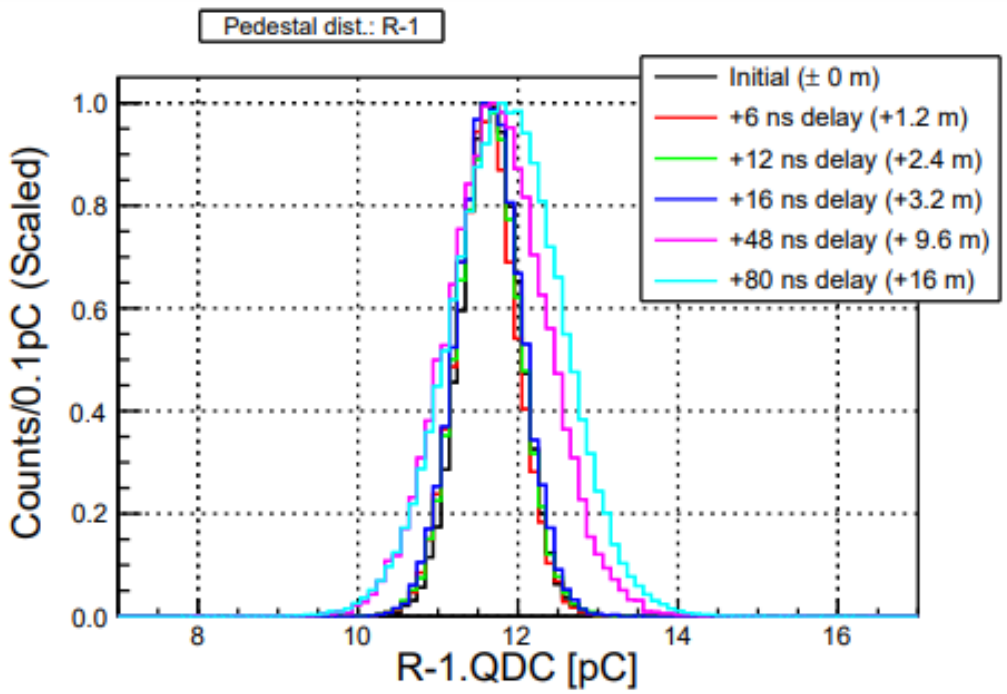
ToFL

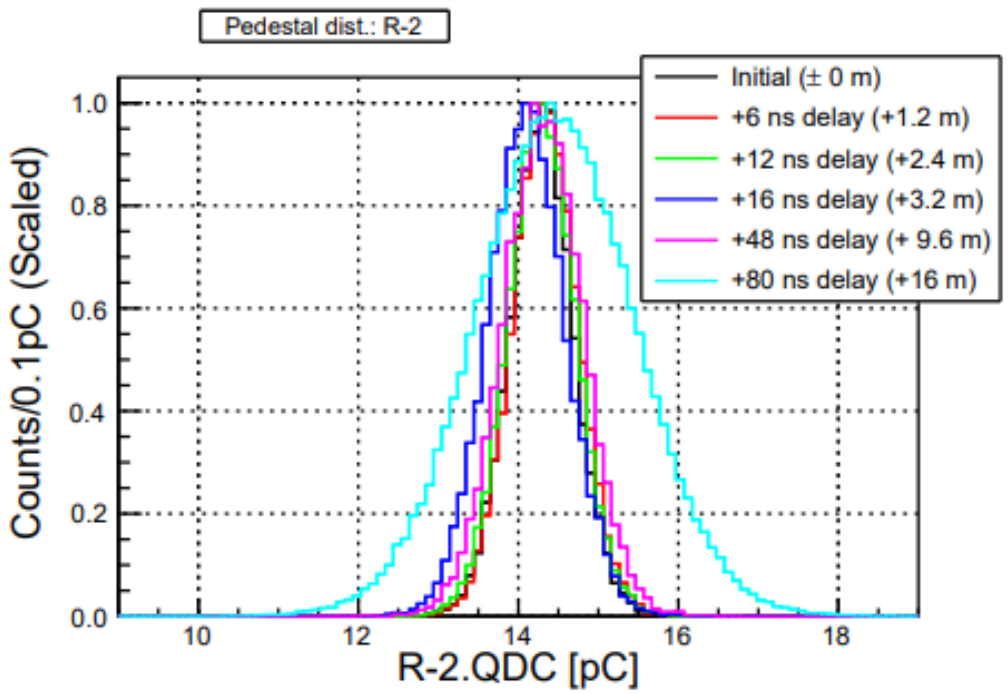
LoFt

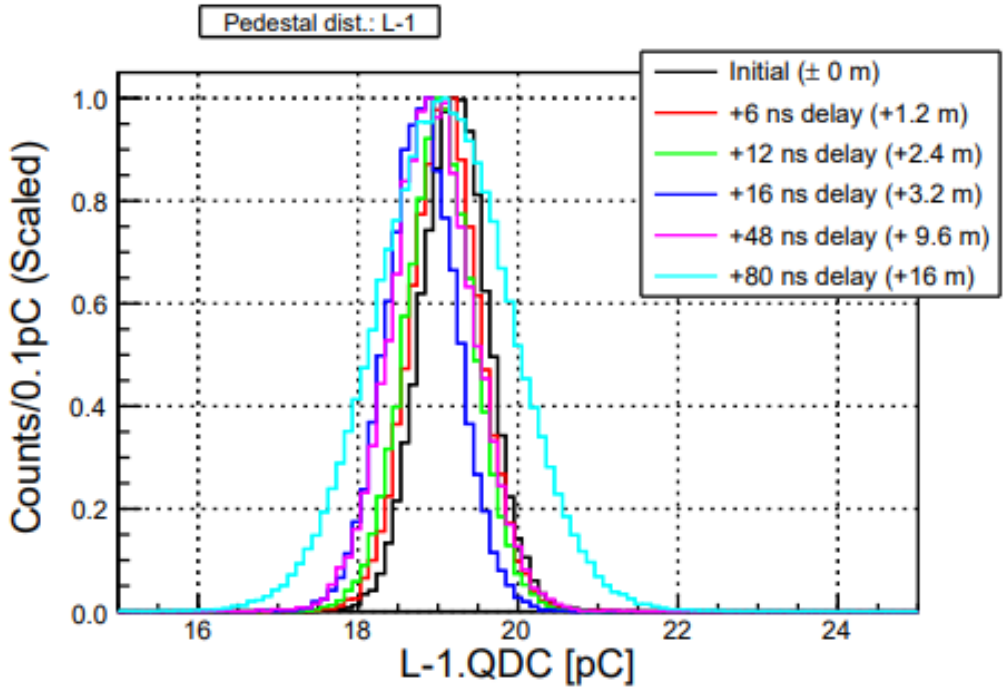
似てる(??)

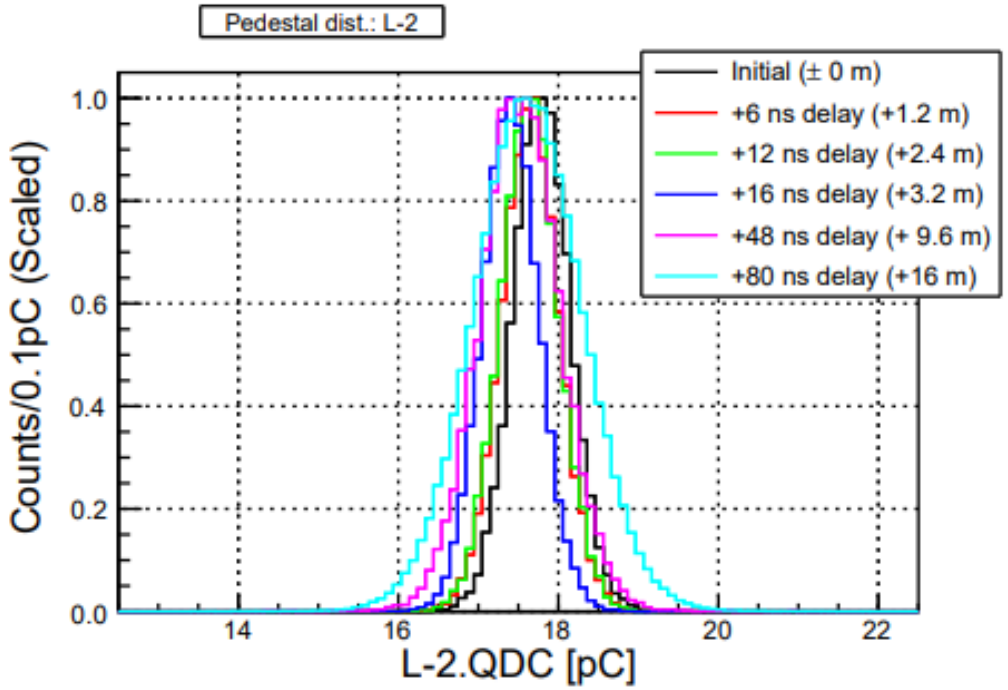
(並べてみたら言うほどでもありませんでした…)

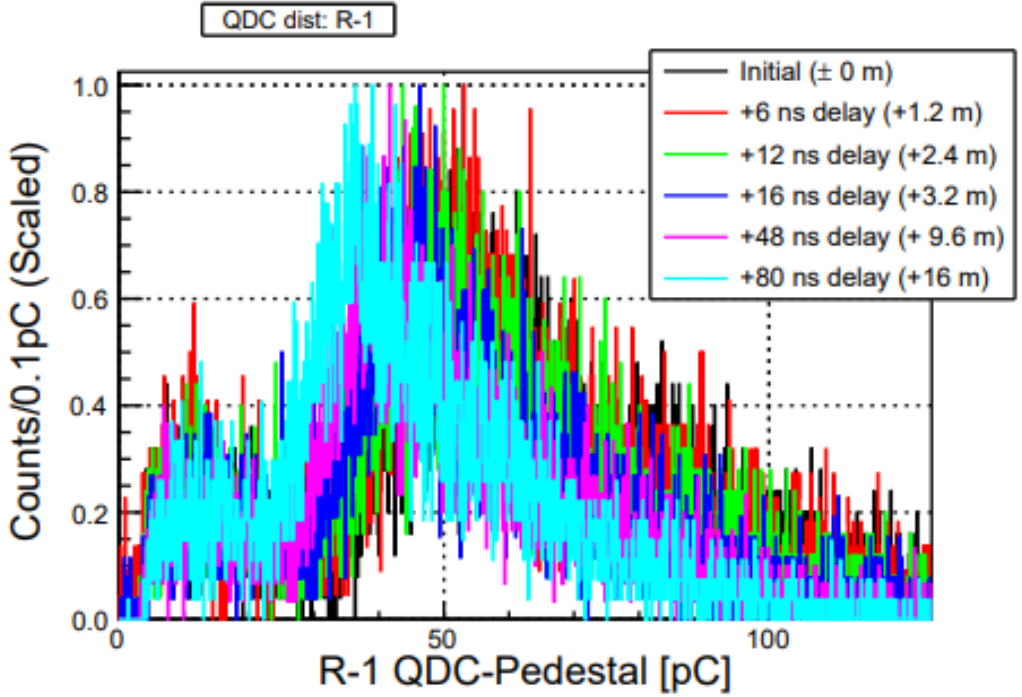

Output form MPPC
Bias supply V_b

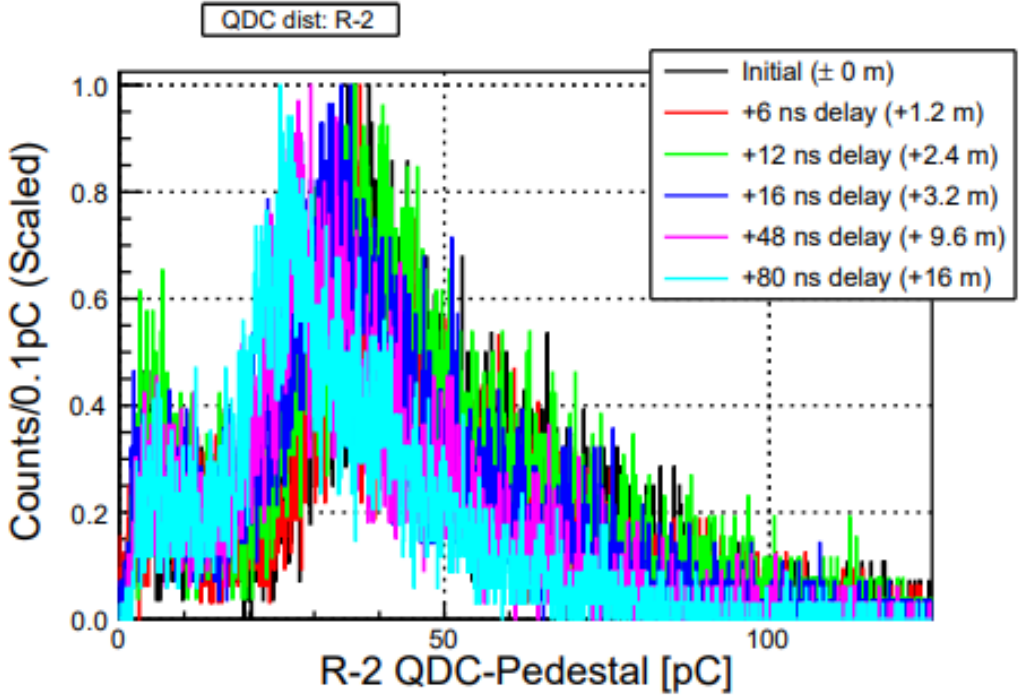

Pedestal dist.: R-1
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
R-1.QDC [pC]

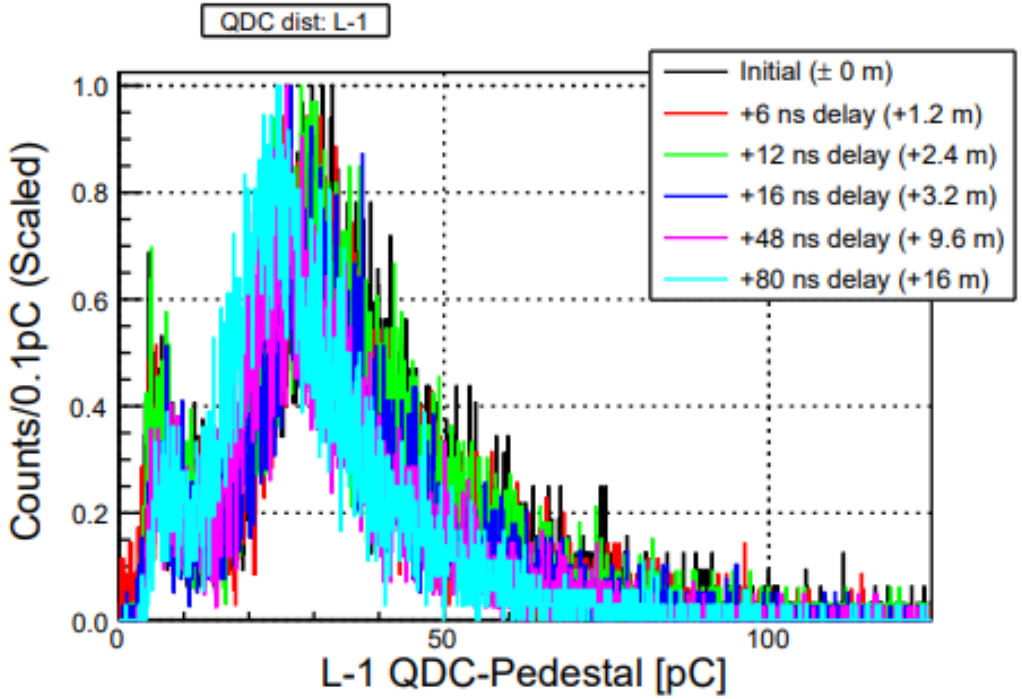

Pedestal dist.: R-2
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
R-2.QDC [pC]

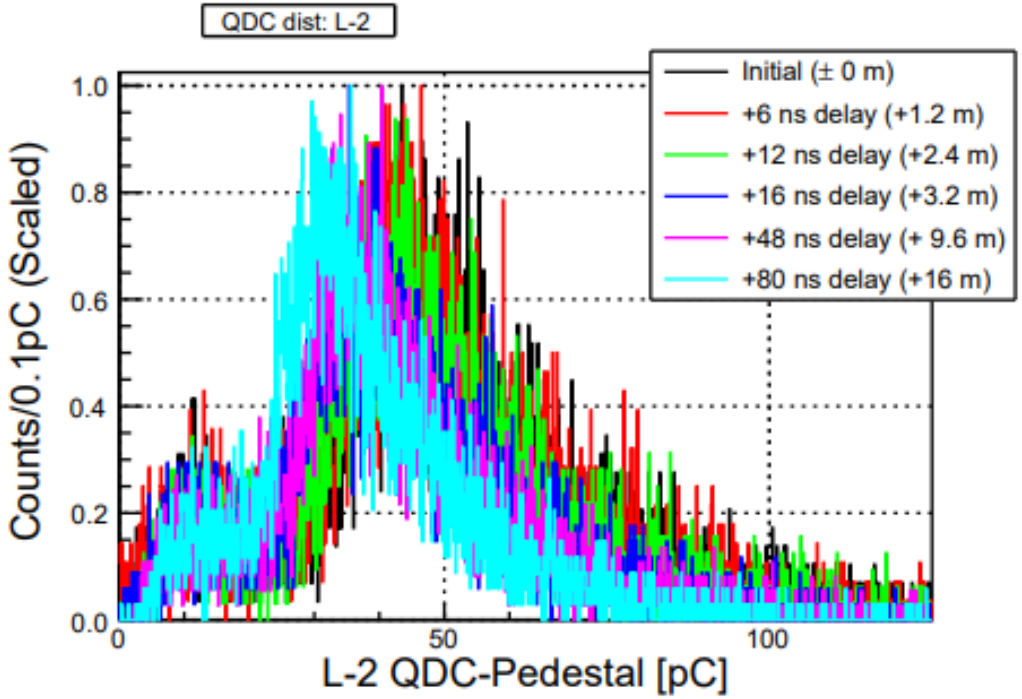

Pedestal dist.: L-1
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
L-1.QDC [pC]

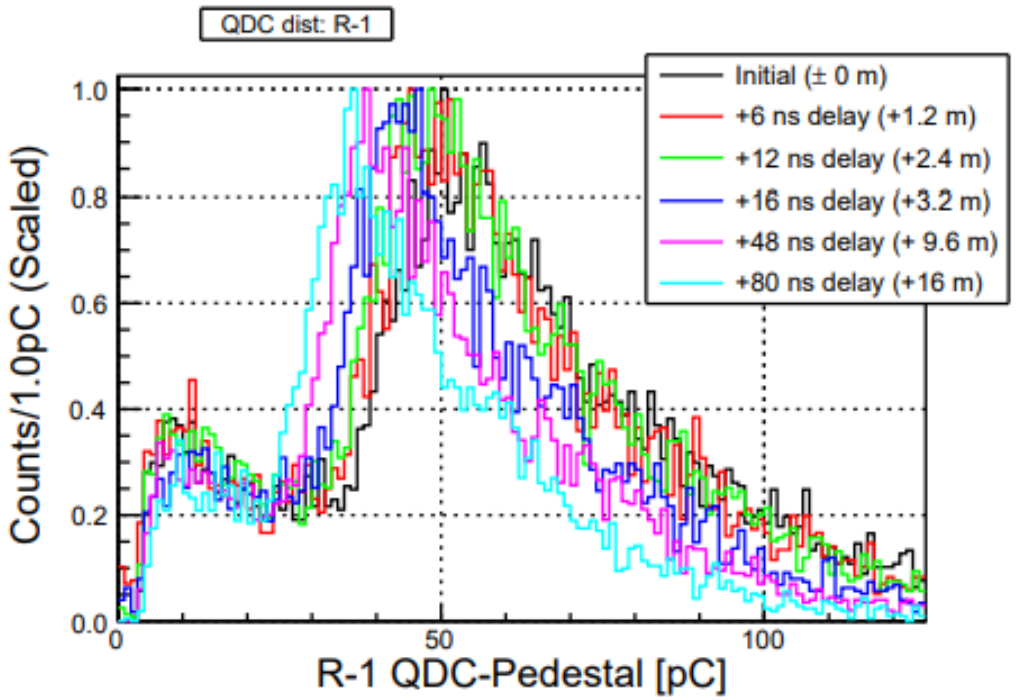

Pedestal dist.: L-2
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
L-2.QDC [pC]

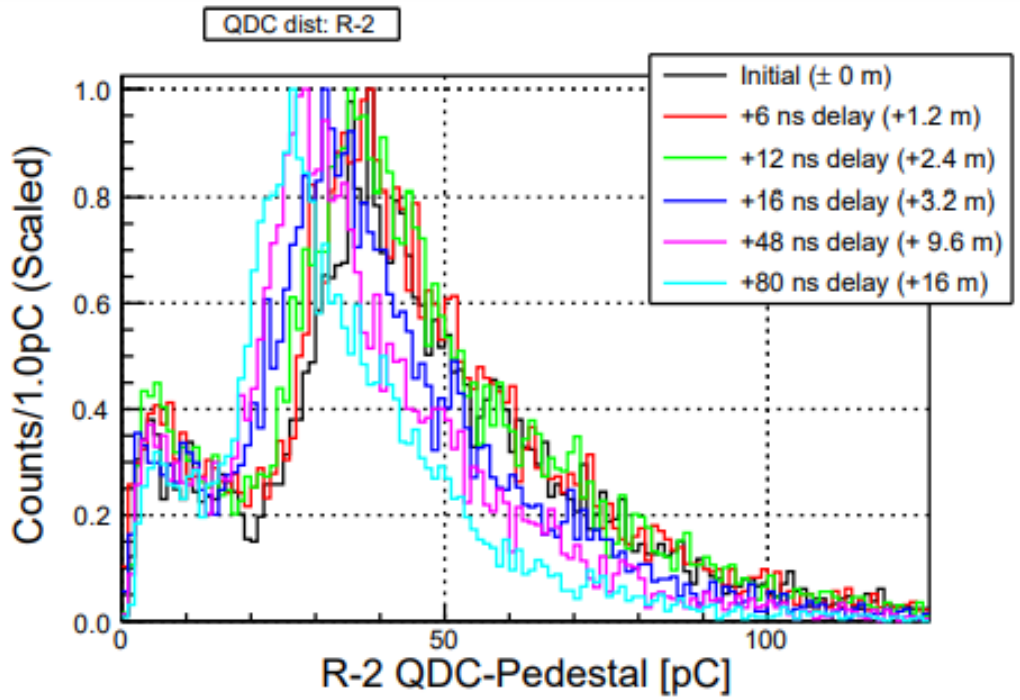

QDC dist: R-1
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
R-1 QDC-Pedestal [pC]

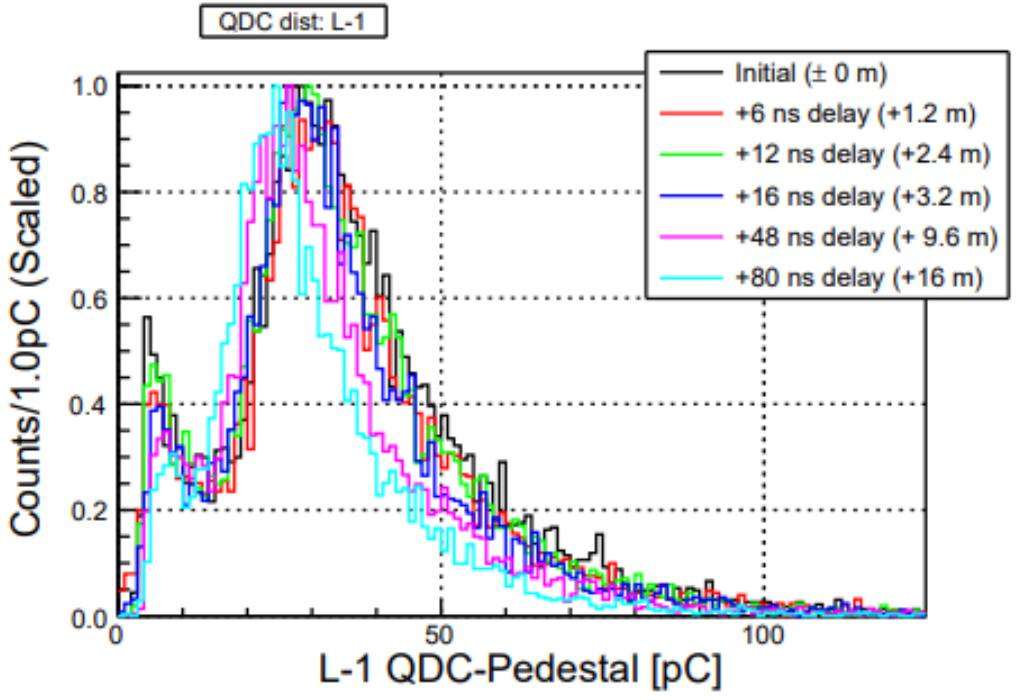

QDC dist: R-2
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
R-2 QDC-Pedestal [pC]

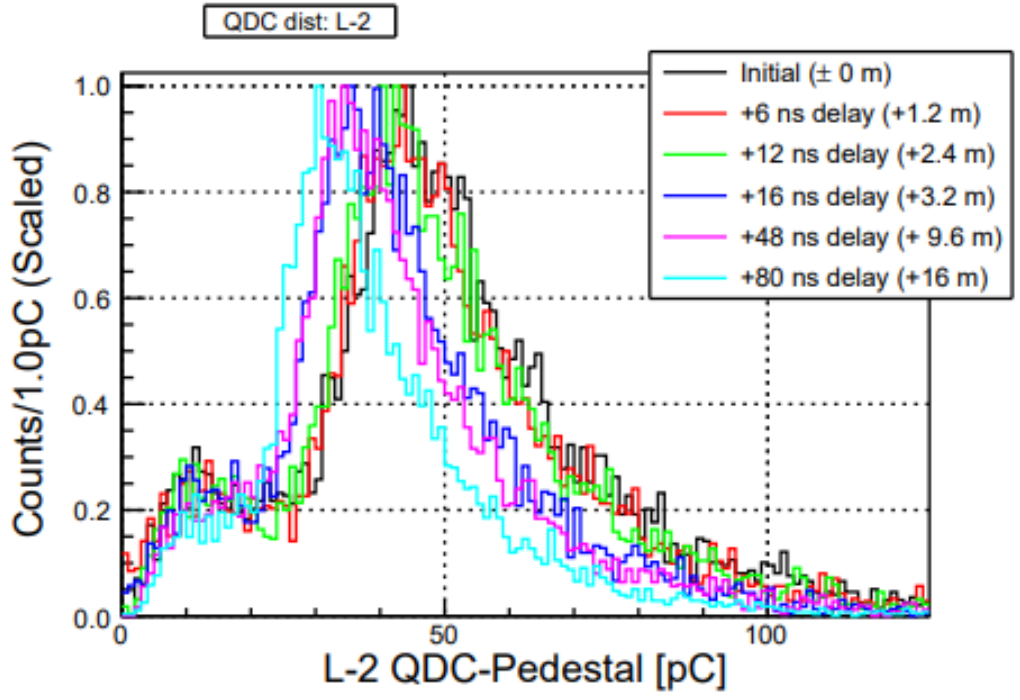

QDC dist: L-1
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
L-1 QDC-Pedestal [pC]

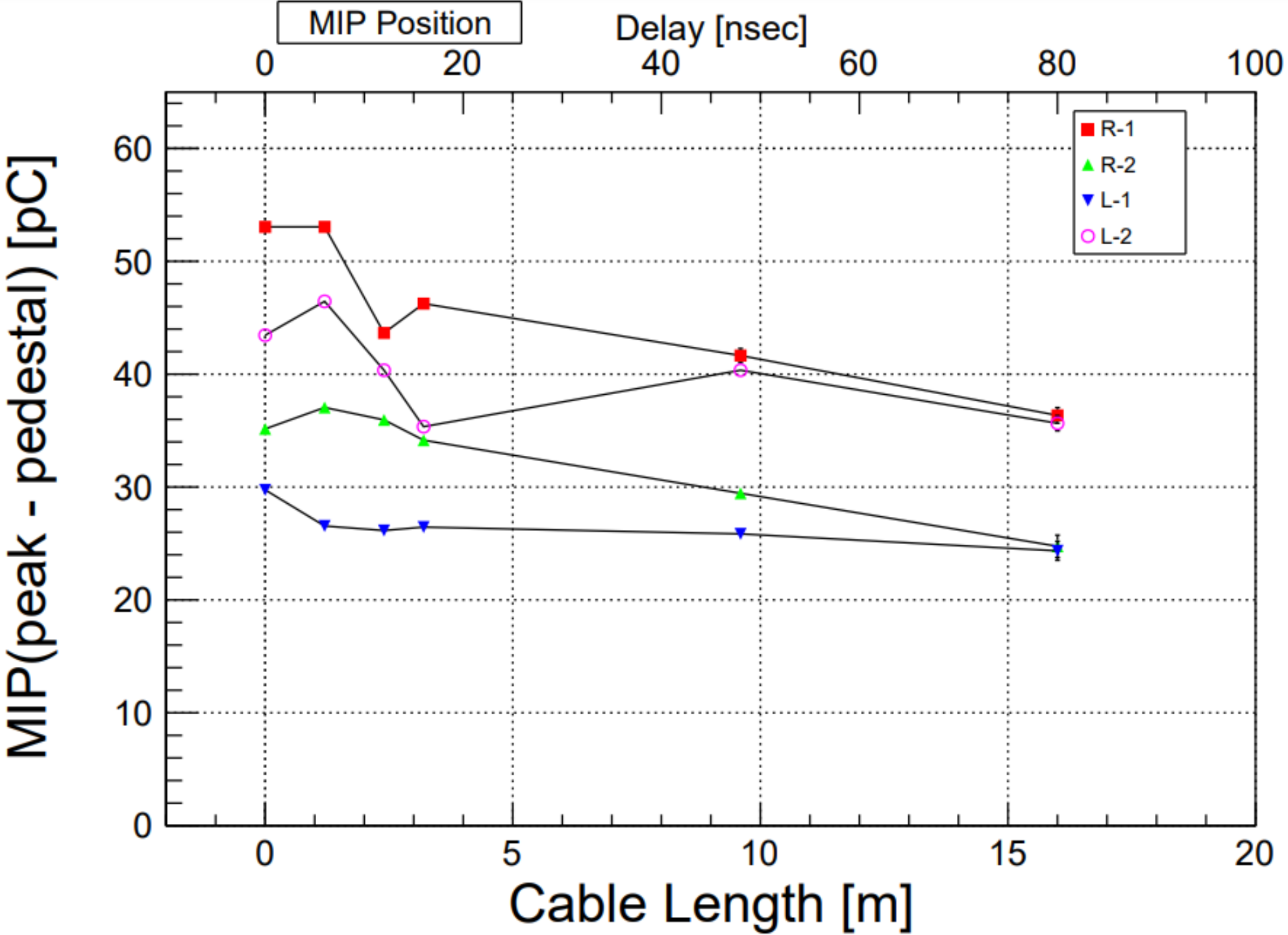

QDC dist: L-2
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/0.1pC (Scaled)
L-2 QDC-Pedestal [pC]

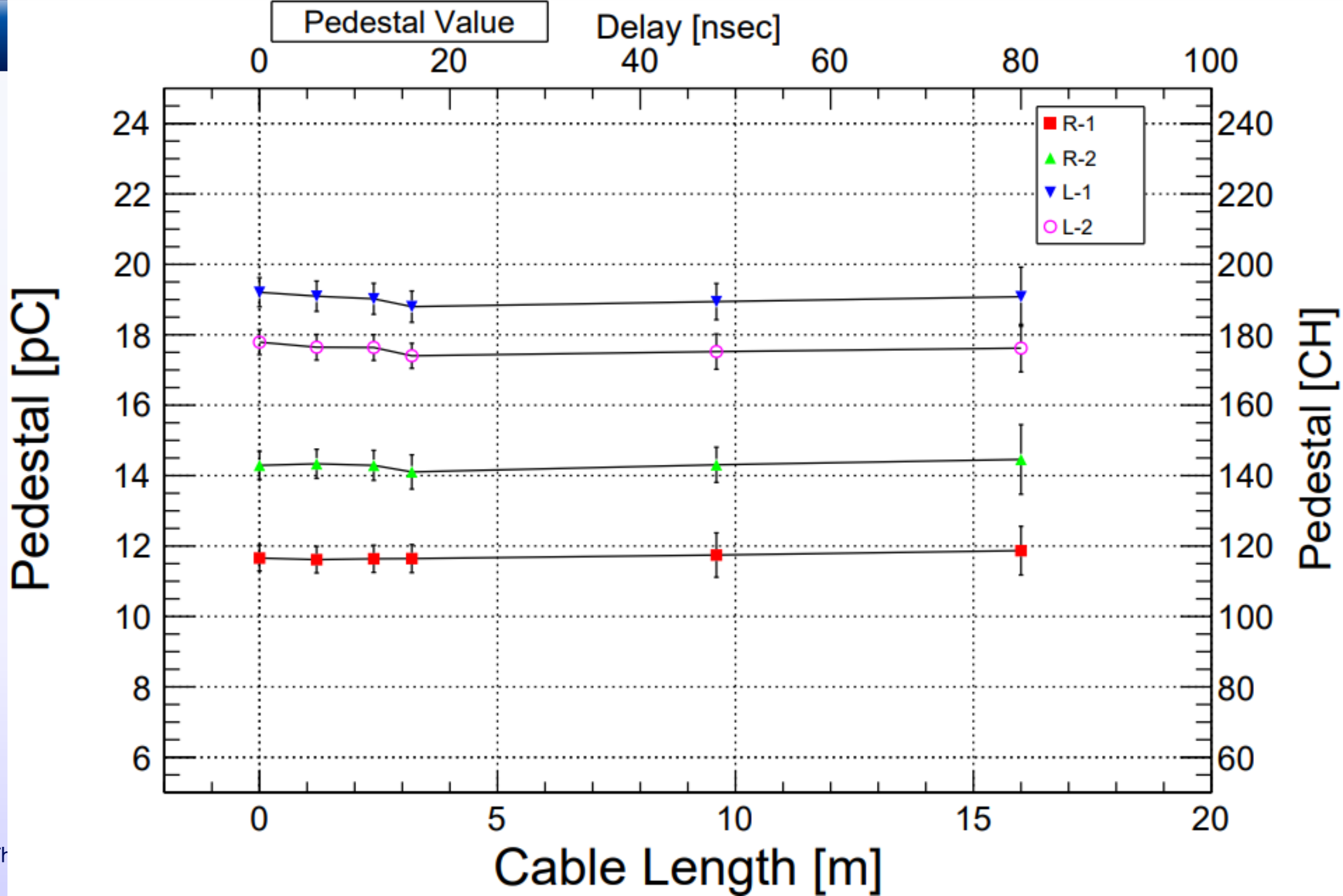

QDC dist: R-1
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/1.0pC (Scaled)
R-1 QDC-Pedestal [pC]

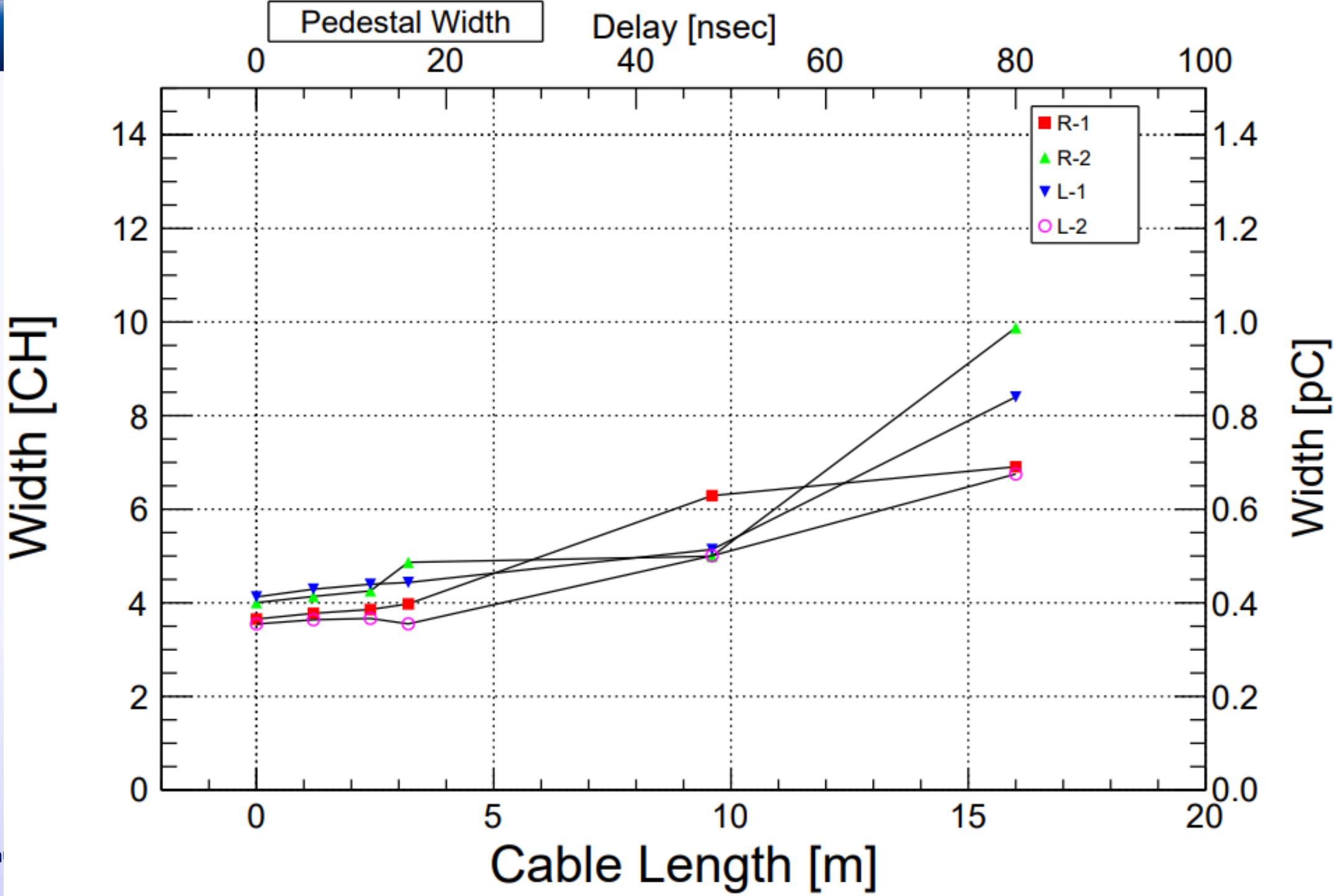

QDC dist: R-2
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/1.0pC (Scaled)
R-2 QDC-Pedestal [pC]


QDC dist: L-1
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/1.0pC (Scaled)
L-1 QDC-Pedestal [pC]


QDC dist: L-2
Initial (± 0 m)
+6 ns delay (+1.2 m)
+12 ns delay (+2.4 m)
+16 ns delay (+3.2 m)
+48 ns delay (+ 9.6 m)
+80 ns delay (+16 m)
Counts/1.0pC (Scaled)
L-2 QDC-Pedestal [pC]


MIP Position
Delay [nsec]
0
20
40
60
80
100
R-1
R-2
L-1
L-2
MIP(peak - pedestal) [pC]
0
10
20
30
40
50
60
0
5
10
15
20
Cable Length [m]


Pedestal Value
Delay [nsec]
0
20
40
60
80
100
R-1
R-2
L-1
L-2
Pedestal [pC]
Pedestal [CH]
24
22
20
18
16
14
12
10
8
6
240
220
200
180
160
140
120
100
80
60
0
5
10
15
20
Cable Length [m]


Pedestal Width
Delay [nsec]
0
20
40
60
80
100
R-1
R-2
L-1
L-2
Width [CH]
Width [pC]
Cable Length [m]
0
2
4
6
8
10
12
14
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
0
5
10
15
20

New circuit design using CADLUS X

- In CADLUS X, There's no model of 6-PIN connector (21602X3GSE)
- But 4-PIN model (21602X4GSE) exists.