Design of 4×4 multiplier from schematic to layout

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Abstract—In this paper a low power and high speed 4X4 multiplier is designed using TSMC 0.18nm CMOS Technology. The important factors in VLSI Design are power, area, speed and design time. Now-a-days, power and speed has become a crucial factor in Digital Signal Processor (DSP) Applications. However, different optimization techniques are available in the digital electronic world. The proposed approach a Low power and high speed Multiplier Design based on Modified Column bypassing technique mainly used to reduce the switching power activity. While this technique offers great dynamic power savings, due to their interconnection. In this work, a low power and high speed multiplier with Hybridization scheme is presented. This scheme is combination of booth encoder algorithm and column bypass technique is called modified column bypassing scheme. The simulations are performed in 0.18µm CMOS Technology in Cadence Virtuoso tools with operating voltage ±1.8v.

Index Terms—Multiplier, CMOS, Column Bypassing, Digital Signal Applications (DSP), Row Bypassing, Booth encoder

I. Introduction

As one of the key components of modern CPU, multiplier is a widely studied computer architecture which take the responsbility of most of the calculation operation in computer. Currently widely used multiplier inculding Booth multiplier, Sequential multiplier, combinational multiplier, Wallace tree multiplier [1]. The performance of the multiplier is a key fact that will greatly affect the performance of processors, so the design of a small, fast and energy efficiency multiplier is a prior problem we need to pay attention to today.

In this report, we will demostrate the design procedure of the 4×4 multiplier. In secition III, we will introduce the design of basic components including NAND gate, AND gate, XOR gate and invertor then we assemble them into main componet of a multiplier, half adder and full adder. In section V we will build the multiplier and the performance of the multiplier will be tested in section VI.

II. Our Problem and design idea

In this project we are assigned to design a classcial 4×4 bit multiplier as small and fast as possible, and we also wish we could use high level design to increase the design speed. To achieve our goal, we will focus on the following design principles. Firstly, we will minimize the width of each components and the space between them under the constrain of design rule, that will help us achiveve the minimum space. Secondly, we need to aviod using high layer of metal which is the main cause of delay. Finally we can find the minimun kinds of components we need by apply top-to-down design.

To design the multiplier start from the high level structure of the multiplier, as shown in Figure 1, a multiplier consists of half adder, full adder, and AND Gate, and a step futher, we can move our attention to the structure of full adder and half adder. In Fig 2 and 3, we can see the two differnt kinds of adders are consist of NAND Gate, XOR Gete, and AND Gate, while and gate can be divided into NAND Gate and invertor, so what we need is NAND Gate, Inverter and XOR Gate, though XOR Gate can be divided into more simple gates, but to reduce the space, we will design the XOR Gate as a single component.

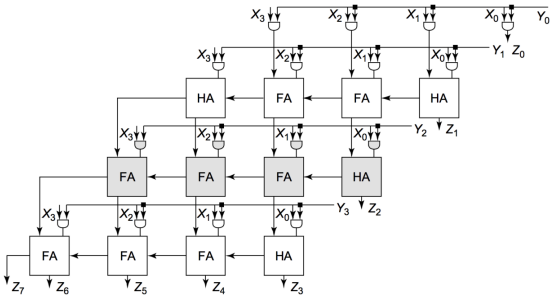

Fig. 1: High level structure of 4x4 multiplier

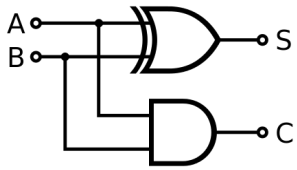

Fig. 2: Half adder

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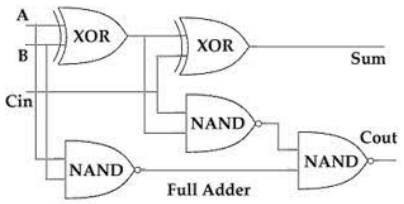

Fig. 3: Full adder

III. Design and verication of basic components

A. Inverter

The simpliest structure is Inverter consists of a pmos and a nmos as shown in Fig 4, they all have 0.18um in length, which is the minimun length of gate under 0.18 um TSMC technology, and after a balence between space and speed, we choose 4um as the width of pmos and 1.6um as the width of the nmos, to make sure all the gates perform well, the size of other gates will equivlent the inverter.

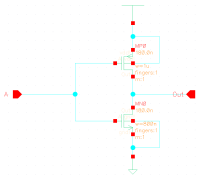

Fig. 4: Schematic of Inverter

Then we will test the performance of the inverter, we add three different extrinsic load capacitors: C1 = 15 fF, C2 = 8*C1, and C3 = 64*C1 to the output of the inverter and test its delay, the result is listed in Table I. To measure the propagation delay, we will

TABLE I: The delay of inverter

Cap	15f F		120f F		960f F	
State	Up	Down	Up	Down	Up	Down
Delay(ns)	0.125	0.068	0.553	0.263	3.918	1.792

B. NAND Gate

NAND Gate is one of the most important basic gates, to make the gate equivlent to inverter we choose 4um as the width of the PMOS, and 3.2um as the width of NMOS.

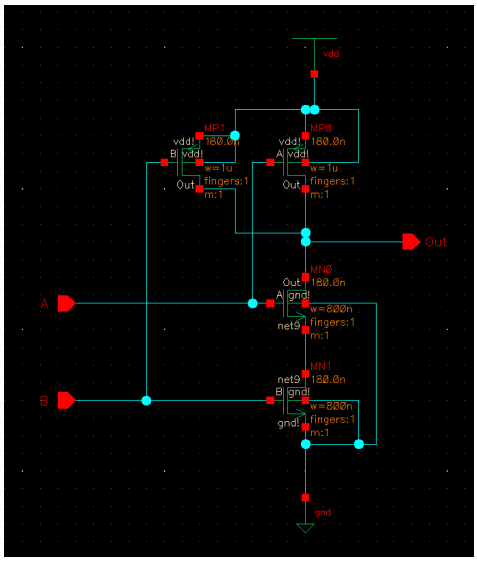

Fig. 5: Schematic of NAND Gate

The performance of NAND Gate will be tested under the same method as Inverter.

TABLE II: The delay of NAND Gate

Cap	15f F		120f F		960f F	
State	Up	Down	Up	Down	Up	Down
Delay(ns)	0.134	0.095	0.558	0.383	4.931	2.589

C. AND Gate

To make things more simplfied, we use a inverter and a NAND Gate to assemble an AND Gate, so the size of MOS transistors in AND Gate can be refered from the size of NAND Gate and Inverter.

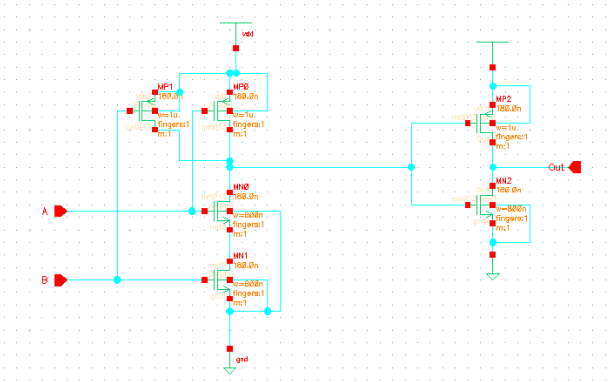

Fig. 6: Schematic of AND Gate

The performance of AND Gate will be tested under the same method as Inverter.

D. XOR Gate

For XOR Gate, we have same MOS size as Inverter, as all the PMOSs have width 4um and NMOSs have width 1.6nm.

TABLE III: The delay of AND Gate

Cap	15f F		120f F		960f F	
State	Up	Down	Up	Down	Up	Down
Delay(ns)	0.161	0.147	0.591	0.344	3.955	1.870

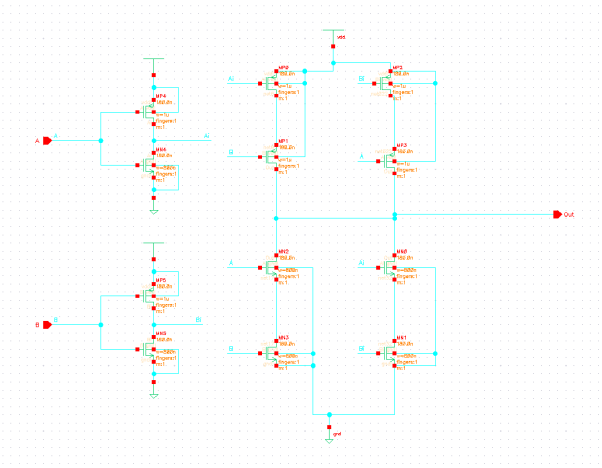

Fig. 7: Schematic of XOR Gate

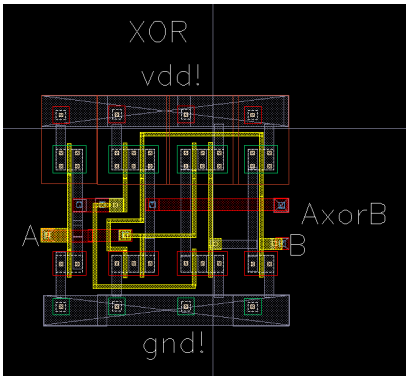

Fig. 8: Layout of XOR Gate

The performance of XOR Gate is shown in Table IV.

TABLE IV: The delay of XOR Gate

Cap	15f F		120f F		960f F	
State	Up	Down	Up	Down	Up	Down
Delay(ns)	0.259	0.101	1.088	0.392	7.689	2.496

IV. Adder

For adder, more horizontal wire are required, it is hard to avoid using high level metal wire and the area will be big if we put all the MOS pairs in a line. To solve this problem, we put all the pairs in to two layers, and we also use poly and metal1 as wire as many as possible so we can reduce the area and delay. More importantly we put the pairs in two row, so wiring vertally is possible, which greatly shorten the length of wire.

A. Half Adder

A half adder is a conbination of a AND Gate and a XOR Gate, each of their input A and B are connected together and the outout of XOR Gate is defined as Sum, the outpt of AND is defined as Carry. The size of the transistors can be refered from XOR Gate and AND Gate introduced before.

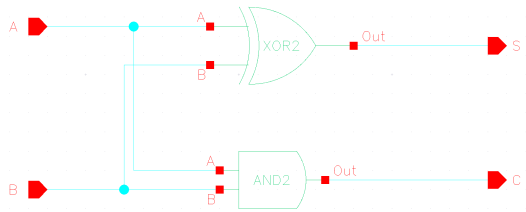

Fig. 9: Schematic of Half Adder

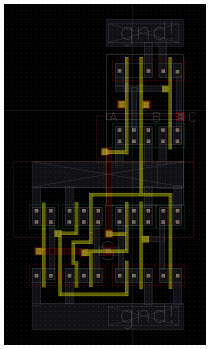

Fig. 10: Layout of Half Adder

B. Full Adder

As shown in Fig 11, a full adder is a combination of XOR Gates and NAND gates, the structure here is simplified from the classical design in which a full adder contains two half adder and AND Gate, so we can save a lot of area.

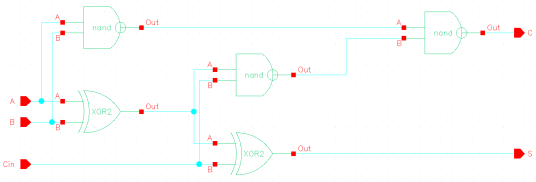

Fig. 11: Schematic of Full Adder

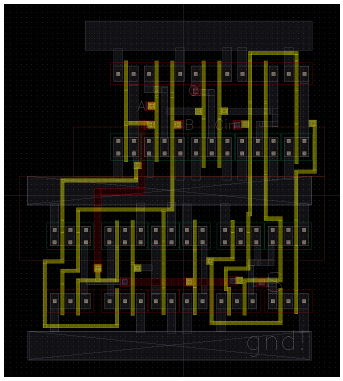

Fig. 12: Layout of Full Adder

V. Assemble of the multiplier

A. Schemetic

The schematic of the multiplier is shown in Fig 13, it has contians many full adders half adders and and gates. we connect them together as the design shown before.

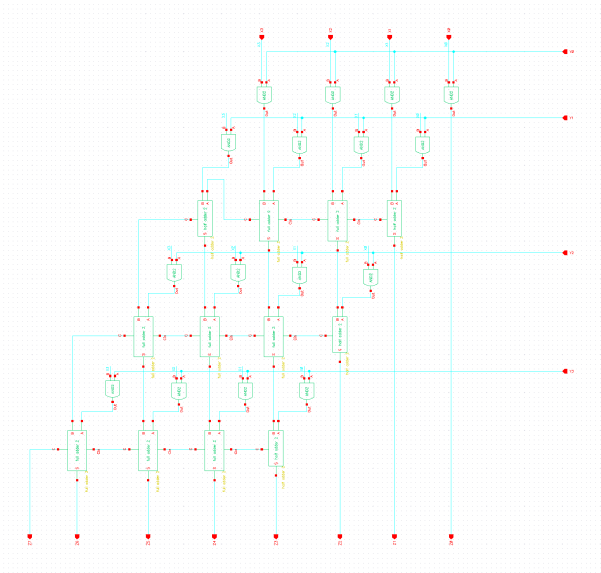

Fig. 13: Schematic of 4×4 bit multiplier

B. Layout

In the layout, we use the low level layer as wire to reduce the delay time. We use poly, metal1, metal2, and some metal3 as the connection wire between each components.

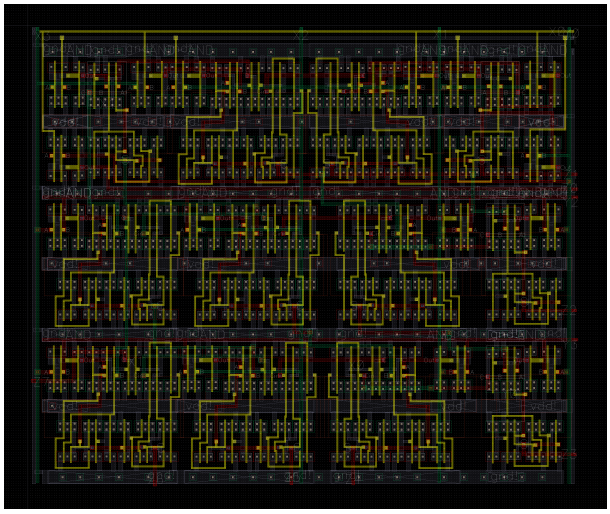

Fig. 14: Layout of 4×4 bit multiplier

VI. Varication and benckmark of the multiplier

After we finish the design of the multiplier we need to test the performance of the multiplier.

A. Area of the Layout

As we tested, the area of the layout is ((0.39, -52)(62, 0)), $3276 \mu m^2$

B. propagation delay

Here we will compare the post-layout delay measurements with the schematic level delay measurement 50f F cap is attached to the output. We apply two set of input to the multiplier so we can get the transfer data of all output. The first set is $0000 \times 1111 = 11100001$ and the second set is $0010 \times 1111 = 00011110$. As we measure, the maxmun down-to-up delay is 1.915ns and uo-to-down delay is 0.96ns, the plots are shown in Appendix.

VII. Conclusion

In this project, we experience the procedure of Top to Down design and Down to Top Develop, we first design the multiplier in hignest level, then we gradually split each of the component so we can get the basic logic gate we need. The development procedure start form the bisic logic gate, we design half adder and full adder based on these logic gates, finally the multiplier will be constructed by adders. In each level a serises of test were done to make sure the design functions well. During the layout procedure, we change the way transistors were put, so the size and delay is reduced.

References

[1] S. Kumar, 'A Review of Different Type of Multipliers and Multiplier-Accumulator Unit.', vol. 2, no. 4, p. 5, 2013.
[2] N. Maheshwari, 'A Design of 4X4 Multiplier using 0.18 um Technology', International Journal of Latest Trends in Engineering and Technology, vol. 2, no. 1, p. 7, 2013.
[3] M. Krishnamurthy, 'A. Joseph vijay1, Scholar, Department of', p. 10.

[4] N. Singh and M. Z. Alam, 'Design and Implementation of Pipelined 4-Bit Binary Multiplier Using M.G.D.I. Technique', Management Research, vol. 2, no. 3, p. 7, 2014.
[5] 'Design of Low Power and High Speed 4X4 Multiplier using Modified Column Bypassing Scheme for DSP Applications', ijrte, vol. 8, no. 2S3, pp. 643–647, Aug. 2019, doi: 10/gj4nkd.
[6] M. H. Riaz, S. A. Ahmed, Q. Javaid, and T. Kamal, 'Low power 4×4 bit multiplier design using dadda algorithm and optimized full adder', in 2018 15th International Bhurban Conference on Applied Sciences and Technology (IBCAST), Islamabad, Jan. 2018, pp. 392–396. doi: 10/gj4nkf.
[7] S. Agwa, E. Yahya, and Y. Ismail, 'Variability mitigation using correction function technique', in 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), Abu Dhabi, United Arab Emirates, Dec. 2013, pp. 293–296. doi: 10/gj4nkg.

VIII. Appendix

A. Delay of basic Gates

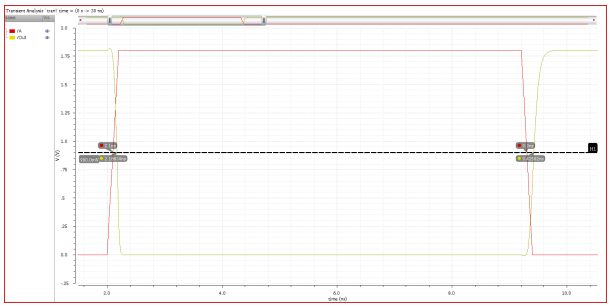

Fig. 15: Delay of Inverter with output capacitance 15f F

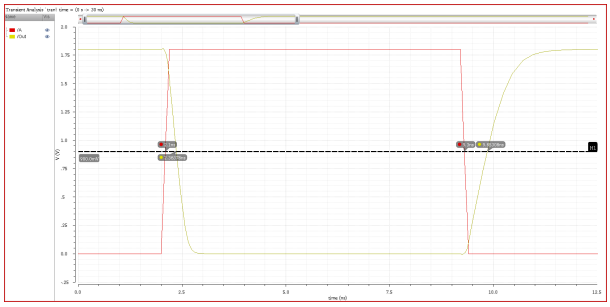

Fig. 16: Delay of Inverter with output capacitance 120f F

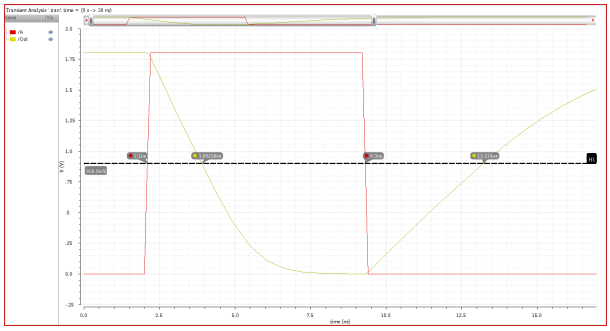

Fig. 17: Delay of Inverter with output capacitance 960f F

1) Inverter:
2) NAND Gate:
3) AND Gate:
4) XOR Gate:

B. Delay of the multiplier

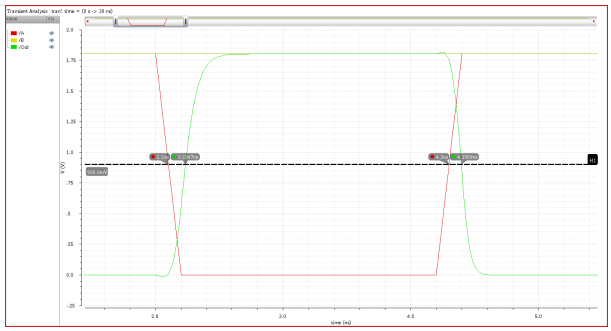

Fig. 18: Delay of NAND Gate with output capacitance 15f F

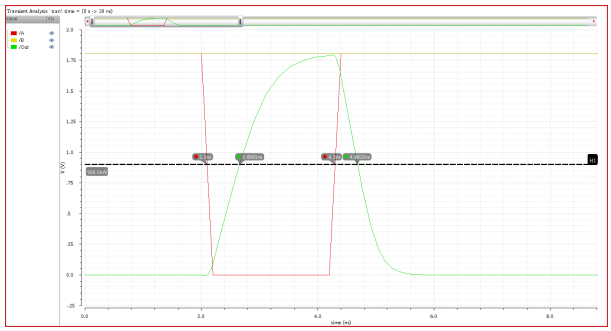

Fig. 19: Delay of NAND Gate with output capacitance 120f F

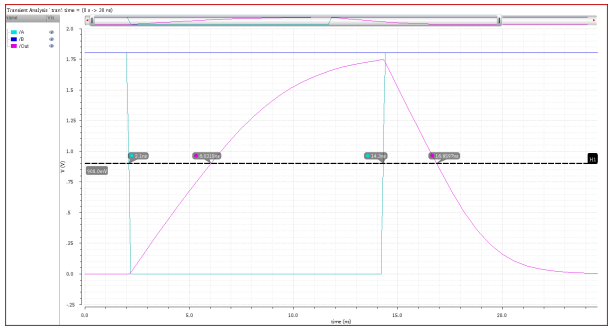

Fig. 20: Delay of NAND Gate with output capacitance 960f F

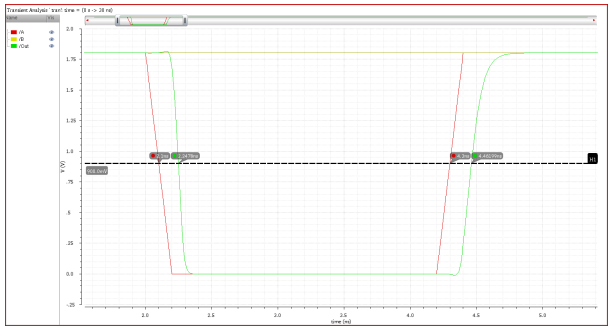

Fig. 21: Delay of AND Gate with output capacitance 15f F

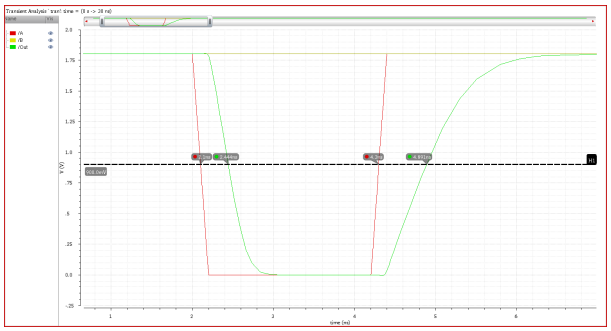

Fig. 22: Delay of AND Gate with output capacitance 120f F

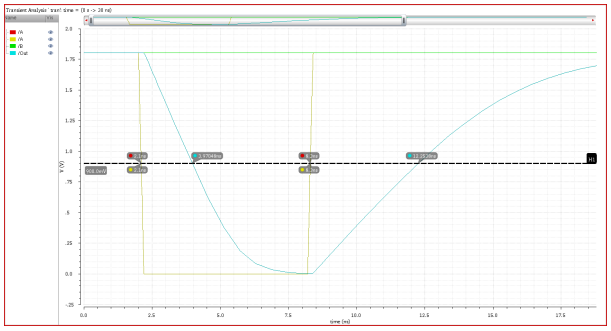

Fig. 23: Delay of AND Gate with output capacitance 960f F

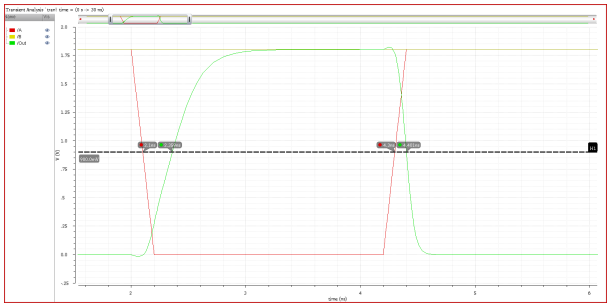

Fig. 24: Delay of XOR Gate with output capacitance 15f F

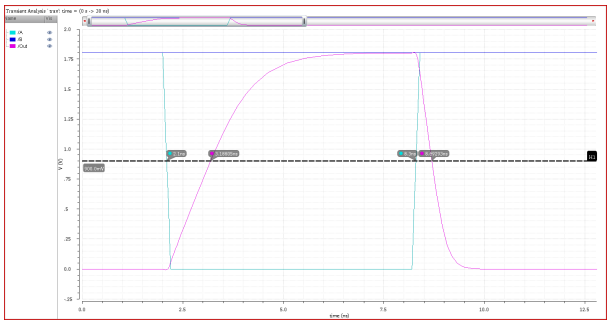

Fig. 25: Delay of XOR Gate with output capacitance 120f F

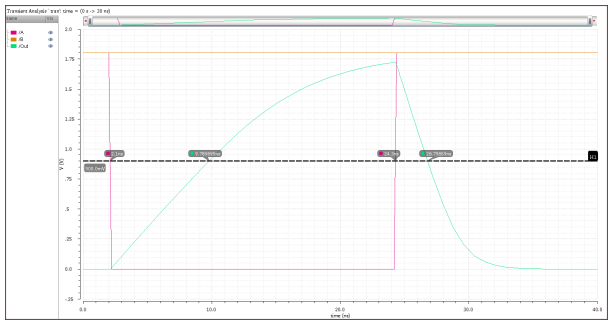

Fig. 26: Delay of XOR Gate with output capacitance 960f F

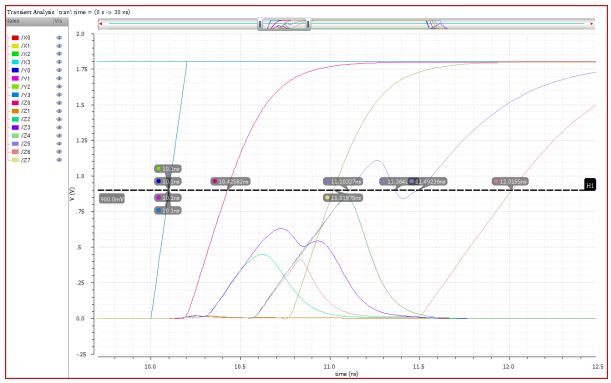

Fig. 27: Low to high delay of 11100001

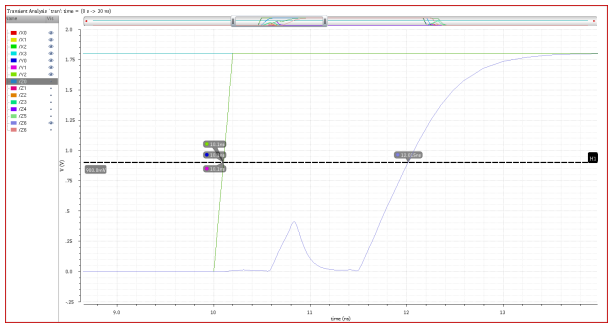

Fig. 28: Low to high delay of 11100001

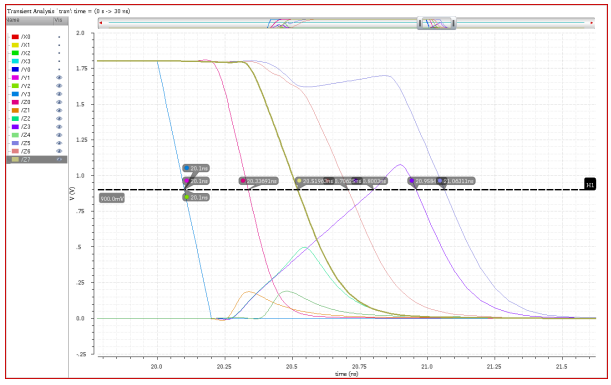

Fig. 29: High to low delay of 11100001

Fig. 30: High to low delay of 11100001