Project Report Format and Deliverables

Names of Group Members
E-mails of Group Members

The report should not exceed eight pages and it is recommended to include the following sections.

I. Introduction

In the introduction, students are asked to give a short introduction on the subject. This would include:

1. A brief background study related to the topic.

2. Motivation of the project.

3. Possible application of the design.

II. Problem Formulation

Explain briefly the objectives of the project. For example the design of low power array multiplier, with minimum delay and minimum silicon area. Explain how you achieve these objectives.

III. CMOS Design and Simulation Results

In this section students should first start by describing the global architecture with clear drawing(s). A top- down description is encouraged. In this section students are encouraged to go through the different circuit diagrams as well as the sizing of the transistors, simulation layout and post-layout simulation. Students are encouraged to put more emphasis on how they are taking care of the objectives set. This section should also include the analysis of the critical delay, study of the floor-planning for the different blocks, and the final circuit together with the physical layout and its verification. The details that should be covered in this section include the following parts with tables and descriptions.

(1) Standard cell library

You need to develop a library of basic (standard) cells that are used for the multiplier design. All the components in the library (inverters and more complex gates that are needed for the final multiplier design) must be briefly introduced. Prepare a Table with

the transistors sizes (both width and length in micrometers), output low-to-high propagation delay, and output high-to-low propagation delay of each basic cell that is used in the multiplier design. If you have different sizes of the same type of logic gate, you need to report the size and delay of each different sized gate in your library. Produce the delay data using post-layout simulation for each type of gate. Add the Table in your report. Apply an input signal with rise and fall times of 0.2 ns (10% to 90% signal transition time) for measuring the delays. For each basic gate, report three different delays with three different extrinsic load capacitors: C1 = 15 fF, C2 = 8*C1, and C3 = 64*C1. Discuss the relationship between delay and extrinsic load capacitance in the report. How does this relationship change as you go from a CMOS inverter to more complex gates with more than one input? Provide your answers in the report.

15f
120f
960f

(2) Half Adder

Explain the circuit structure and operation of the half adder that is used in multiplier design. Provide the circuit schematic in the report. Provide the sizes (both width and length in micrometers) of all the transistors.

(3) Full Adder

Explain the circuit structure and operation of the full adder that is used in multiplier design. Provide the circuit schematic in the report. Provide the sizes (both width and length in micrometers) of all the transistors.

(4) 4x4-bit Array Multiplier

Explain the structure and operation of the array multiplier. Provide the circuit structure in the report. Clearly label all the inputs and outputs. Clearly show all the connections among various components. Determine the number of critical (longest) delay paths in the 4x4-bit array multiplier. Identify and report the input vectors that excite these critical propagation delay paths. Show one of these critical delay paths on the figure. Measure the propagation delay of the multiplier with schematic level simulation. Assume each product output drives 50 fF extrinsic load capacitor. Report the delays.

(5) 4x4-bit Array Multiplier Layout Area and Delay

Show the layout of your array multiplier in the report. Report the area of your layout. Measure the post-layout propagation delay and report it in your report. Assume each product output drives 50 fF extrinsic load capacitor. Compare the post-layout delay measurements with the schematic level delay measurement. Explain the differences. Discuss the limitations of the schematic level circuit simulation tool. Discuss the importance of accurate resistance and capacitance extraction for correct delay estimation with CADENCE tools.

IV. Conclusions

A conclusion on the project should be provided here. Students should attempt to answer the following questions: What did you achieve in this project? What were the difficulties? How do you propose to further improve this work?

References (list all the references you used, such as papers, books, website links, etc.)

[1]. Author, Journal or proceedings, pages, Vol. Number, Publisher and Year.