



# Analog Integrated Circuits Project Report

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## LNA

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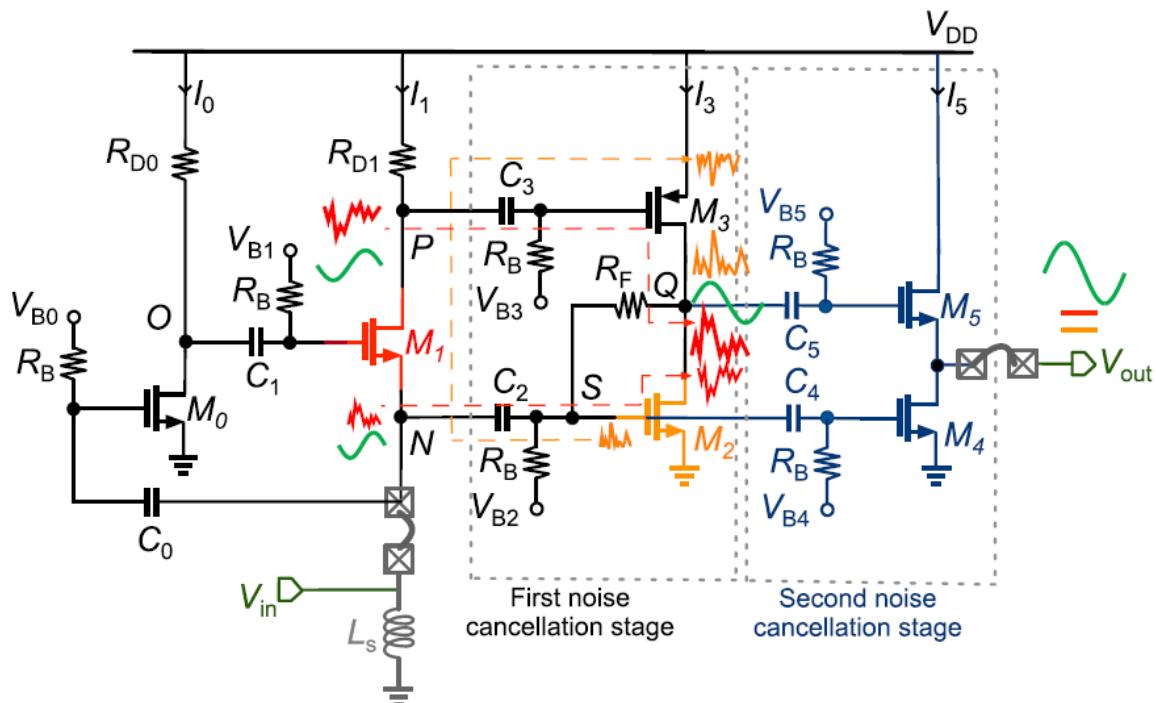
## 1 | Introduction

We simulated a two-stage low-noise amplifier with Cadence-Virtuoso, based on the paper *A 20 MHz-2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS* written by Amir Bozorg and Robert Bogdan Staszewski. In our final simulated circuit, using the Virtuoso Cadence with transistor models 'ami06N' and 'ami06P', the S11 demonstrates a value of less than -10 dB from the range of tens of megahertz up to around 2.9 GHz. At a frequency of 1 GHz and 1.2 GHz, the noise figures are 4.13 dB and 4.66 dB, respectively, while the voltage gains are 16.66 dB and 14.02 dB, respectively, at the same frequencies.

The originally proposed structure of this two-staged low-noise amplifier is discussed in section 2. Followed by the modified structure is represented in section 3, along with some basic analysis of the circuit and the simulation results with Cadence-Virtuoso, as the DC operating points, scattering parameters, noise figure, gain, and linearity. The layout of the circuit is demonstrated lastly in section 4.

## 2 | The Original Structure

The reference paper of our project is '*A 20 MHz-2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS*', from Amir Bozorg and Robert Bogdan Staszewski, which can be found in <https://ieeexplore.ieee.org/document/9493708> (DOI: 10.1109/TCSI.2021.3092960). The initially proposed structure is as shown in Figure 2.1 with the corresponding parameters listed in Table 2.1, 2.2, 2.3 and 2.4.



**Figure 2.1:** Proposed Two-Fold Noise Cancellation LNA

This architecture uses a common-gate input branch of M1 to provide wideband input

matching to  $50\Omega$ . Then follows two stages of common-source structure to implement the noise-cancelling, where the first NC stage consists of a pMOS/nMOS pair of M3 and M2, and the second NC stage indicates the branch of M5 and M4. To be more precise, the first noise-cancelling stage is used to cancel the channel thermal noise originated by the input transistor M1, by amplifying the voltage noise N through M2 and adding it to the voltage noise P amplified through M3, which is also a main part of the structure in a conventional noise-cancellation technique. However, the noise of M2 and M3 could also negatively impact the overall noise performance, where M2 represents the dominant noise source as the input matching stage does not provide enough gain. The second noise-cancelling stage is therefore utilized to cancel the channel thermal noise of M2 and M3.

Moreover, the external input shunt inductor  $L_s$  is placed at the source of M1 to provide a DC current path, meanwhile cancelling the deleterious effect of the parasitic capacitance of transistors M0, M1, M2, and M4. The value of  $L_s$  is set as  $1.3\mu H$  to guarantee a proper input matching condition with input impedance reaching about  $50\Omega$  and  $S11$  lower than  $10dB$ .

**Table 2.1:** Size of the Transistors

<b>M0</b>	(1um/180nm) × 20
<b>M1</b>	(1um/30nm) × 8
<b>M2</b>	(1um/180nm) × 30
<b>M3</b>	(1um/50nm) × 12
<b>M4</b>	(1um/50nm) × 8
<b>M5</b>	(1um/20nm) × 16

The multiplier shown in the above Table 2.1 represents the dimension of the transistors, which can be set in the 'multiplier' in the transistor settings.

**Table 2.2:** Values of Resistors and Capacitance

$R_{D0}$	$R_{D1}$	$R_F$	$R_B$	$C_{0-5}$
$560\Omega$	$780\Omega$	$20k\Omega$	$50k\Omega$	$1pF$

The resistance  $R_F$  is a negative feedback resistor, which is used to prevent the variation of DC voltage at node Q, as node Q is of high impedance and its voltage can vary substantially.

**Table 2.3:** Biase Voltage

$V_{B0}$	$V_{B1}$	$V_{B2}$	$V_{B3}$	$V_{B4}$	$V_{B5}$
0.65V	0.50V	0.48V	0.35V	0.60V	0.70V

**Table 2.4:** Measured Current

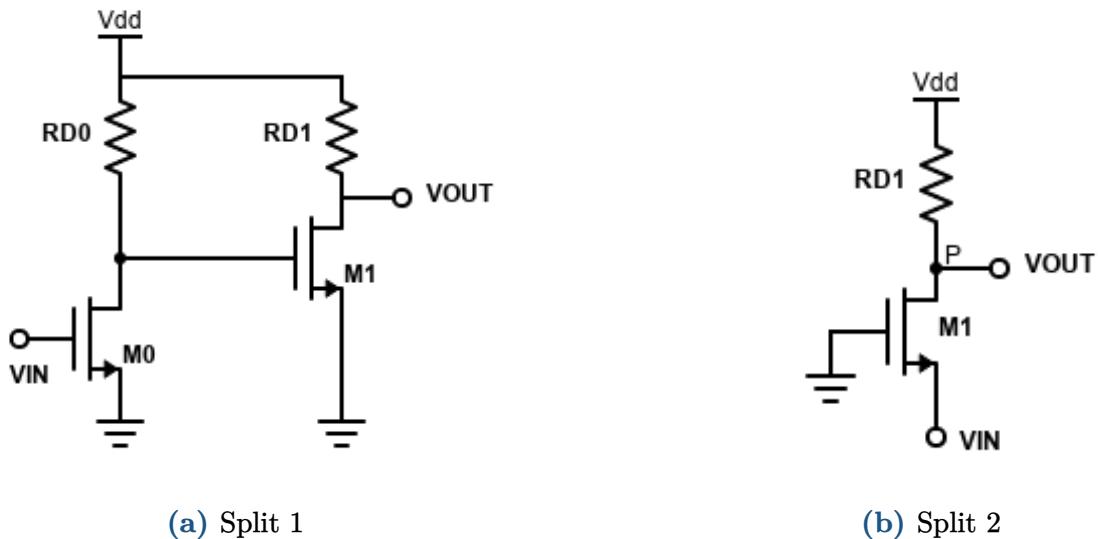
$I_0$	$I_1$	$I_3$	$I_5$
1mA	0.7mA	1.3mA	1.1mA

## 3 | Analyses and Simulation

### 3.1 | Circuit Analyse

According to the originally proposed circuit in the referenced paper, as in Figure 2.1, the analysis of the circuit is as follows.

Starting from the input impedance, which is a critical parameter to determine the level of input matching with S11. This value is related to the branches of M0 and M1. Above all, we split the input into two parts to derive each equivalent impedance, in order to obtain the total equivalent transconductance of the two branches, the circuits are as shown in Figure 3.1.


**Figure 3.1:** Analyzed circuit for input impedance, by splitting the input

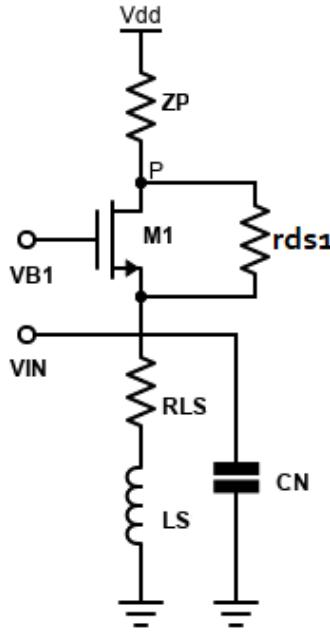
The separate equivalent impedance seen from Figure 3.1a and Figure 3.1b respectively are,

$$G_1 = (-g_{m0}R_{D0})(-g_{m1}) = g_{m0}g_{m1}R_{D0} \quad (3.1)$$

$$G_2 = g_{o1} + g_{m1} + g_{mb1} \quad (3.2)$$

Summing the two components up, the equivalent transconductance of M0 and M1 can be obtained, lumping with the body effect of M1,

$$G_{M1} = G_1 + G_2 = g_{m0}g_{m1}R_{D0} + g_{o1} + g_{m1} + g_{mb1} = (1 + g_{m0}R_{D0})(g_{m1} + g_{mb1}) \quad (3.3)$$



**Figure 3.2:** Equivalent circuit for the input stage at M1, adding the external inductor and its series resistance

An equivalent circuit for the branch of M1 is shown in Figure 3.3, which has been taken into account with the external values of the series inductor, the equivalent impedance, and parasitic capacitance.

The upper part equivalent resistance seen from the input can be expressed as,

$$R_{in} = \frac{r_{ds1} + Z_P}{1 + G_{m1}r_{ds1}} \quad (3.4)$$

where  $Z_P$  is the equivalent small-signal impedance seen from the drain of M1 towards the ground, which is expressed in Equation 3.5, and  $r_{ds1}$  is the drain-to-source resistance of M1.

$$Z_P = R_{D1} \left\| \left[ r_{ds1} + \frac{1}{sC_N} \| sL_S (1 + G_{m1}r_{ds1}) \right] \right\| \frac{1}{sC_P} \quad (3.5)$$

where  $C_P$  is the total parasitic capacitance to ground at node P. Combining all the terms together, an expression of input impedance can be obtained,

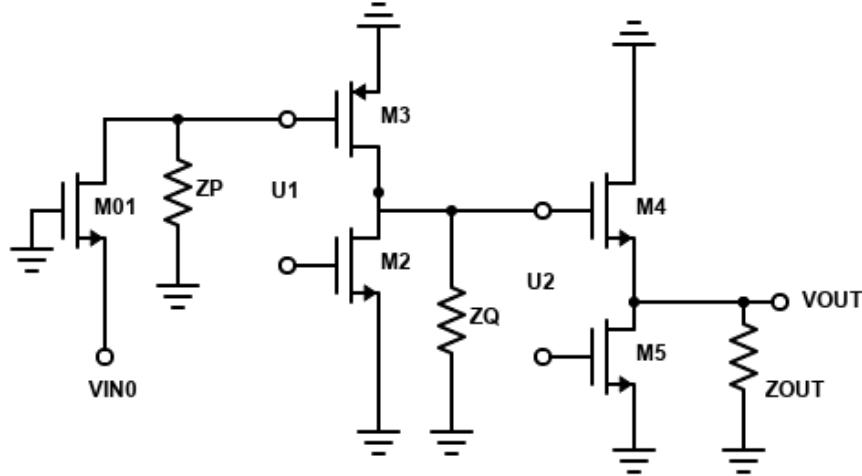
$$Z_{in} = (R_{LS} + sL_s) \| R_{in} \| \frac{1}{sC_N} \quad (3.6)$$

Here, the series inductor  $L_s$  at the input is used for input matching and damping the total parasitic capacitance seen by the input nodes,  $C_N$ . The  $R_{LS}$  is the series resistance of  $L_s$ . The upon expression is then expanded as,

$$Z_{in} = \frac{1}{\frac{1}{R_{LS} + sL_s} \frac{1+G_{m1}r_{ds1}}{r_{ds1} + Z_P} sC_N} \quad (3.7)$$

$$= \frac{R_{LS} + sL_s}{C_N L_s s^2 + \left( R_{LS} C_N + L_s \frac{(1+r_{ds1}G_{m1})}{(r_{ds1}+Z_p)} \right) s + R_{LS} \frac{(1+r_{ds1}G_{m1})}{(r_{ds1}+Z_p)} + 1} \quad (3.8)$$

The voltage gain of the entire circuit is calculated as the multiply of the gains of different stages, the small signal model of the entire structure is as shown in Figure 3.3, where M01 is an equivalent transistor as the froner stage.



**Figure 3.3:** Sketch of the Equivalent Small Signal Circuit

The voltage gain can be then expressed as,

$$|A_v| \cong \frac{1}{2} [(G_{m1}g_{m3}|Z_P| + g_{m2}) Z_Q g_{m5} + g_{m4}] |Z_{out}| \quad (3.9)$$

Here,  $Z_Q$  and  $Z_{out}$  are respectively defined as the impedance seen from node Q and the output impedance, which are expressed as follows,

$$Z_Q = r_{ds2} \| r_{ds3} \| \frac{1}{sC_Q} \quad (3.10)$$

$$Z_{out} = r_{ds4} \| r_{ds5} \| \frac{1}{sC_{out}} \quad (3.11)$$

where  $C_Q$  is the total parasitic capacitance at node Q and  $C_{out}$  is the output parasitic capacitance.

## 3.2 | The Modified Structure

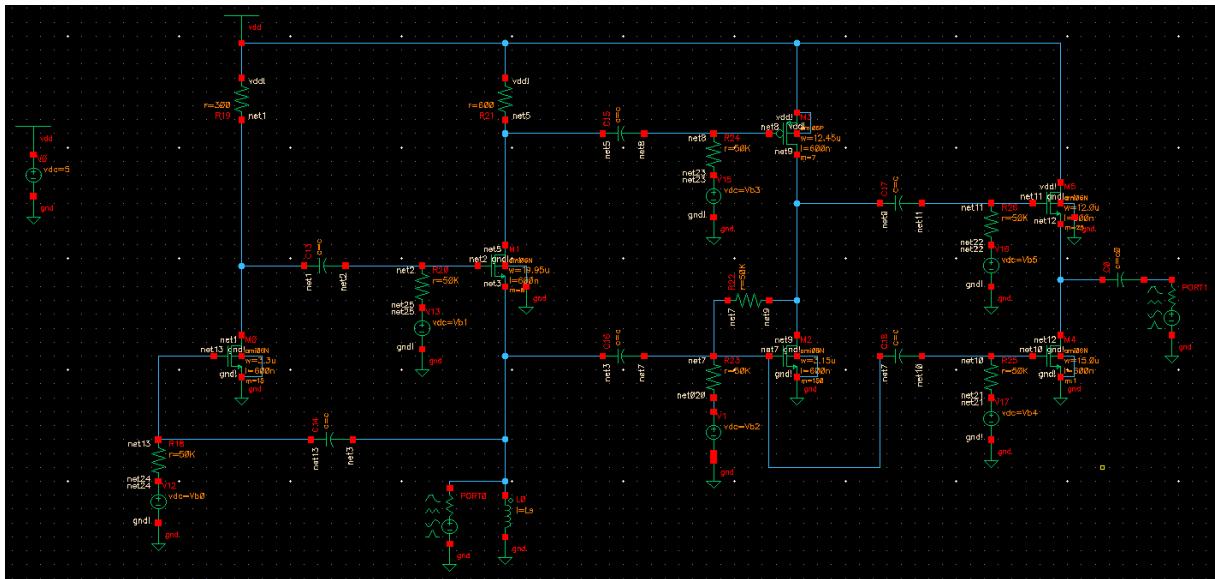
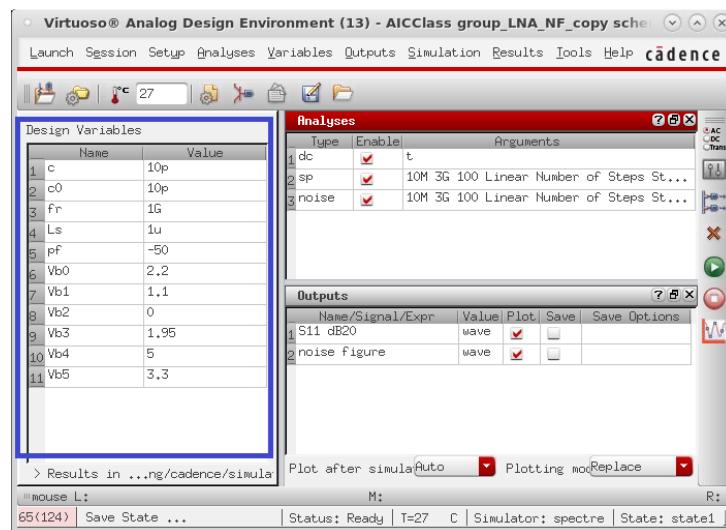
The utilized transistor models in this report are 'ami06N' and 'ami06P'. Several parameters have been determined in the first place from the model's datasheet: The threshold voltage of NMOS and PMOS are respectively  $V_{th,N} = 0.7086V$ ,  $V_{th,P} = -0.9180V$ , and  $K_n = \frac{1}{2}\mu_n C_{ox} = 57.8\mu A/V^2$ ,  $K_p = \frac{1}{2}\mu_p C_{ox} = -18.9\mu A/V^2$ .

Initially, we determined  $V_{DD} = 5V$ . The size of the transistors is determined during the simulation, which has been listed in Table 3.1.

**Table 3.1:** Transistors

Modified	Width(grid units)	Length(grid units)	Multiplier
$M_0$ $(3.3\mu m/600nm) \times 15$	22	4	15
$M_1$ $(19.95\mu m/600nm) \times 8$	133	4	8
$M_2$ $(3.15\mu m/600nm) \times 150$	21	4	150
$M_3$ $(12.45\mu m/600nm) \times 7$	83	4	7
$M_4$ $(15.0\mu m/600nm) \times 1$	100	4	1
$M_5$ $(12.0\mu m/600nm) \times 25$	80	4	25

The modified and simulated schematic cell of the circuit is shown in Figure 3.4, with the design parameters for simulation in Figure 3.5.


**Figure 3.4:** The Schematic of the Modified circuit

**Figure 3.5:** The Set of Design Parameters

The specific parameters of the bias voltage and value of series resistance are represented in Table 3.2 and Table 3.3, respectively.

**Table 3.2:** Biase Voltage of the Modified Circuit

$V_{B0}$	$V_{B1}$	$V_{B2}$	$V_{B3}$	$V_{B4}$	$V_{B5}$
2.20V	1.10V	0.00V	1.95V	5.00V	3.30V

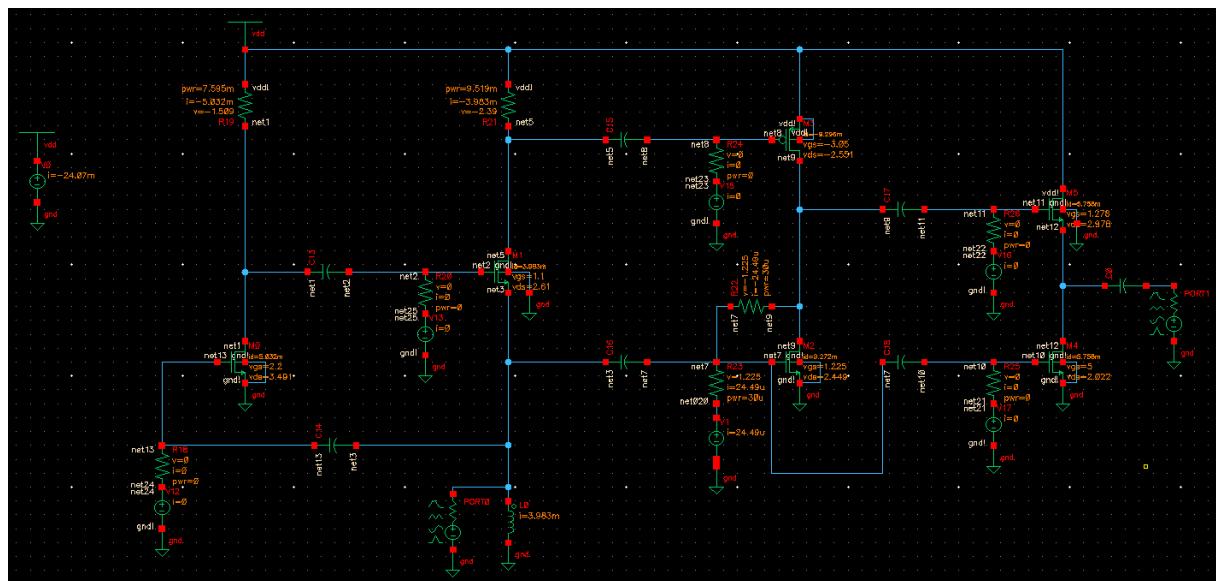
**Table 3.3:** Series Resistance

$R_{D0}$	$R_{D1}$	$R_F$	$R_B$
$300\Omega$	$600\Omega$	$50k\Omega$	$50k\Omega$

### 3.3 | DC Operating Points

In order to obtain the DC operating points in the Cadence Virtuoso, a 'dc' simulation is needed. Firstly, the input and output ports should be set, which respectively indicate the 'port0' and 'port1' in the schematic (Figure 3.4). As shown in Figure 3.7, we set port0 (input) with  $50\Omega$  resistance as a 'sine' source with frequency and amplitude set as ' $fr = 1GHz$ ' and ' $pf = -50dBm$ ' in the design parameter (Figure 3.5), and port1 (output) as 'dc' with  $50\Omega$  load resistance.

Figure 3.8a shows the process of choosing for the 'dc' simulation while Figure 3.8b represents the way for annotating the DC operating values on the schematic, which the schematic with DC operating results is demonstrated in Figure 3.6.



**Figure 3.6:** The Schematic with Annotation of DC Operating Points

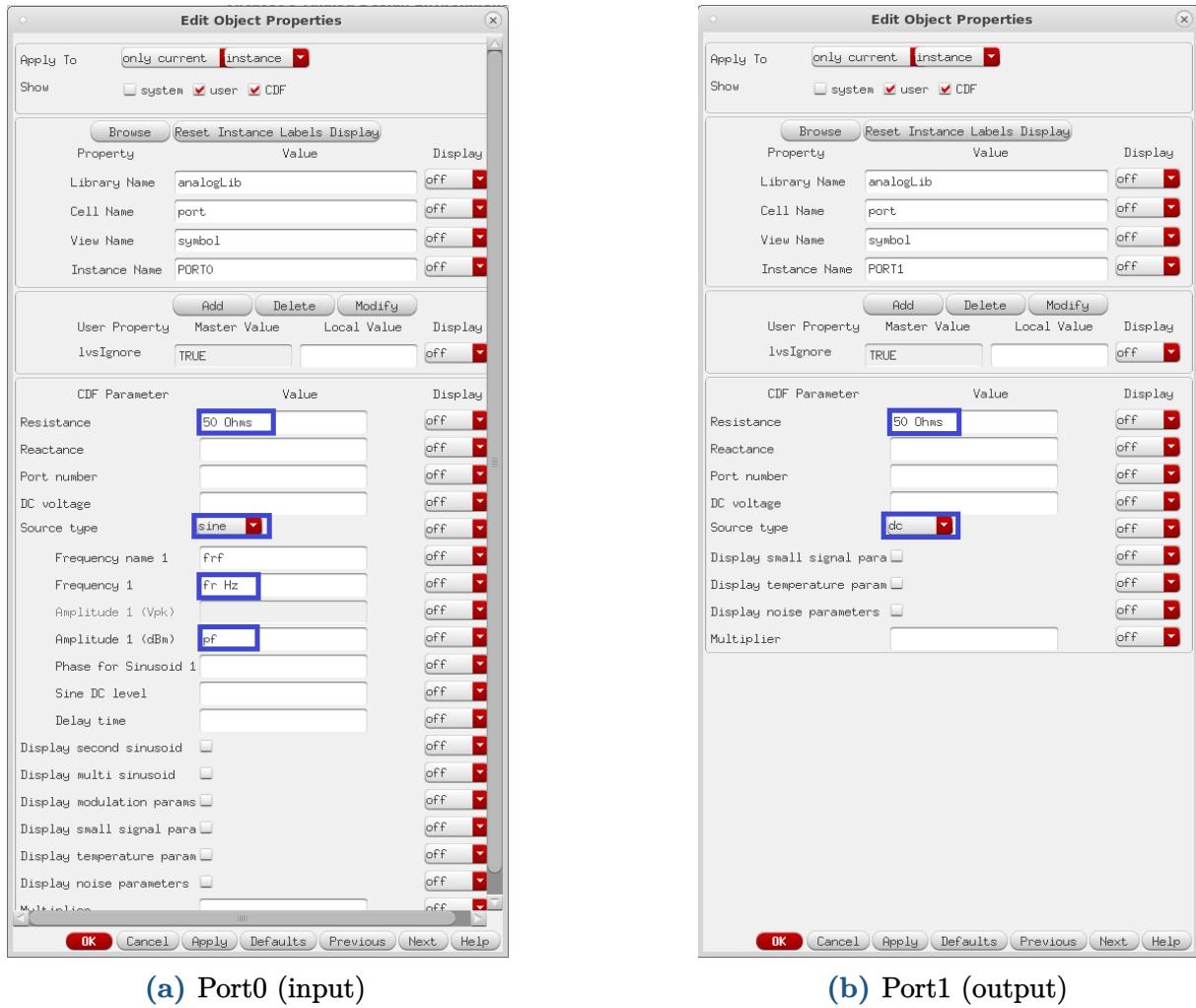


Figure 3.7: Set of Port0 (input) and Port1 (output)

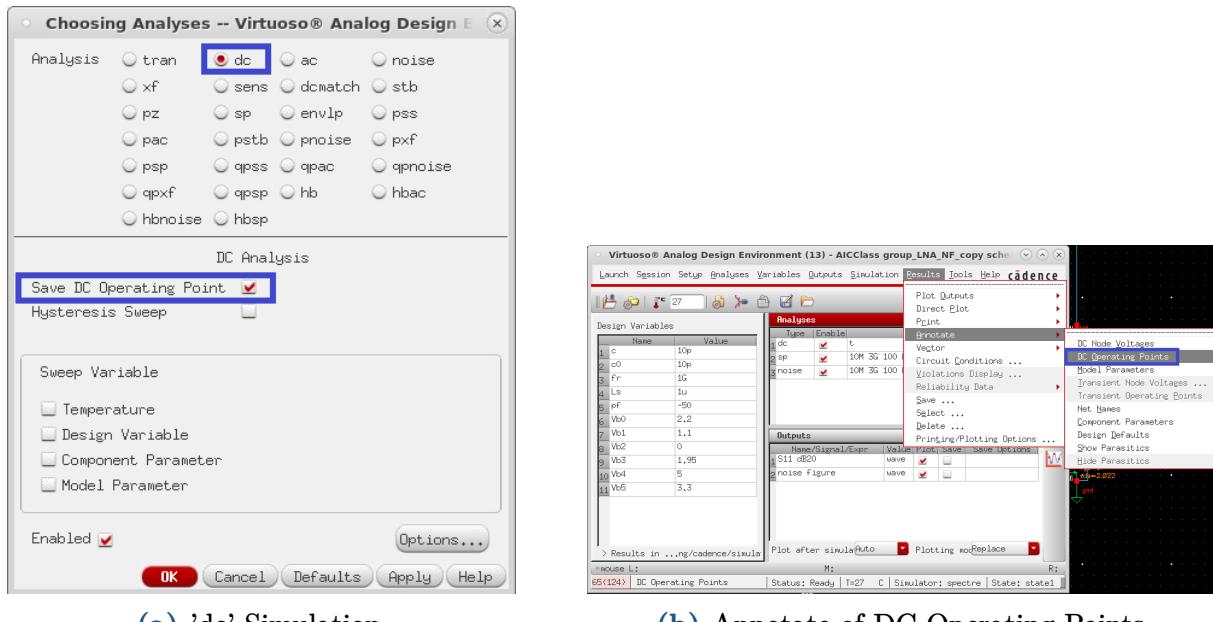


Figure 3.8: DC Simulation and Annotation

The measured DC current for each branch is represented in Table 3.4.

**Table 3.4:** Current Measurement

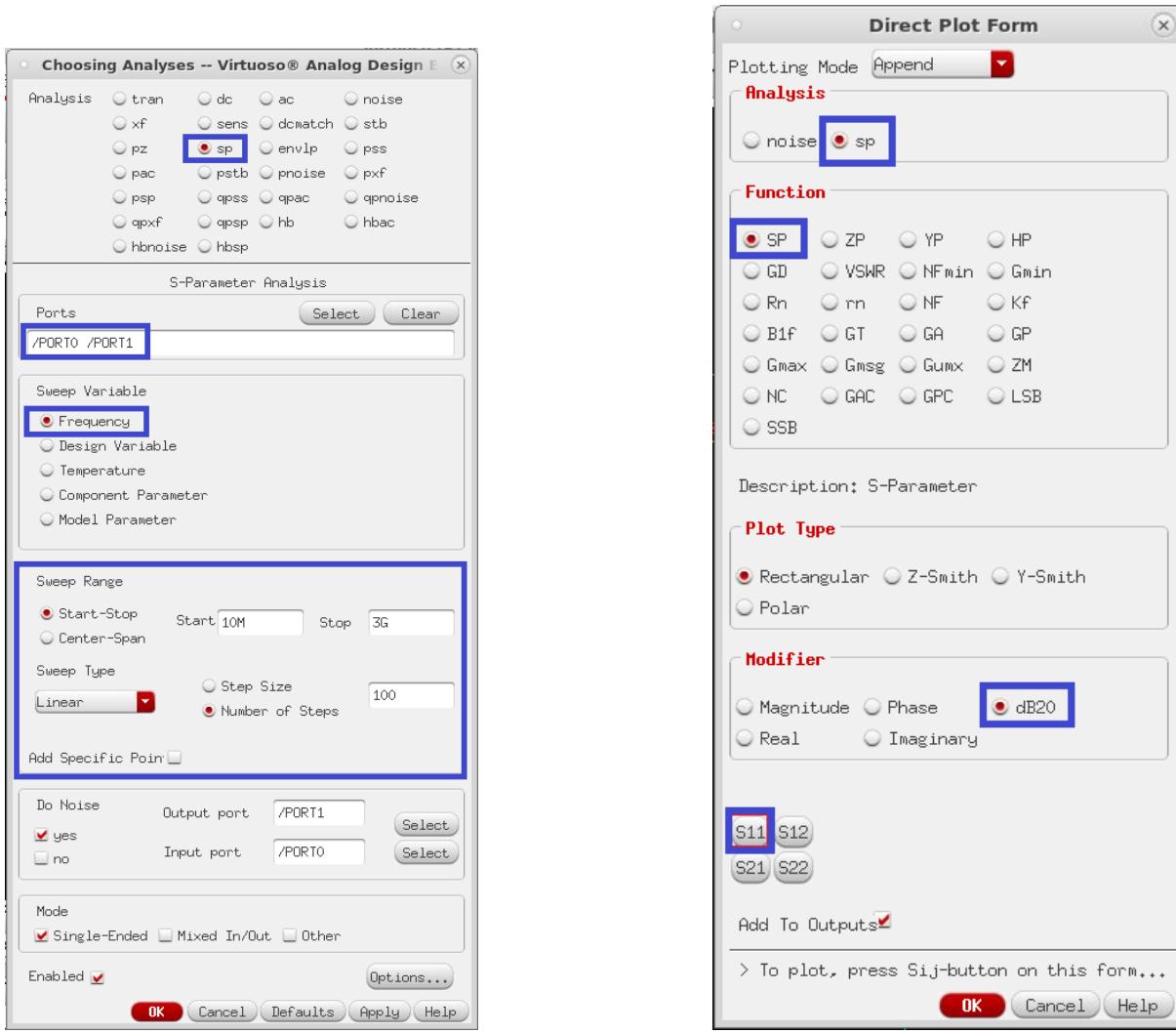
$I_0$	$I_1$	$I_3$	$I_5$
5.032mA	3.983mA	9.296mA	5.758mA

The consuming power could therefore be calculated as,

$$P = V_{dd} \times I_{total} = 5V \times (5.032 + 3.983 + 9.296 + 5.758)mA = 123.35mW \quad (3.12)$$

### 3.4 | Input Matching Simulation

In this part, the input matching is evaluated with the simulation of the parameter S11. The utilized simulation program is the 'sp' simulation. Figure 3.9a represents the settings of the 'sp' simulation, which uses the same schematic as in Figure 3.6. The ports of 'port0' and 'port1' have been selected in the first step, where the settings of the ports are the same as the simulation with 'dc' as in Figure 3.7. The sweep variable is set as frequency, and the range has been selected as 10MHz to 3GHz, as our interested frequency is up to around 1.2GHz. Then the direct plot block is operated as in Figure 3.9b, where the 'SP' item is ticked to present the results of the scattering parameters with the modifier of 'dB20'. Here for the input matching, S11 is the parameter of concern, which represents the level of reflection in the circuit.

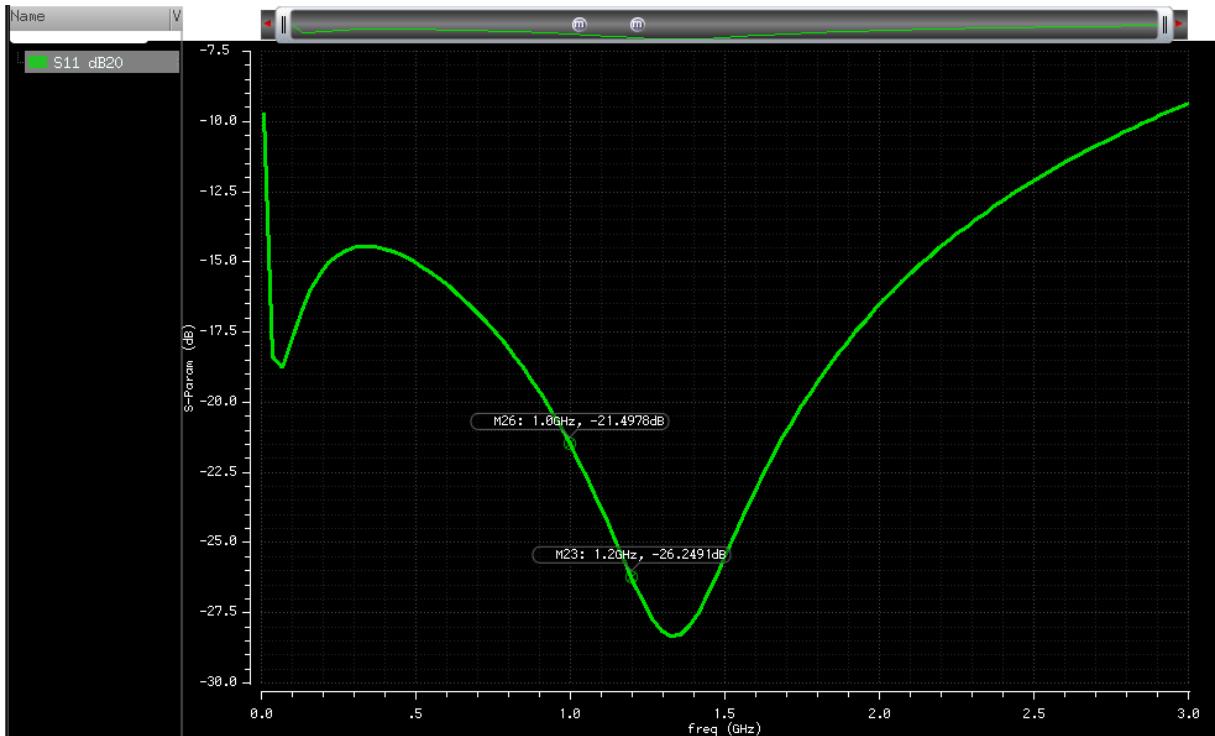


(a) 'SP' Simulation

(b) Simulation of S11

**Figure 3.9:** S-Parameter Simulation Process

The results of S11 are as shown in Figure 3.10. The structure shows good input matching generally in the simulated frequency range, which is lower than -10dB from the low frequency to about 2.9GHz. On the particular points at 1GHz and 1.2GHz, the value of S11 reached -21.50dB and -26.25dB respectively.



**Figure 3.10:** Simulated S11

### 3.5 | Noise Simulation

In this part, the noise figure of the circuit is to be analyzed and simulated. The noise figure is defined in Equation 3.13.

$$F = \frac{\text{input } S/N \text{ ratio}}{\text{output } S/N \text{ ratio}} = \frac{S_i}{N_i} \frac{N_o}{S_o} = \frac{N_o}{G N_i} \quad (3.13)$$

The noise power is derived from the current noise,

$$I_n^2 = 4kT\gamma g_m \quad (3.14)$$

The noise figure of the first noise cancellation stage is expressed as Equation 3.16.

$$F_{(1st)} = 1 + F_{M2} + F_{M3} \quad (3.15)$$

$$\cong 1 + \frac{\gamma}{\alpha R_s g_{m2}} + \frac{\gamma}{\alpha |Z_P|^2 (G_{m1}) g_{m3}} \quad (3.16)$$

where the terms of  $F_{M2}$ ,  $F_{M3}$  are derived as follows,

$$F_{M2} = \frac{4kTg_{m2}|Z_Q|^2\gamma}{4kTR_S A_v'^2 \alpha} = \frac{4g_{m2}}{R_S(|Z_P|G_{m1}g_{m3} + g_{m2})^2 \alpha} \frac{\gamma}{\alpha} \cong \frac{1}{R_S(g_{m2})} \frac{\gamma}{\alpha} \quad (3.17)$$

$$F_{M3} = \frac{4kTg_{m3}|Z_Q|^2\gamma}{4kTR_s A_v'^2 \alpha} = \frac{4g_{m3}}{R_S(|Z_P|G_{m1}g_{m3} + g_{m2})^2 \alpha} \frac{\gamma}{\alpha} \cong \frac{1}{|Z_P|^2 G_{m1}g_{m3}} \frac{\gamma}{\alpha} \quad (3.18)$$

The impedance  $Z_Q$  and  $Z_P$  are the impedance at node Q and node P. The noise figure of the proposed second-stage noise cancellation structure is as in Equation 3.19.

$$F_{(2nd)} = 1 + F_{M4} + F_{M5} + F_{R_{D1}} \quad (3.19)$$

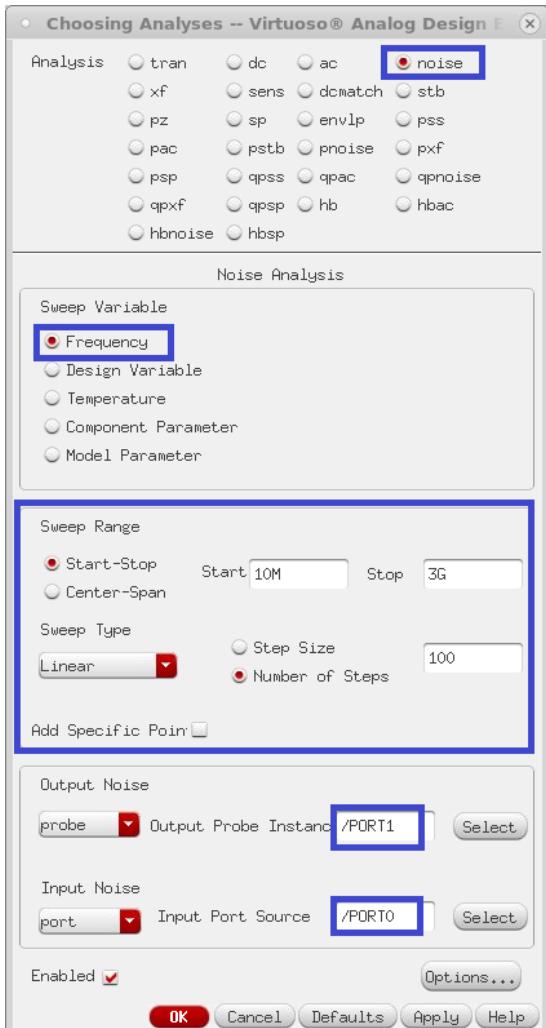
where the terms of  $F_{M4}$ ,  $F_{M5}$ ,  $F_{R_{D1}}$  are given by following relations,

$$F_{M4} = \frac{4kTg_{m4}|Z_{\text{out}}|^2\gamma}{4kTR_sA_v^2}\alpha = \frac{\gamma 4g_{m4}}{\alpha R_s [(|Z_P|G_{M1}g_{m3} + g_{m2})g_{m5}|Z_Q| + g_{m4}]^2} \quad (3.20)$$

$$F_{M5} = \frac{4kTg_{m5}|Z_{\text{out}}|^2\gamma}{4kTR_sA_v^2}\alpha = \frac{\gamma 4g_{m5}}{\alpha R_s [(|Z_P|G_{m1}g_{m3} + g_{m2})g_{m5}|Z_Q| + g_{m4}]^2} \quad (3.21)$$

$$F_{R_{D1}} = \frac{4kTR_{D1}(g_{m3}g_{m5}|Z_QZ_{\text{out}}|)^2(Z_{o1}/(Z_{o1} + R_{D1}))^2}{4kTR_sA_v^2} \simeq \frac{4Z_Q^2}{G_{m1}R_{D1}(1 + Z_Q)^2} \quad (3.22)$$

The simulation process of the noise figure is as shown in Figure 3.11, which is an implementation of the 'noise' simulation. Here, the frequency is also set as the sweep variable as in Figure 3.11a, starting from 10MHz and stopping at 3GHz, to see the noise figure behavior at the lower frequency band of 10MHz to 1.2GHz. Also, the ports setting in this part is the same as the former ones, as in Figure 3.7. Figure 3.11b is a presentation of the direct plot form setting for the parameter of the noise figure.



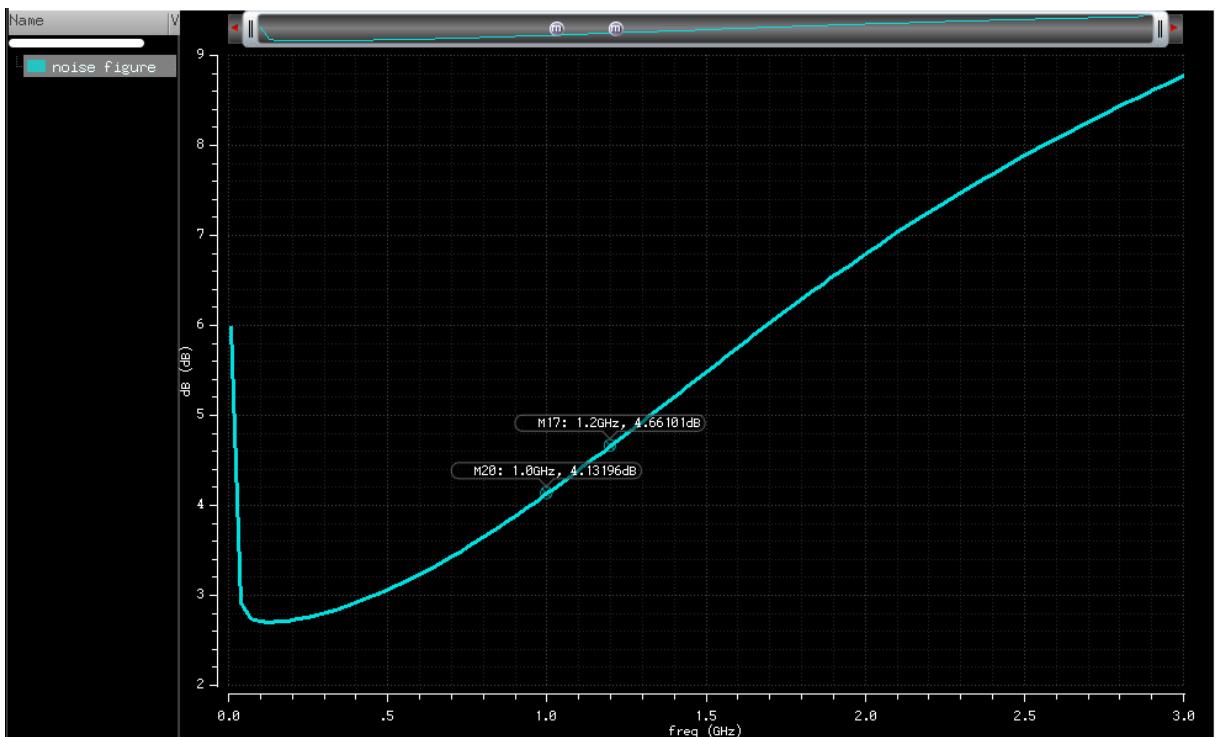
(a) 'noise' Simulation



(b) Simulation of Noise Figure

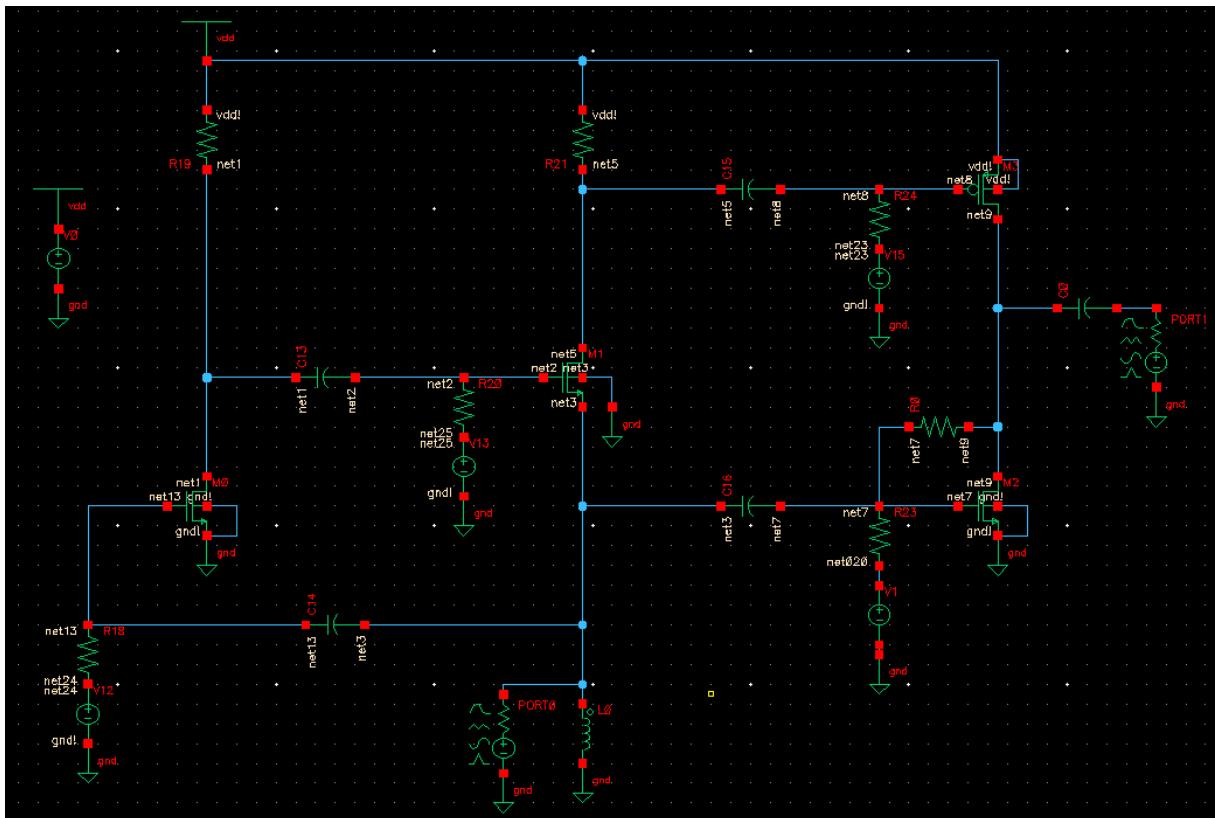
**Figure 3.11:** Noise Figure Simulation Process

The simulation results of the noise figure are demonstrated in Figure 3.12. A downward trend can be first witnessed at very low frequencies, until around 100MHz, where NF reaches about 2.7dB, while the noise figure is then increasing with the higher frequency. At 1GHz frequency and 1.2GHz, the noise figure is respectively 4.13dB and 4.66dB, which could be moderate values for this model.



**Figure 3.12:** Simulated Noise Figure

A comparison is also made in this part with the structure with only a first-stage noise-canceling, as shown in Figure 3.13.

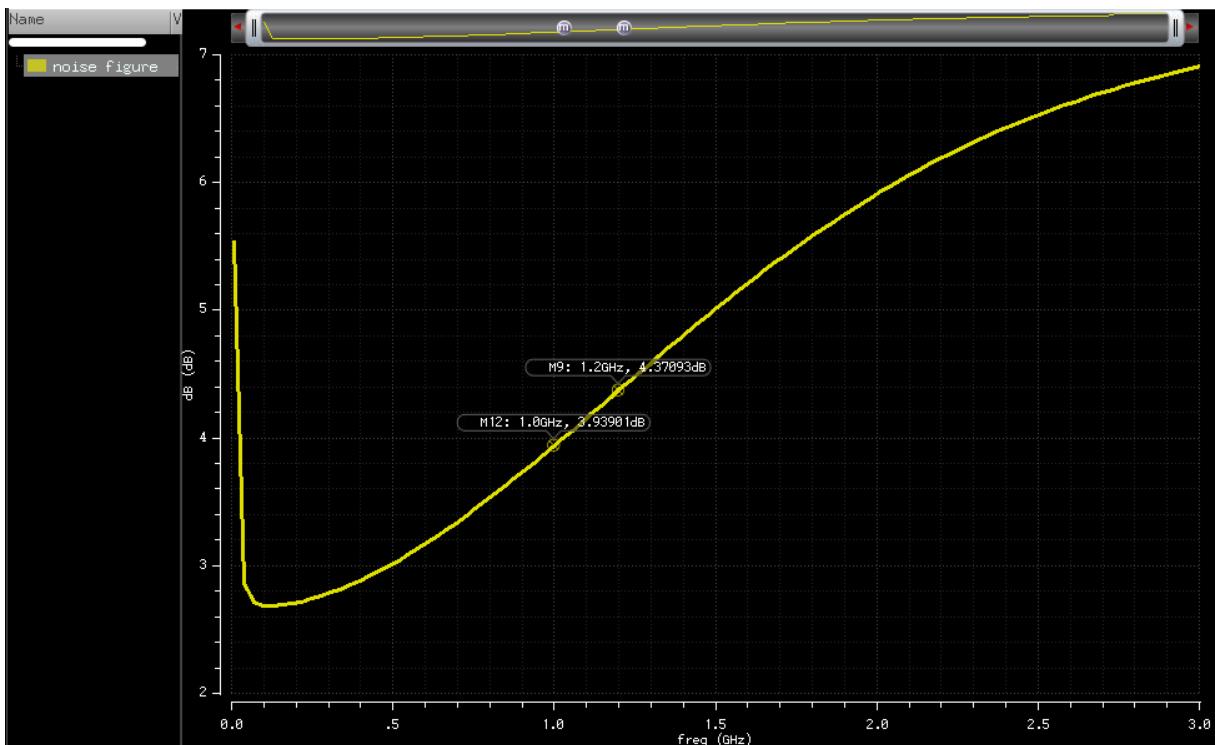


**Figure 3.13:** The Schematic of the First-Stage Structure

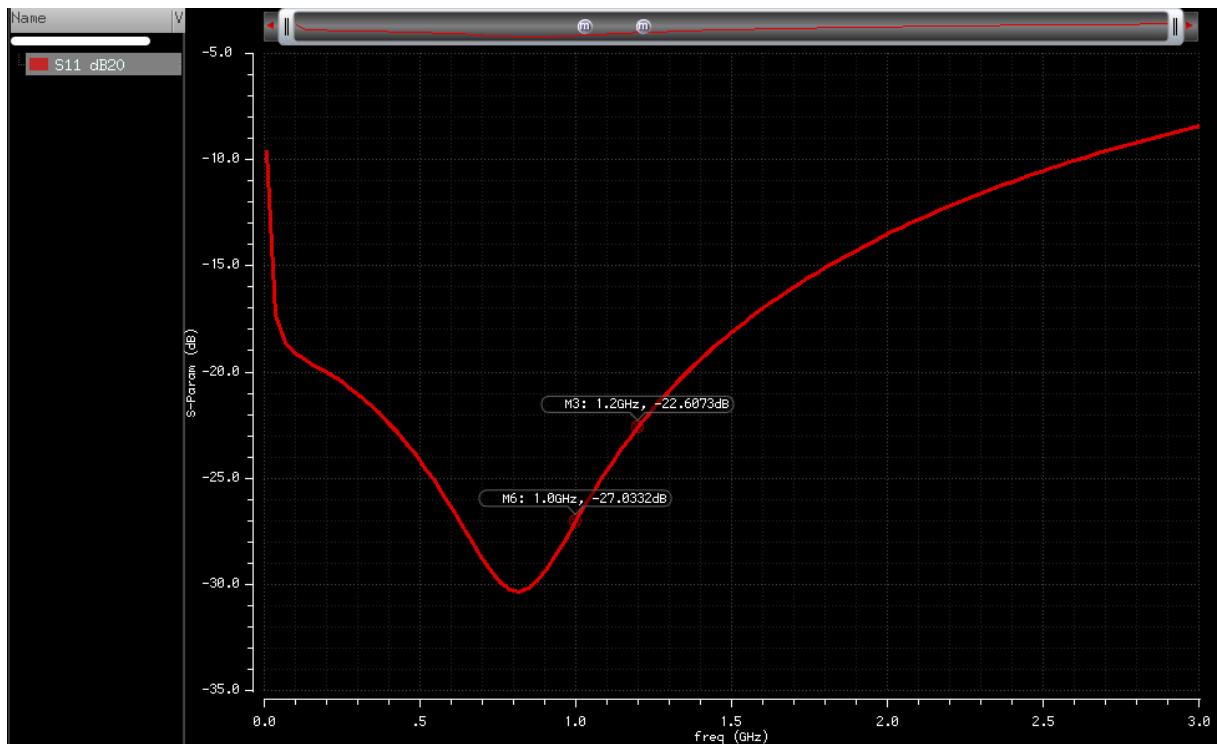
The simulation results of the 1st-stage noise-canceling structure are presented as follows, where Figure 3.14 shows the parameter of noise figure and Figure 3.15 shows the parameter of S11.

Unlike the referenced paper, the behavior of the noise figure with this model shows better results compared with the two-stage structure. At 1.2GHz, the noise figure for this reduced structure is 4.38dB, slightly lower than the former one. Also at 1GHz, the noise figure here is 3.94dB, 0.7dB lower than the full structure.

The reason lies in the different models we used, the used model in this simulation is 600nm technology, whereas in the original paper used 28nm CMOS. Also, as the main noise in this structure is the thermal noise, which is determined by the transconductance of the resistors. This value in our model can be much larger than the one proposed in the referenced paper, due to the larger size of the transistors. However, the trade-off of different parameters also heavily effected the behavior of the noise figure. When we tried to modify the components parameters to reduce the value of NF, other values like DC operating points and IIP3 would be seriously suffered.

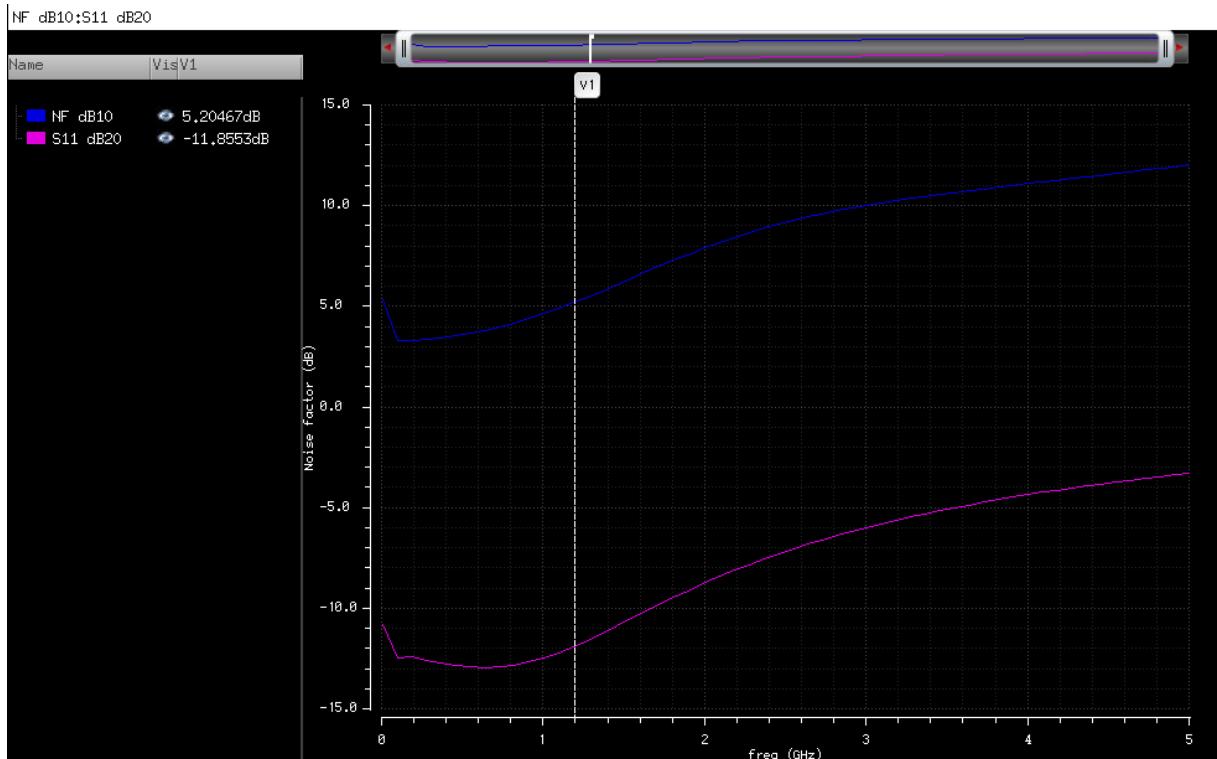


**Figure 3.14:** Noise Figure of 1st-Stage



**Figure 3.15:** S11 of 1st-Stage

Another attempt is made with the structure setting the Vdd to 3V. The results become a little worse at 5.20dB for the noise figure.



**Figure 3.16:** The Parameters with Vdd=3V

### 3.6 | Gain Simulation

A simulation of parameter S21 is operated here in the first place, where the procedure is the same as the simulation of S11, as shown in Figure 3.17. The results are presented in Figure 3.18, which could reach 21.27dB at 189.4MHz. And we can observe the bandwidth is from 78.20 MHz to 429.92 MHz in this simulation.



**Figure 3.17:** Simulation Block of S21

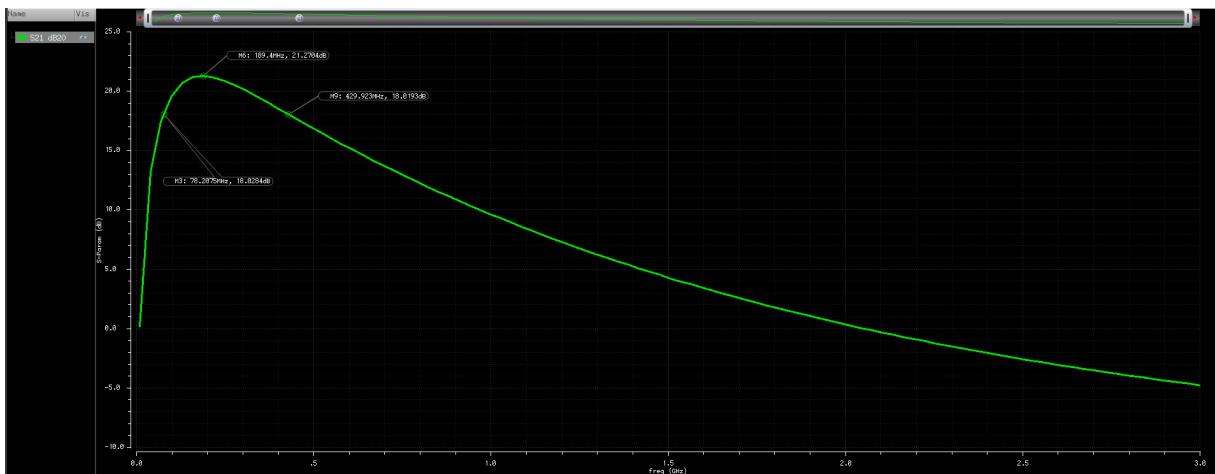


Figure 3.18: S21 Parameter

In order to operate the simulation of the voltage gain and phase, the 'ac' simulation is to be used. The input and output ports should be firstly modified as a 'Vdc' source and an output port respectively, as shown in Figure 3.19. The simulation process is as shown in Figure 3.20.

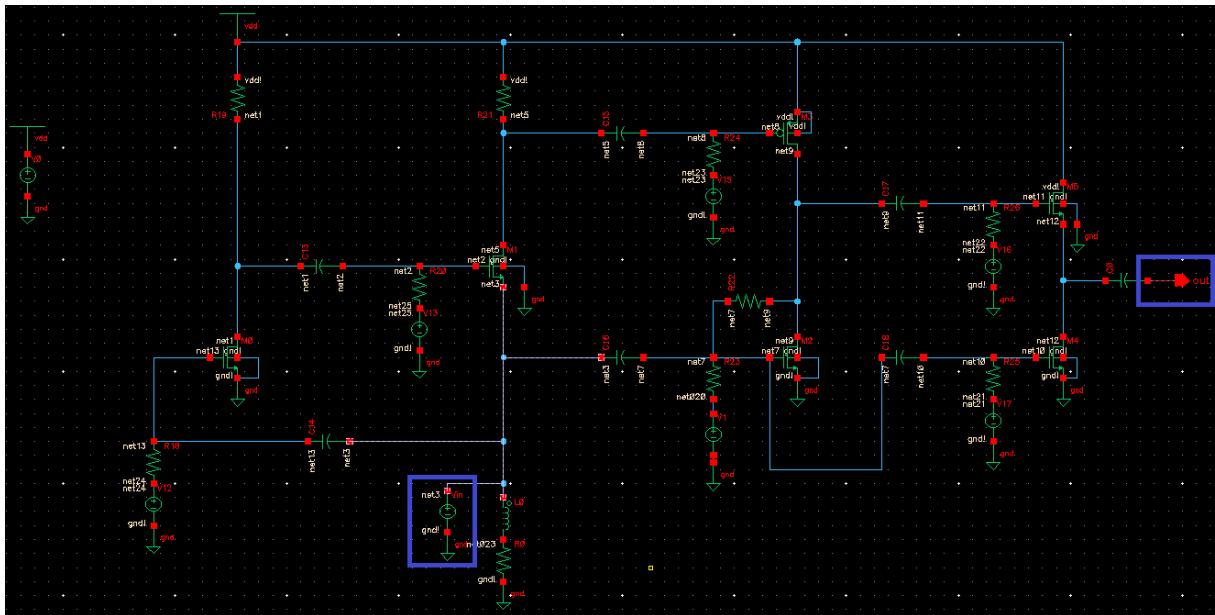


Figure 3.19: Simulation Schematic of 'ac' Simulation

Similar to the former simulations, the frequency sweep here is also set as 10MHz to 3GHz, as shown in Figure 3.20a. Figure 3.20b shows the process of displaying the results, by pressing 'AC Gain and Phase' and then selecting the out port and VDC input in the schematic, the results could present automatically, as in Figure 3.21 and Figure 3.22.

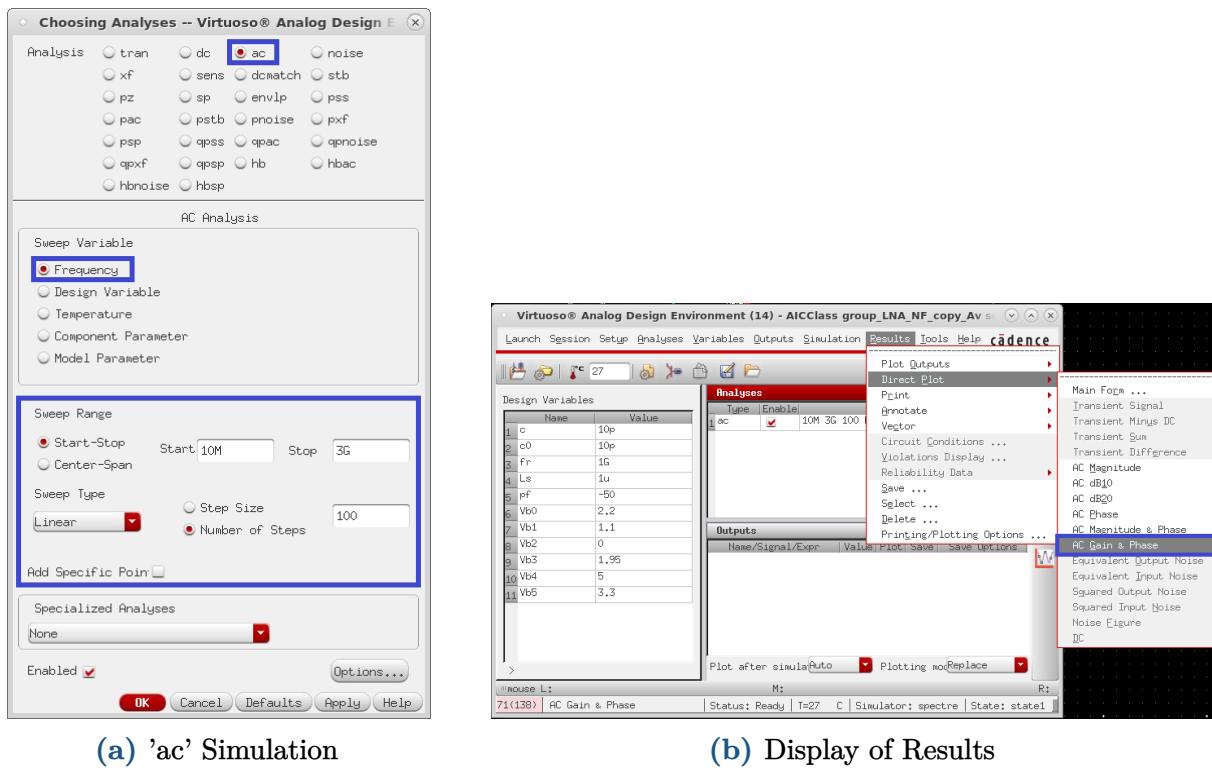


Figure 3.20: 'ac' Simulation Process

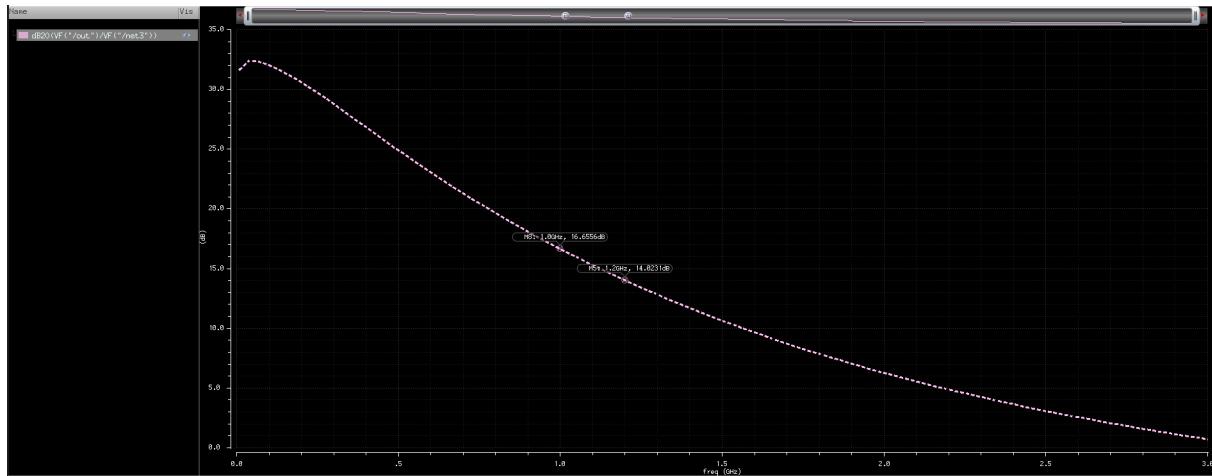
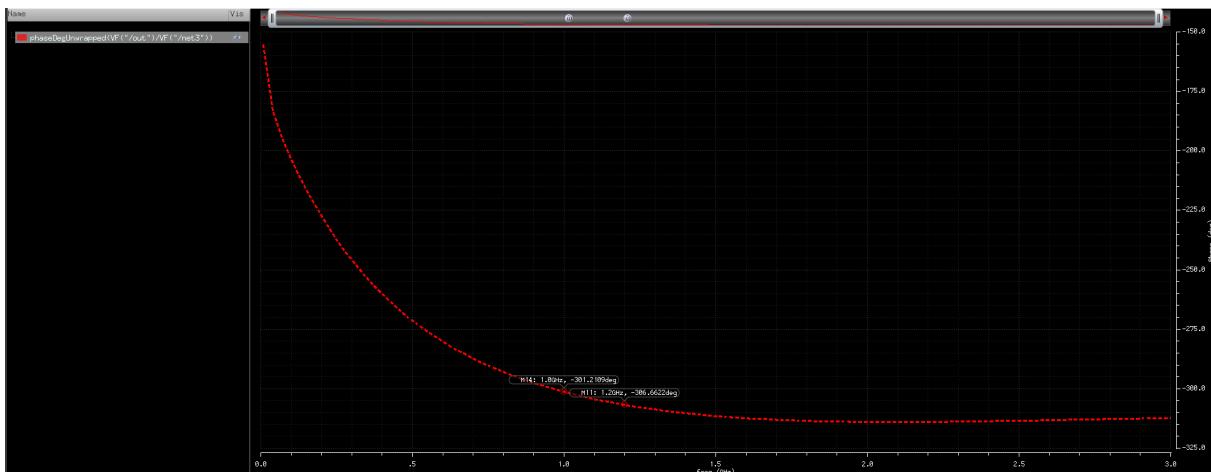


Figure 3.21: Simulated Gain

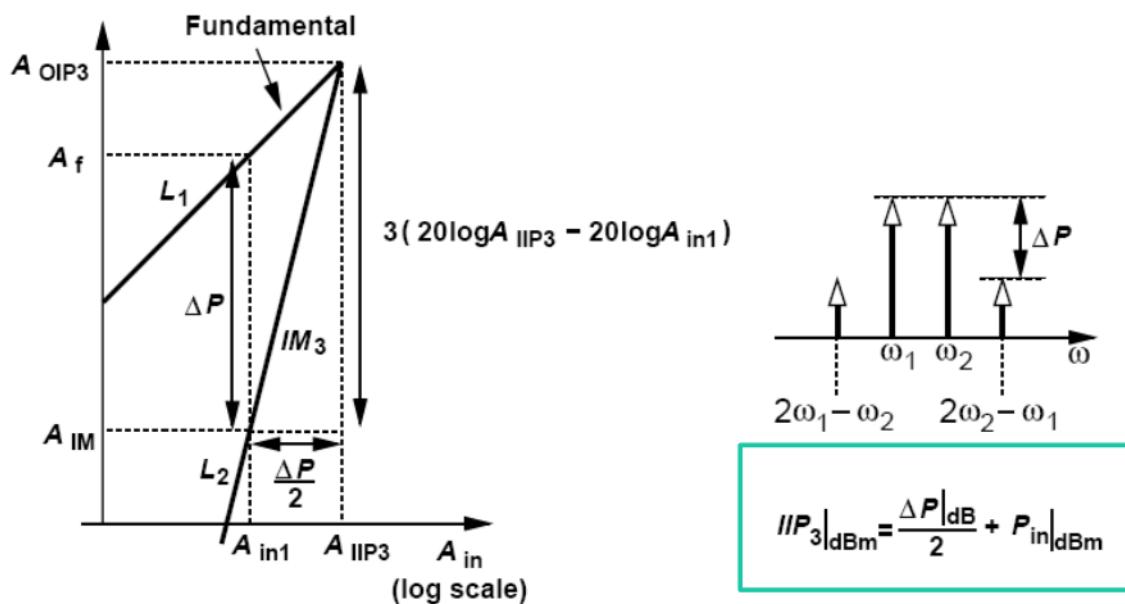
The voltage gain here could reach 16.66dB and 14.02dB respectively at 1GHz and 1.2GHz, which represents rather good behavior. The corresponding phases are -301.21 degrees and -306.66 degrees for 1GHz and 1.2GHz.



**Figure 3.22:** Simulated Phase

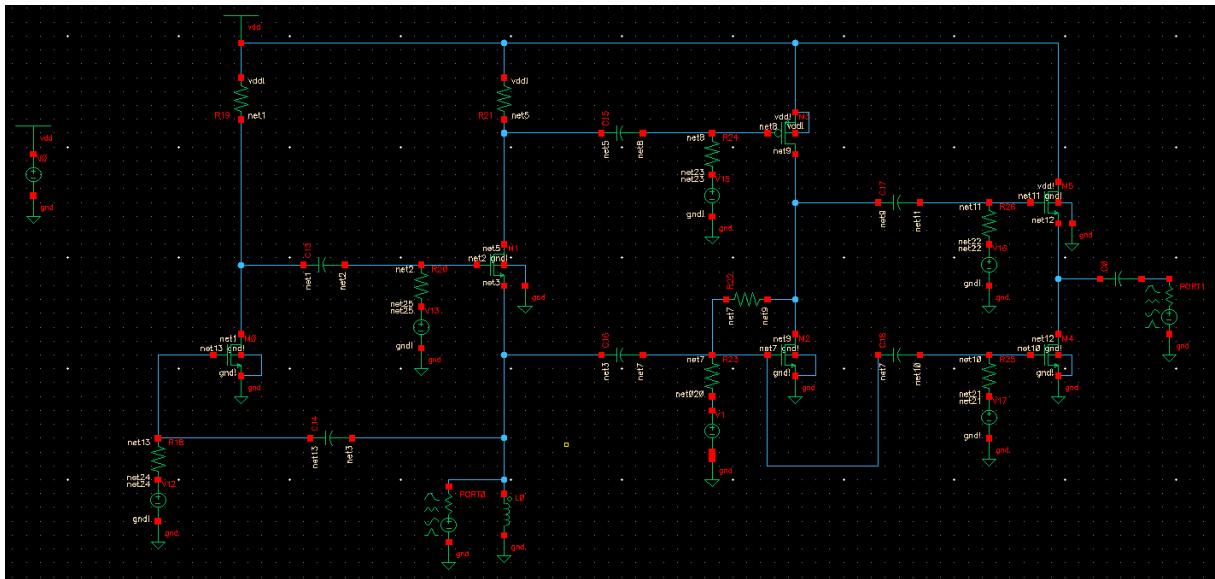
### 3.7 | Linearity Simulation

The linearity can be indicated by the parameter of IIP3, which refers to the input of the third-order intercept point (IP3). We focus on the third-order distortion here since the even-order distortion components are ideally zero and third-order distortion typically dominates. The graphic illustration of this parameter is shown in Figure 3.23. With higher values of IIP3, the circuit shows better behavior of linearity.



**Figure 3.23:** Graphical Illustration of the Third-Order Intercept-Point

The 'hb' simulation is the implementation to present the values of IIP3. As the first step, the ports in the schematic have been modified before the simulation, as shown in Figure 3.24, where now the input- and output- ports are once again changed into two simulation ports, 'port0' and 'port1'.



**Figure 3.24:** The Schematic of 'hb' Simulation

Another modification here is for the input port, 'port0', as shown in Figure 3.25. In order to operate a two-tone test to get parameter IIP3, the 'port0' here has been activated the second sinusoid. Taken the 1.2GHz simulation as an example, as shown in the 'Design Variables' in Figure 3.26, the first frequency 'f1' is set to 1.2GHz while the second tone 'f2' is set to 1.3GHz, as 'f1'+100MHz, while the amplitudes for both tones are set as -20dBm.

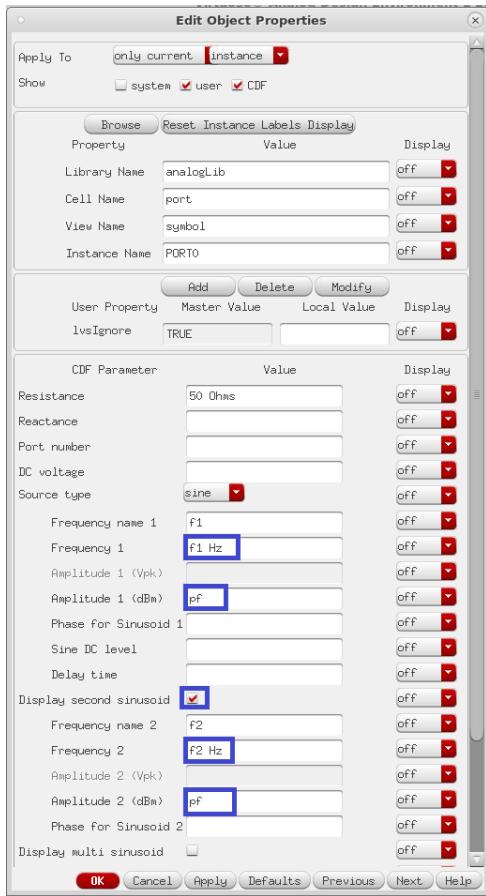


Figure 3.25: The Set of Port0 with Two Tones

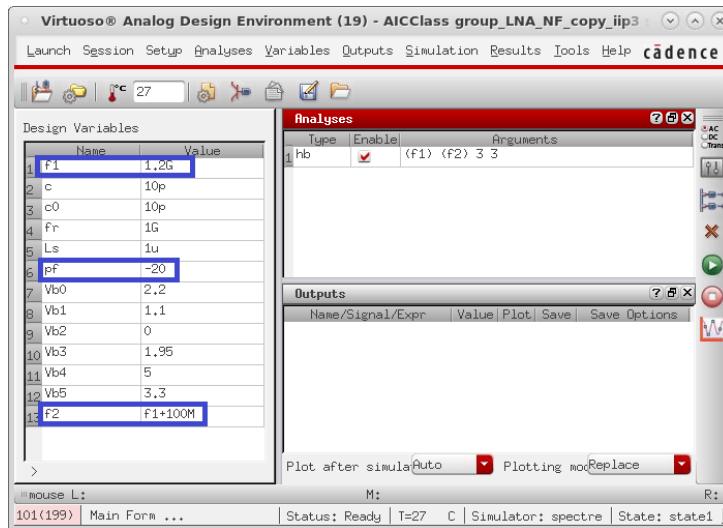
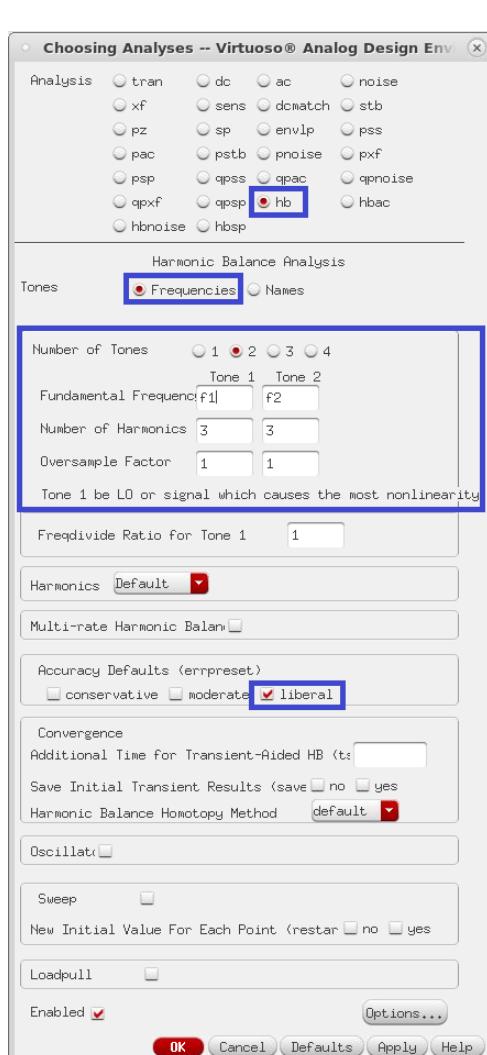


Figure 3.26: Design Parameters of 'hb' Simulation

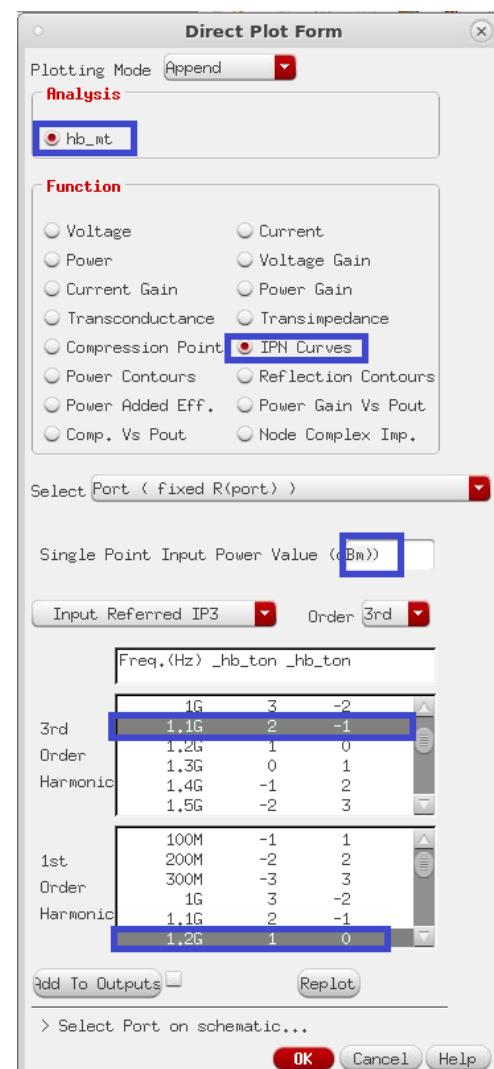
The following simulation settings are presented in Figure 3.27. In Figure 3.27a, the two tones have been set also with frequency 'f1' and 'f2' in 'hb' simulation block, and with the number of harmonics of three. Figure 3.27b shows the operation of the simulation 'IPN Curves', where the 'Single Point Input Values' is set as -20dBm, same in the design parameter. With chose of 3rd and 1st order frequencies as 1.1GHz and 1.2GHz, the results



can be shown after pressing the output port 'port1'.



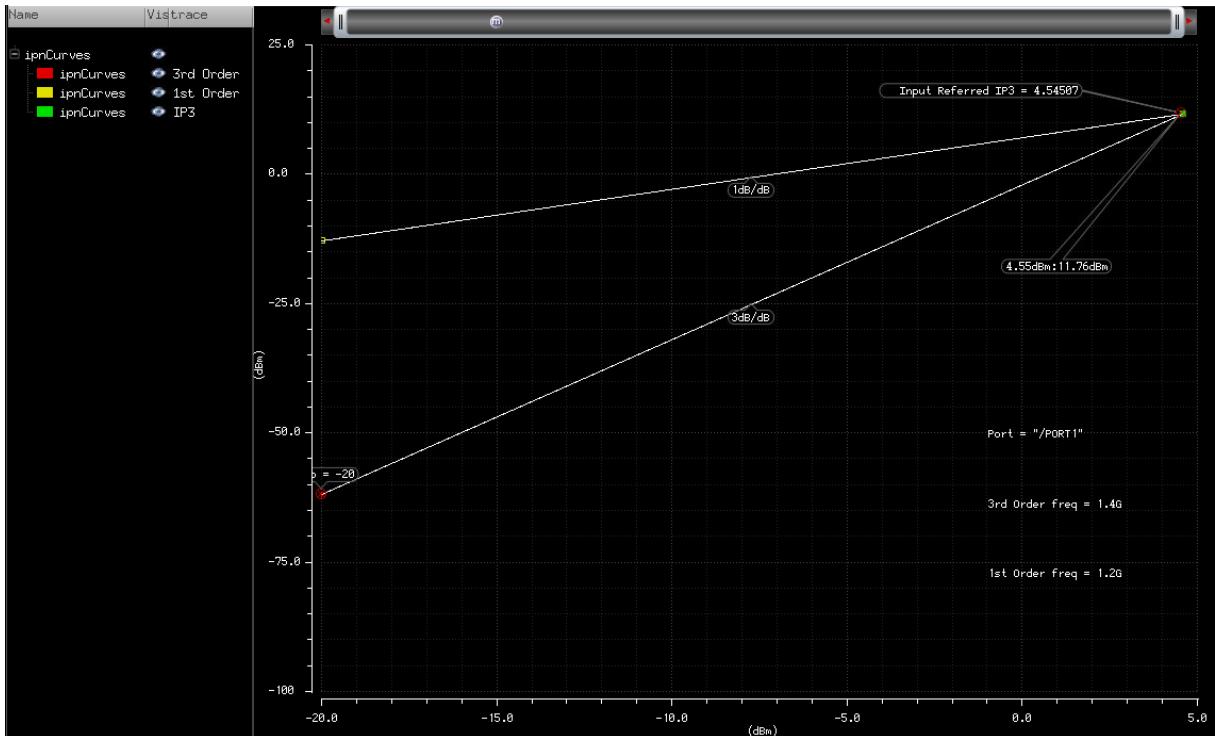
(a) 'hb' Simulation



(b) Simulation of IP3 Curve

Figure 3.27: 'hb' Simulation Process

Figure 3.28 demonstrates the results for the upon simulations, where the value of the IIP3 finally reaches 4.1dB, which shows rather a good linearity.



**Figure 3.28:** IIP3 with 1.2GHz

Other simulations from 1GHz to 4GHz have been launched with the results as follows in Table 3.6, which show satisfactory behavior in the interested frequency band. The red-colored values in Table 3.6 are the selected frequencies for the 1st and 3rd-order harmonics in Figure 3.27b, which uses for obtaining the final results.

**Table 3.5:** Simulation Results of IIP3 at Different Frequencies [GHz]

$f_1$	$f_2$	$(2f_1 - f_2)$	$(2f_2 - f_1)$	$IIP3[dBm]$
1	1.1	0.9	1.2	2.10
2	2.2	1.8	2.4	8.54
3	3.3	2.7	3.6	11.25
4	4.4	3.6	4.8	14.14

### 3.8 | Conclusion

A comparison is made here between the results in the referenced paper and our project. Another paper [2] utilized a 500nm CMOS process is also related here for comparison. Obviously, in order to achieve a wide bandwidth, the LNA circuit must be designed with components that have a high-frequency response and low parasitic capacitance and inductance. The smallest wide bandwidth for the circuit depends on the specific design goals and constraints, as well as the technology used in the fabrication process. That is one of the reasons why our bandwidth is a bit narrower compared with the paper one. On another hand, we already tried to modify our LNA circuit, because we want to achieve a lower noise figure, which indicates that the LNA is able to amplify the desired signal while adding less noise to the signal, thus preserving the SNR better. While our initial

expectation for the NF was not met and it has dropped to 4.66 dB at 1.2 GHz, it is possible that this is the limit imposed by the different transistor processes and device parameter settings.

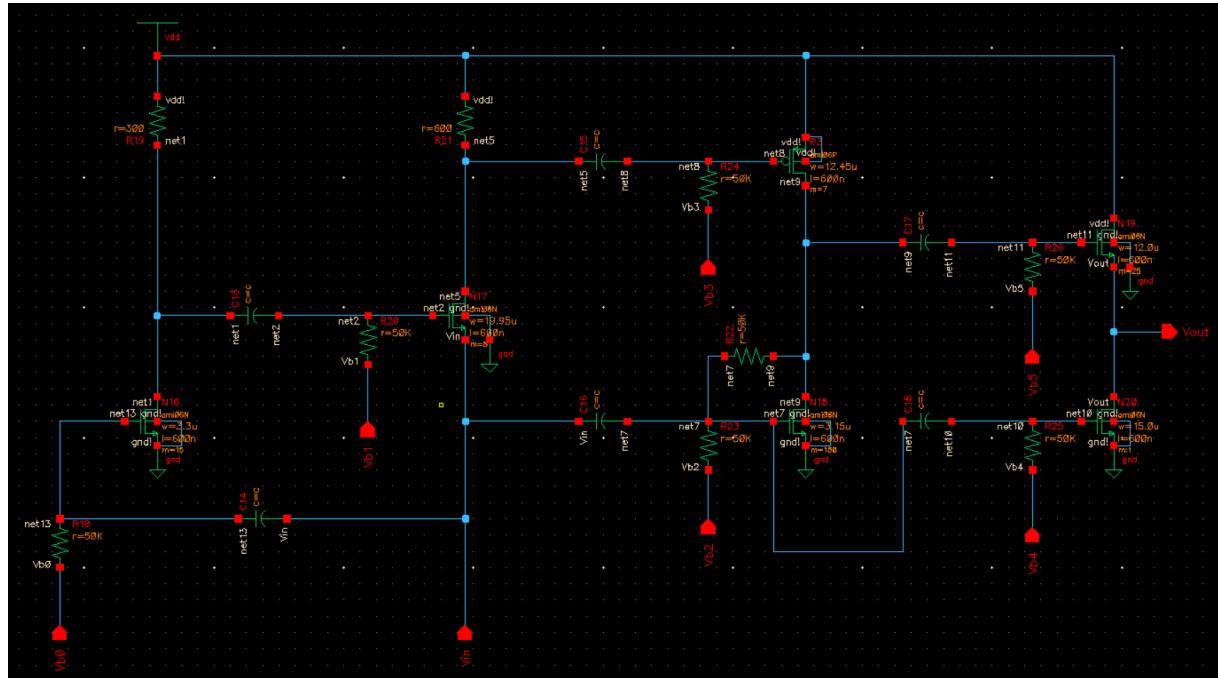
**Table 3.6:** Summary and Comparison

	Referenced Paper	Reported	[2]
Transistor Process	28nm	600nm	500nm
Vdd [V]	1	5	2.4
Power [mW]	4.1	123.35	-
NF [dB]	2.5 ~ 3.5	2.7 ~ 4.66	2.8
S11 [dB]	<-15	<-13	-
S21 [dB]	18.5	21.26	15
Av [dB]	18	16.66	-
IIP3 [dBm]	+1.29 ~ +4.25	+2.10 ~ +4.55	-8
Bandwidth [GHz]	0.02-2	0.078-0.43	-

## 4 | Layout

### 4.1 | A new cell for Proposed Two-Fold Noise Cancellation LNA

At the first, a new cell (schematic view) is created with our circuit and we provided pins to replace the output and input and all the bias voltage sources, as shown in Figure 4.1.



**Figure 4.1:** The new cell in schematic view

## 4.2 | The creation of capacitors

In order to create a capacitor, we chose the POLY layer(red) to draw a rectangular for the bottom plate and chose the ELEC layer(yellow) for the top plate. And then, we added vias for the different metal layers. After multiple adjustments, the final capacitance value is 9.995 pF, which is very close to our expectation of 10 pF and the check of DRC is passed(DRC stands for Design Rule Check). As shown in Figure 4.2 and Figure 4.3.

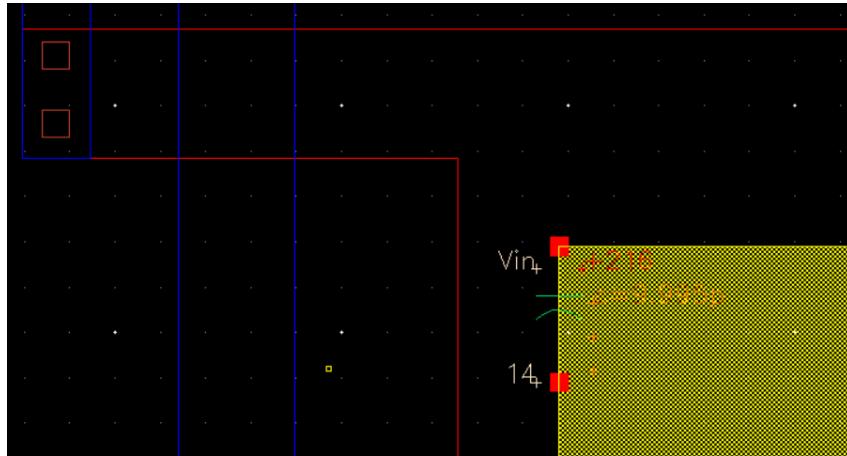


Figure 4.2: The capacitor in extracted view(partial)

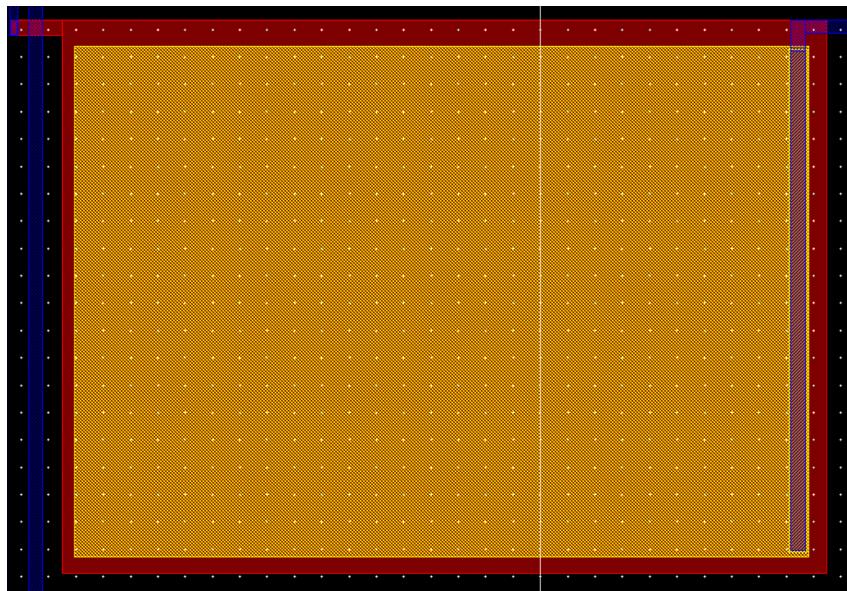
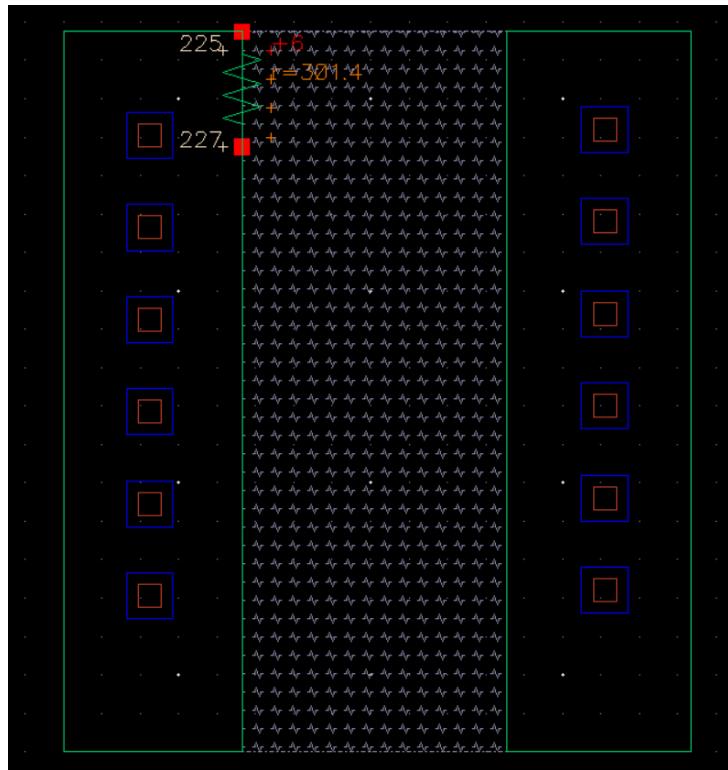


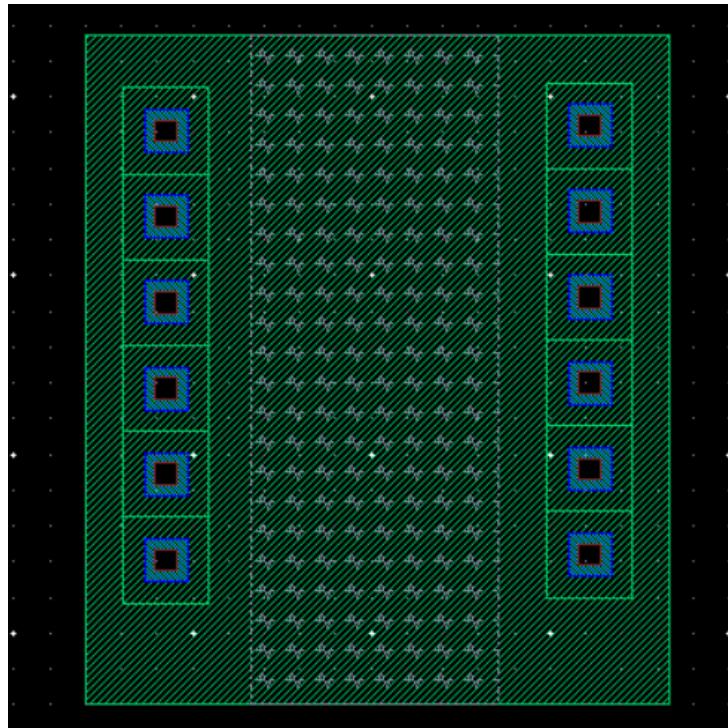
Figure 4.3: The capacitor in layout view

## 4.3 | The creation of resistors

With the aim of building a resistor for  $R_{D0}$ , which is  $300 \Omega$ , we drew a rectangle of n-well first and then used an existing ntap to contact the well (there are 6 vias for each side), and applied the resistivity layer. After multiple adjustments, the final resistance value is  $301.4 \Omega$  and the check of DRC is passed. As shown in Figure 4.4 and Figure 4.5.



**Figure 4.4:** The resistor  $R_{D0}$  in extracted view

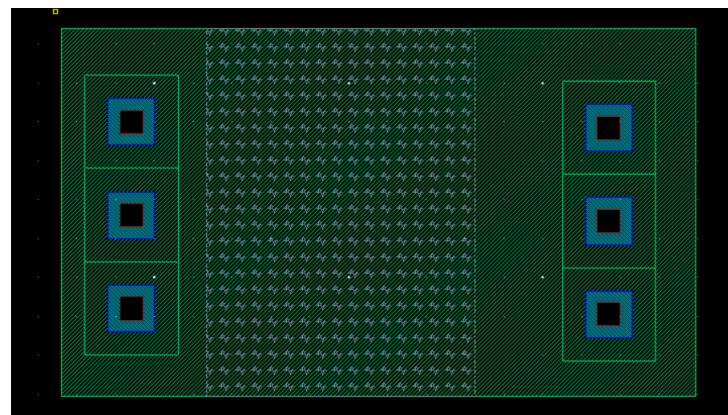


**Figure 4.5:** The resistor  $R_{D0}$  in layout

In the same way, as mentioned above, we built a resistor for  $R_{D1}$ , which is  $600 \Omega$ . After multiple adjustments, the final resistance value is  $598 \Omega$  and the check of DRC is passed. As shown in Figure 4.6 and Figure 4.7.

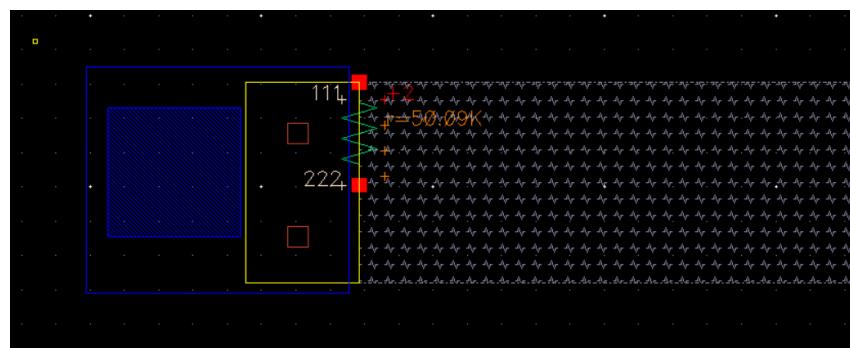


**Figure 4.6:** The resistor  $R_{D1}$  in extracted view

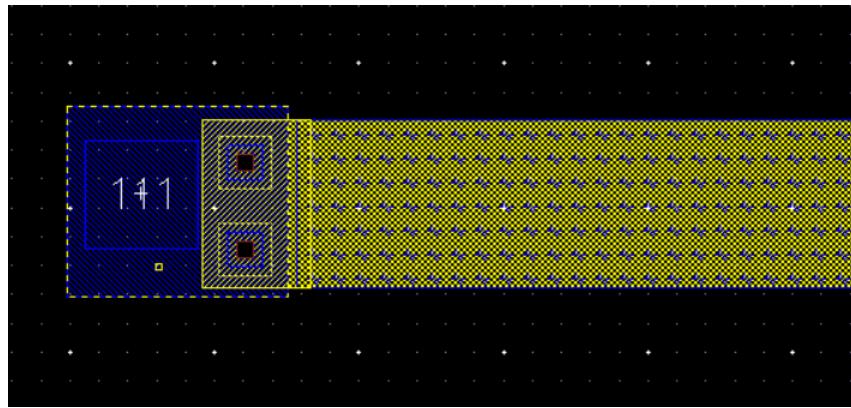


**Figure 4.7:** The resistor  $R_{D1}$  in layout

To achieve a large resistor, we need to apply a high resistivity layer and use ELEC(yellow) as our base layer instead of using an n-well layer. We added pins of metal 1 to allow proper connections of the extracted view. After multiple adjustments, the final resistance value is  $50.09\text{k}\Omega$ . We will use it for our resistors that  $R_B$  is  $50\text{k}\Omega$  and the check of DRC is passed. As shown in Figure 4.8 and Figure 4.9. In the process, we gave the pins a temporary name of 111, and Later, these names will be modified to facilitate pairing and connection during the final layout design.



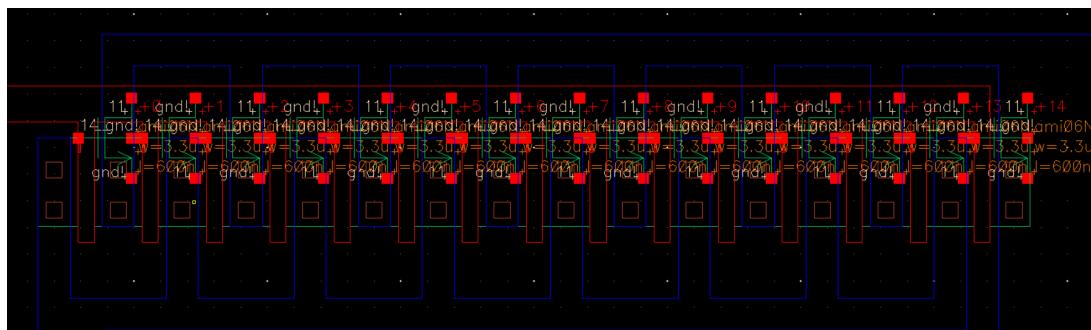
**Figure 4.8:** The resistor  $R_B$  in extracted view(partial)



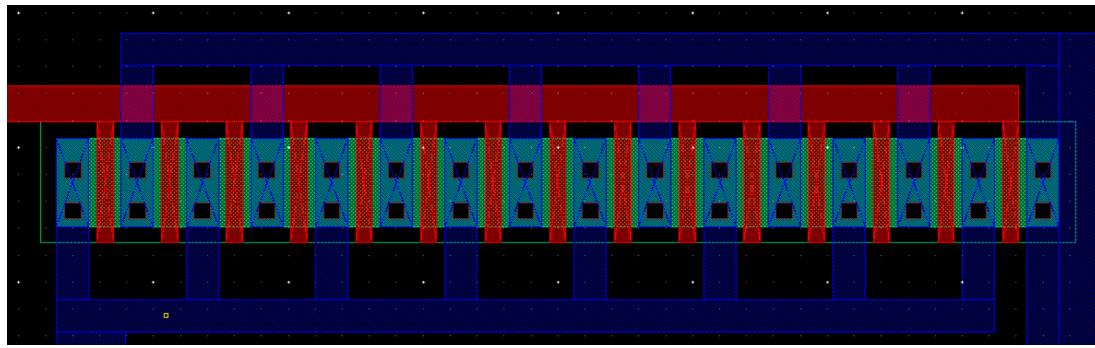
**Figure 4.9:** The resistor  $R_B$  in layout(partial)

#### 4.4 | The creation of NMOS and PMOS transistors

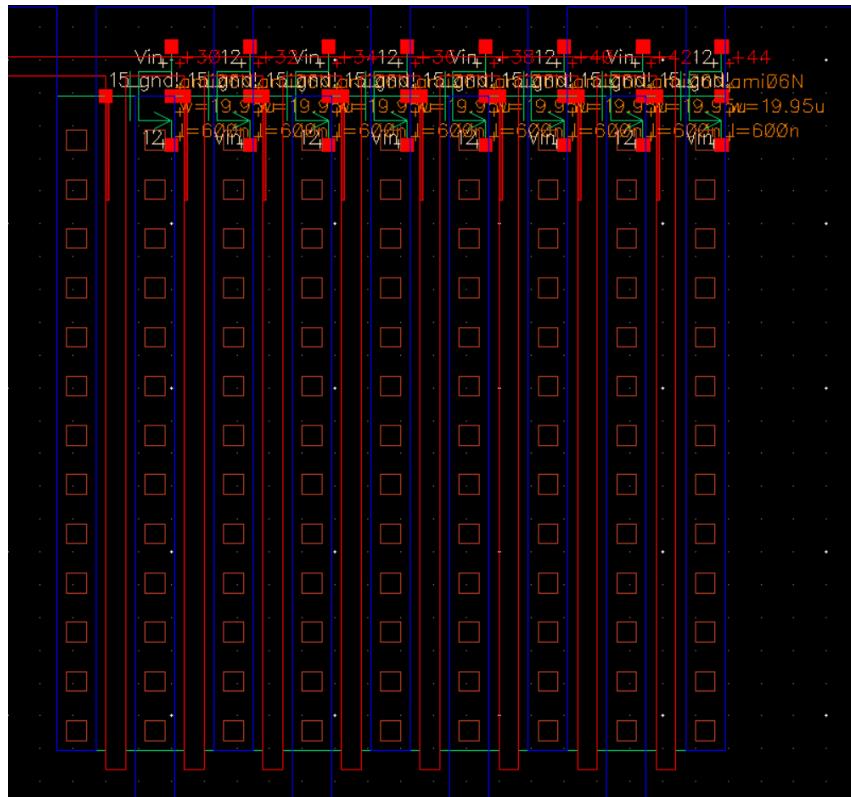
In our design, we have a configuration consisting of 4 NMOS transistors and 1 PMOS transistor. We created a new layout cell view in Virtuoso and selected the NMOS or PMOS transistor from the 'NCSU\_TechLib\_ami06' library by going to the 'Create Instance' tool. After positioning the transistor in the desired location by using the mouse, we adjusted the width and length of the transistor by using the 'Edit Instance Properties' tool. As shown in Figure 4.10, Figure 4.12, Figure 4.14, Figure 4.16, Figure 4.18 and Figure 4.20, these extracted views represent transistors that we expect to design. In Figure 4.11, Figure 4.13, Figure 4.15, Figure 4.17, Figure 4.19 and Figure 4.21, these layouts show transistors that we expect to design. When we completed the layout, they were verified successfully by running a Design Rule Check (DRC) and Layout Versus Schematic (LVS) check would be checked later.



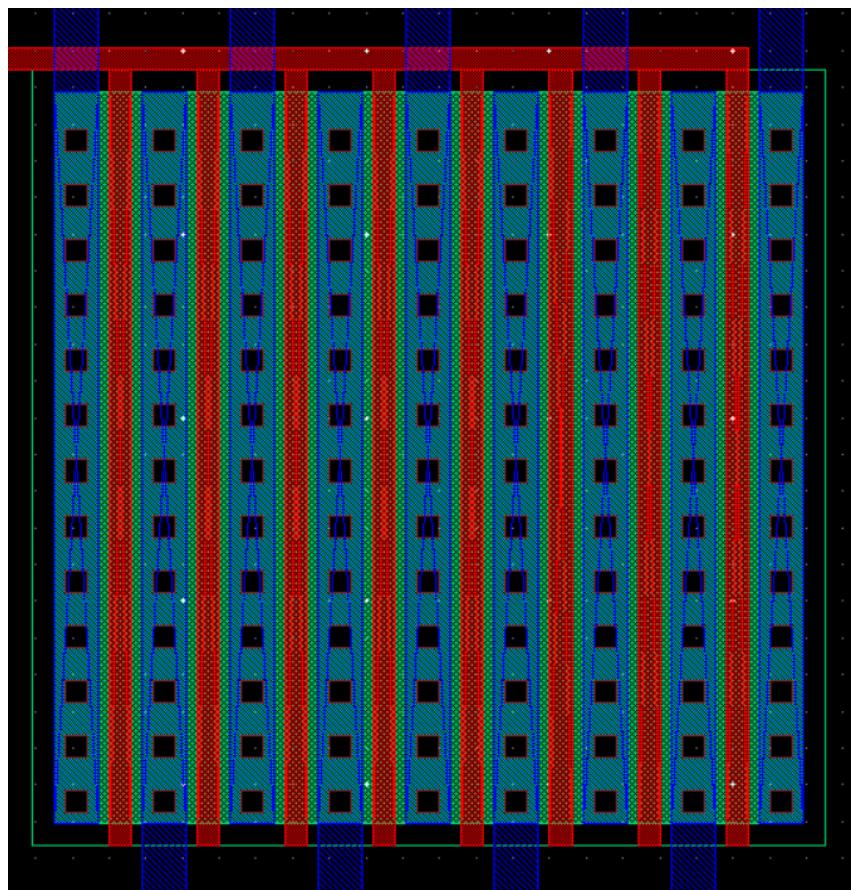
**Figure 4.10:** The NMOS transistor(M0) in extracted view



**Figure 4.11:** The NMOS transistor(M0) in layout



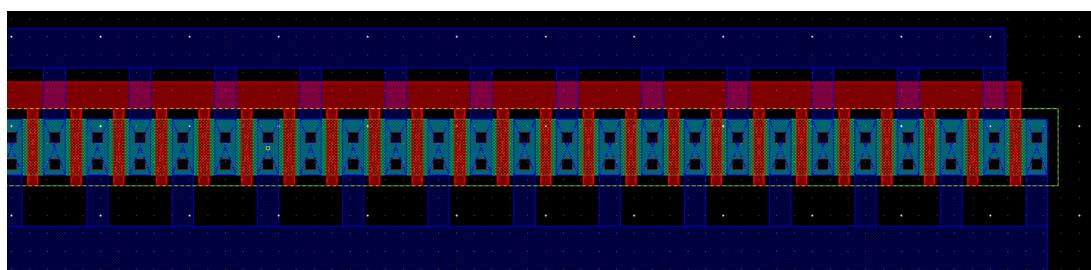
**Figure 4.12:** The NMOS transistor(M1) in extracted view



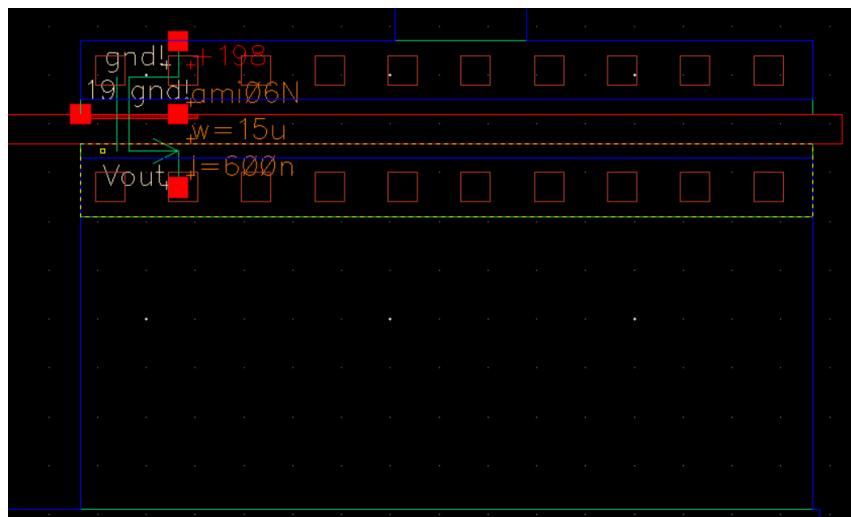
**Figure 4.13:** The NMOS transistor(M1) in layout



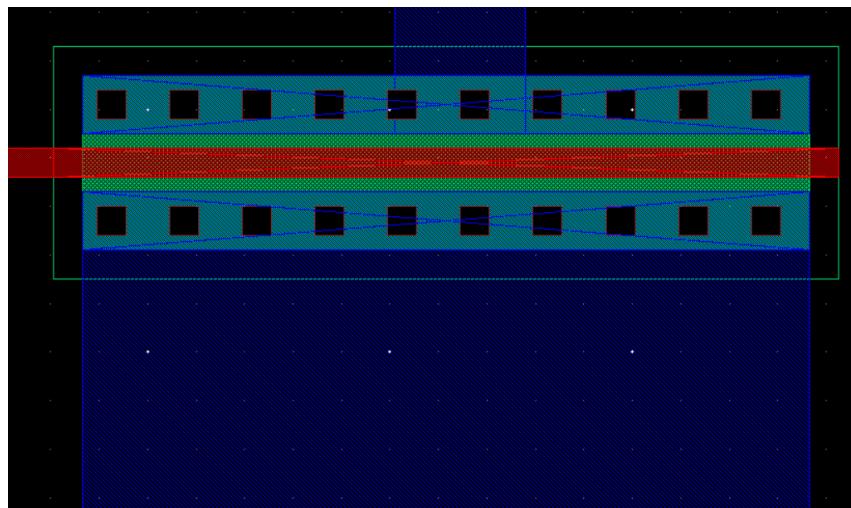
**Figure 4.14:** The NMOS transistor(M2) in extracted view(partial)



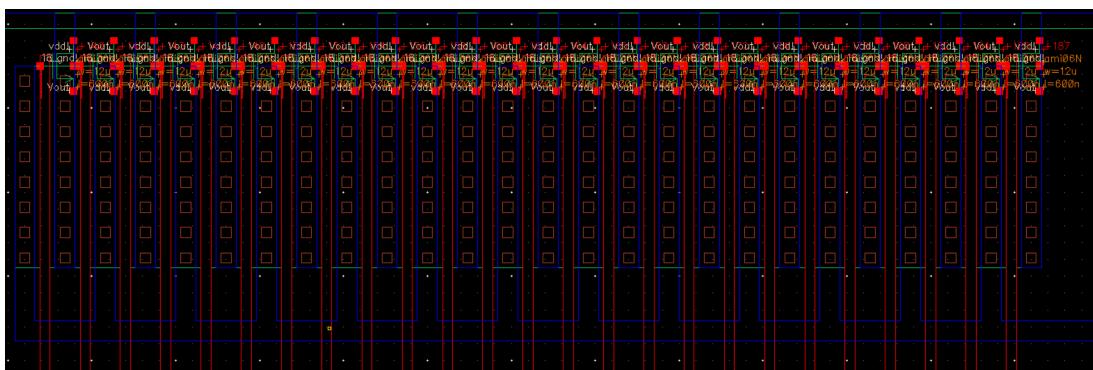
**Figure 4.15:** The NMOS transistor(M2) in layout(partial)

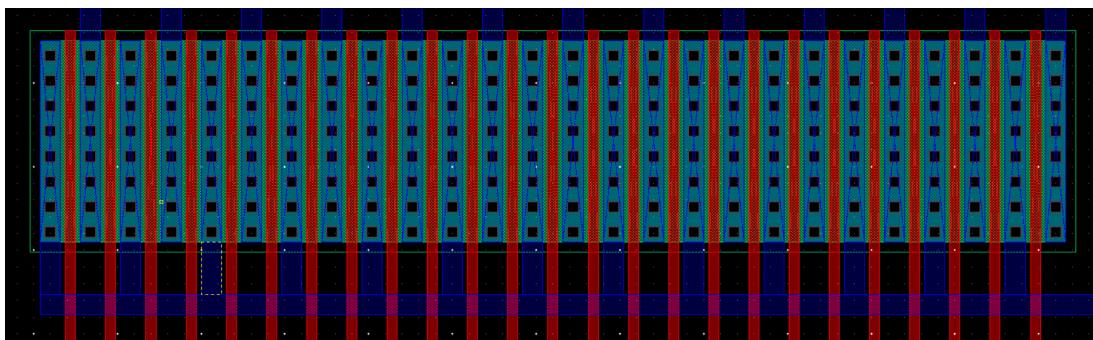


**Figure 4.16:** The NMOS transistor(M4) in extracted view

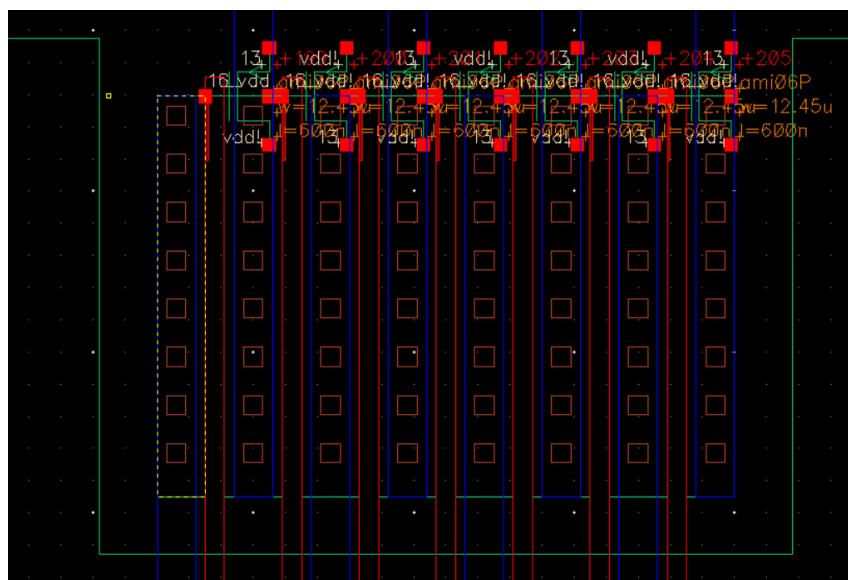


**Figure 4.17:** The NMOS transistor(M4) in layout

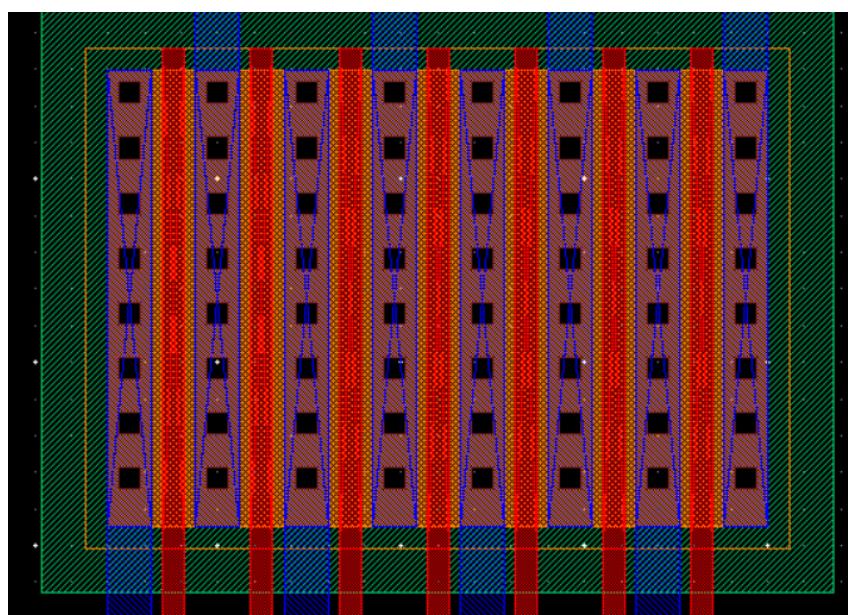




**Figure 4.19:** The NMOS transistor(M5) in layout



**Figure 4.20:** The PMOS transistor(M3) in extracted view



**Figure 4.21:** The PMOS transistor(M3) in layout

## 4.5 | The final layout of the cell

Finally, we built the final layout cell view for our circuit, as shown in Figure 4.22. In figure 4.23, shows the final cell in extracted view.

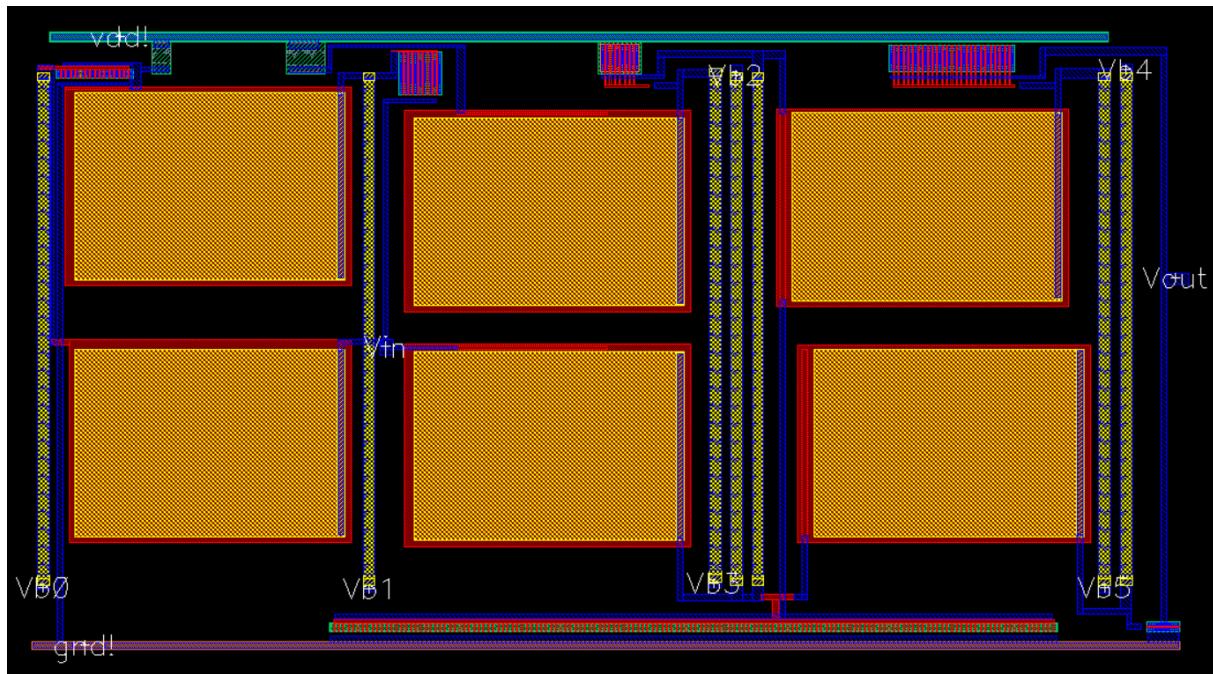


Figure 4.22: The layout of the final cell

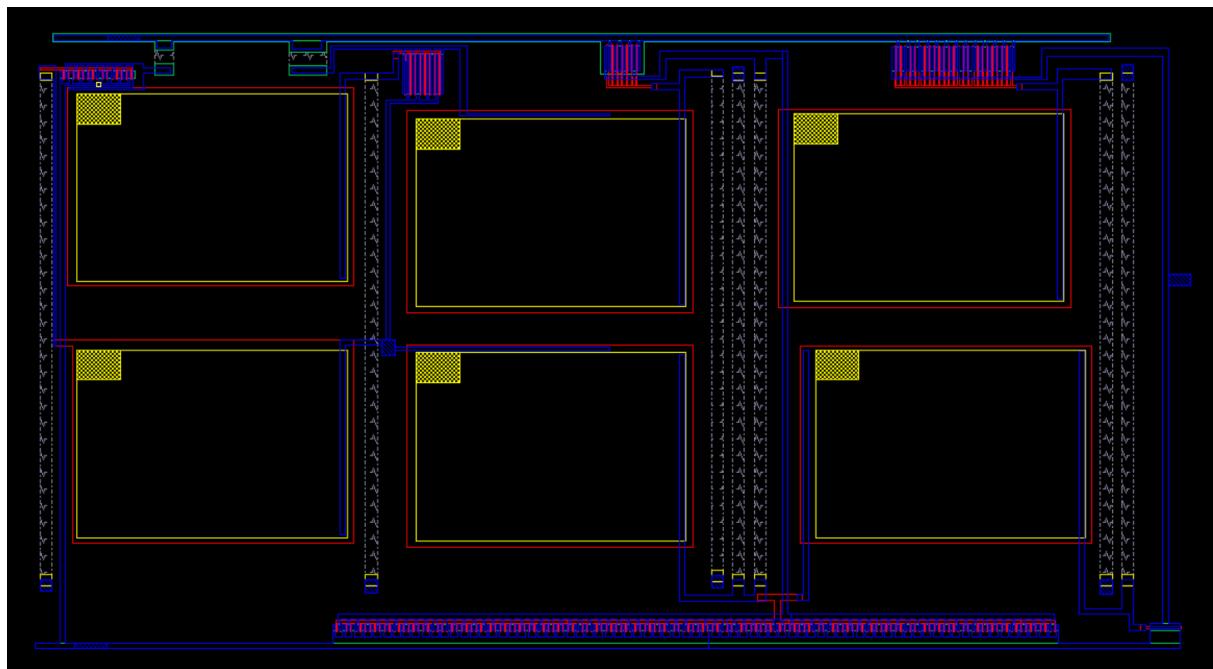


Figure 4.23: The extracted view of the final cell

The purpose of DRC is to ensure that the layout conforms to the design rules. As shown in Figure 4.24, in this physical design tool Virtuoso, DRC checks are performed well.



```
***** Summary of rule violations for cell "LNA_finally layout" *****
Total errors found: 0
```

**Figure 4.24:** The DRC of the final layout cell

The purpose of LVS(LVS stands for Layout vs. Schematic) is to ensure that the layout is an accurate representation of the original schematic and that there are no errors or mismatches between the two. During LVS, the tool will compare the layout and schematic data and check for differences, such as missing or extra connections, mismatched device sizes, or errors in the netlist. In Figure 4.25, we got a match. So our electrical properties of the circuit, such as resistance, and capacitance, match the original schematic.



**Figure 4.25:** The LVS of the final layout cell



## A | Reference

- [1] Bozorg, Amir, and Robert Bogdan Staszewski. “A 20 MHz–2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-Nm CMOS.” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 1, Jan. 2022, pp. 42–50, <https://doi.org/10.1109/tcsi.2021.3092960>.
- [2] Litmanen, P., et al. “A 2.0-GHz Submicron CMOS LNA and a Downconversion Mixer.” IEEE Xplore, 1 May 1998, [ieeexplore.ieee.org/document/698852](http://ieeexplore.ieee.org/document/698852).
- [3] Behzad Razavi. DESIGN of ANALOG CMOS : Integrated Circuits. 2017.
- [4] Gray, Paul R. Analysis and Design of Analog Integrated Circuits, 5th Edition. Wiley Global Education, 5 Jan. 2009.
- [5] Tony Chan Carusone, et al. Analog Integrated Circuit Design. Hoboken, Nj Wiley, 2012.