

VLSI Design: Final Project

Topic: ORCA_TOP Physical Design

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Introduction



Design Flow

Floorplaning



Power Routing



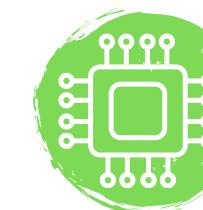
Placement



Clock Tree Synthesis



Routing

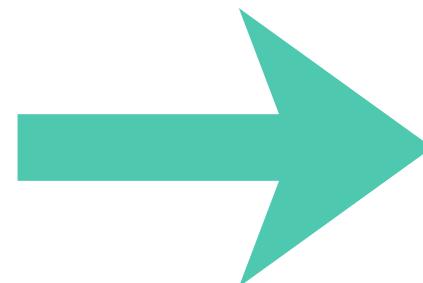
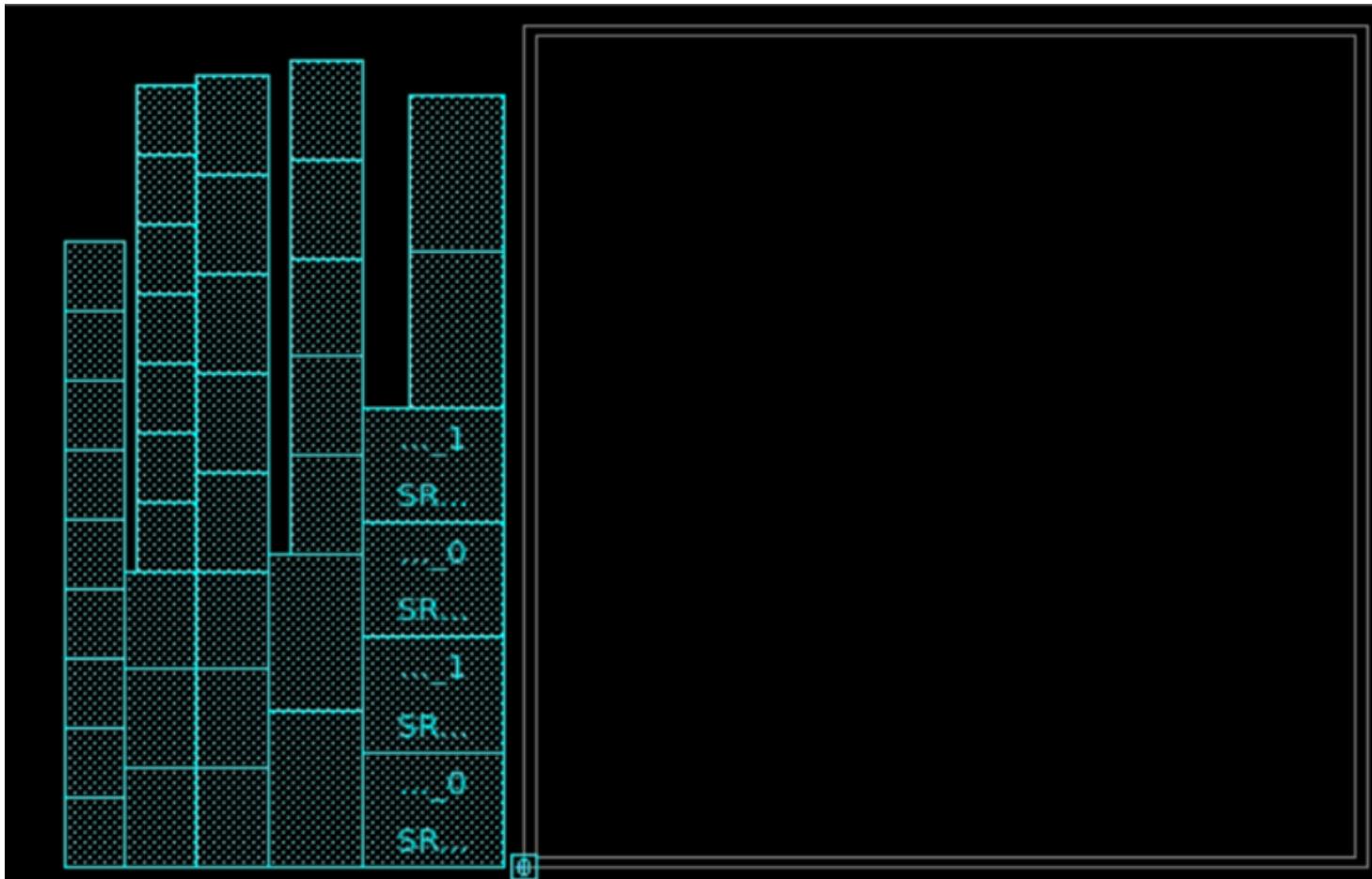


Project Design Specifications

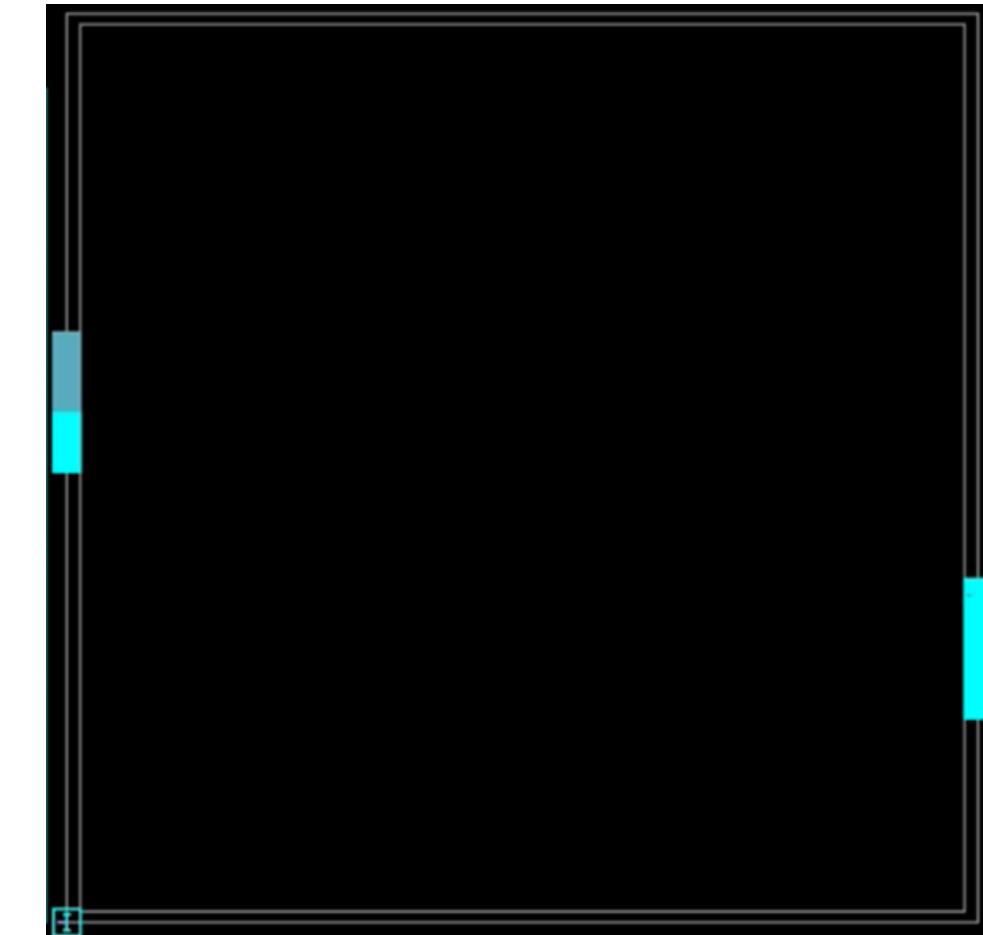
Architecture	RISC-V 32-bit processor core
Tool worked	Synopsys Fusion Compiler
Technology	saed32nm (32/28nm)
No. of Macros	40
No. of Power Domains	2
No. of I/O Ports	240
No. of Standard Cell	~53k
No. of Metal layers	9

Floorplanning

Initialize core area: utilization 0.75, R-shaped, offset 10



Port placement



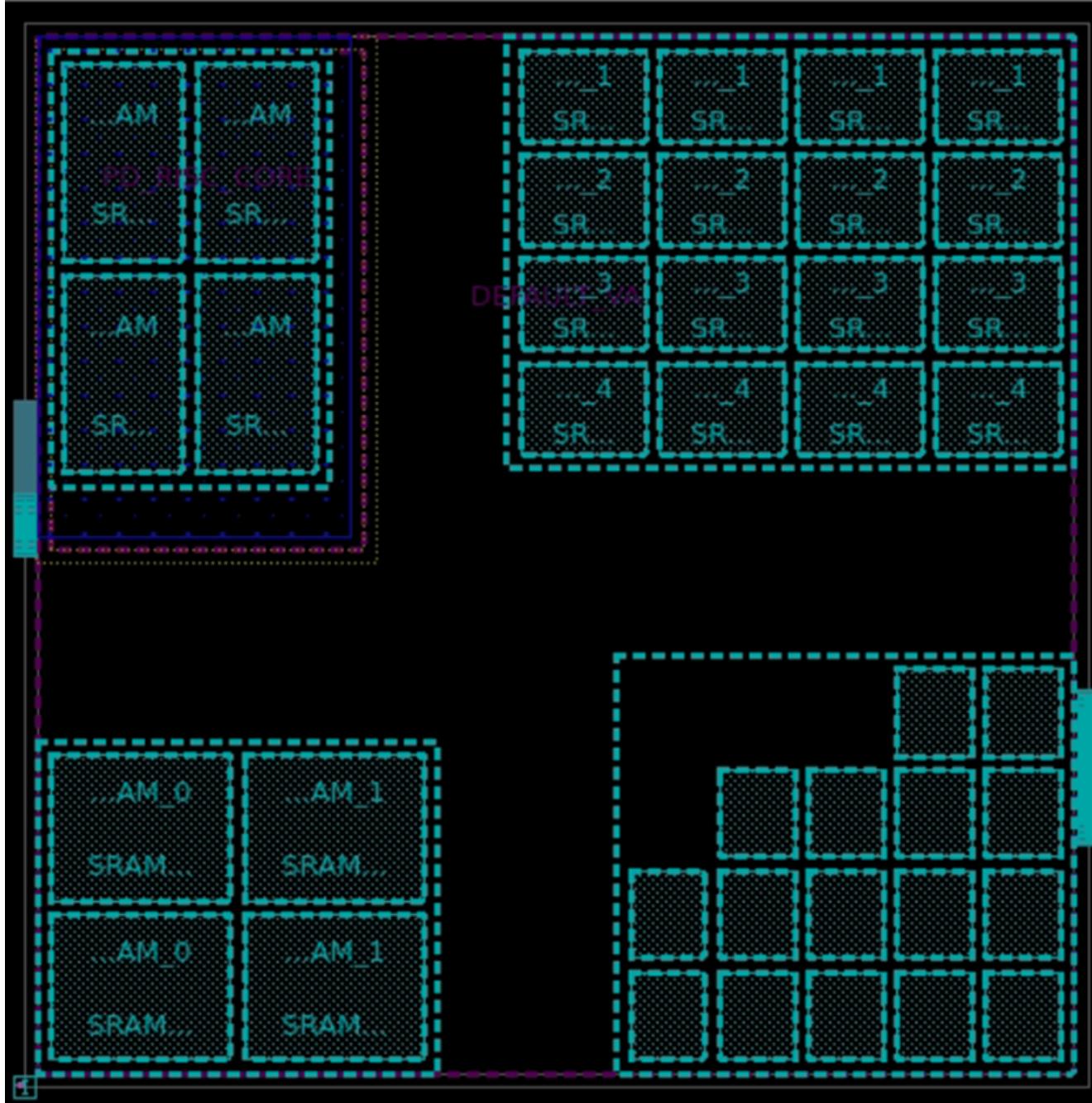
```
initialize_floorplan \
    -core_utilization 0.75 \
    -core_offset 10 \
    -shape Rect \
    -side_ratio {1 1} \
    -use_site_row
```

I/O Pin Placement

- Existing pin constraints cleared
- Input ports assigned to layers **M5/M7 (Side 1)**
- Output ports assigned to layers **M5/M7 (Side 3)**
- Pin offsets controlled for balanced distribution
- Automatic pin placement executed

Floorplanning

Macros placement & Create voltage area



Move by hand

Data Flow Flylines To know which macros should be together

Macro Configuration

Could not extract array structure, please configure the array below. **x**

Array Channel width
Rows 1 Columns 1 Horizontal 10.00 Flexible
Fill Vertical 10.00

Macro cells

Order	Reference name	Full name
1	SRAMLP2RW32x4	I_PCI_TOP/I_P...CI_FIFO_RAM_7
	SRAMLP2RW32x4	I_PCI_TOP/I_P...CI_FIFO_RAM_5
	SRAMLP2RW64x32	I_SDRAM_TOP/...D_FIFO_RAM_1
	SRAMLP2RW64x32	I_SDRAM_TOP/...D_FIFO_RAM_0
	CDRAM_DDIM64x32	I_CDRAM_TOP/...D_FIFO_RAM_1

Ok Cancel Apply Default

Using Macro Array to config chanel width (spacing) between macros

Adding keepout margin for Macros

1. Shift + H: Draw a shape
2. Click on shape and press Q
3. Get bbox
4. Put bbox to -region

```
create_voltage_area
  -power_domains PD_RISC_CORE
  -guard_band {{10 10}}
  -region {{10.0000 406.4160} {241.3440 775.7760}}
```

Floorplanning

```
fc_shell> check_legality -verbose
*****
Report : Legality
*****
```

VIOLATIONS BY CATEGORY:

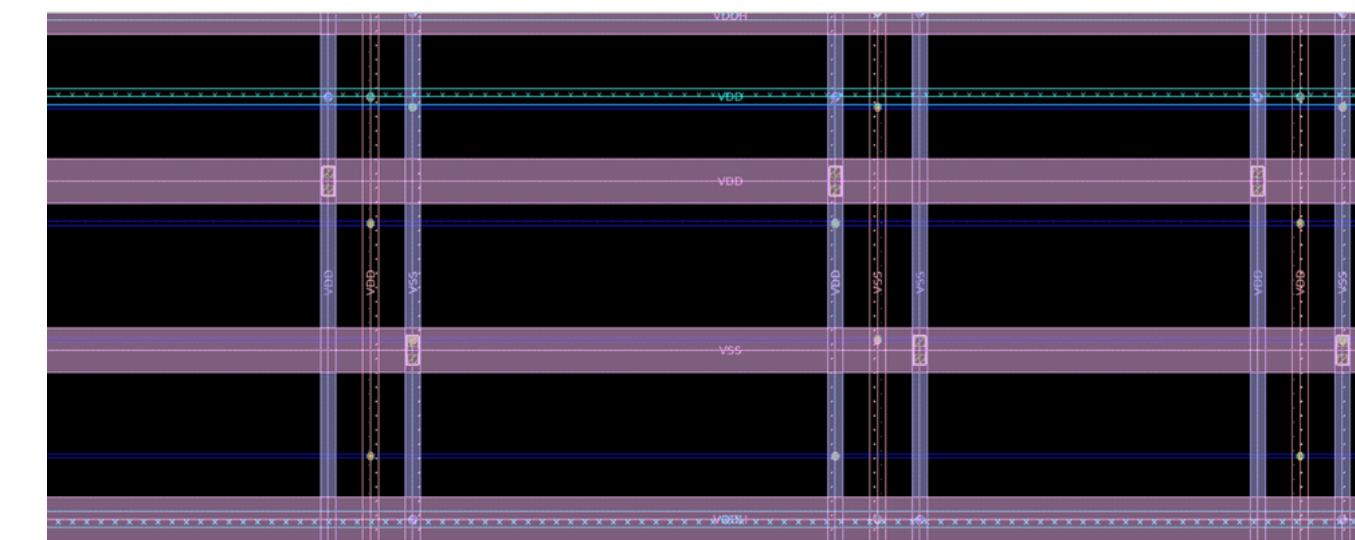
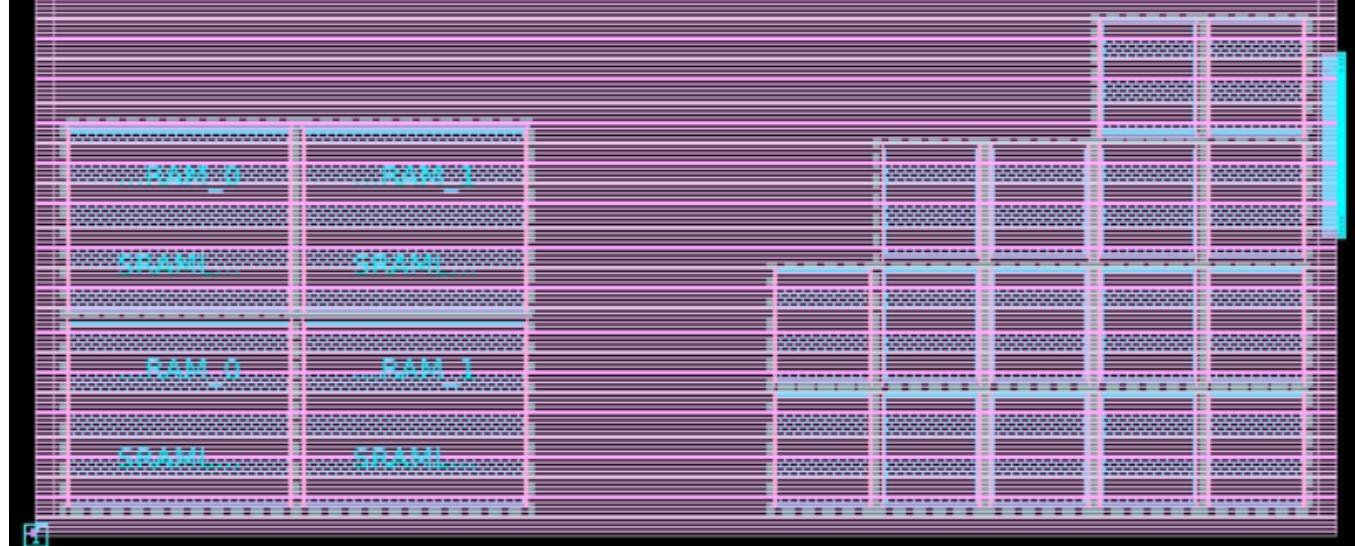
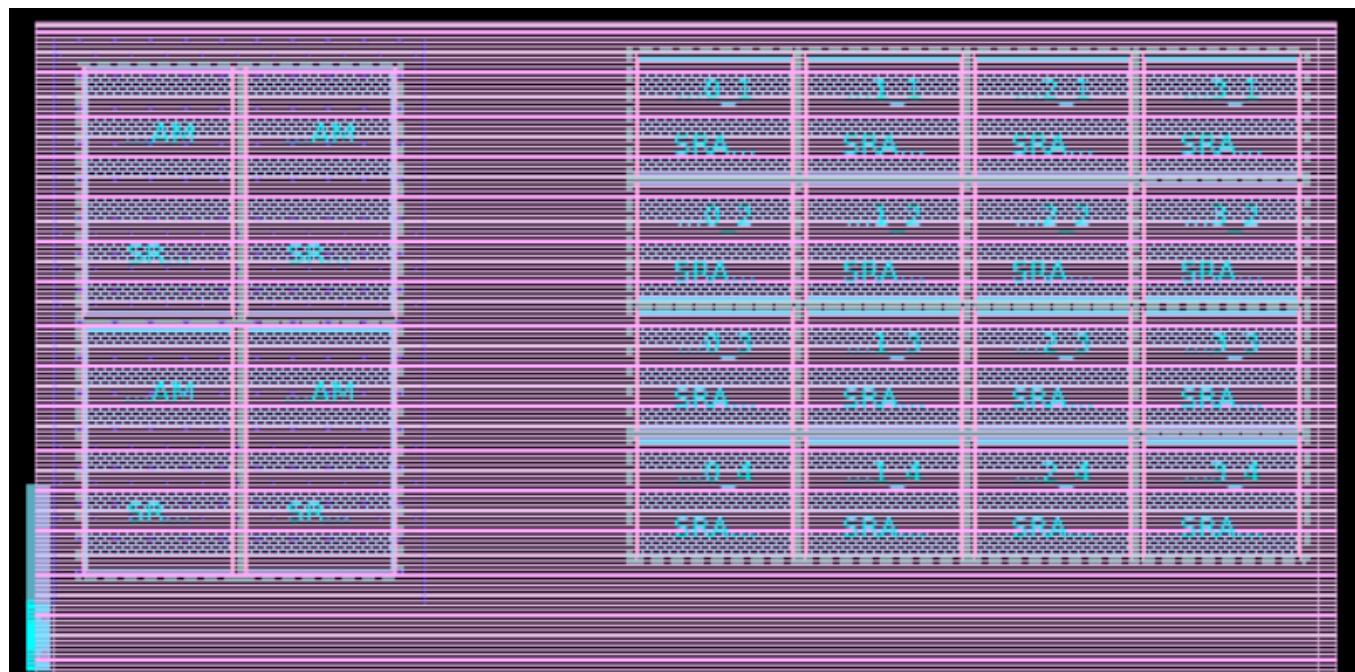
MOVABLE	APP-FIXED	USER-FIXED	DESCRIPTION
0	0	0	Two objects overlap.
0	0	0	A cell violates a pnet.
0	0	0	A cell is illegal at a site.
0	0	0	A cell is not aligned with a site.
0	0	0	A cell has an illegal orientation.
0	0	0	A cell spacing rule is violated.
0	0	0	A layer rule is violated.
0	0	0	A cell is in the wrong region.
0	0	0	Two cells violate cts margins.
0	0	0	Two cells violate coloring.
0	0	0	TOTAL

TOTAL 0 Violations.

```
fc_shell> check_pg_drc -ignore_std_cells -do_not_check_shapes_in_hier_blocks
Command check_pg_drc started at Mon Feb 23 23:47:50 2026
Command check_pg_drc finished at Mon Feb 23 23:47:52 2026
CPU usage for check_pg_drc: 1.84 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 2.01 seconds ( 0.00 hours)
No errors found.
fc_shell>
```

```
fc_shell> report_utilization
*****
Report : report_utilization
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Sat Feb 14 08:44:53 2026
*****
Utilization Ratio: 0.7068
Utilization options:
- Area calculation based on: site_row of block ORCA_TOP
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area: 586645.6781
Total Capacity Area: 247983.8036
Total Area of cells: 175285.9124
Area of excluded objects:
- hard_macros : 270039.1823
- macro_keepouts : 68622.6922
- soft_macros : 0.0000
- io_cells : 0.0000
- hard_blockages : 0.0000
Total Area of excluded objects: 338661.8745
Ratio of excluded objects: 0.5773
Utilization of site-rows with:
- Site 'unit': 0.7068
0.7068
fc_shell>
```

Power Routing



1. Multi-Voltage Power Architecture

- Two voltage domains:
 - DEFAULT_VA** → VDD / VSS
 - PD_RISC_CORE** → VDDH / VSS
- Independent PG mesh per voltage area
- Global M9 layer distributes VDD, VDDH, and VSS

2. Standard Cell Power Rails (M1)

- M1 horizontal rails for standard cell power connection
- Blocked over hard macros (respect **keepout regions**)
- Separate rail strategies per voltage domain

3. Hierarchical Power Mesh (M6–M9)

- M6 (Vertical), M7 (Horizontal), M8 (Vertical) → Local mesh per voltage area
- M9 (Horizontal) → Global top-level distribution
- Track-aligned stripe generation
- Custom via rules from M9 down to M6 and std-cell connections
- **IR drop** optimized via stacked via strategy

4. Macro Power Planning

- Dedicated PG regions created per macro
- M5/M6 power rings around macros
- Separate rings for:
 - VDD/VSS (Default domain)
 - VDDH/VSS (RISC domain)
- Scattered pin connection from macro pins to rings

Power Routing

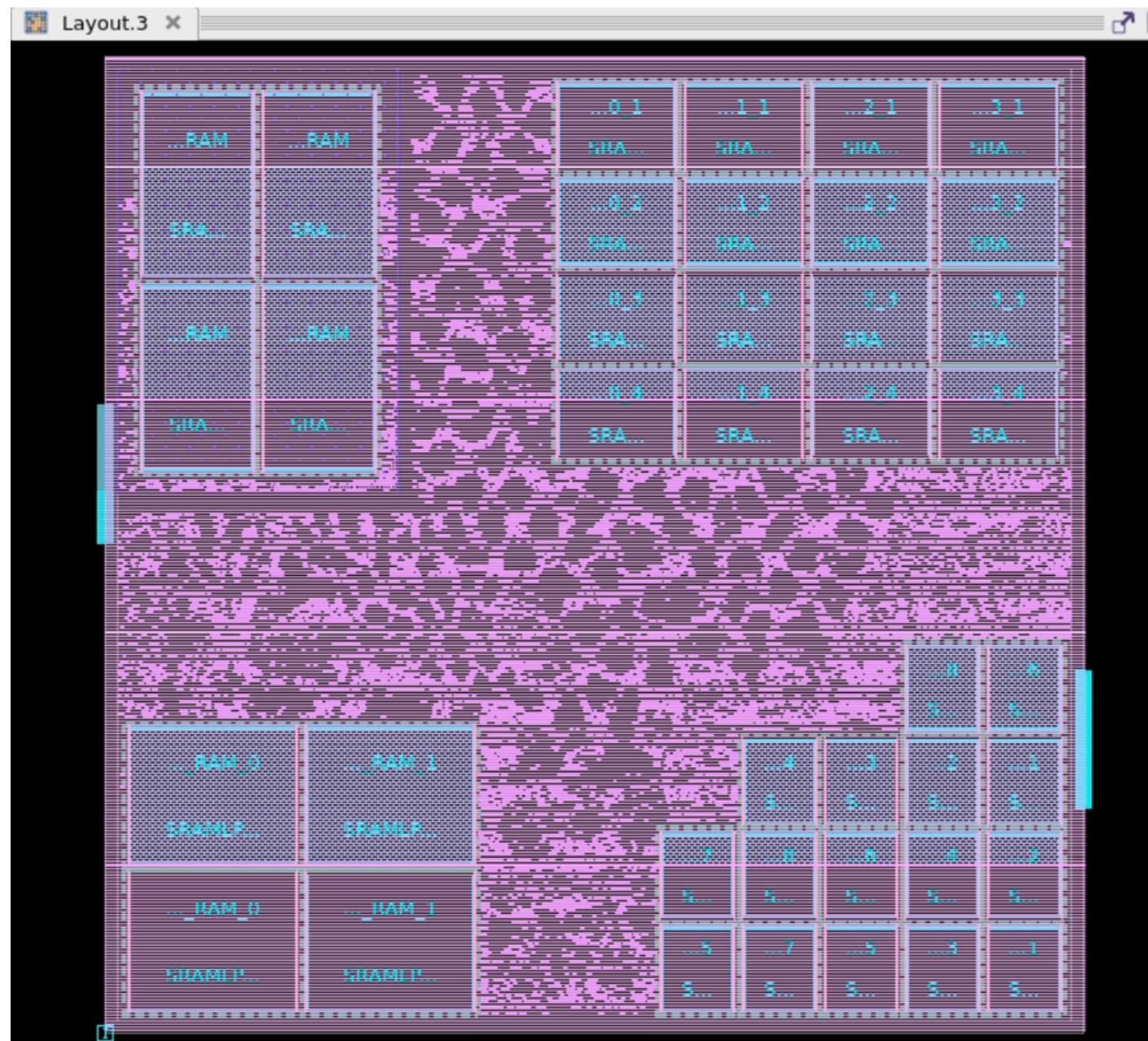
```
fc_shell> check_legality
=====
 2D Rule Check Legality Report =====
          Violating Cells
Legality Rules      Moveable AppFixed UserFixed Total
-----
overlap            0     0     0     0
spacing_rule       0     0     0     0
cell_on_site       0     0     0     0
legal_orient       0     0     0     0
va_bound           0     0     0     0
pg_drc             0     0     0     0
-----
Total Violations  0     0     0     0
=====
```

```
fc_shell> check_pg_missing_vias
Check net VDD vias...
Number of missing vias: 0
Checking net VDD vias took 0 seconds.
Check net VDDH vias...
Number of missing vias: 0
Checking net VDDH vias took 0 seconds.
Check net VSS vias...
Number of missing vias: 0
Checking net VSS vias took 1 seconds.
Overall runtime: 1 seconds.
fc_shell>
```

```
fc_shell> check_pin_placement -wire_track true
No violation has been found
***Summary***
-----
Type of Violation | Count
-----+-----+
Missing Pins      | 0
Pins Off Track    | 0
Pin Short          | 0
Technology Spacing | 0
-----+-----+
Total Violations  | 0
-----
```

```
fc_shell> check_pg_connectivity
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD Secondary Net:
Primary Net : VDDH Secondary Net:
Primary Net : VSS Secondary Net:
Loading cell instances...
Number of Standard Cells: 80257
Number of Macro Cells: 40
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 3626
Number of VDD Vias: 67372
Number of VDD Terminals: 0
*****Verify net VDD connectivity*****
Number of floating wires: 721
Number of floating vias: 0
Number of floating std cells: 52877
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VDDH Wires: 504
Number of VDDH Vias: 1808
Number of VDDH Terminals: 0
*****Verify net VDDH connectivity*****
Number of floating wires: 107
Number of floating vias: 0
Number of floating std cells: 5760
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 6549
Number of VSS Vias: 81489
Number of VSS Terminals: 0
*****Verify net VSS connectivity*****
Number of floating wires: 464
Number of floating vias: 0
Number of floating std cells: 57656
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Overall runtime: 4 seconds.
```

Placement



1. Routing Layer Constraint

- Routing layers limited from **M1 to M8**
 - Controls routing resource usage during placement optimization

2. Tie Cell Handling

- Enable tie cell usage during optimization
 - Max fanout per tie cell = 8
 - Allow tool to insert tie cells automatically

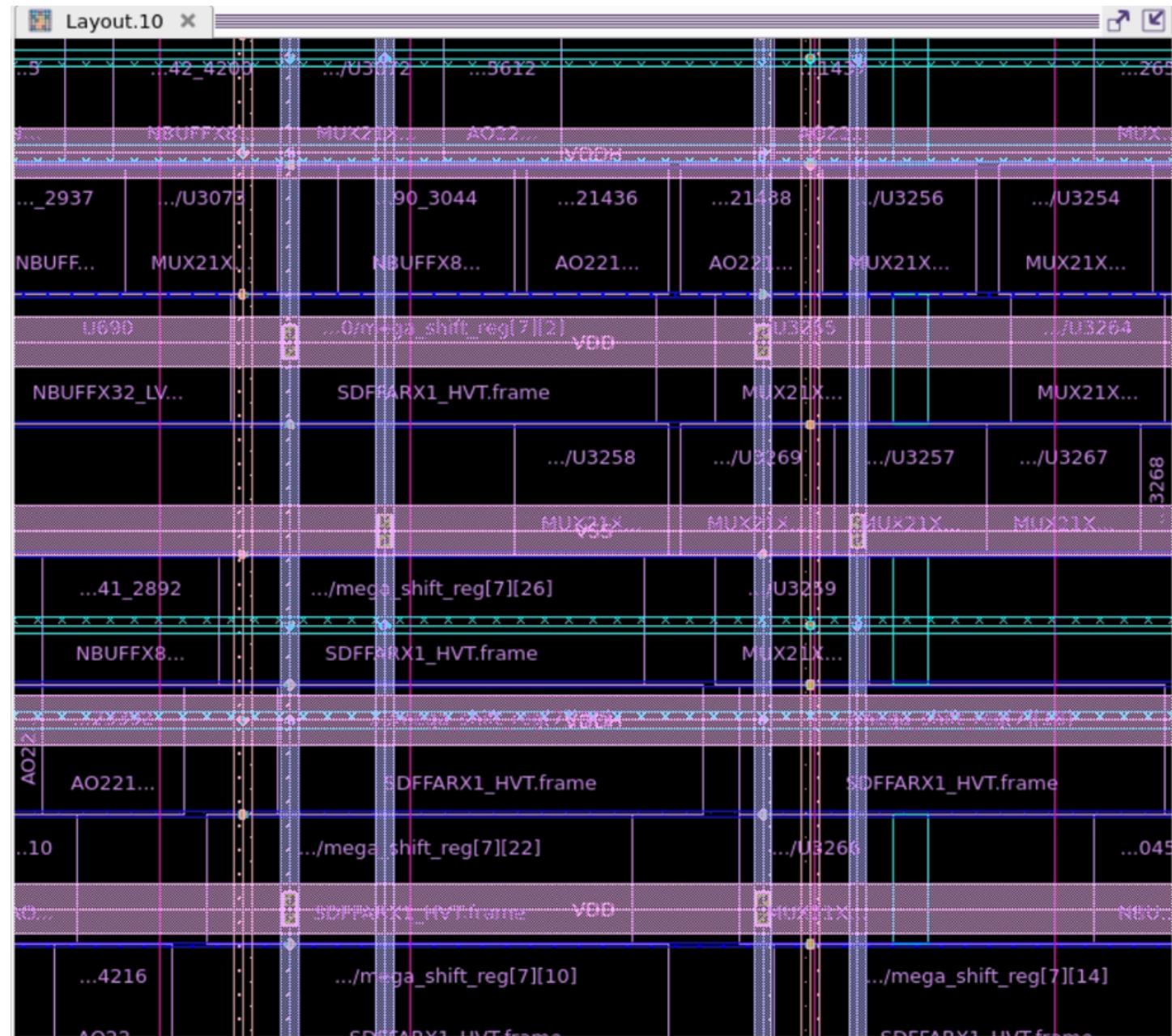
3. Density Control Strategy

- Enable RDE (Routing Driven Estimation)
 - Enhanced automatic density control activated
 - Timing-aware and congestion-aware placement enabled

4. Scan Chain Optimization

- Read scan DEF before placement
 - Stop flow if scan DEF is missing
 - Enable scan chain reordering & optimization

Placement



5. High-Effort Optimization Settings

- Advanced legalizer enabled
- Congestion effort = High
- Timing effort = High
- Area effort = Ultra
- Buffer area effort = Ultra
- Global routing effort = High

6. Clock & Power Aware Placement

- Clock-aware placement enabled
- Power-aware optimization enabled
- Leakage optimization = conventional

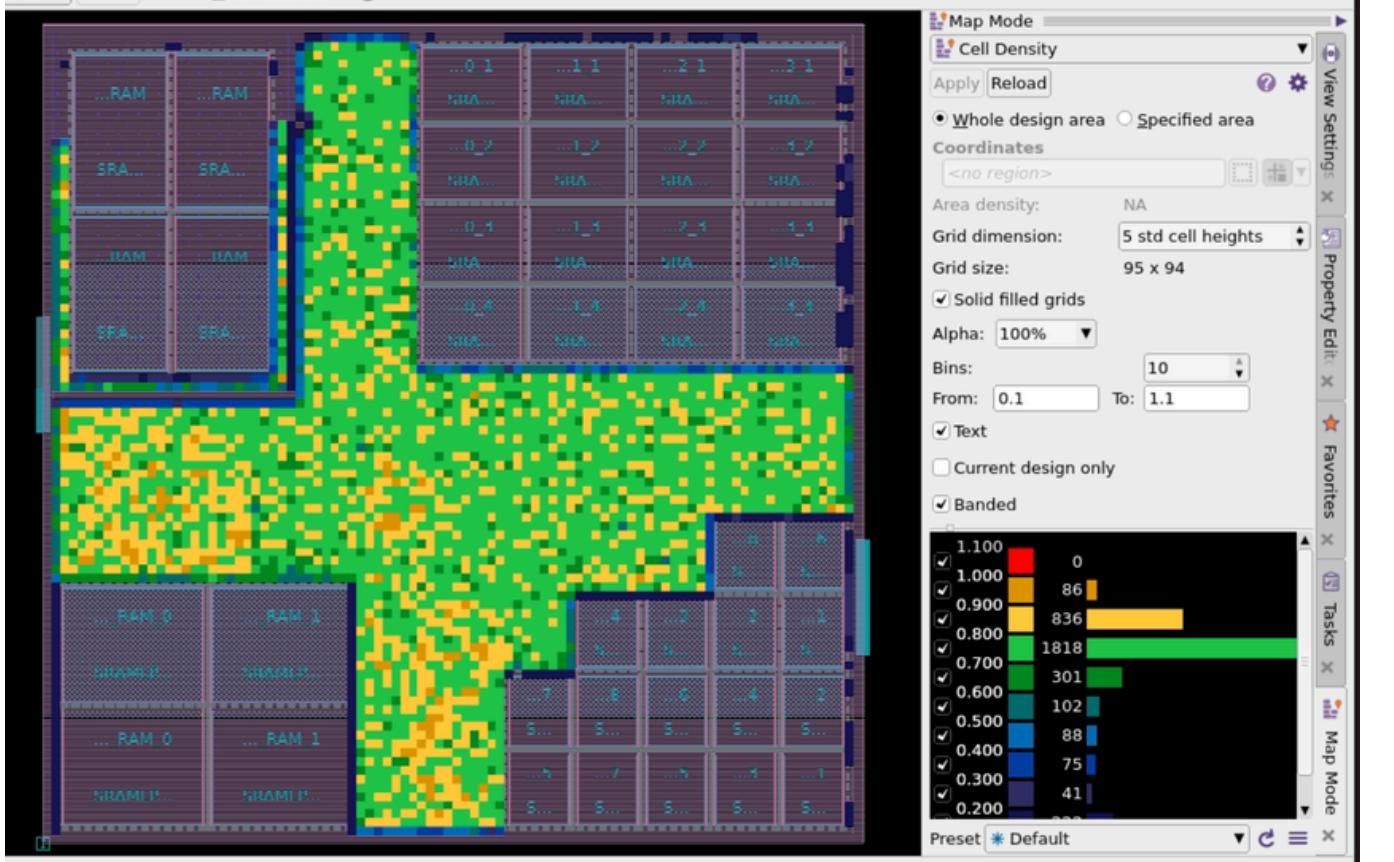
7. Naming & Feature Control

- Prefix added for new cells: POPT_
- Disabled advanced features:
 - Clock gate latency estimation
 - CCD (Concurrent Clock Data optimization)

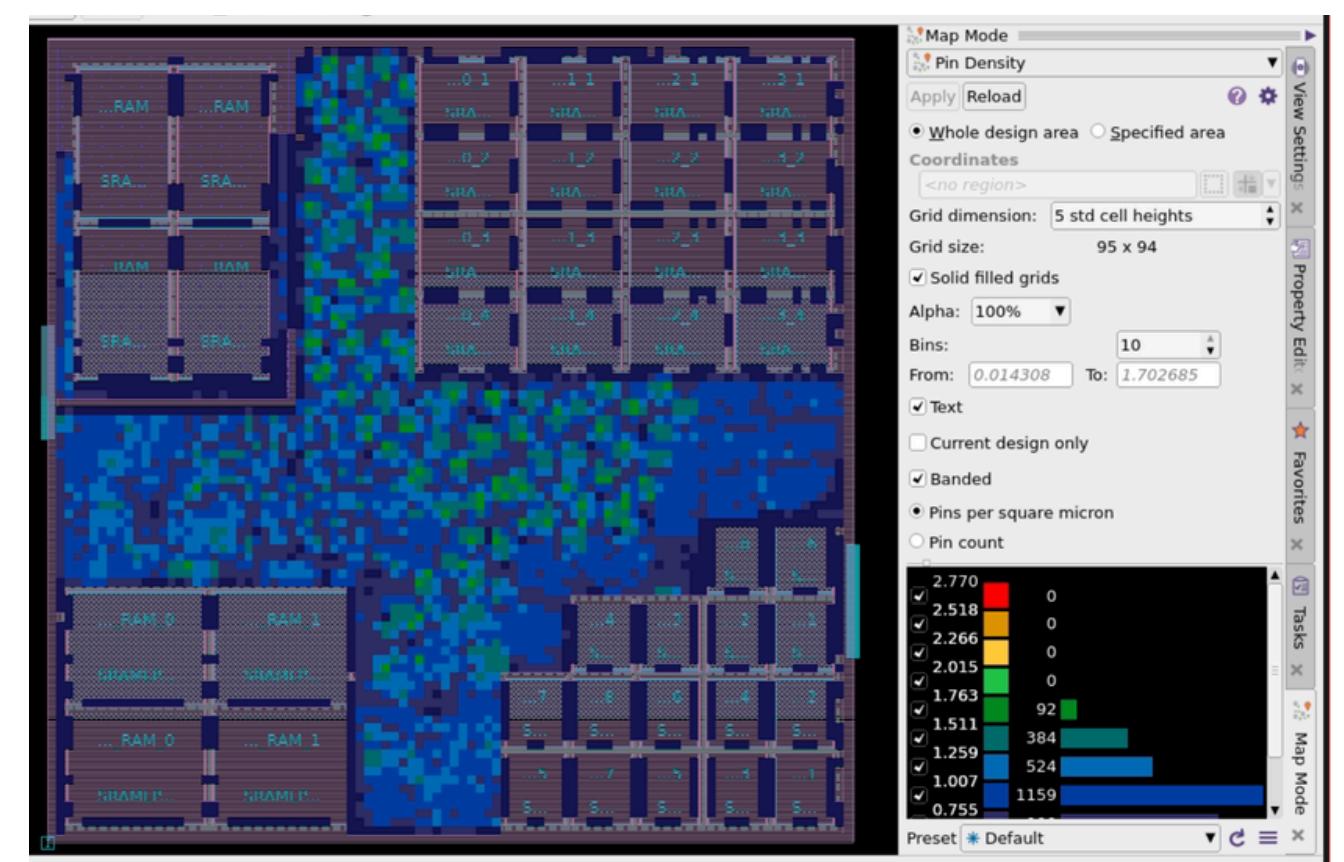
8. Execution

- Run place_opt
- Automatic power/ground connection after placement

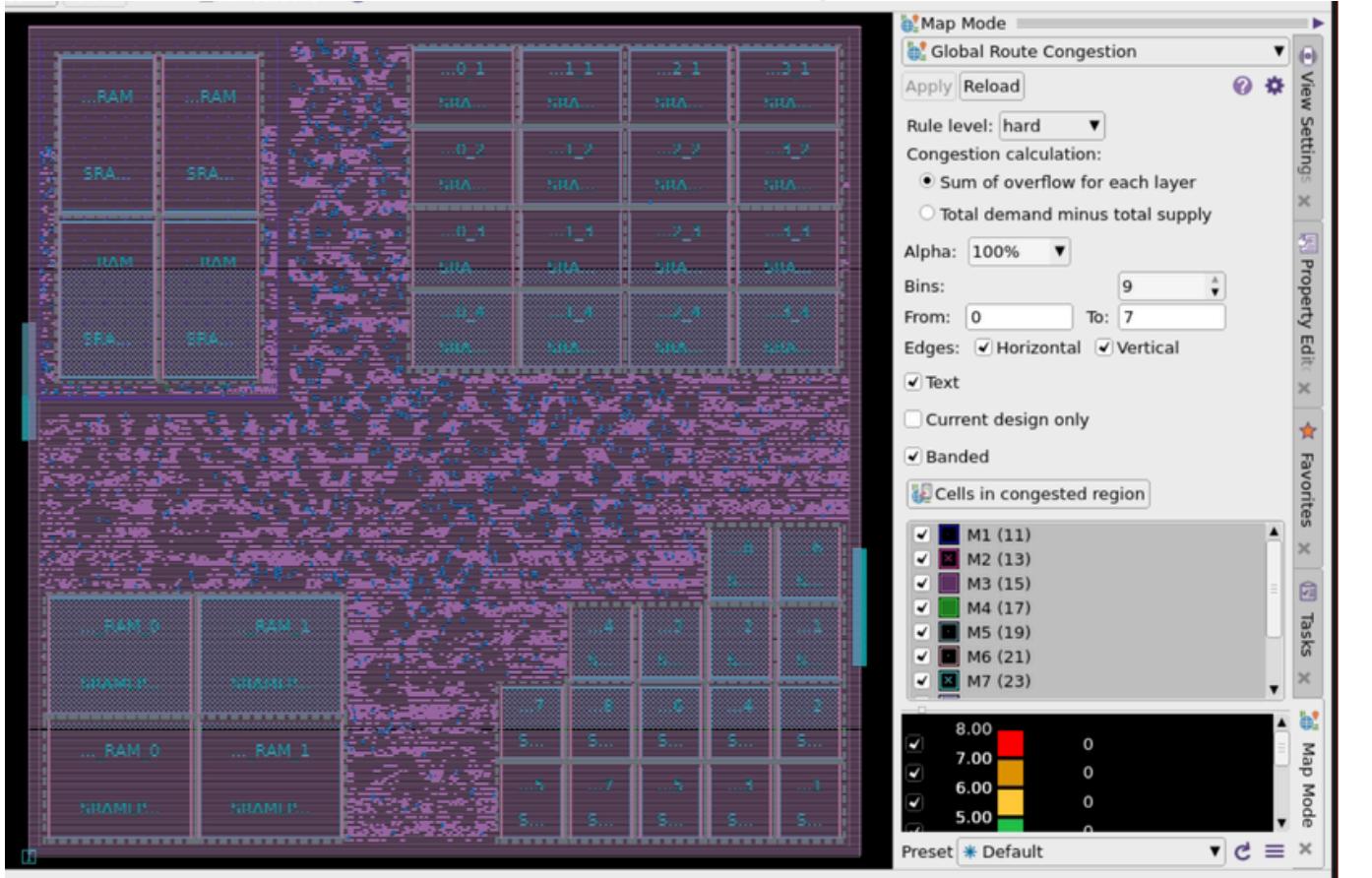
Cell Density



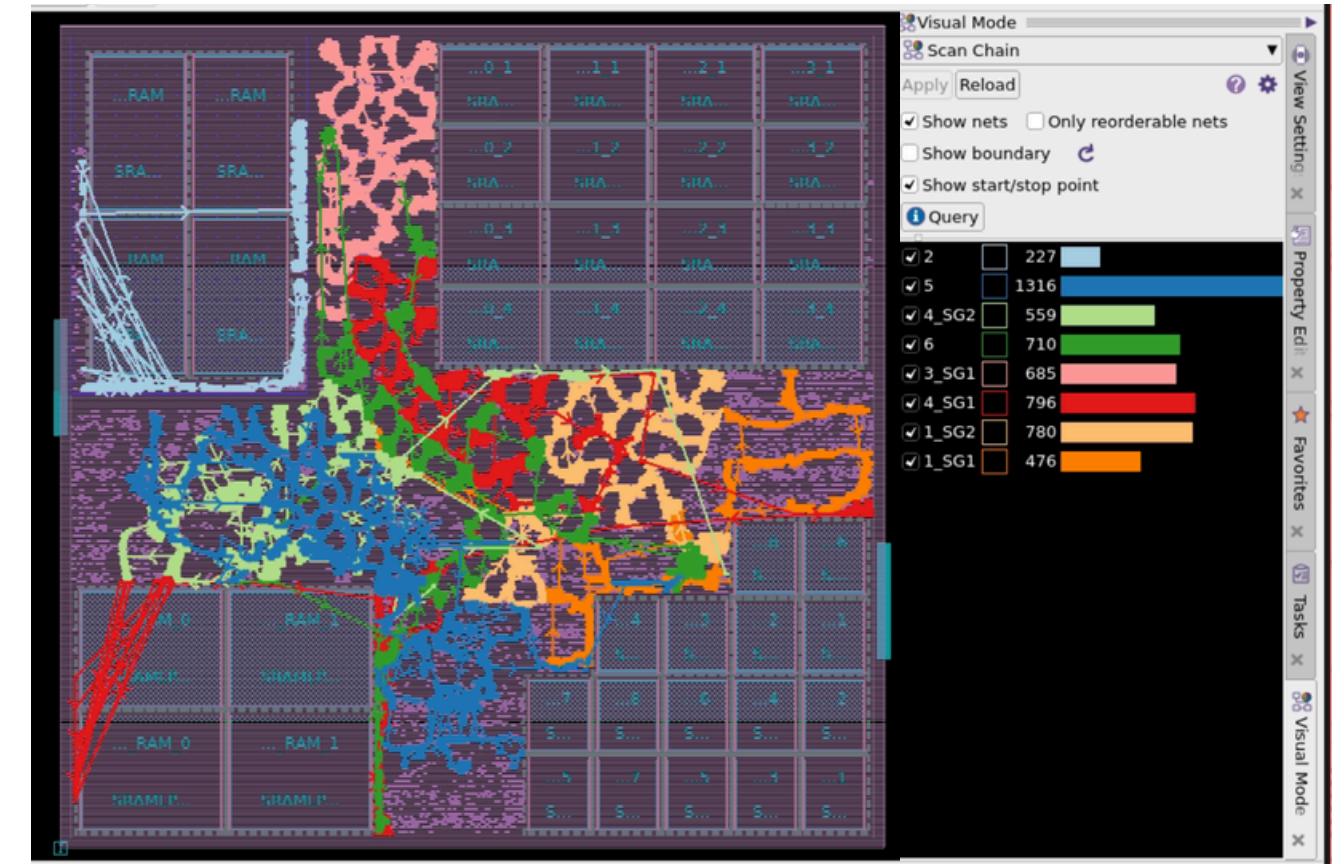
Pin Density



Global Route Congestion



Scan Chain



Placement

```
fc_shell> check_legality
=====
2D Rule Check Legality Report =====
          Violating Cells
Legality Rules      Moveable AppFixed UserFixed Total
-----
overlap           0       0       0       0
spacing_rule      0       0       0       0
cell_on_site      0       0       0       0
legal_orient      0       0       0       0
va_bound          0       0       0       0
pg_drc            0       0       0       0
-----
Total Violations 0       0       0       0
=====
Information: Dynamic Rule Ordering (DRO): true
NPLDRC: Processed 263 libCells; 256 unique
NPLDRC: 263 LibCell Equivalence info written to file
NPLDRC Place Cache: unique cache elements 1768
NPLDRC Place Cache: read cache elements 1768
NPLDRC Place Cache: hit rate 100.0% (0 / 59026)
NPLDRC Access Cache: unique cache elements 6255
NPLDRC Access Cache: read cache elements 6255
NPLDRC Access Cache: hit rate 100.0% (0 / 59026)
```

```
fc_shell> check_mv_design
*****
Report : check_mv_design
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Tue Feb 24 04:37:10 2026
*****
----- Summary -----
Information: Total 0 error(s) and 0 warning(s) from check_mv_design. (MV-082)
```

```
fc_shell>
report_qor -summary
*****
Report : qor
    -summary
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Tue Feb 24 04:38:55 2026
*****
Timing
-----
Context          WNS        TNS        NVE
-----
func_ss0p75v125c_cmax
                  (Setup)    -1.75     -672.21    1213
test_ss0p75v125c_cmax
                  (Setup)    -0.35     -1.03      3
Design          (Setup)    -1.75     -672.21    1213
func_ss0p75v125c_cmax
                  (Hold)     -0.18     -3.38      124
test_ss0p75v125c_cmax
                  (Hold)     -0.20     -32.65    424
Design          (Hold)     -0.20     -32.71    425
-----
```

Placement

```
fc_shell> report_constraint
*****
Report : constraint
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Tue Feb 24 04:45:18 2026
*****
```

Constraint	Cost
min_delay/hold	0.69 (VIOLATED)
max_delay/setup	0.35 (VIOLATED)
max_transition	46.94 (VIOLATED)
max_capacitance	251.38 (VIOLATED)
min_capacitance	0.00 (MET)

report_utilization

```
report_utilization -config util_config
*****
```

```
Report : report_utilization
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Tue Feb 24 04:43:36 2026
*****
```

```
Utilization Ratio:          0.7289
Utilization options:
- Area calculation based on: core_area of block ORCA_TOP
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                586645.6781
Total Capacity Area:        254043.9686
Total Area of cells:        185185.3295
Area of excluded objects:
- hard_macros      : 264884.2695
- macro_keepouts   : 67717.4400
- soft_macros      : 0.0000
- io_cells         : 0.0000
- hard_blockages   : 0.0000
Total Area of excluded objects: 332601.7095
Ratio of excluded objects:    0.5670
```

0.7289

report_utilization (PD_RISC_CORE)

```
report_utilization -config util_config -of_objects [get_voltage_areas PD_RISC_CORE]
*****
```

```
Report : report_utilization
```

```
Design : ORCA_TOP
```

```
Version: V-2023.12-SP4
```

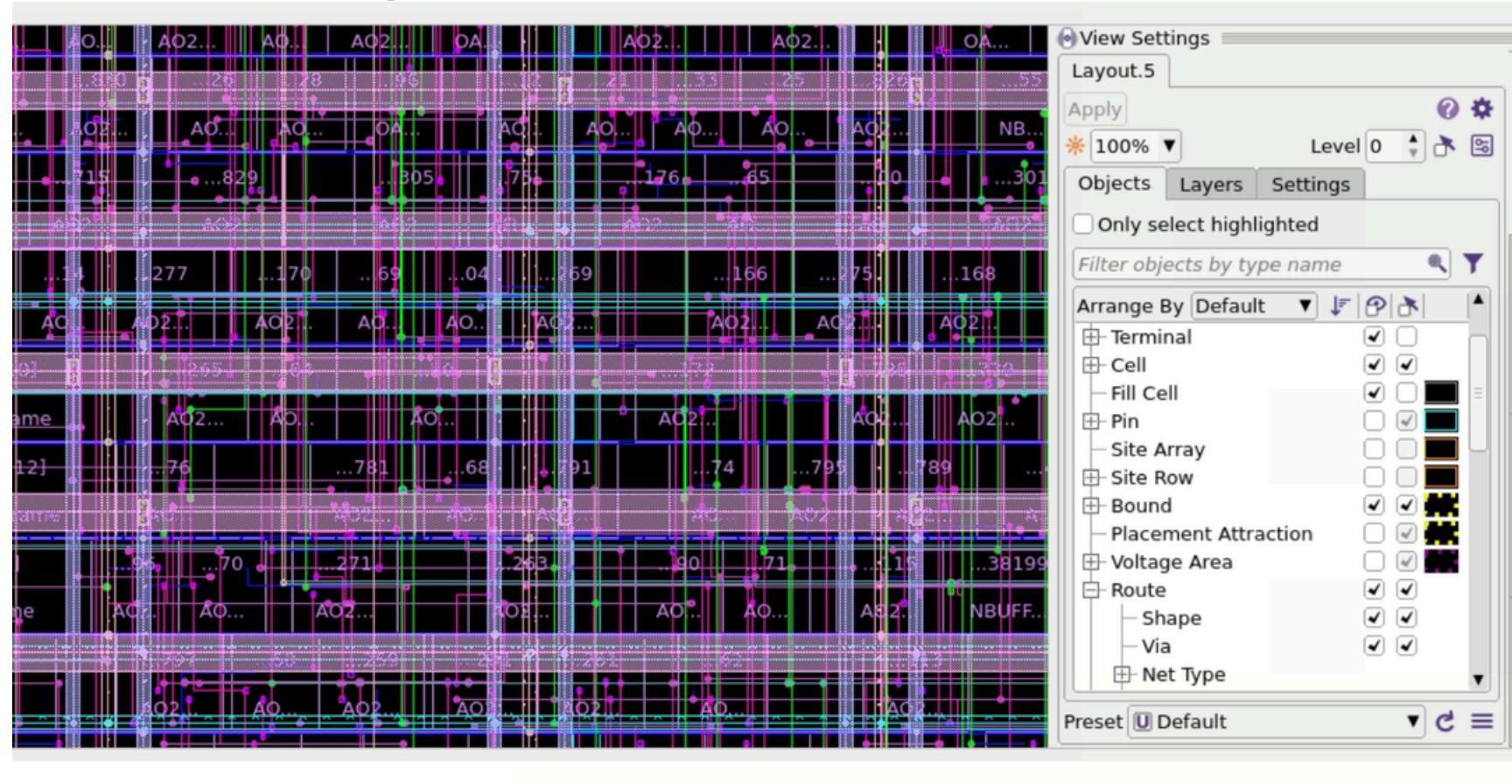
```
Date   : Tue Feb 24 04:44:04 2026
*****
```

```
Utilization Ratio:          0.5404
Utilization options:
- Area calculation based on: Voltage area PD_RISC_CORE
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                77050.1830
Total Capacity Area:        16119.3000
Total Area of cells:        8711.0397
Area of excluded objects:
- hard_macros      : 51184.6830
- macro_keepouts   : 9746.2000
- soft_macros      : 0.0000
- io_cells         : 0.0000
- hard_blockages   : 0.0000
Total Area of excluded objects: 60930.8830
Ratio of excluded objects:    0.7908
```

0.5404

Clock Tree Synthesis

Clock path routed



1. Multi-Scenario Setup

- Dedicated CTS and ClockOpt scenarios
- Propagated clock enabled post-CTS
- Multi-corner timing optimization

2. CTS Build & Route

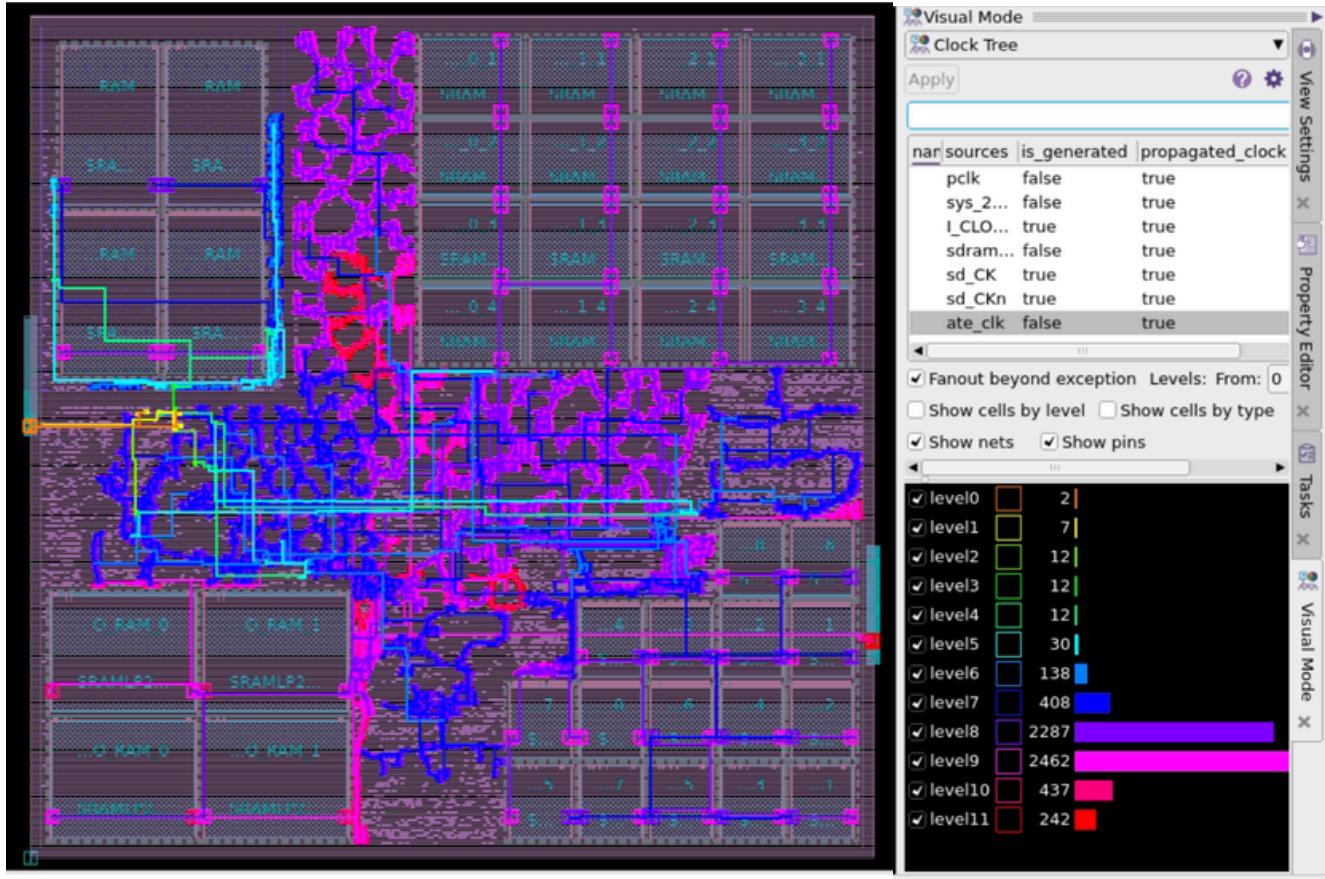
- `clock_opt` (`build_clock` → `route_clock`)
- Routing layers: **M5–M8**
- Selected LVT buffers / inverters / CG cells only
- CRPR removal enabled
- Local skew optimization
- Target skew: **100 ps**
- Max transition: **0.15**

3. CTS Routing Strategy

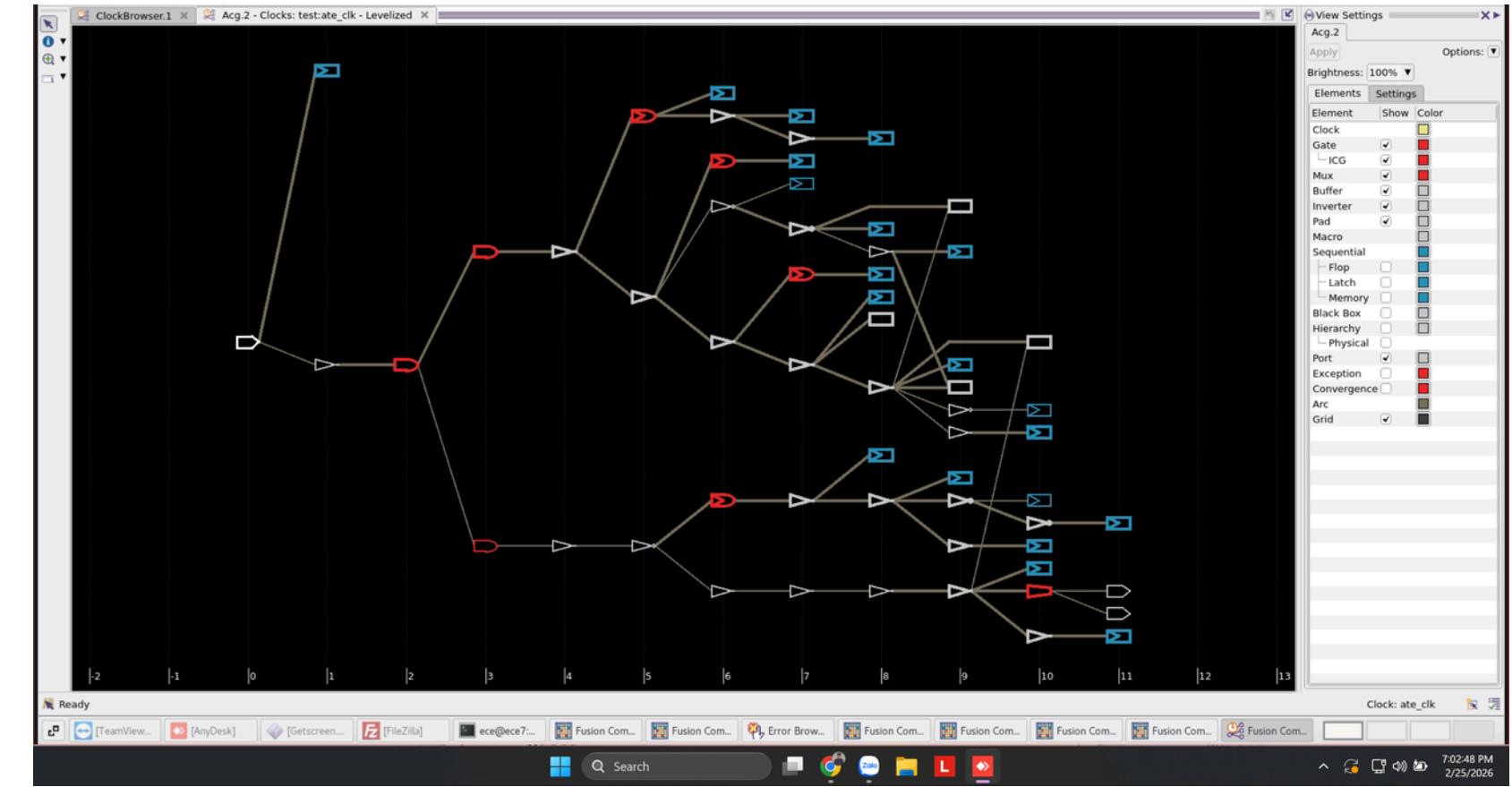
- Custom NDR (2w2s style)
- Increased width & spacing (especially upper metals)
- Higher spacing weight on **M5–M8**
- Improves SI and clock stability

Clock Tree Synthesis

ate_clk Clock Tree



ate_clk Leveled Clock Tree



4. Post-CTS Optimization

- clock_opt (final_opto → final_opto)
- Routing layers extended to **M1–M9**
- High-effort hold fixing
- Congestion-aware refinement
- Clock-aware scan reorder
- Dedicated hold-fix cells enabled

5. Implementation Controls

- Tie cells enabled (max fanout = 8)
- CTS cell filtering via lib_cell_purpose
- Instance prefixes:
 - CTS_
 - CLKOPT_
- Automatic PG reconnection

Clock Tree Synthesis

```
fc_shell> report_constraint
*****
Report : constraint
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Wed Feb 25 07:10:04 2026
*****
```

Constraint	Cost
min_delay/hold	0.46 (VIOLATED)
max_delay/setup	0.00 (MET)
max_transition	111.10 (VIOLATED)
max_capacitance	1061.41 (VIOLATED)
min_capacitance	0.00 (MET)

```
fc_shell> report_congestion
*****
Report : congestion
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Wed Feb 25 08:44:46 2026
*****
```

Layer	overflow		# GRCs has	
Name	total	max	overflow (%)	max overflow
Both Dirs	658	2	655 (0.15%)	3
H routing	657	2	654 (0.29%)	3
V routing	1	1	1 (0.00%)	1

```
*****
Report : global timing
    -format { narrow }
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Thu Feb 26 03:36:18 2026
*****
```

Setup violations

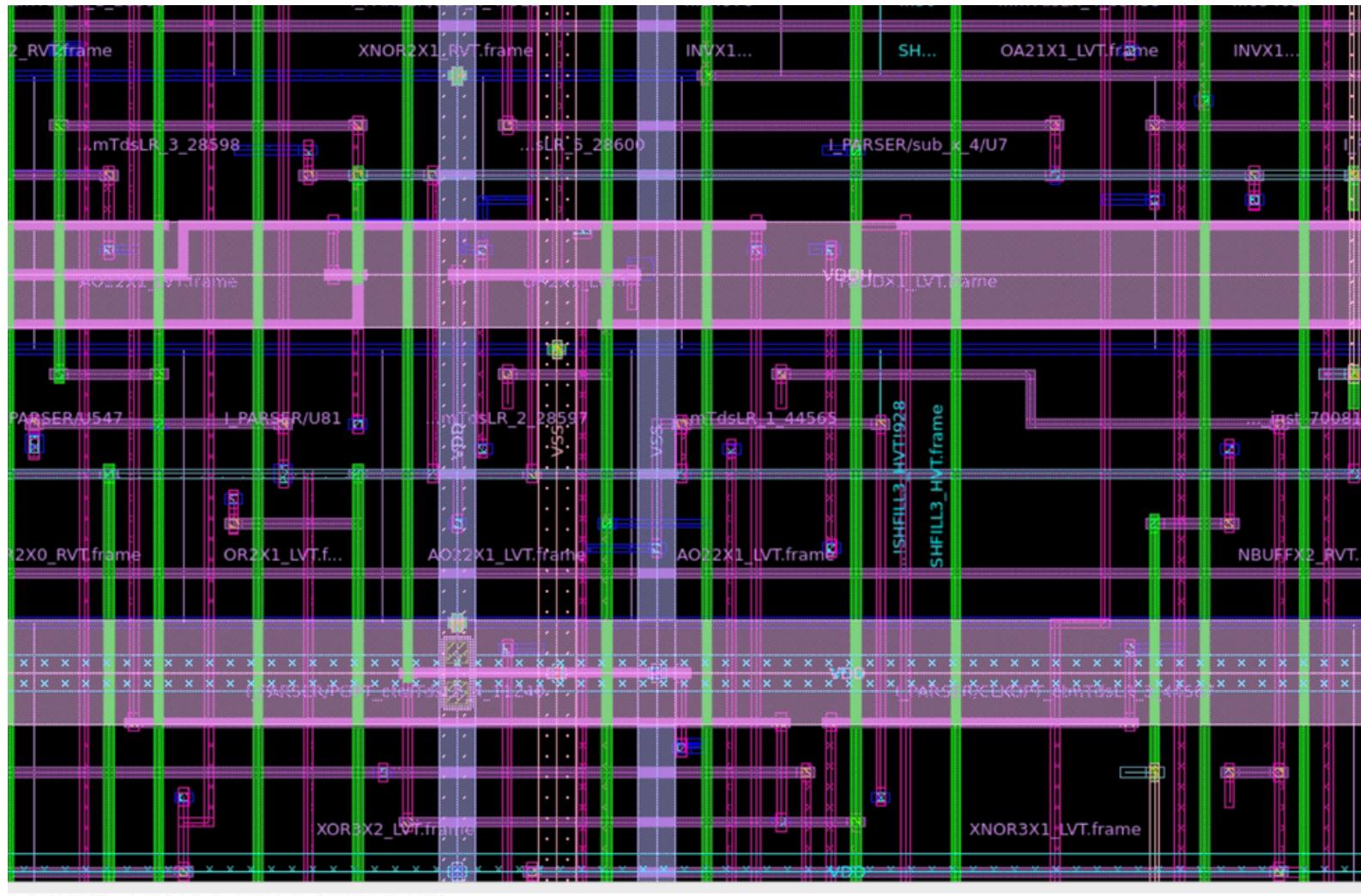
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-2.47	-2.47	0.00	0.00	0.00
TNS	-1275.47	-1275.47	0.00	0.00	0.00
NUM	1669	1669	0	0	0

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.44	-0.44	0.00	0.00	0.00
TNS	-194.95	-194.95	0.00	0.00	0.00
NUM	4319	4319	0	0	0

Routing

Routed net



1. Multi-Scenario Setup

- Dedicated Route and RouteOpt scenarios configured
- Propagated clock enabled after CTS
- Multi-corner timing analysis activated
- Setup & Hold analyzed simultaneously
- Crosstalk-aware timing analysis enabled
- In-design parasitic estimation using report_parasitic

2. Global & Detail Routing

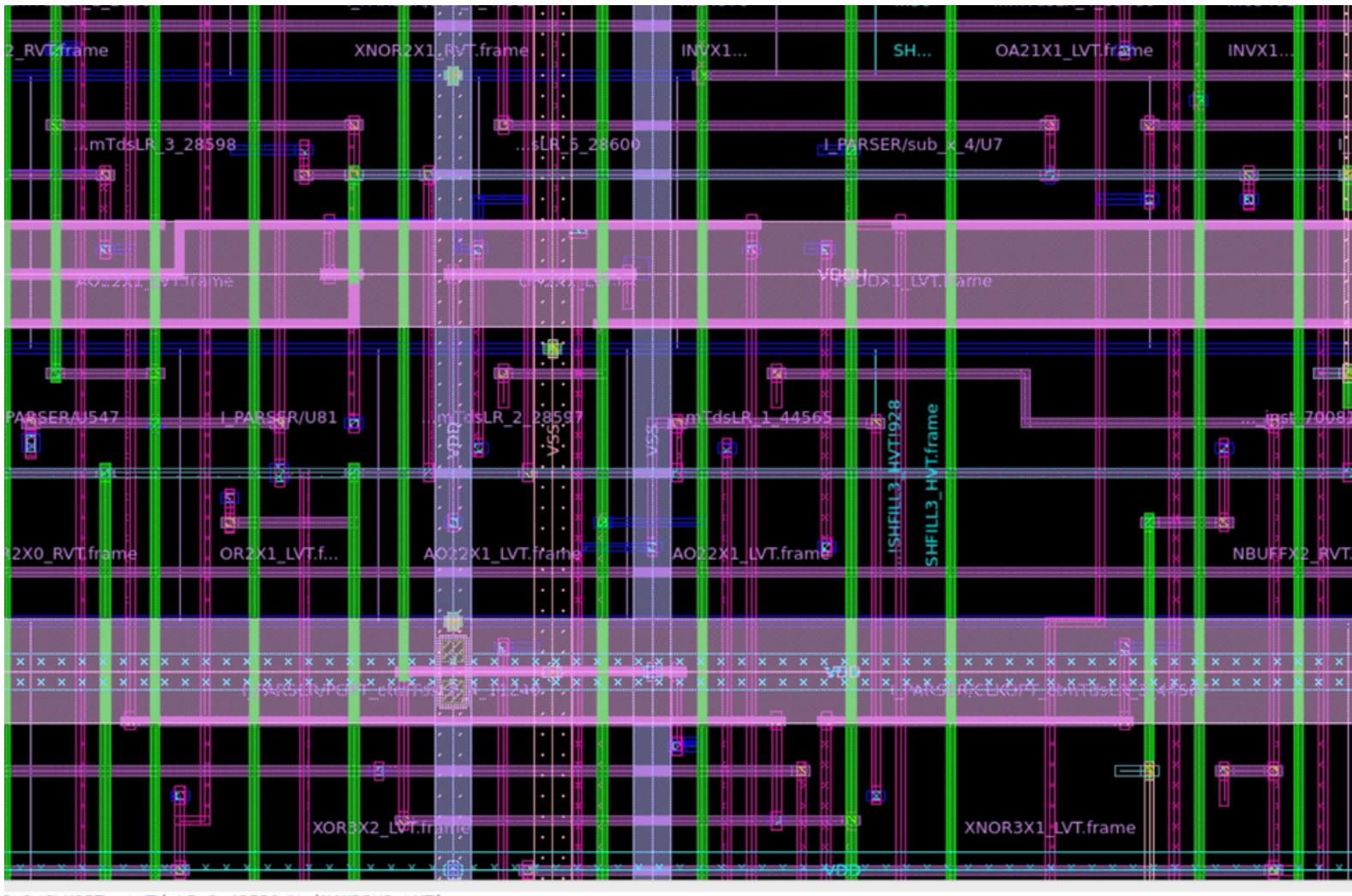
- **route_auto** flow execution (global → track → detail)
- Full routing layers utilized: **M1–M9**
- Timing-driven routing enabled
- Crosstalk-driven routing enabled
- High routing effort level applied
- DRC-aware routing strategy
- Congestion-aware routing refinement

3. Clock Routing Strategy

- Dedicated clock routing layers: **M5–M8**
- Custom NDR applied (2w2s style)
- Increased metal width for clock nets
- Increased spacing for clock nets (especially upper metals)
- Higher spacing weight on **M5–M8**
- Clock nets protected from aggressive optimization
- Reduced coupling noise and improved clock stability

Routing

Routed net



4. Post-Route Optimization (RouteOpt)

- **route_opt** flow execution
 - High-effort hold fixing enabled
 - Simultaneous setup & hold optimization
 - SI-aware delay recovery
 - Clock latency re-computed after routing
 - Congestion-aware cell refinement
 - Scan chain reordering support
 - Incremental routing optimization
 - Timing re-validation after parasitic update

5. RC & Timing Validation

- Post-route parasitic estimation using **report_parasitic**
 - Timing analysis with extracted wire RC
 - Setup degradation analyzed after routing
 - Hold improvement monitored due to the added wire delay
 - Slack comparison pre-route vs post-route

6. Reliability & Implementation Controls

- Antenna-aware routing enabled
- Automatic antenna diode insertion
- Power-aware route optimization enabled
- Tie cell constraints maintained
- Automatic PG reconnection after optimization
- DRC/LVS clean check before signoff handoff

Routing

```
fc_shell> report_global_timing
Information: Timer using 'CRPR'. \(TIM-050\)
*****
Report : global timing
  -format { narrow }
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Wed Feb 25 19:26:33 2026
*****  
  
Setup violations
-----
      Total  reg->reg  in->reg  reg->out  in->out
-----
WNS     -1.46    -1.46     0.00     0.00     0.00
TNS    -290.18   -290.18     0.00     0.00     0.00
NUM       358      358      0        0        0
-----  
  
Hold violations
-----
      Total  reg->reg  in->reg  reg->out  in->out
-----
WNS     -0.03    -0.02    -0.03     0.00     0.00
TNS     -0.22    -0.17    -0.04     0.00     0.00
NUM       18       16       2        0        0
-----
```

```
report_utilization -config util_config
*****
Report : report_utilization
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Wed Feb 25 19:10:05 2026
*****
Utilization Ratio: 0.7678
Utilization options:
  - Area calculation based on: core_area of block ORCA_TOP
  - Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area: 586645.6781
Total Capacity Area: 254043.9686
Total Area of cells: 195064.9233
Area of excluded objects:
  - hard_macros : 264884.2695
  - macro_keepouts : 67717.4400
  - soft_macros : 0.0000
  - io_cells : 0.0000
  - hard_blockages : 0.0000
Total Area of excluded objects: 332601.7095
Ratio of excluded objects: 0.5670
0.7678
```

Routing

Report_parasitics

```
*****
Report : parasitics
    -late
    -rise
Module : ORCA_TOP
Mode   : test
Corner : ss0p75v125c_cmax
Scenario: test_ss0p75v125c_cmax
Version: V-2023.12-SP4
Date   : Wed Feb 25 20:21:29 2026
*****
Corner : ss0p75v125c_cmax

cap units: 1.00fF  res units: 1.00MOhm  time units: 1.00ns

Current delay calculation style: auto
Current min Elmore tau: 0.00s
Current min Arnoldi tau: 2.00ps

Total nets: 58144  RC networks: 58144 (100.00%)

Grand total early parasitic network R: 2.581700  C: 119374.891088
Grand total early lumped parasitic C: 119374.891064
Grand total late parasitic network R: 2.581700  C: 119374.891088
Grand total late lumped parasitic C: 119374.891064

Average pins per network: 3.73
Average caps per network: 19.05
Average xCaps per network: 16.08
Average resistors per network: 18.05
Cap/pin ratio: 5.11
```

check_legality

```
=====
2D Rule Check Legality Report =====
          Violating Cells
Legality Rules      Moveable AppFixed UserFixed Total
-----
overlap           0     0     0     0
spacing_rule       0     0     0     0
cell_on_site       0     0     0     0
legal_orient       0     0     0     0
va_bound           0     0     0     0
pg_drc             0     0     0     0
-----
Total Violations  0     0     0     0
=====

Information: Dynamic Rule Ordering (DRO): true
```

check_mv_design

```
*****
Report : check_mv_design
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Wed Feb 25 22:35:36 2026
*****
```

----- Summary -----

Information: Total 0 error(s) and 0 warning(s) from check_mv_design. [\(MV-082\)](#)

Routing

report_constraints

```
report_constraints
*****
Report : constraint
Design : ORCA_TOP
Version: V-2023.12-SP4
Date   : Wed Feb 25 22:42:46 2026
*****
Constraint          Cost
-----
min_delay/hold      0.62  (VIOLATED)
max_delay/setup     0.00  (MET)
max_transition      104.91 (VIOLATED)
max_capacitance    1089.75 (VIOLATED)
min_capacitance    0.00  (MET)
```

check_lvs

```
Total number of input nets is 57516.
Total number of short violations is 20.
Total number of open nets is 3.
Open nets are VDD VDDH VSS
Total number of floating route violations is 20.
Elapsed = 0:00:37, CPU = 0:00:36
```

```
fc_shell> check_pg_missing_vias
Check net VDD vias...
Number of missing vias on VIA1 layer: 1
Total number of missing vias: 1
Checking net VDD vias took 1 seconds.
Check net VDDH vias...
Number of missing vias on VIA5 layer: 24
Total number of missing vias: 24
Checking net VDDH vias took 1 seconds.
Check net VSS vias...
Number of missing vias: 0
Checking net VSS vias took 2 seconds.
Overall runtime: 5 seconds.
```

check_routes

Verify Summary:

```
Total number of nets = 57332, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
                                         0 ports without pins of 0 cells connected to 0 nets
                                         0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 8306
Total number of antenna violations = no antenna rules defined
Information: Routes in non-preferred voltage areas = 256 (ZRT-559)
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked
```

Summary

Design Overview

- 32-bit RISC-V processor core
 - ~53K standard cells
 - 40 hard macros
 - 2 voltage domains (VDD / VDDH)
 - 9 metal layers
 - 75% core utilization

Implementation Highlights

- Multi-voltage **floorplanning** with dedicated voltage areas
- Hierarchical power mesh (M6–M9) with macro power rings
- Congestion-aware and timing-driven placement (RDE enabled)
- Skew-targeted CTS (100ps target) with NDR-protected clock routing
- SI-aware routing and post-route optimization
- In-design parasitic estimation using **report_parasitics**
- **~0.9ns** setup recovery from Post-CTS to Post-Route

Observations

- Setup degradation observed after CTS due to propagated clock latency
- Partial timing recovery achieved during RouteOpt
- Routing congestion concentrated around macro channels
- DRC/LVS is not fully clean, **require** additional ECO iterations

Learning Outcomes

- Developed insight into timing–congestion–power trade-offs and how implementation decisions impact timing convergence.
- Practical understanding of timing evolution across PD stages
- Impact of utilization and macro placement on congestion
- Multi-voltage power planning strategy implementation
- Clock tree design and optimization trade-offs
- Importance of iterative refinement for signoff-quality design

THANK YOU

Reference:

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<https://github.com/abdelazeem201>