ELEC 4320 Final Project Proposal: Enhanced Real-Time Stereo Depth Estimation with Pseudo-Color and Ranging

1. Introduction and Project Goal

This project proposes the design and implementation of an advanced real-time stereo vision system on the Basys3 FPGA platform, utilizing dual OV7670 cameras for depth estimation. The core goal is to significantly **enhance the algorithmic robustness, visualization quality, and application features** of a open-source depth map project (https://github.com/Archfx/FPGA_depthMap), ensuring the design meets the originality and complexity requirements for the course.

The system will transition from a basic black-and-white depth map display to a high-utility ranging system with modern visualization.

2. Proposed Design Enhancements (Innovation & Complexity)

The existing baseline project typically uses the resource-efficient but low-robustness **Sum of Absolute Differences (SAD)** algorithm. To increase technical difficulty and algorithmic quality, the following core modules will be designed and integrated in Verilog:

Feature	**Baseline Project (SAD/Gray scale)**	**Proposed Enhancement**	**Technical Difficulty & Project Merit**
Stereo Matching Core	Sum of Absolute Differences (SAD)	**Census Transform & Hamming Distance**	**High.** Requires designing a register-based windowing module (3x3 or 5x5) and a fully pipelined Hamming Weight/Popcount circuit. This provides robust matching against brightness variations, a key weakness of the baseline.
Image Output	Grayscale Depth Map (0-255)	**Pseudo-Color Visualization (Heatmap)**	**Medium.** Requires a small Read-Only Memory (ROM) or Look-Up Table (LUT) to map the 8-bit disparity value to 12-bit RGB color codes (e.g., Red=Near, Blue=Far). This vastly improves visual interpretation.
Application Layer	Passive Display	**Real-Time Digital**	**Medium.** Implements a disparity-to-distance conversion ($Z = fB/d$) and a Binary-to-BCD

		Ranging	module to display the distance (in cm) of the object at the center of the frame onto the **Basys3 4-digit 7-segment display**.
Image Quality	Raw Disparity Output	**3x3 Median Filtering (Post processing)**	**High.** Requires a 3x3 sliding window (using BRAM as line buffers) and a parallel sorting network to calculate the median, effectively eliminating "salt and pepper" noise from the depth map.

3. Core Module Elaboration and I/O Utilization

The design will be divided into the following key modules, fully satisfying the functional requirements:

Module Name	**Functionality**	**On-Chip Memory / Sequential Logic**	**I/O Utilization**
Camera / VGA Drivers	Interfaces dual OV7670 to receive data and outputs to a VGA monitor.	Line Buffers (BRAM access)	**Output:** VGA Signal (Hsync, Vsync, RGB)
Census Matching Core	Generates bit strings and computes Hamming Distance for disparity.	Registers for 3x3/5x5 windowing.	N/A
Distance Ranging FSM	Implements the **Finite State Machine (FSM)** to control the depth processing pipeline, calculate distance, and manage the multi-stage 7-segment display refresh.	Control Registers	**Input:** Center Button (BTN_C) to freeze / unfreeze the distance.
Output Module	Maps disparity to pseudo-color and drives the 7-segment display.	ROM/LUT for Color Mapping.	**Output:** 7-Segment Display, LEDs for status.
User Input	Selects operating mode (Raw Disparity, Filtered Disparity, or Ranging).	Registers for mode selection.	**Input:** DIP Switches (SW[1:0]) for mode select.

4. Technical Difficulty Evaluation

1. **Algorithmic Complexity:** The shift from SAD (simple subtraction/addition) to **Census Transform + Hamming Distance** significantly increases the logic complexity, requiring a deeper understanding of image processing and highly optimized bit-manipulation logic in Verilog.
2. **Pipelining and Timing:** The Basys3's Artix-7 FPGA is resource-constrained. Achieving real-time frame rates (e.g., 30 FPS) with the complex Census and optional Median Filter modules will necessitate **heavy pipelining and optimization** to prevent timing violations, which is a major design challenge.

3. **Resource Management:** Efficient management of the limited on-chip **BRAM** is critical for the necessary line buffers and ROMs, requiring careful memory partitioning and addressing logic.

4. **I/O Integration:** The project utilizes four distinct I/O components (Dual OV7670, VGA, Switches/Buttons, 7-Segment Display), demonstrating high interaction and full utilization of the Basys3 peripherals.

5. Project Timeline

Task	Oct. 31 - Nov. 15	Nov. 16 - Nov. 30	Dec. 1 - Dec. 15	Dec. 16/17
Core Modules	Camera/VGA Drivers Adaptation & Test.	Census Transform Core Design & Simulation.	Median Filter / Post-processing integration.	Final Debugging & Demo Prep.
Feature Modules	Pseudo-Color LUT Design. Binary-to-BCD/7-Seg Driver Design.	FSM Integration & Control Logic (Mode switching).	Ranging Formula Implementation & Calibration.	Presentation & Demo.
Documentation	Proposal Submission.	Module Documentation (Schematics, I/O).	Final Report Compilation and Citation.	Final Submission.