

ELE 734 Prelab 4

Q1. Full Adder:

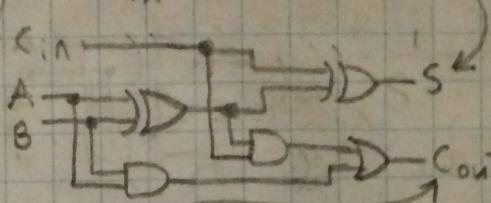
C_{in}	A	B	$C_{out} + S$
0	0	0	00
0	0	1	01
0	1	0	01
0	1	1	10
1	0	0	01
1	0	1	10
1	1	0	10
1	1	1	11

$$S = \overline{C_{in}}\overline{A}\overline{B} + \overline{C_{in}}A\overline{B} + C_{in}\overline{A}\overline{B} + C_{in}AB$$

$$S = \overline{C_{in}}(\overline{A}B + A\overline{B}) + C_{in}(\overline{A}\overline{B} + AB)$$

$$S = C_{in}(A \oplus B) + C_{in}(\overline{A} \oplus \overline{B})$$

$$S = C_{in} \oplus (A \oplus B)$$



$$C_{out} = \overline{C_{in}}AB + C_{in}\overline{A}B + C_{in}A\overline{B} + C_{in}AB$$

$$C_{out} = \overline{C_{in}}AB + C_{in}(\overline{A}B + A\overline{B} + AB)$$

$$C_{out} = \overline{C_{in}}AB + C_{in}AB + C_{in}(\overline{A}\overline{B} + A\overline{B})$$

$$C_{out} = (\overline{C_{in}} + C_{in})AB + C_{in}(A \oplus B)$$

$$C_{out} = AB + C_{in}(A \oplus B)$$

XOR Gate with minimum NAND gates

X	Y	$X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

$$X \oplus Y = \overline{X}Y + X\overline{Y}$$

$$(\overline{X} + \overline{Y})(X + Y)$$

$$X \oplus Y = (0) + \overline{X}Y + X\overline{Y} + (0)$$

$$\overline{X}X$$

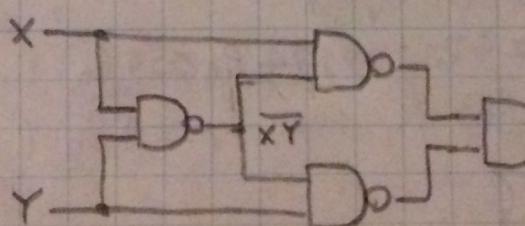
$$X \oplus Y = (\overline{Y}Y) + \overline{X}Y + X\overline{Y} + (X\overline{X})$$

$$X \oplus Y = Y(\overline{X} + \overline{Y}) + X(\overline{X} + \overline{Y})$$

$$= (Y \cdot \overline{(XY)}) + (X \cdot \overline{(XY)})$$

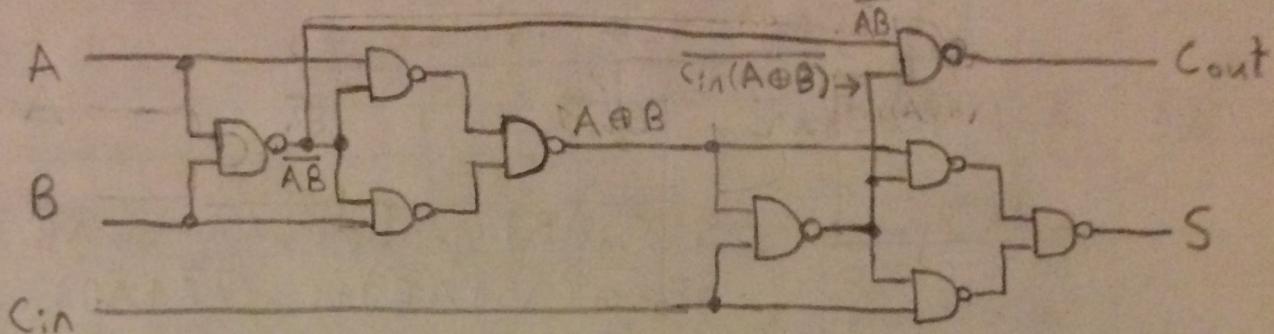
$$= \overline{[X \cdot \overline{(XY)} + Y \cdot \overline{(XY)}]}$$

$$X \oplus Y = \overline{[X \cdot \overline{(XY)}]} \cdot \overline{[Y \cdot \overline{(XY)}]}$$



$$X \oplus Y = \overline{\overline{X} \cdot \overline{Y}} \cdot \overline{X \cdot \overline{Y}}$$

$$C_{out} = \overline{[AB + C_{in}(A \oplus B)]} = \overline{\overline{AB}} \cdot \overline{C_{in}(A \oplus B)}$$



Q2. Student ID = 500822828 $\rightarrow C_{load} = 50FF + 285F = 785F$

NMOS & PMOS Unit Transistor Capacitance & Resistance

$$C \approx C_g = C_{ox} \cdot W \cdot L = \frac{\epsilon_{ox}}{t_{ox}} WL$$

from Lab 2, $t_{ox} = 4.08\text{nm}$, $\epsilon_{ox} = 3.9\epsilon_0$, $\epsilon_0 = 8.854 \cdot 10^{12} \frac{\text{F}}{\text{m}}$

$$C \approx \frac{\epsilon_{ox}}{t_{ox}} WL = \frac{3.9\epsilon_0}{t_{ox}} \cdot WL = \frac{3.9(8.854 \cdot 10^{12} \frac{\text{F}}{\text{m}})}{(4.08\text{nm})} \cdot (1\mu\text{m})(180\text{nm})$$

$$C \approx 1.523408824 \cdot 10^{-15} \text{F} \approx 1.523f\text{F}$$

for unit NMOS:

$$R_n = \frac{P \cdot L}{A} = \frac{L}{\sigma A}$$

$$\sigma = ne\mu_n$$

$$R_n = \frac{L}{(ne\mu_n)A}$$

$$\frac{R_p}{R_n} = \frac{\left[\frac{L}{(ne\mu_p)A} \right]}{\left[\frac{L}{(ne\mu_n)A} \right]} = \frac{L}{ne\mu_p A} \cdot \frac{ne\mu_n A}{L} = \frac{\mu_n}{\mu_p}$$

$$R_p = \frac{L}{(ne\mu_p)A}$$

$$\sigma = pe\mu_p \approx ne\mu_p$$

$$\frac{R_p}{R_n} = \frac{\mu_n}{\mu_p} \rightarrow R_p = \frac{\mu_n}{\mu_p} R_n \quad \text{from Lab 2, } \mu_n = 459 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$$

$$R_p = \frac{\left(459 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right)}{\left(109 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right)} R_n$$

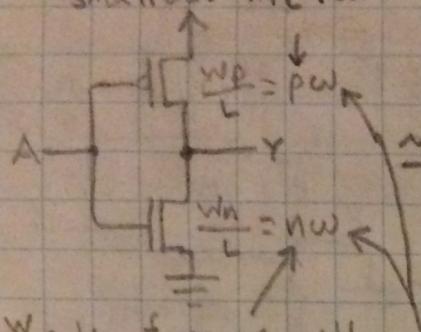
$$\mu_p = 109 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$$

$$R_p \approx 4.21109174 R_n \approx 4 R_n$$

Let $R_n = R$, then $R_p \approx 4 R_n$

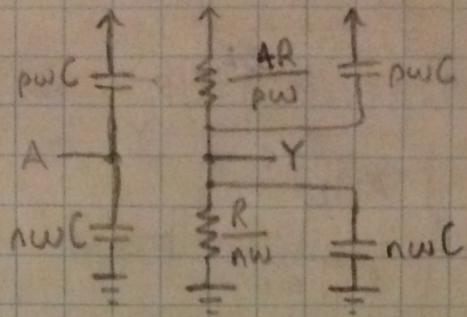
Unit Inverter Gate

smallest W/L ratio of PMOS with $L = 180\text{nm}$



smallest $\frac{W}{L}$ ratio of NMOS with
 $L = 180\text{nm}$

circuit size



$$\frac{4R}{pw} = \frac{R}{nw}$$

$$\frac{4}{1} = \frac{p}{n}$$

$$\frac{4}{1} \approx \frac{p}{n}$$

$$C_{in} = pwC + nwC$$

$$C_{in} = (p+n)wC$$

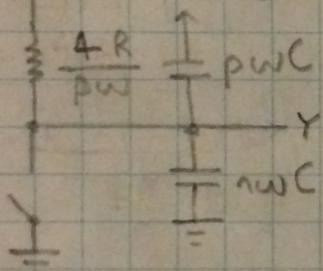
if $w=1$ for smallest size (unit) inverter

$$C_{in} = (p+n)(1)C$$

$$C_{in} \approx (4+1)C$$

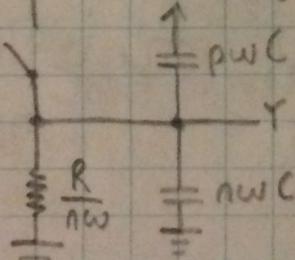
$$C_{in} \approx 5C$$

when $Y=1$



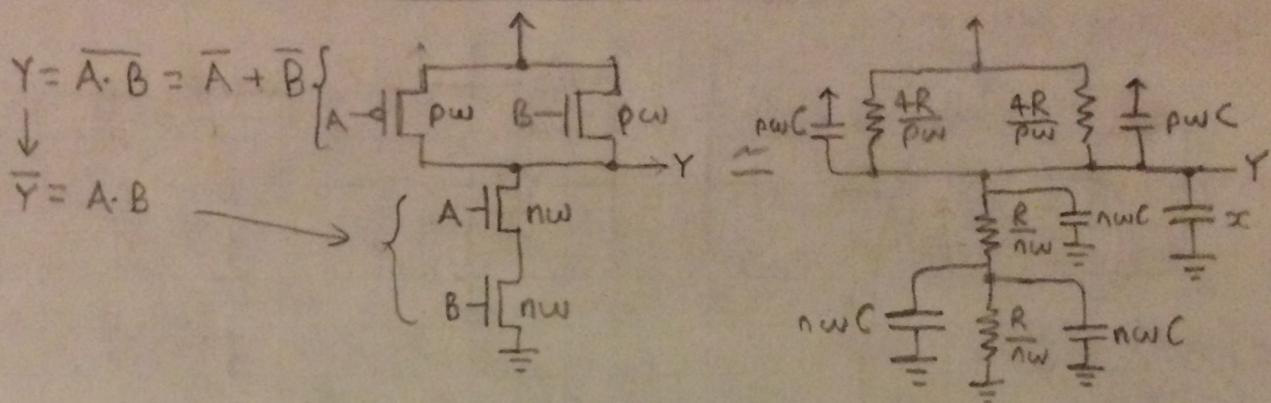
$$\begin{aligned} t_{pd़r} &= \frac{4R}{pw} (pwC + nwC) \\ &= R(C + \frac{n}{p}C) \\ &= 4R(C + \frac{1}{4}C) = 4R \cdot \frac{5}{4}C = 5RC \end{aligned}$$

when $Y=0$



$$\begin{aligned} t_{pdf} &= \frac{R}{nw} (pwC + nwC) = \frac{R}{(1)w} ((4)wC + (1)wC) \\ &= \frac{R}{w} 5wC = 5RC = t_{pd़r} \end{aligned}$$

NAND2 Gate Delay



in worst case delay, NAND gate must deliver the same current as inverter. \therefore resistance of NAND must be the same as the inverter of the same circuit size (w).

when Y rises to 1, $I_{NAND} = I_{INV}$

$$\frac{V_{DD}-V_Y}{\left(\frac{4R}{(4)w}\right)} = \frac{V_{DD}-V_Y}{\left(\frac{4R}{pw}\right)}$$

$$\frac{1}{\left(\frac{1}{4}\right)} = \frac{1}{\left(\frac{1}{p}\right)}$$

$$4 = p$$

when Y falls to 0,

$$\frac{V_Y-0V}{\left(\frac{R}{(1)w}\right)} = \frac{V_Y-0V}{\left(\frac{R}{nw} + \frac{R}{nw}\right)}$$

$$\frac{1}{\left(\frac{R}{w}\right)} = \frac{1}{\left(\frac{2R}{nw}\right)}$$

$$\frac{w}{R} = \frac{n w}{2R}$$

$$1 = \frac{n}{2}$$

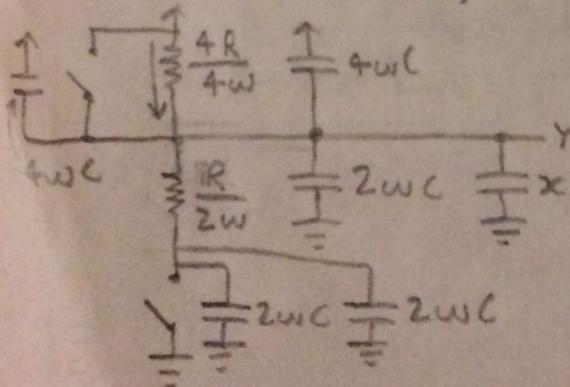
$$2 = n$$

for NAND gate $\rightarrow C_{in} = pwC + nwC = (4)wC + (2)wC = 6wC$

$$g = \frac{\text{NAND input cap}}{\text{INV input cap}} = \frac{6wC}{5wC} = \frac{6}{5}$$

$$h = \frac{\text{NAND load cap}}{\text{NAND input cap}} = \frac{x}{6wC}$$

when Y rises to 1,



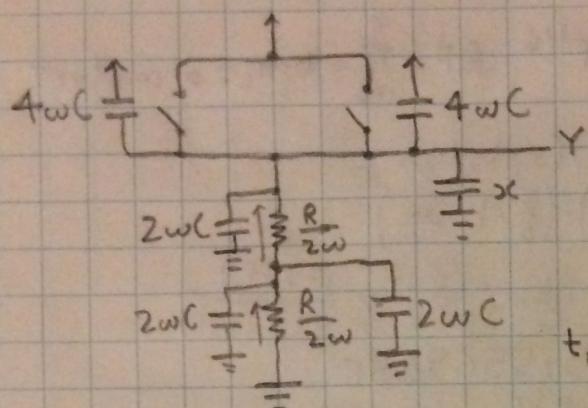
$$t_{pdR} = \frac{4R}{4w} (4wC + 4wC + 2wC + x + 2wC + 2wC)$$

$$t_{pdR} = \frac{R}{w} (14wC + x)$$

$$t_{pdR} = 14RC + \frac{Rx}{w}$$

(4)

when Y falls to 0 for NAND,



$$t_{pd\$} = \frac{R}{2w} (2wL + 2wC + 2wC + 4wC + 4wC + x)$$

$$+ \frac{R}{2w} (2wC + 4wC + 4wC + x)$$

$$= \frac{R}{2w} (14wC + x) + \frac{R}{2w} (10wC + x)$$

$$t_{pd\$} = \frac{R}{2w} (24wC + 2x) = 12RC + \frac{Rx}{w}$$

$$t_p = \frac{t_{pd\$} + t_{pd\$}}{2} = \frac{(12RC + \frac{Rx}{w}) + (14RC + \frac{Rx}{w})}{2}$$

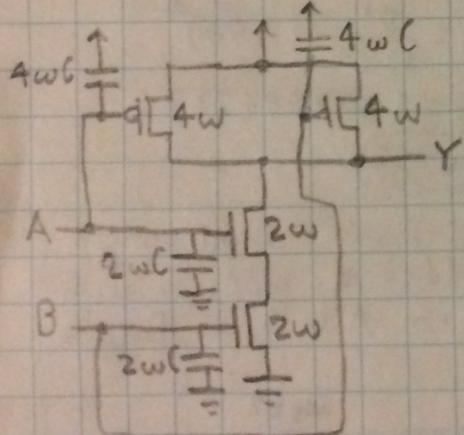
$$t_p = \frac{26RC + \frac{2Rx}{w}}{2} = 13RC + \frac{Rx}{w}$$

$$\text{Normalized Delay: } d = \frac{\text{delay for NAND}}{\text{delay for unloaded INV}} = \frac{t_p}{5RC} = \frac{13RC + \frac{Rx}{w}}{5RC}$$

$$d = \frac{13}{5} + \frac{x}{5wC} = \frac{13}{5} + \frac{6}{5} \cdot \frac{x}{6wC}$$

$$\therefore p = \frac{13}{5}, g = \frac{6}{5}, h = \frac{x}{6wC}$$

Sizing NAND Gates in Full Adder



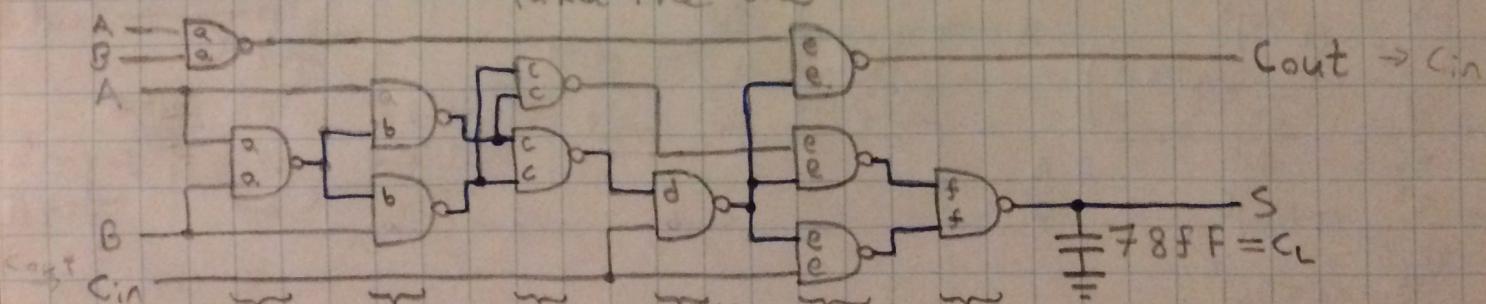
for each input (A, B)

$$C_{in} = 4wC + 2wC$$

$$C_{in} = 6wC$$

$$\frac{C_{in}}{6C} = w$$

Minimize delay on path with longest delay
(aka the one with the most NAND gates)



$$P_1 = \frac{13}{5} \quad P_2 = \frac{13}{5} \quad P_3 = \frac{13}{5} \quad P_4 = \frac{13}{5} \quad P_5 = \frac{13}{5} \quad P_6 = \frac{13}{5}$$

$$g_1 = \frac{6}{5} \quad g_2 = \frac{6}{5} \quad g_3 = \frac{6}{5} \quad g_4 = \frac{6}{5} \quad g_5 = \frac{6}{5} \quad g_6 = \frac{6}{5}$$

$$b_1 = 2 \quad b_2 = 2 \quad b_3 = 1 \quad b_4 = 3 \quad b_5 = 1 \quad b_6 = 1$$

$$h_1 = \frac{b_1}{a} \quad h_2 = \frac{c}{b} \quad h_3 = \frac{d}{c} \quad h_4 = \frac{e}{d} \quad h_5 = \frac{f}{e} \quad h_6 = \frac{c_L}{f}$$

delay of full adder: $d = \sum_{i=1}^6 (p_i + g_i b_i h_i) = \sum_{i=1}^6 p_i + \sum_{i=1}^6 (g_i b_i h_i)$

$\sum_{i=1}^6 (g_i b_i h_i)$ can be minimized by $g_i b_i h_i = F^{1/6}$ if $F = \prod_{i=1}^6 g_i b_i h_i = \text{a constant}$

$$F = (g_1 b_1 h_1)(g_2 b_2 h_2)(g_3 b_3 h_3)(g_4 b_4 h_4)(g_5 b_5 h_5)(g_6 b_6 h_6)$$

$$= \left(\frac{6}{5} \cdot 2 \cdot \frac{b}{a}\right) \left(\frac{6}{5} \cdot 2 \cdot \frac{c}{b}\right) \cdot \left(\frac{6}{5} \cdot 1 \cdot \frac{d}{c}\right) \cdot \left(\frac{6}{5} \cdot 3 \cdot \frac{e}{d}\right) \cdot \left(\frac{6}{5} \cdot 1 \cdot \frac{f}{e}\right) \cdot \left(\frac{6}{5} \cdot 1 \cdot \frac{g}{f}\right)$$

$$F = \left(\frac{6}{5}\right)^6 \cdot 2 \cdot 2 \cdot 3 \cdot \frac{c_L}{a} = \left(\frac{6}{5}\right)^6 \cdot 2 \cdot 2 \cdot 3 \cdot \frac{c_L}{(6C)} = \left(\frac{6}{5}\right)^6 \cdot 2 \cdot \frac{c_L}{C} = \left(\frac{6}{5}\right)^6 \cdot 2 \cdot \frac{(78fF)}{(1.5235f)}$$

$$F \approx 305.7705172 = \text{a constant!} \rightarrow F^{1/6} \approx 2.595569136$$

$\therefore \sum_{i=1}^6 p_i b_i h_i$ is minimized when $g_i b_i h_i = F^{1/6}$

$$g_1 b_1 h_1 = F^{1/6}$$

$$\frac{6}{5} \cdot 2 \cdot \frac{b}{a} = F^{1/6}$$

$$b = \frac{5}{12} a F^{1/6}$$

$$b = \frac{5}{12} (6C) F^{1/6}$$

$$b = \frac{5}{2} c F^{1/6}$$

$$w_2 = \frac{b}{6C} = \frac{5}{2} c F^{1/6}$$

$$w_2 = \frac{5}{12} F^{1/6}$$

$$w_2 \approx 1.08148714$$

$$w_2 \approx 1$$

$$g_2 b_2 h_2 = F^{1/6}$$

$$\frac{6}{5} \cdot 2 \cdot \frac{c}{b} = F^{1/6}$$

$$c = \frac{5}{12} b F^{1/6}$$

$$c = \frac{5}{12} (\frac{5}{12} c F^{1/6}) F^{1/6}$$

$$c = \frac{25}{24} c (F^{1/6})^2$$

$$w_3 = \frac{c}{6C} = \frac{\frac{25}{24} c (F^{1/6})^2}{6C}$$

$$w_3 = \frac{25}{144} (F^{1/6})^2$$

$$w_3 = \frac{25}{144} (2.596)^2$$

$$w_3 \approx 1.169614434$$

$$w_3 \approx 1$$

$$g_3 b_3 h_3 = F^{1/6}$$

$$\frac{6}{5} \cdot 1 \cdot \frac{d}{c} = F^{1/6}$$

$$d = \frac{5}{6} c F^{1/6}$$

$$d = \frac{5}{6} (\frac{25}{24} c (F^{1/6})^2) F^{1/6}$$

$$d = \frac{125}{144} c (F^{1/6})^3$$

$$w_4 = \frac{d}{6C} = \frac{(\frac{125}{144} c (F^{1/6})^3)}{6C}$$

$$w_4 = \frac{125}{864} (F^{1/6})^3$$

$$w_4 = \frac{125}{864} (2.596)^3$$

$$w_4 \approx 2.529845938$$

$$w_4 \approx 2 \text{ or } 3$$

$$g_4 b_4 h_4 = F^{1/6}$$

$$\frac{6}{5} \cdot 3 \cdot \frac{e}{d} = F^{1/6}$$

$$e = \frac{5}{18} d F^{1/6}$$

$$e = \frac{5}{18} (\frac{125}{144} c (F^{1/6})^3) F^{1/6}$$

$$e = \frac{5^4}{12 \cdot 6^3} c (F^{1/6})^4$$

$$w_5 = \frac{e}{6C} = \frac{(\frac{5^4}{12 \cdot 6^3} c (F^{1/6})^4)}{6C}$$

$$w_5 = \frac{5^4}{12 \cdot 6^4} \cdot (F^{1/6})^4$$

$$w_5 = \frac{5^4}{12 \cdot 6^4} (2.596)^4$$

$$w_5 \approx 1.823997237$$

$$w_5 \approx 2$$

$$g_5 b_5 h_5 = F^{1/6}$$

$$\frac{6}{5} \cdot 1 \cdot \frac{f}{e} = F^{1/6}$$

$$f = \frac{5}{6} e F^{1/6}$$

$$f = \frac{5}{6} (\frac{5^4}{12 \cdot 6^3} c (F^{1/6})^4) F^{1/6}$$

$$f = \frac{5^5}{12 \cdot 6^4} c (F^{1/6})^5$$

$$w_6 = \frac{f}{6C} = \frac{(\frac{5^5}{12 \cdot 6^4} c (F^{1/6})^5)}{6C}$$

$$w_6 = \frac{5^5}{12 \cdot 6^5} (F^{1/6})^5$$

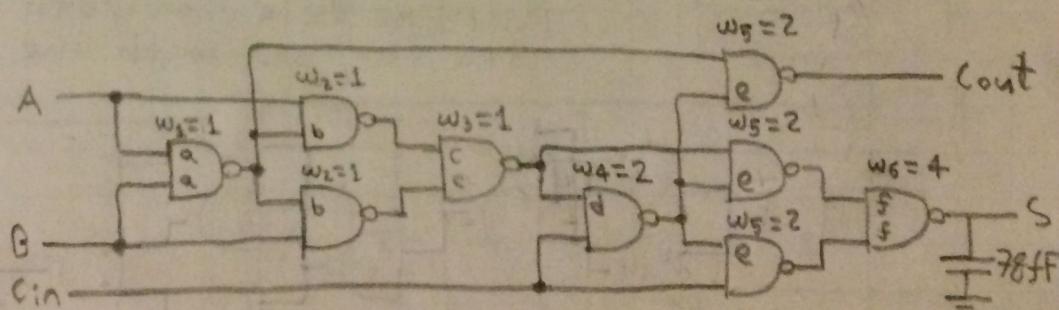
$$w_6 = \frac{5^5}{12 \cdot 6^5} (2.596)^5$$

$$w_6 \approx 3.9452591$$

$$w_6 \approx 4$$

for a ,
 $w_0 = \frac{a}{6C} = \frac{(6C)}{6C}$
 $w_1 = 1$

Use these circuit sizes in 9 NAND gate circuit for full adder to approximate minimum delay from A to S or B to S.



(6)