COE838/EE8221: Systems-on-Chip Design

Course Management Summary (Winter 2022)

1. Introduction

This document provides a summary of the course outline while additional details will be made available at the SoC Design course webpage http://www.ee.ryerson.ca/~courses/coe838/ and D2L. D2L will also be used for posting the labs, project, midterm, and final exam submission and posting marks.

2. Course Objectives

This course will cover the basics of system-on-chip (SoC) design, hardware-software co-specification, co-synthesis, network-on-chip (NoC) systems and system-on-programmable-chip technologies. It provides the advance knowledge required for system-on-chip design and development, multi-core architectures and embedded systems on a chip. Students will also be introduced to the main principles of embedded system-on-chip modeling and design using SystemC. Various SoC soft processor cores such as Nios-II, ARM Cortex-A9, and other CPU IPs will be explored. Various design tools including Altera Quartus II and other tools utilized in the labs and projects. Interconnection structures suitable for SoC design will be studied. On-chip busses (e.g. AMBA, Avalon, IBM Core-connect, etc.) and network-on-chip techniques will be discussed in detail. SystemC is also introduced for SoC modeling and analysis.

3. Text Books and Other Teaching Material

1. M. Wolf, Computer as Components: Principles of Embedded Computing System Design, 3rd or 4th edition Morgan Kaufmann-Elsevier Publishers 2012, 2016 ISBN 978-0-12-388436-7, ISBN 97801280538741.
2. Michael J. Flynn, Wayne Luk, Computer System Design: System on Chip, John Wiley and Sons Inc. 2011, ISBN 978-0-470-64336-5
3. SystemC: From the Ground Up, 2nd Edition, D.C. Black, J Donovan, B. Bunton, A. Keist, Springer 2010, ISBN 978-0-387-69958-5.
4. On-Chip Communication Architectures, System on Chip Interconnect, S. Pascricha and N. Dutt, Morgan Kaufmann-Elsevier Publishers 2008, ISBN 978-0-12-373892-9.
5. Embedded Core Design with FPGAs, Z. Navabi, McGraw-Hill 2007, ISBN 978-0-07-147481-8 ISBN 0-07-147481-1.

Relevant review articles to be identified by the instructor and will be available at the course web or library.

4. Course Evaluation and Marking Scheme

- Labs/Project: **30%**
- Mid-Term Test: **25%**
- Final Exam: **45%**

5. Additional Information

i. Midterm Exams will also cover the corresponding labs to enforce individual lab attempts.
ii. Initial Labs will be mainly organized online/virtual on SoC modeling and design using SystemC and other tools.

6. Instructor

Dr. Gul N. Khan **Professor - Computer Engineering**
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Consultation Times: Wednesday 12:00 to 1:00PM, Virtual (via Zoom) after Lecture or by Appointment
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Lab Instructors/Supervisors: Ms. Sunbal Cheema, e-mail: sunbal.cheema@ryerson.ca
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7. Course Outline and Schedule

- A tentative schedule of Lectures, Labs and project is provided. There may be some changes in the schedule if in-person labs cannot be organized in-person during Feb-March 2022 due to COVID-19 situation.
- Amended schedule will be announced in the class and posted on D2L course website if required.
- For schedule updates, please check the announcement pages of the course website and D2L regularly.

Tentative Weekly Schedule

Weeks	Main Topics - Lectures	Labs/Project Virtual (Jan 2022) Planned: ENG412 (Feb-April 2022)
1	System on Chip (SoC) Introduction Introduction to SystemC	
2	Introduction to SystemC, Using SystemC for SoC Co-specification	**Lab1:** SystemC: Introduction and Tutorial
3	SystemC based SoC Modeling & Analysis Hardware-Software Co-synthesis	**Lab1:** Submission **Lab2a:** SoC Accelerator
4	Accelerators & Embedded System Design Basics of Chips and SoC ICs	**Lab2a:** Demo and Submission **Lab2b:** JPEG Encoder/Decoder SoC Design
5	IC Die Area & Cost, Area and Power NoC (Network-on-Chip)	**Lab2b:** Demo and Submission **Lab 3:** DE1-SoC Tutorial - Creating SoCs
6	***Mid-term Exam (Tentative February 16, 2022)***	*** Course Project Introduction**
Study Week Break	*** Start the Course Project ***	Study Week Break
7	NoC based Interconnection - Regular and Application Specific NoC Topologies.	**Lab3:** Submission **Lab4:** Designing and Interfacing Custom IP
8	System on Programmable Chips SoCs Introduction to HPS/FPGA Systems	**Lab4:** Demo and Submission
9	SoC Interconnection: On-Chip Busses: AMBA, IBM Core-connect, Avalon, etc.	**OpenCL (**CPU-GPU) **Bonus Lab (Optional)**
10	Various Soft and other CPU Cores for SoC Multicore and MPSoC Architecture	**Demo of Project Progress** **Project Interim Report**
11	SoC Verification **Invited Lecture by Dr. M. A. Salem,** **AMD Canada Technical Staff Member**	
12	SoC Verification and UVM (Universal Verification Methodology) **Dr. M. A. Salem**	**Project Demo**
13	SoC Application Case Studies. Catching up and Review	**Project Final Report**

Additional Points to be noted:

I. **All the required course specific written reports including labs/assignments will be assessed not only on their technical/academic merit, but also on communication skills of the author as exhibited through these reports.**
II. **There will be a 5% penalty per day for late submission of labs or project.**
III. **The students must follow and adhere to the senate policy 60 on Student Code of Academic Conduct.**
Available at: http://www.ryerson.ca/senate/policies/pol60.pdf
IV. **In the case of no in-person labs/project, there may be some changes in the labs and lecture contents and schedule.**

Midterm and Final exams are scheduled on Feb. 16, 2022 and in the 2nd half of April 2022 respectively.