

Course Title:	
Course Number:	
Semester/Year (e.g.F2016)	

Instructor:	
--------------------	--

<i>Assignment/Lab Number:</i>	
<i>Assignment/Lab Title:</i>	

<i>Submission Date:</i>	
<i>Due Date:</i>	

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: <http://www.ryerson.ca/senate/current/pol60.pdf>

Lab Report for Lab 3

Contents

1.	Schematic of the NOR2 and NAND2 gates.....	2
2.	Schematic of the testbench for the NOR2 and NAND2 gates.....	4
3.	Delay measurement for unskewed, high-skewed and low skewed NOR2 and NAND2 gates.....	6
a.	NOR2 Gate	6
b.	NAND2 Gate	7
4.	The layout and extracted views of the unskewed NOR2 and NND@ gates	8
a.	NOR2 Gate	8
b.	NAND2 Gate	12
5.	Post-layout simulation comparing delay measurement for unskewed NAND2 and NOR2 gates	16
6.	Summary of Results	17

1. Schematic of the NOR2 and NAND2 gates

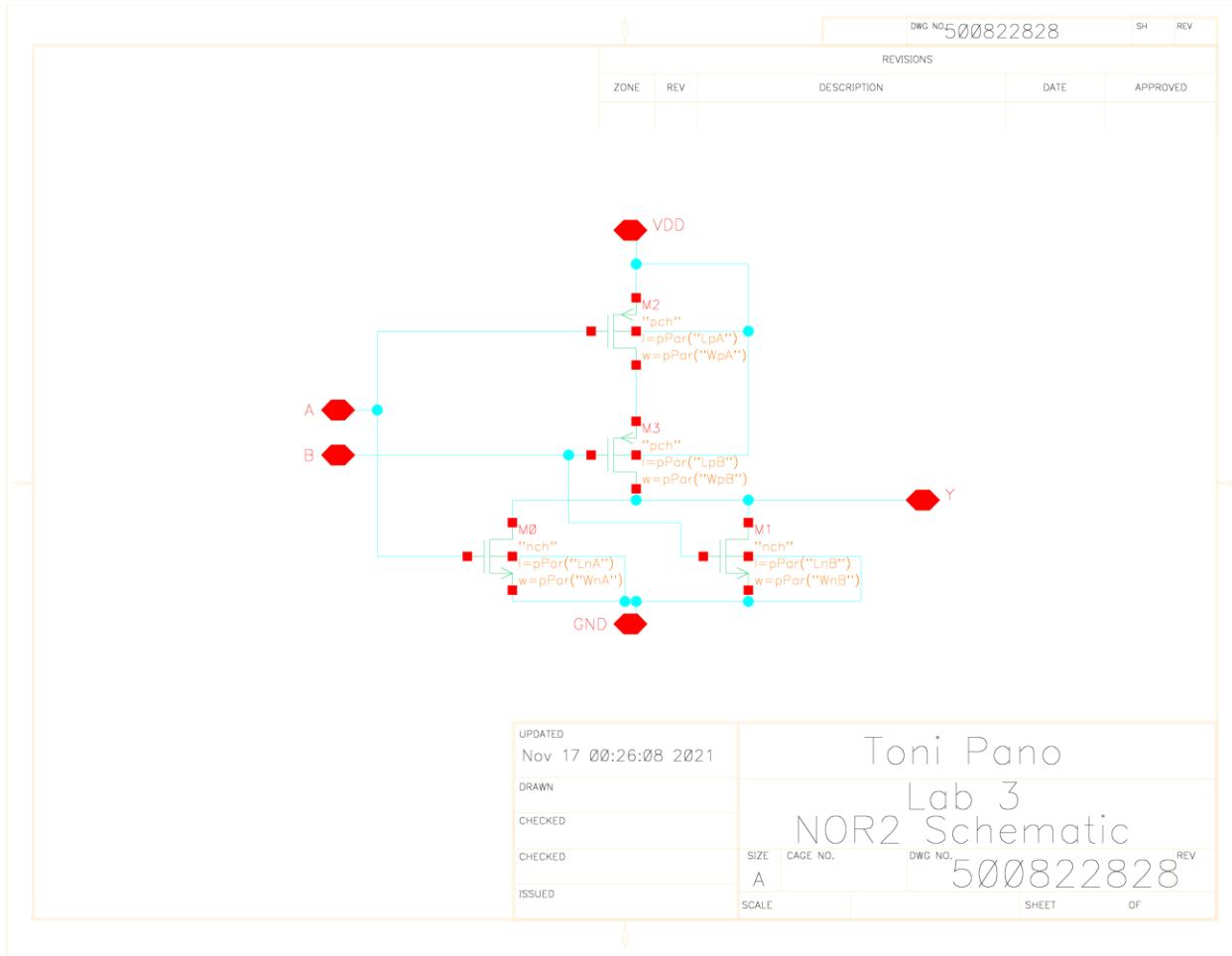


Figure 1.1. Schematic of the NOR2 gate.

Figure 1.2. Schematic of the NAND2 gate.

2. Schematic of the testbench for the NOR2 and NAND2 gates

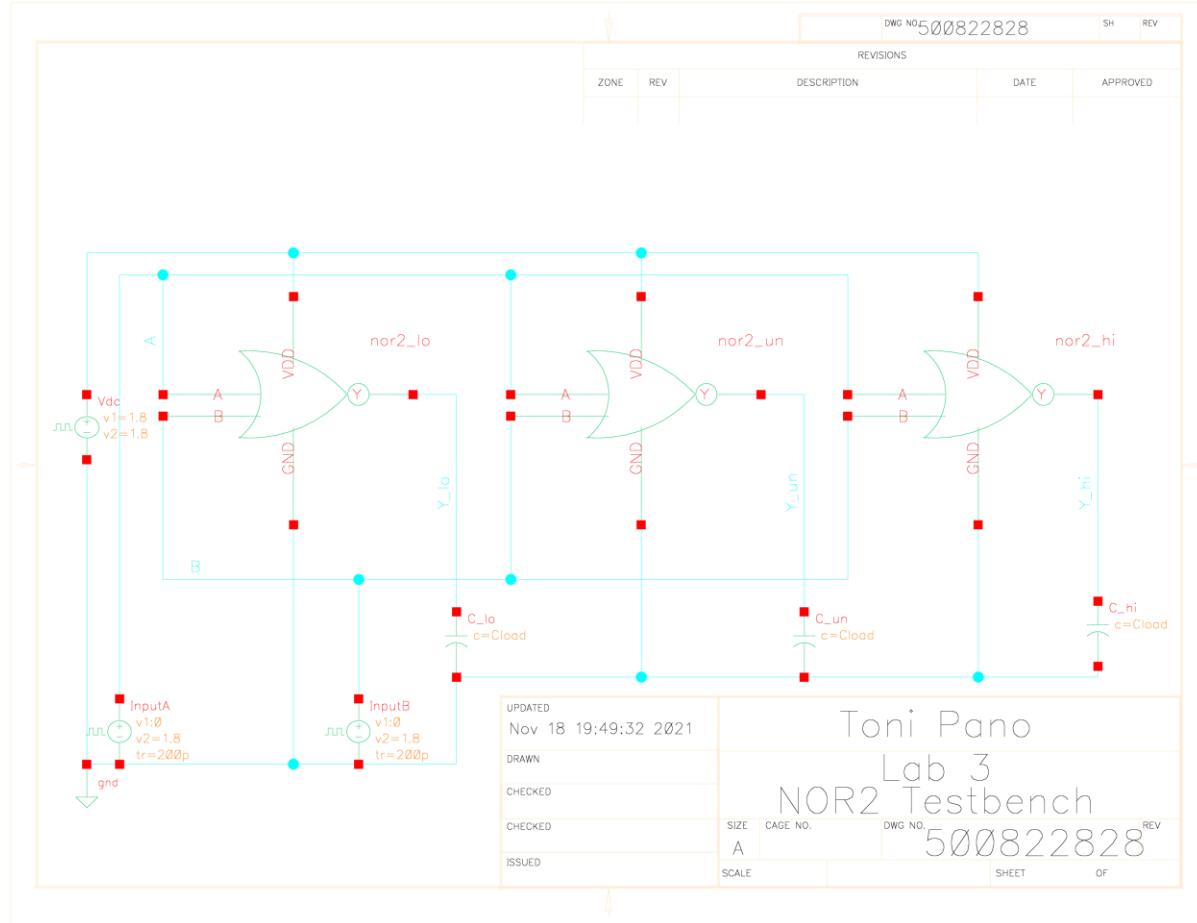


Figure 2.1. Schematic of the testbench for the low skewed (left), unskewed (middle), and high-skewed (right) NOR2 gates.

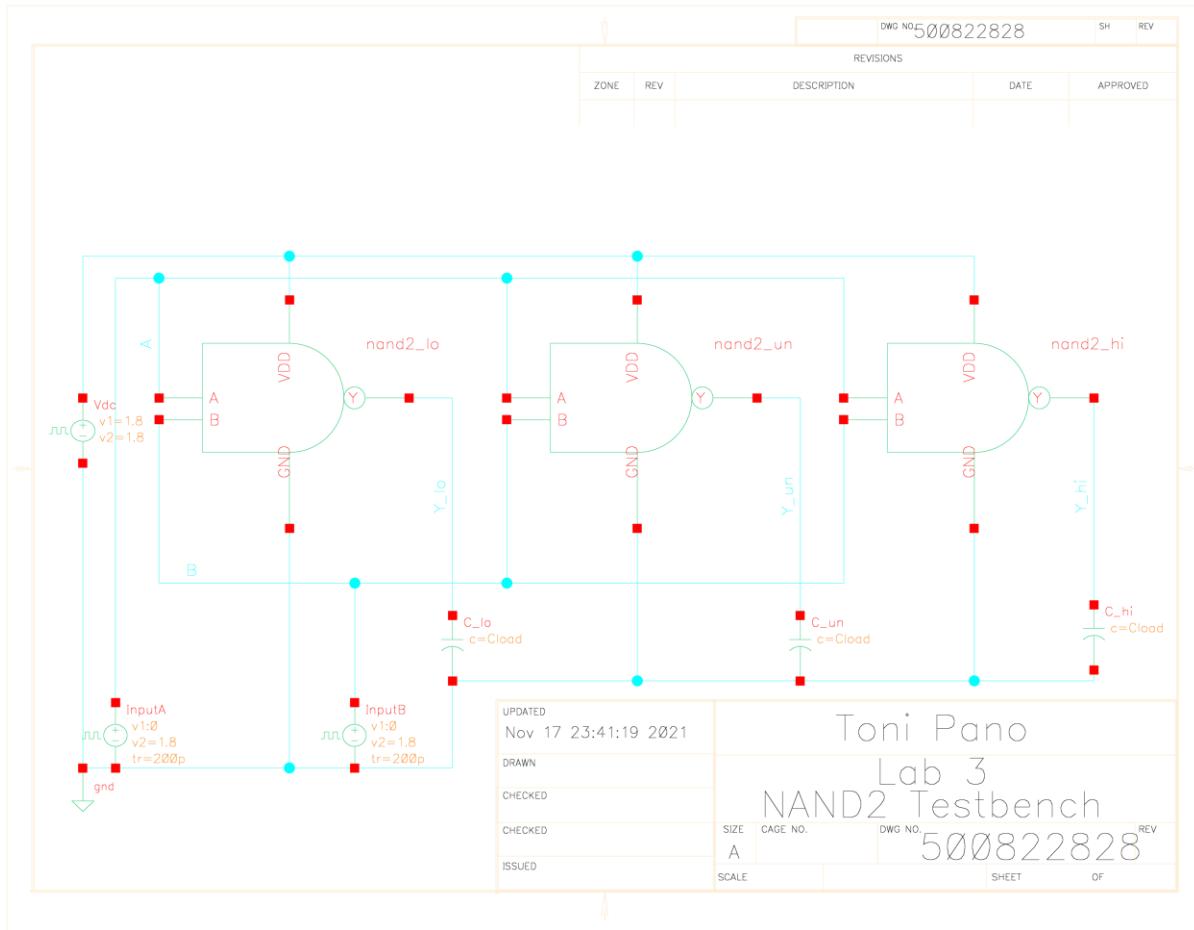


Figure 2.2. Schematic of the testbench for the low skewed (left), unskewed (middle), and high-skewed (right) NAND2 gates.

3. Delay measurement for unskewed, high-skewed and low skewed NOR2 and NAND2 gates

a. NOR2 Gate

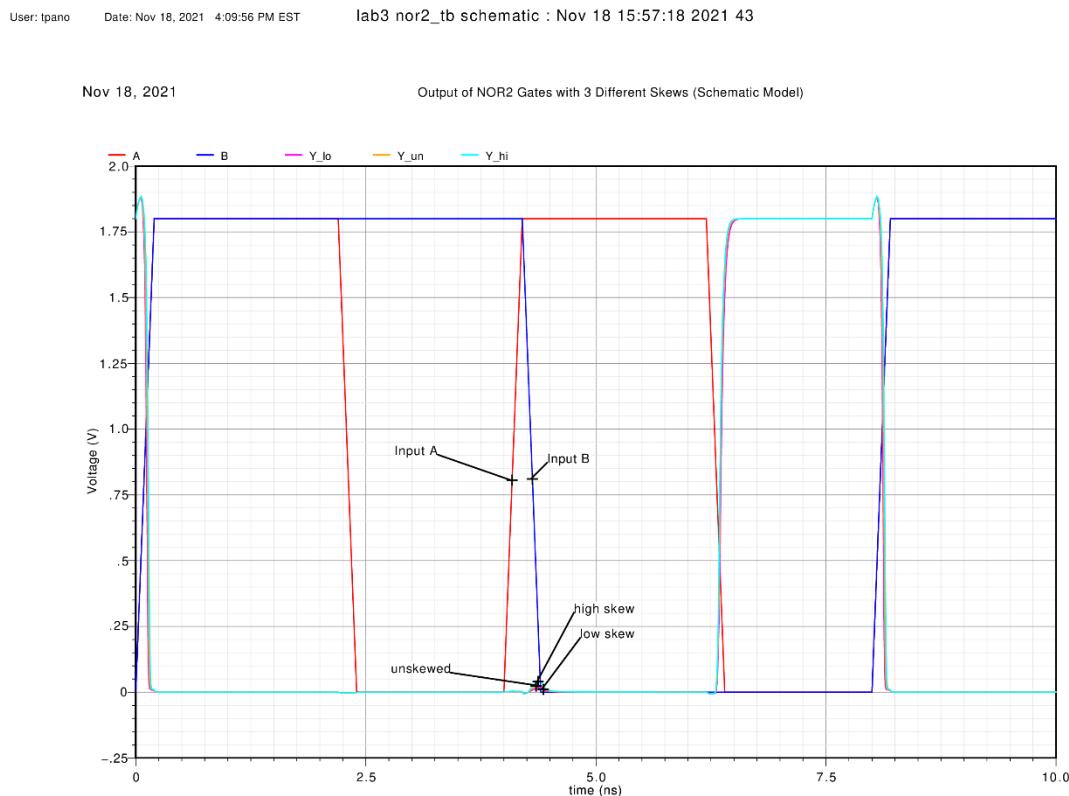


Figure 3.A.1. The output voltage of the NOR2 gate over time, for each combination of A and B input voltages. Each gate has a load capacitance of 50fF.

6	Y_lo Falling Delay	18.16p
7	Y_un Falling Delay	25.71p
8	Y_hi Falling Delay	35.03p

Figure 3.A.2. The falling delay of the low skewed (Y_lo), unskewed (Y_un), and high skewed (Y_hi) NOR2 gates. Each gate has a load capacitance of 50fF.

9	Y_lo Rising Delay	4.062n
10	Y_un Rising Delay	4.055n
11	Y_hi Rising Delay	4.05n

Figure 3.A.3. The rising delay of the low skewed (Y_lo), unskewed (Y_un), and high skewed (Y_hi) NOR2 gates. Each gate has a load capacitance of 50fF.

b. NAND2 Gate

User: tpano Date: Nov 17, 2021 11:43:46 PM EST lab3_nand2_tb schematic : Nov 17 23:41:44 2021 15

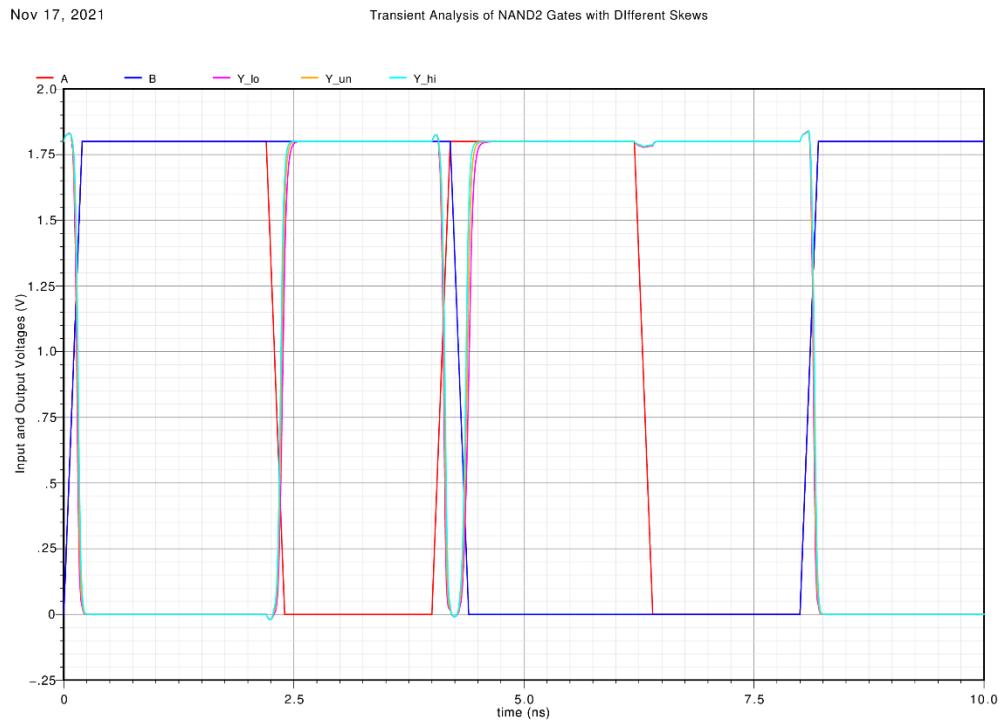


Figure 3.B.1. The output voltage of the NAND2 gate over time, for each combination of A and B input voltages. Each gate has a load capacitance of 50fF.

6	Y_lo Falling Delay	42.6p
7	Y_un Falling Delay	48.94p
8	Y_hi Falling Delay	57.11p

Figure 3.B.2. The falling delay of the low skewed (Y_lo), unskewed (Y_un), and high skewed (Y_hi) NAND2 gates. Each gate has a load capacitance of 50fF.

9	Y_lo Rising Delay	78.27p
10	Y_un Rising Delay	66.15p
11	Y_hi Rising Delay	56.39p

Figure 3.B.3. The rising delay of the low skewed (Y_lo), unskewed (Y_un), and high skewed (Y_hi) NAND2 gates. Each gate has a load capacitance of 50fF.

4. The layout and extracted views of the unskewed NOR2 and NND@ gates

a. NOR2 Gate

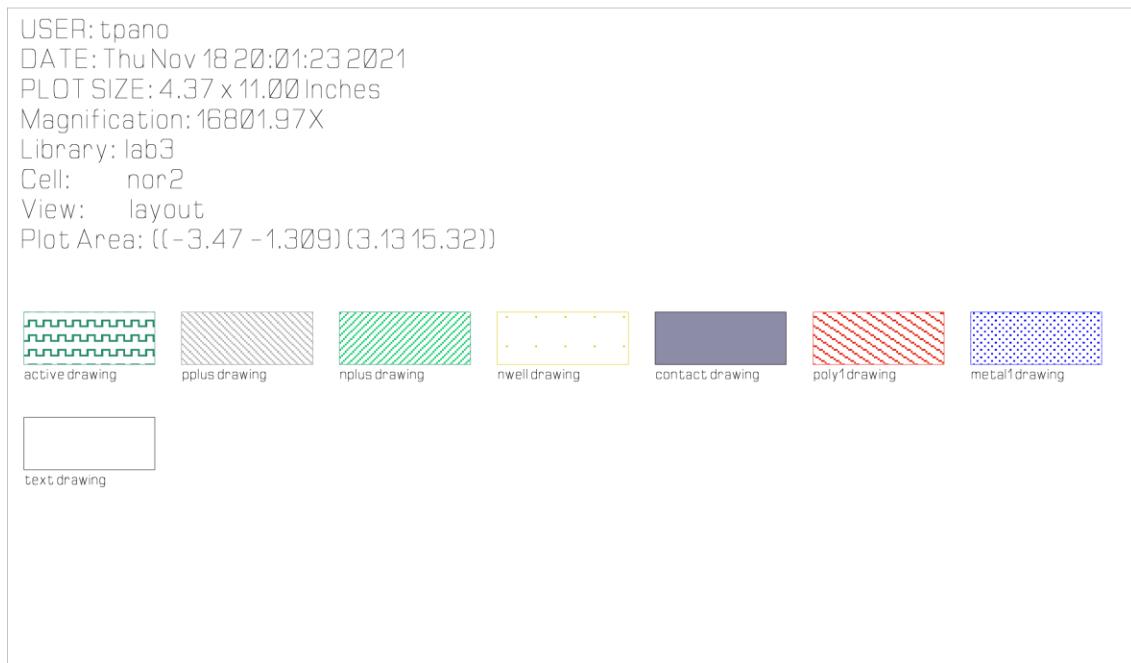


Figure 4.A.1. The legend of the layout view for the unskewed NOR2 gate.

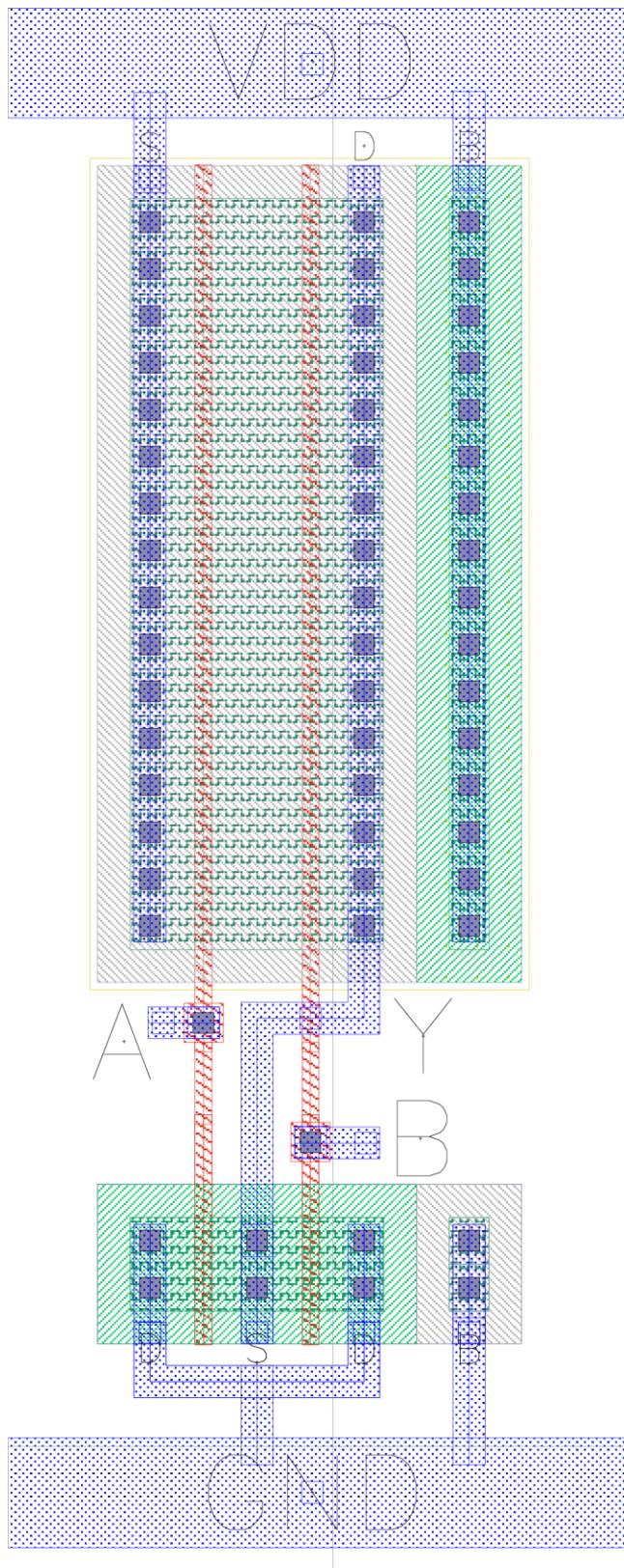


Figure 4.A.2. The layout view of the NOR2 gate.



Figure 4.A.3. The legend of the extracted view for the unskewed NOR2 gate.

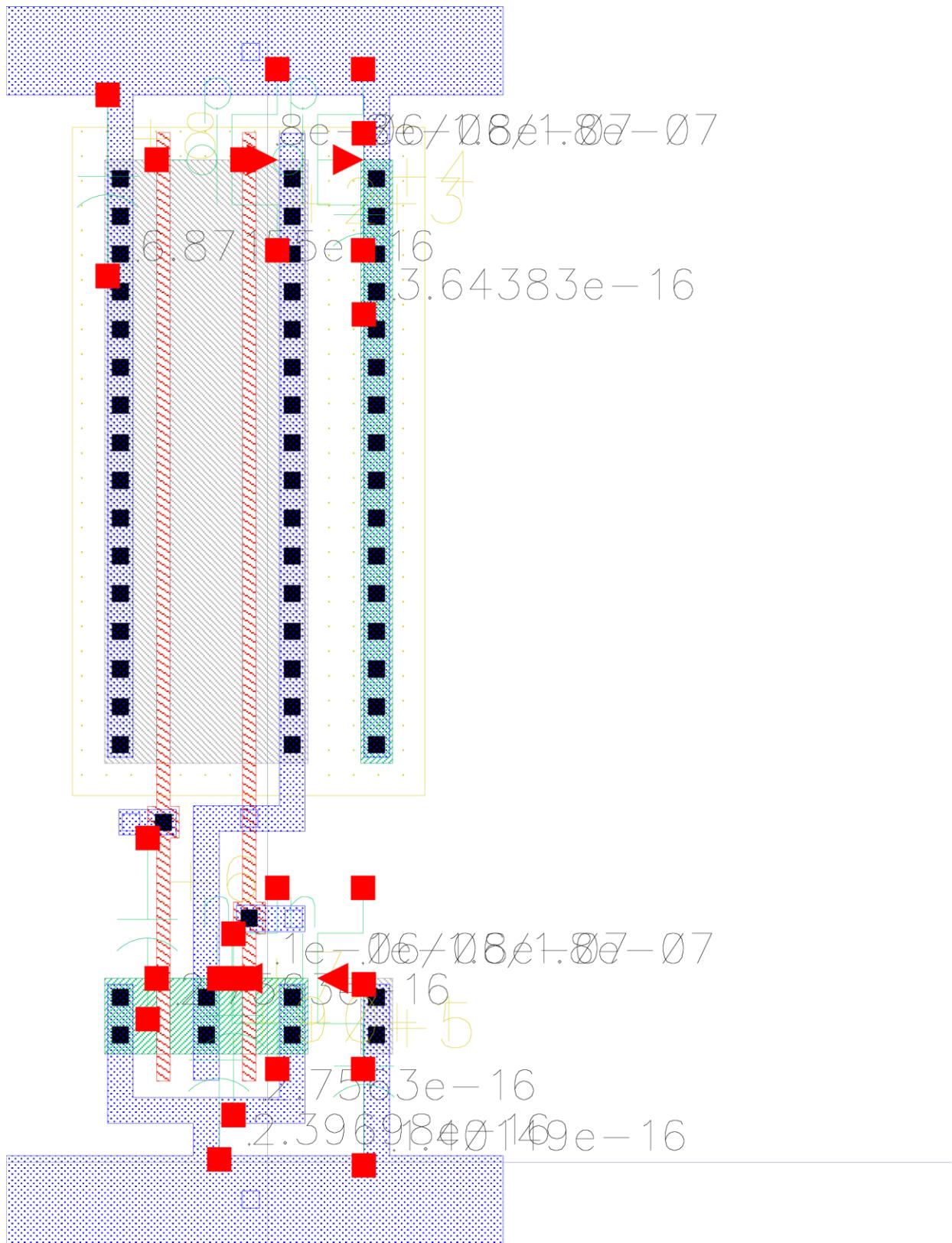


Figure 4.A.4. The extracted view of the NOR2 gate.

b. NAND2 Gate

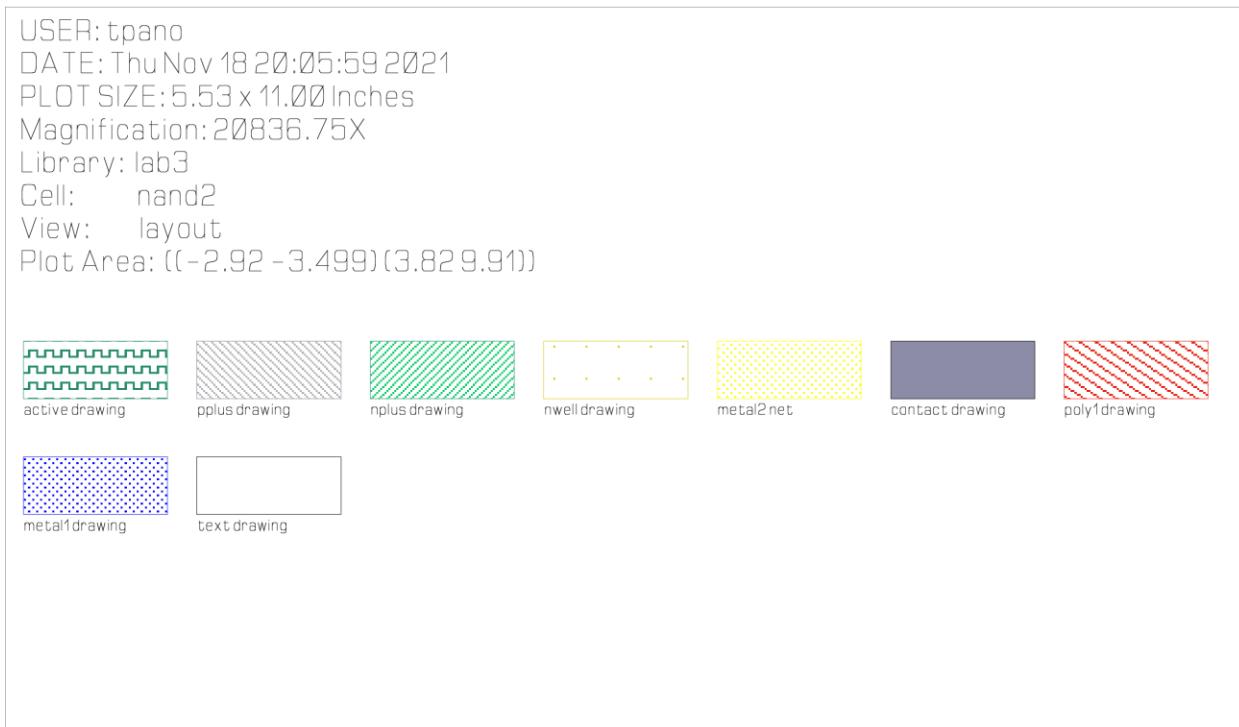


Figure 4.B.1. The legend of the layout view for the unskewed NAND2 gate.

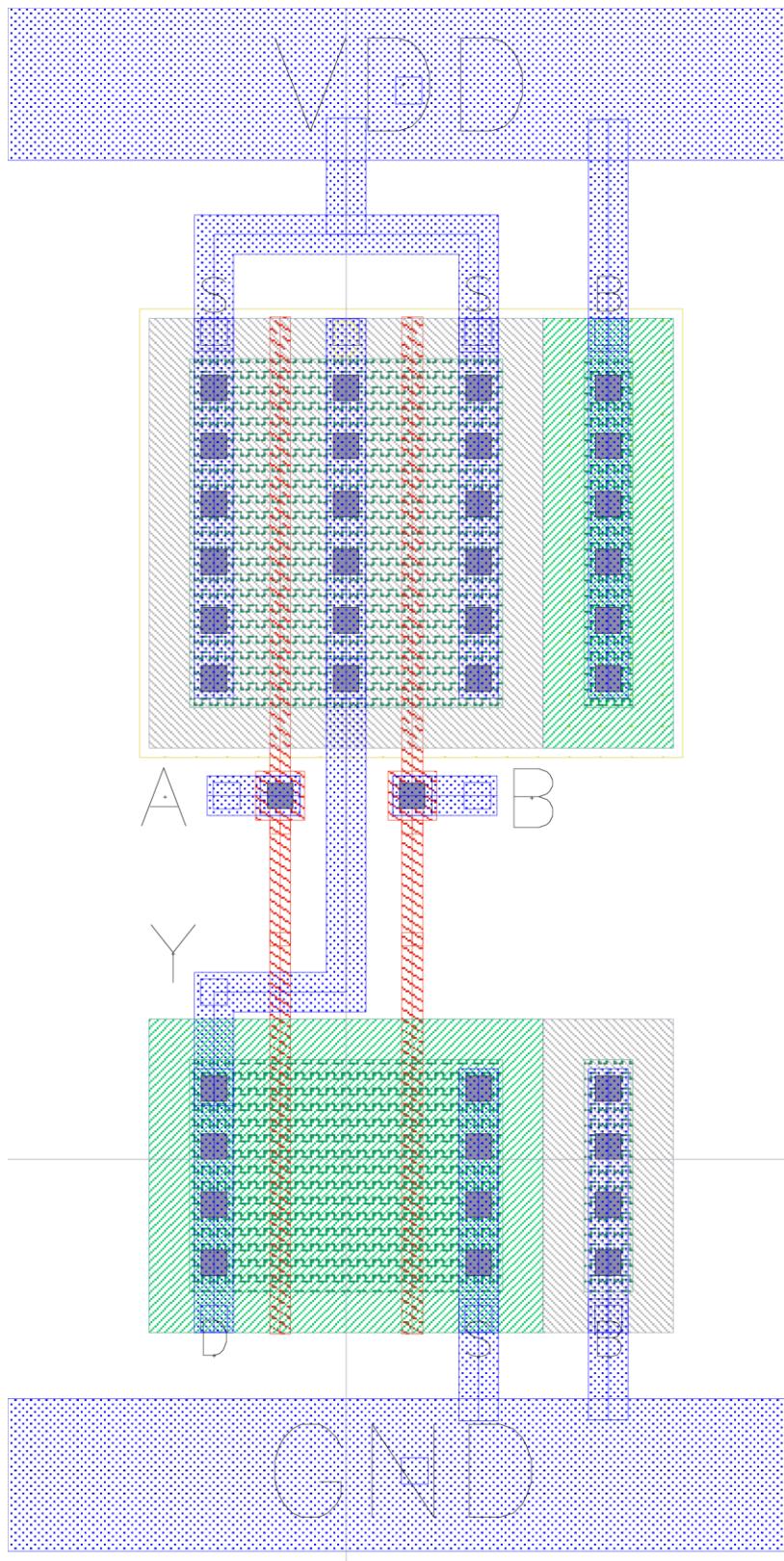


Figure 4.B.2. The layout view of the NAND2 gate.



Figure 4.B.3. The legend of the extracted view for the unskewed NAND2 gate.

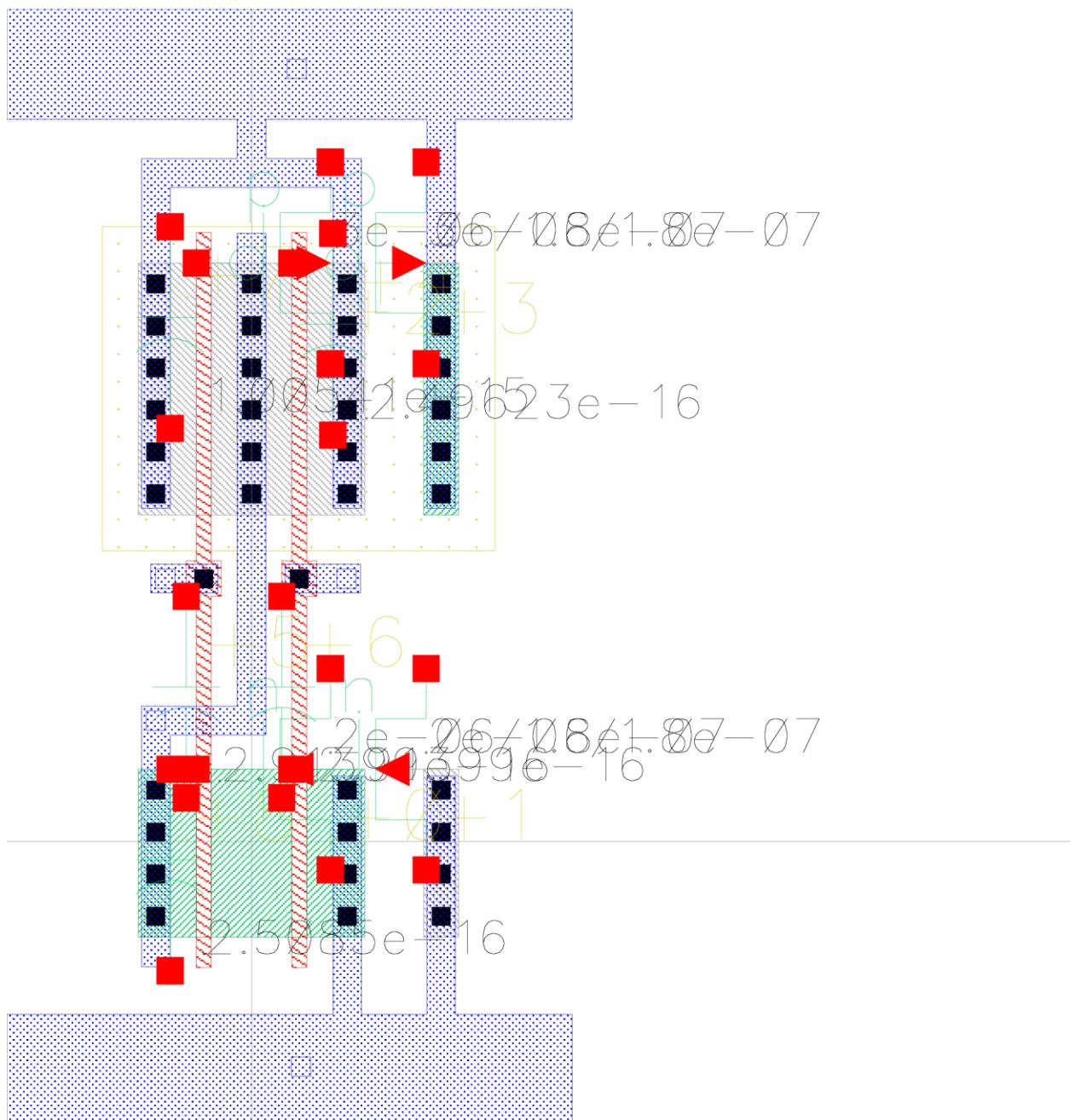


Figure 4.B.4. The extracted view of the NAND2 gate.

5. Post-layout simulation comparing delay measurement for unskewed NAND2 and NOR2 gates

User: tpano Date: Nov 18, 2021 6:46:06 PM EST lab3 nor2_tb_extracted schematic : Nov 18 18:39:26 2021 88

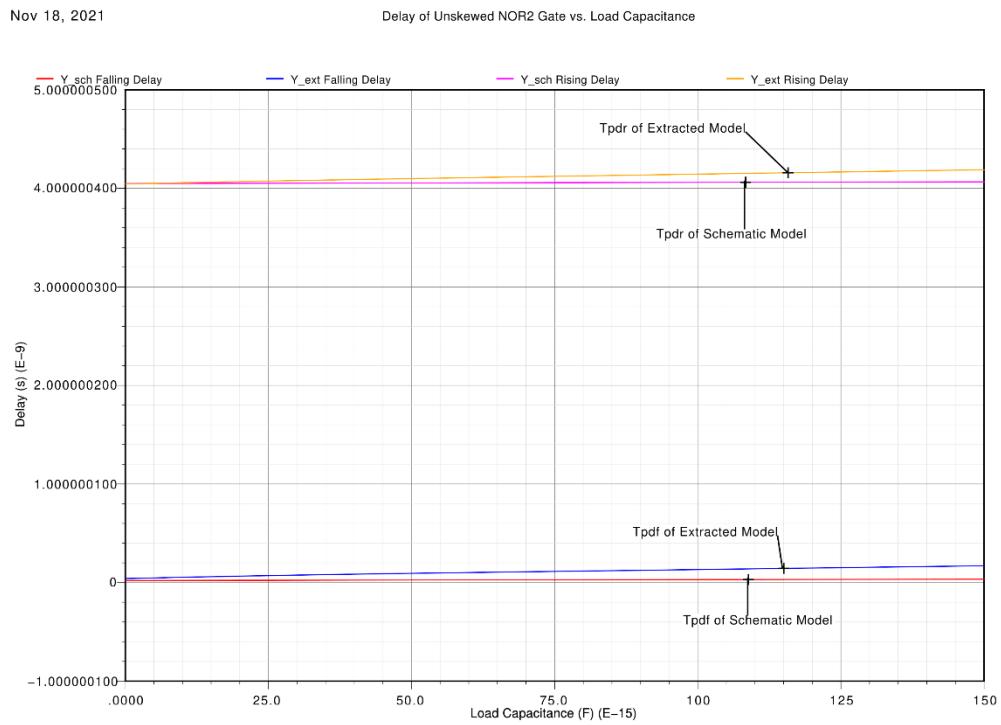


Figure 5.1. Delay measurement for unskewed NOR2 gates as the load capacitance changes from 0F to 150fF. Both the schematic model and extracted model of the NOR2 gate are compared.

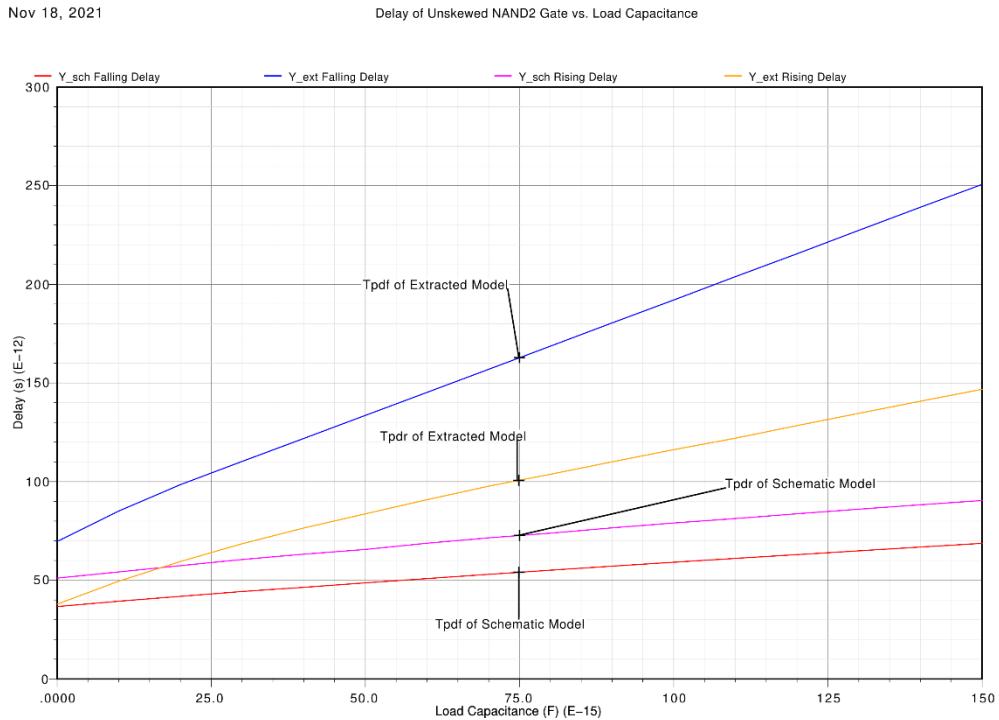


Figure 5.2. Delay measurement for unskewed NAND2 gates as the load capacitance changes from 0F to 150fF. Both the schematic model and extracted model of the NAND2 gate are compared.

6. Summary of Results

The delay of the low skewed, unskewed, and high skewed NOR2 gates show the following trends. The falling delay increases as the skew gets higher, and each falling delay is below 100ps. The rising delay decreases as the skew gets higher, and each rising delay for the NOR2 gate is about 40 times larger than 100ps. The post-layout simulation shows that the delay of the unskewed extracted NOR2 gate model matches the delay of the unskewed schematic model very closely. The extracted model has the same Tpdf and Tpdr that the schematic model does when no load capacitance is present. The extracted model has a slightly higher Tpdf and Tpdr than the schematic model does for all other load capacitance values. This may have occurred because the video of the NOR2 layout for this lab used a Wp/Wn ratio of 8um/1um, which differed from the derived Wp/Wn prelab ratio of 82.408um/20.602um.

The delay of the low skewed, unskewed, and high skewed NAND2 gates show the following trends. The falling delay increases as the skew gets higher, and each falling delay is below 100ps.

The rising delay decreases as the skew gets higher, and each rising delay for the NOR2 gate is below 100 ps. The post-layout simulation shows that the delay of the unskewed extracted NAND2 gate model differs significantly from the unskewed schematic model. Both models have a higher Tpdf than their respective Tpdr. The extracted model's Tpdr is the same as the schematic model's Tpdf when no load capacitance is present. This should not happen if the extracted and schematic models represent an unskewed NAND2 gate. This may have happened because the photo of the layout of the unskewed NAND2 gate in the lab manual uses a Wp/Wn ratio of 3um/2um, which differs significantly from the prelab's derived ratio of 18.427um/18.427um.