Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	Low Power Digital Integrated Circuits
Course Number:	ELE 734
Semester/Year (e.g.F2016)	F2021

Instructor:	Andy Ye

Assignment/Lab Number:	1
Assignment/Lab Title:	Characteristics of MOSFET Devices

Submission Date:	October 12, 2021
Due Date:	October 12, 2021

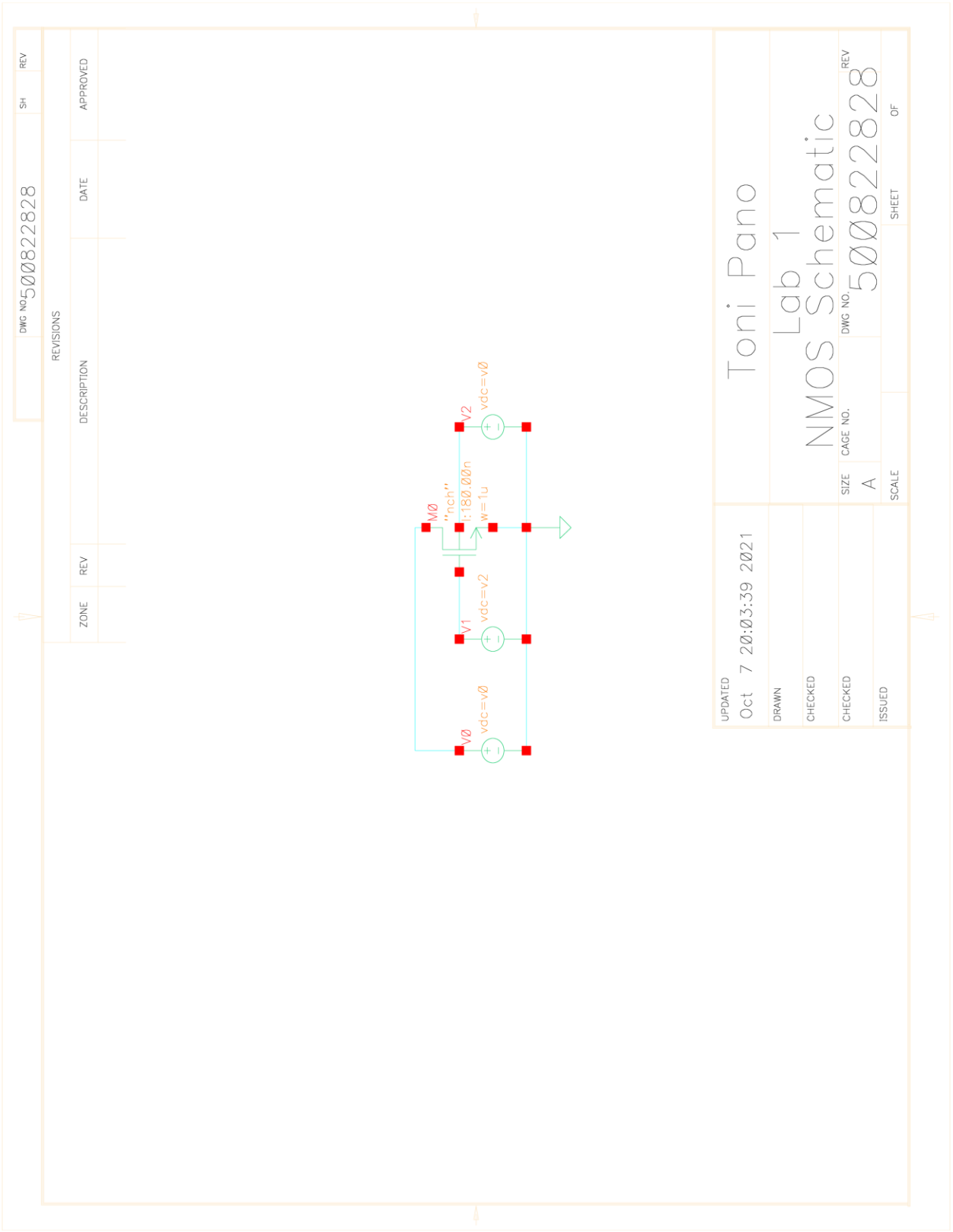
Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Pano	Toni	500822828	7	T.P.

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

Lab 1: Post-Lab Report

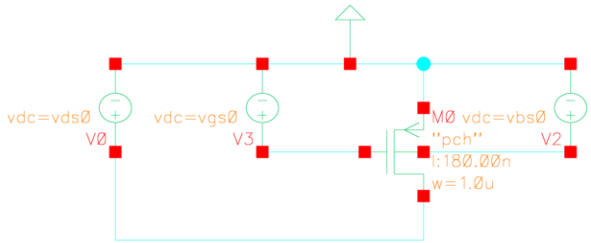
The only deviations from the prelab are the non-ideal Ids-Vgs corves for both the NMOS and PMOS devices. They do not show a constant current value when operating in the saturation region.

1. The schematic of your NMOS and PMOS circuits.



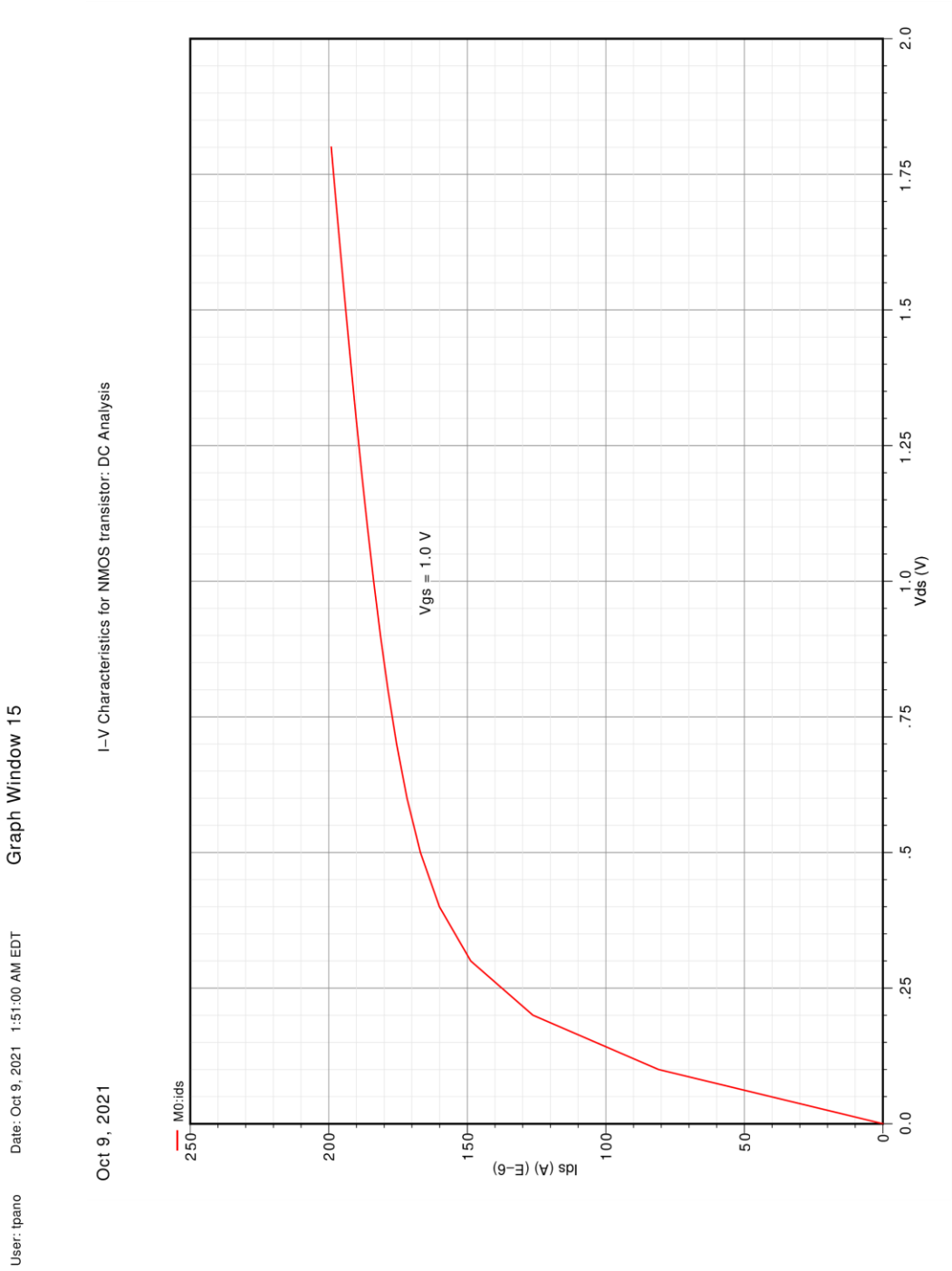
DWG NO. 5Ø0822828	SH	REV

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



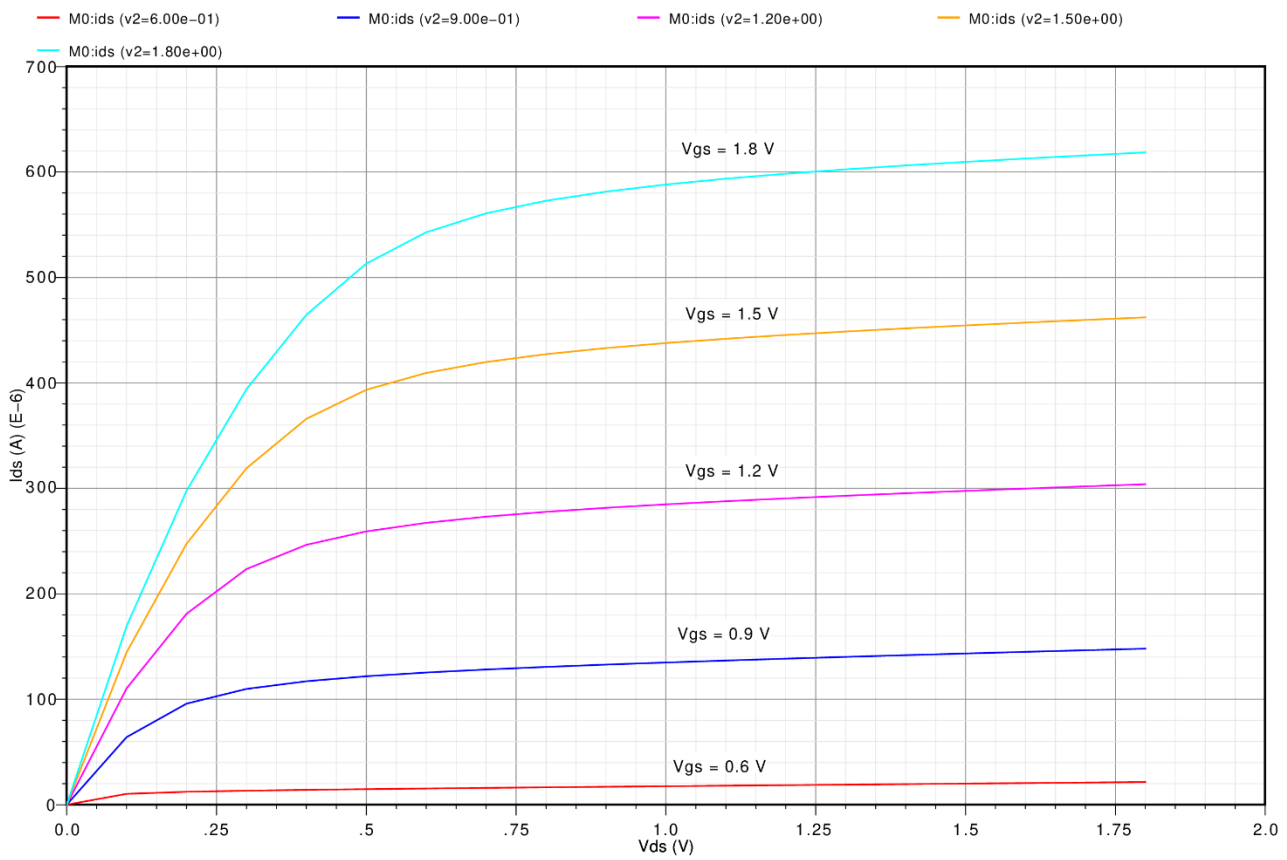
UPDATED Oct 7 20:08:57 2021	Toni Pano		
DRAWN	Lab 1 PMOS Schematic		
CHECKED			
CHECKED	SIZE A	CAGE NO.	DWG NO. 5Ø0822828 REV
ISSUED	SCALE		SHEET OF

2. The family of I-V characteristic waveforms for both NMOS and PMOS devices.



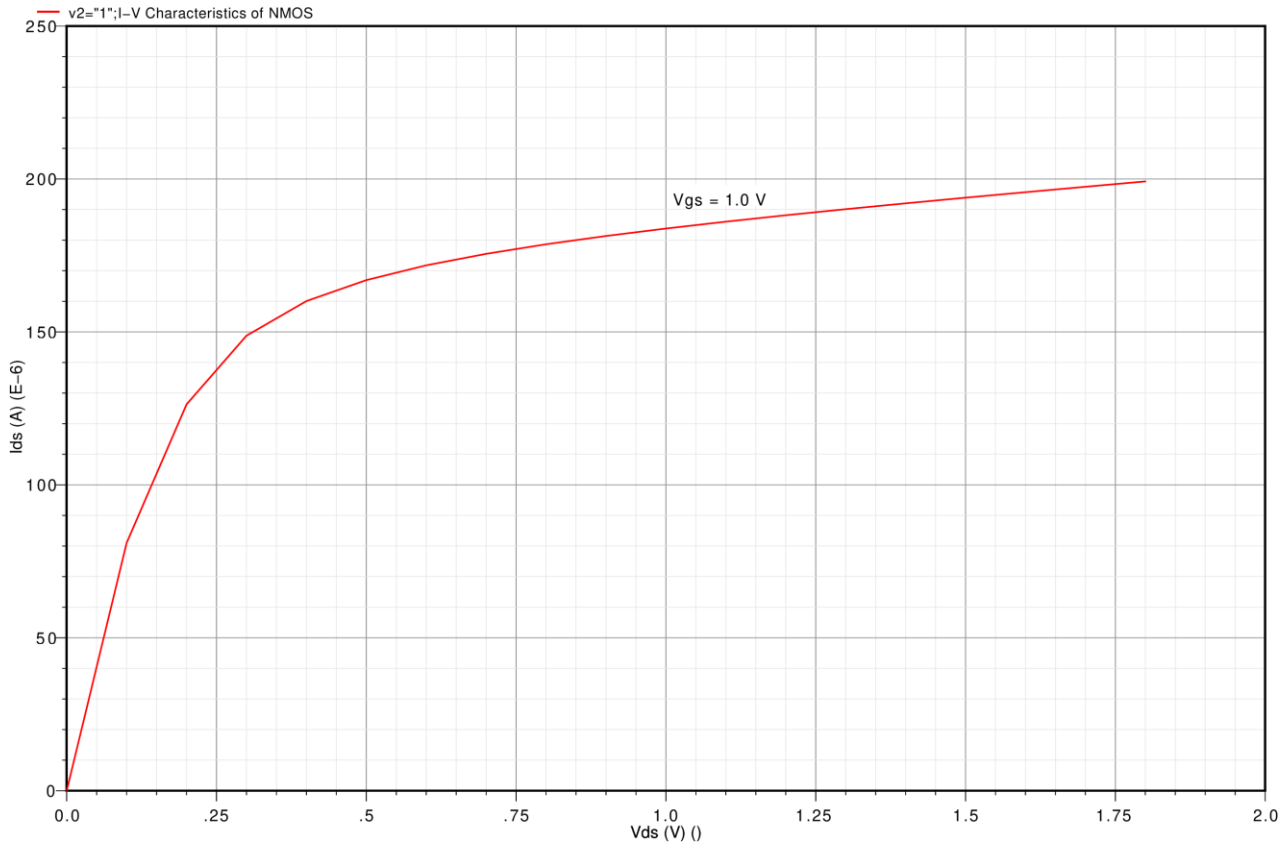
User: tpano Date: Sep 14, 2021 7:59:00 PM EDT Graph Window 57

Sep 14, 2021 I–V Characteristics for NMOS Transistor: DC Parametric Analysis



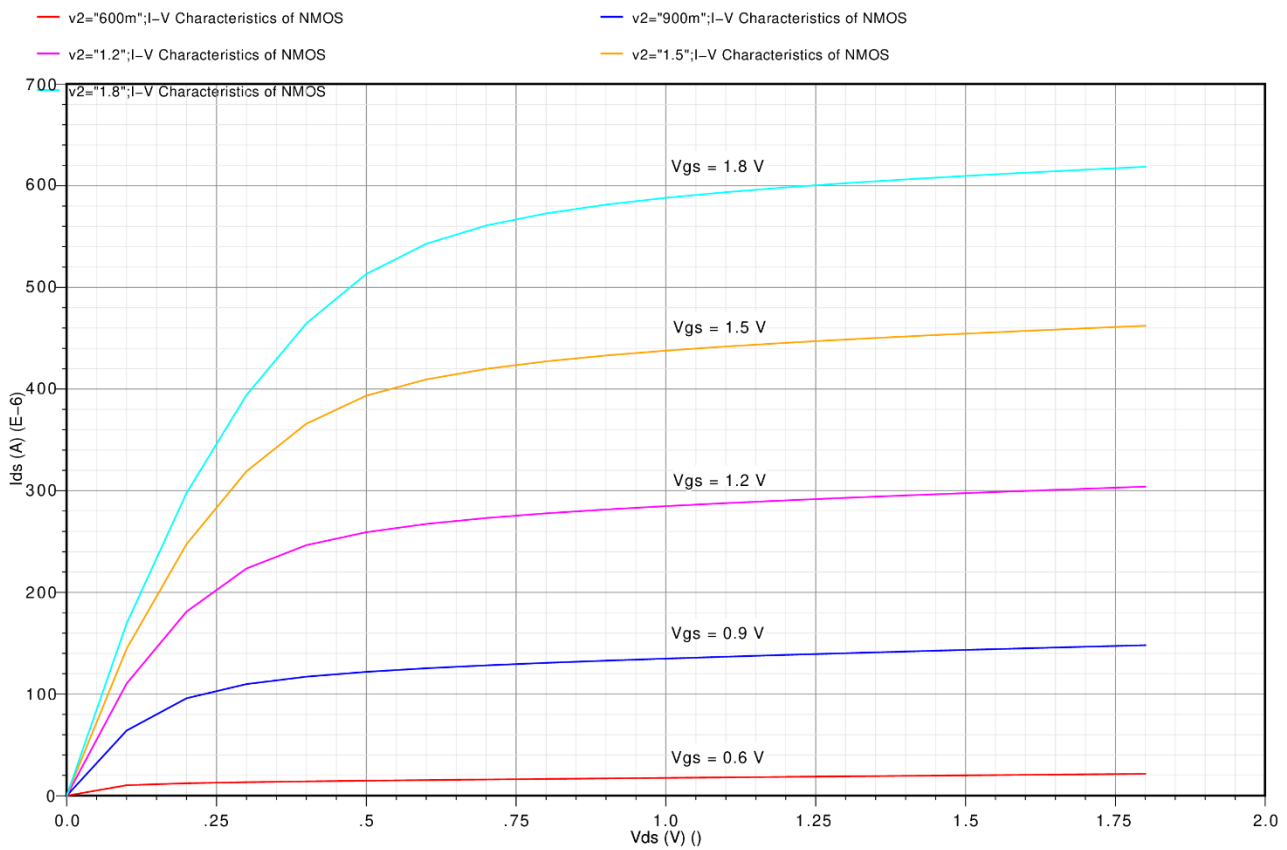
User: tpano Date: Sep 14, 2021 8:25:00 PM EDT lab1 nmos schematic : Sep 14 20:13:16 2021 67

Sep 14, 2021 I–V Characteristics of NMOS: Transient Parametric Analysis – Vds Only



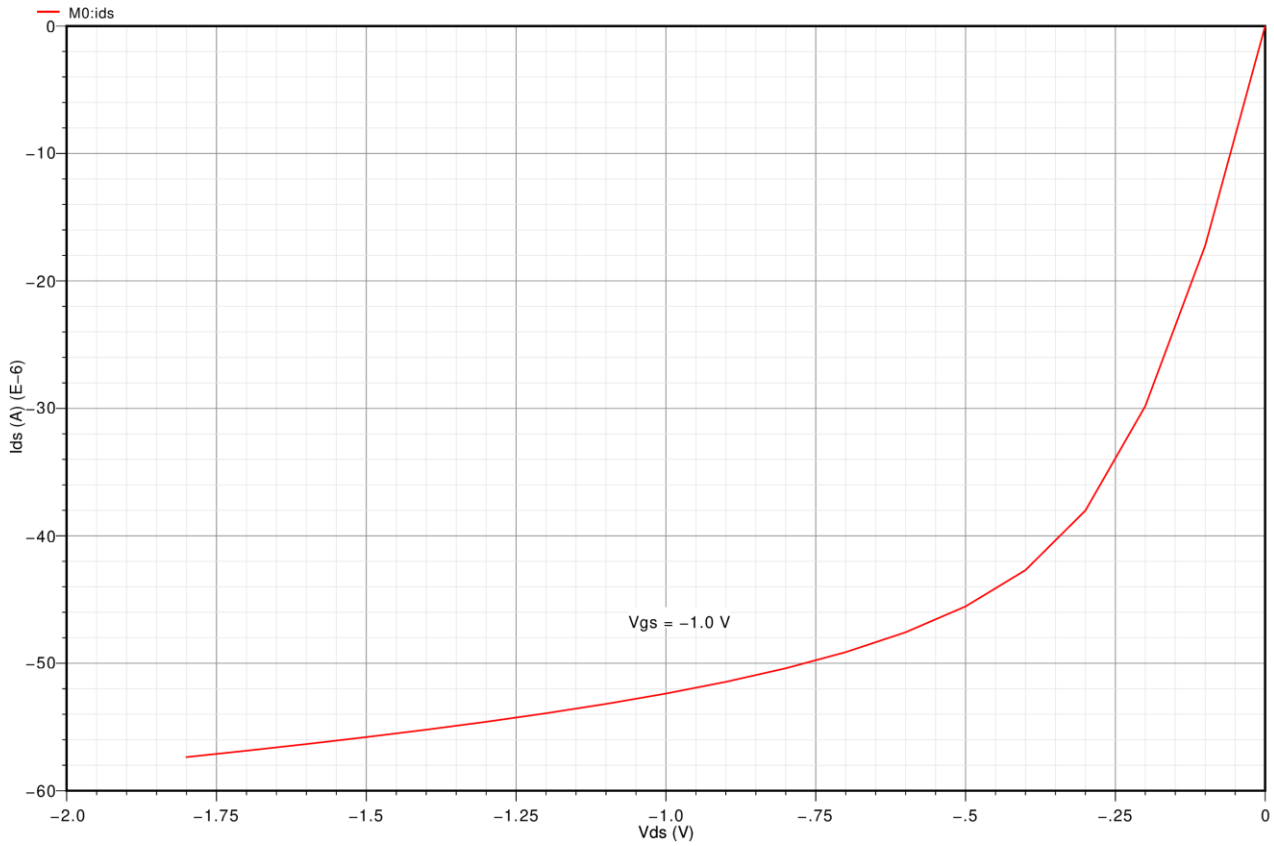
User: tpano Date: Sep 14, 2021 8:52:02 PM EDT lab1 nmos schematic : Sep 14 20:31:44 2021 74

Sep 14, 2021 I–V Characteristics for NMOS transistor: Transient Parametric Analysis – Vds and Vgs



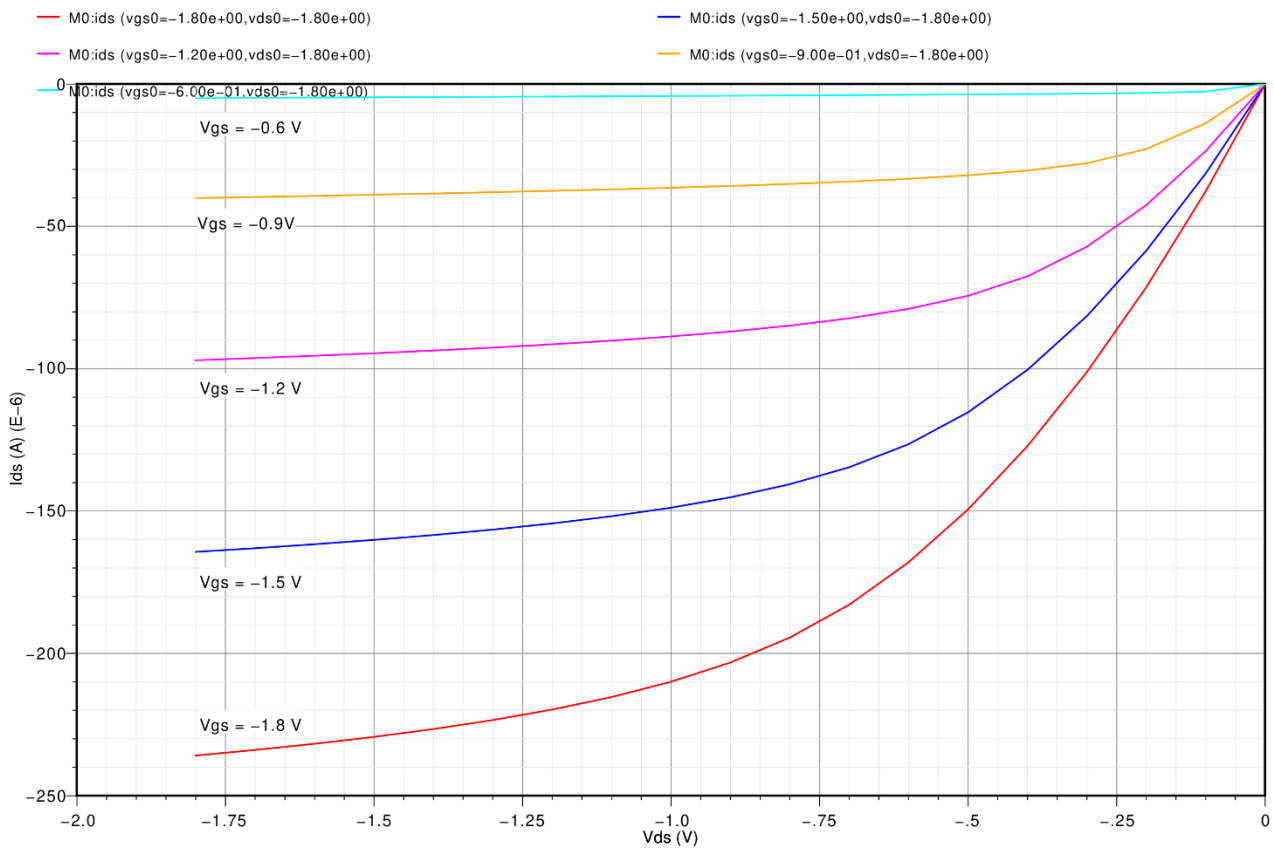
User: tpano Date: Sep 21, 2021 1:30:27 PM EDT Graph Window 31

Sep 21, 2021 I–V Characteristics for PMOS transistor: DC Analysis with single Gate Voltage



User: tpano Date: Sep 21, 2021 1:54:00 PM EDT Graph Window 33

Sep 21, 2021 I–V Characteristics for PMOS transistor: DC Analysis with multiple Gate Voltages



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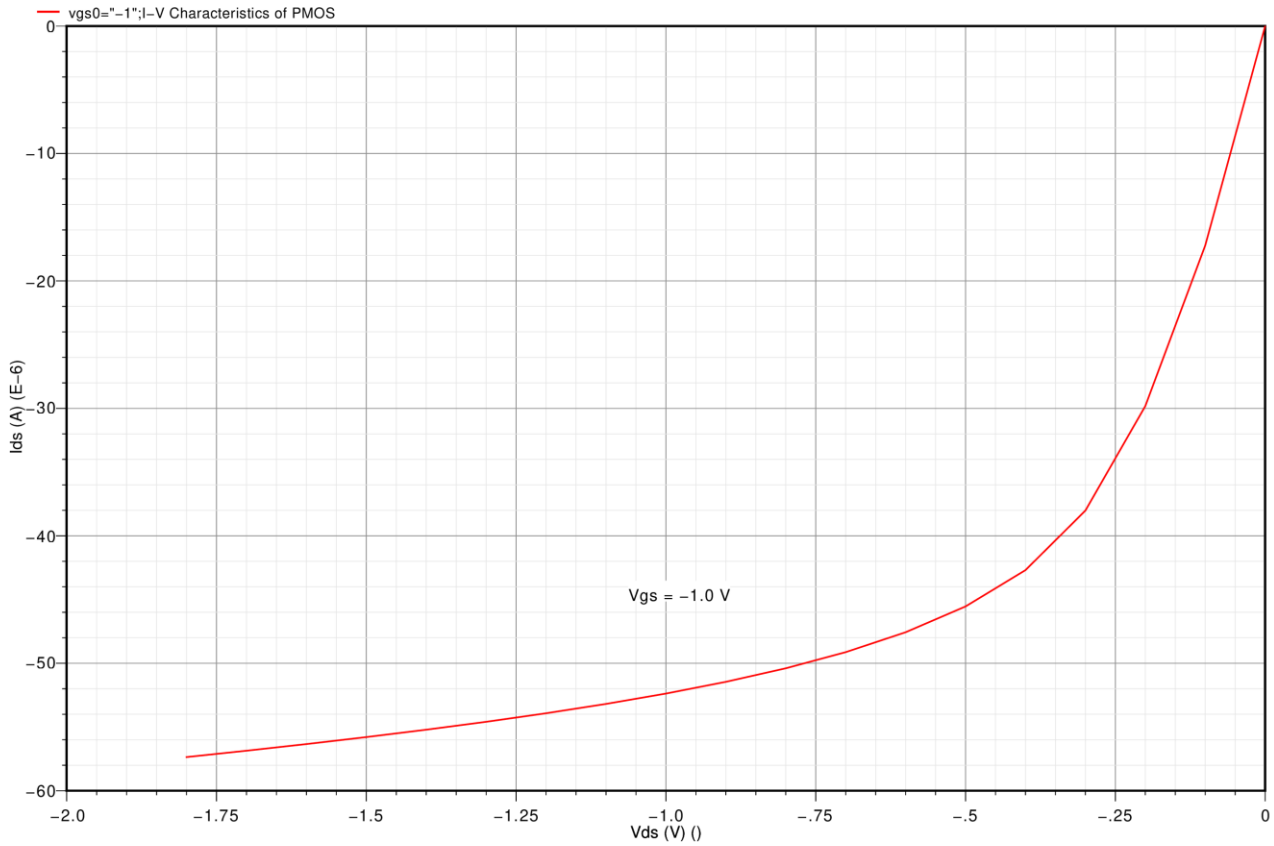
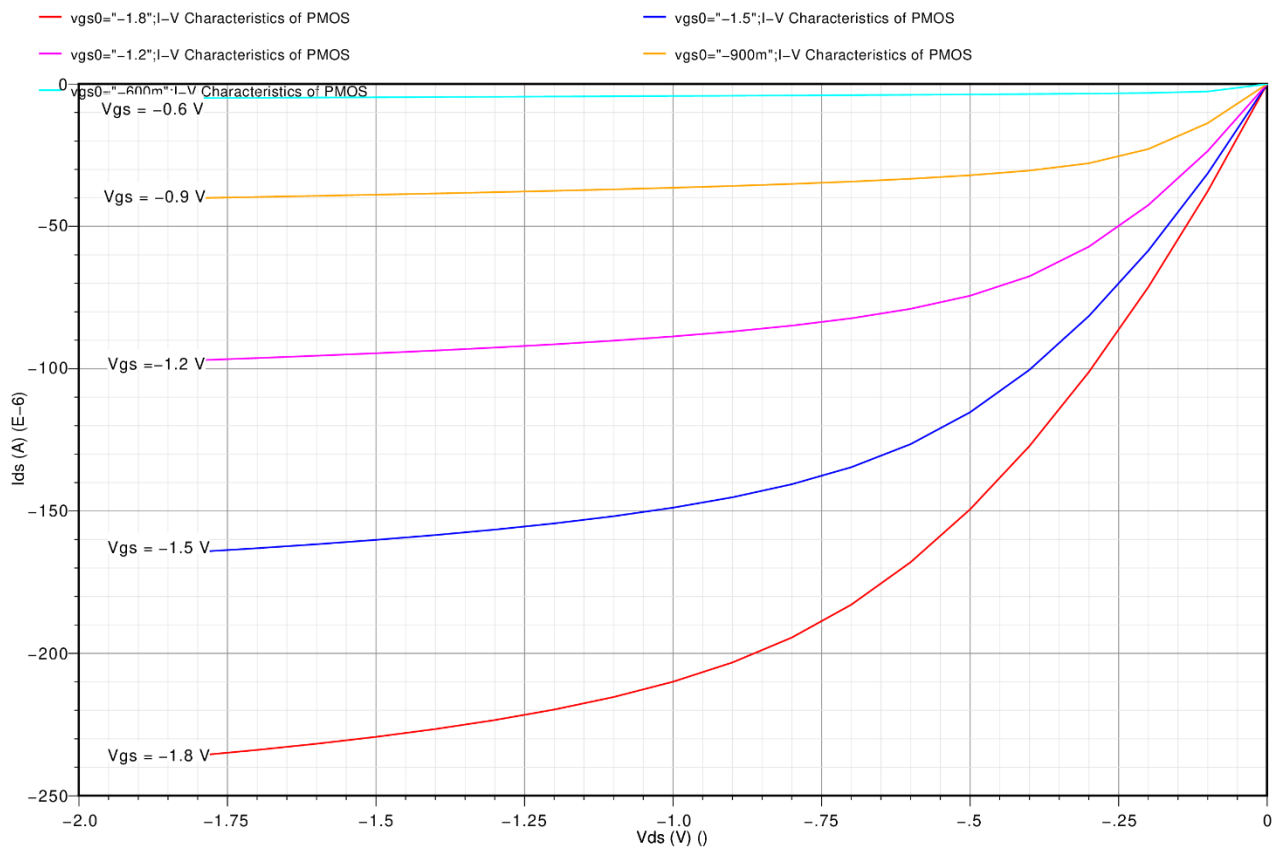
Sep 21, 2021 I–V Characteristics for PMOS transistor: Transient Analysis with single Gate Voltage

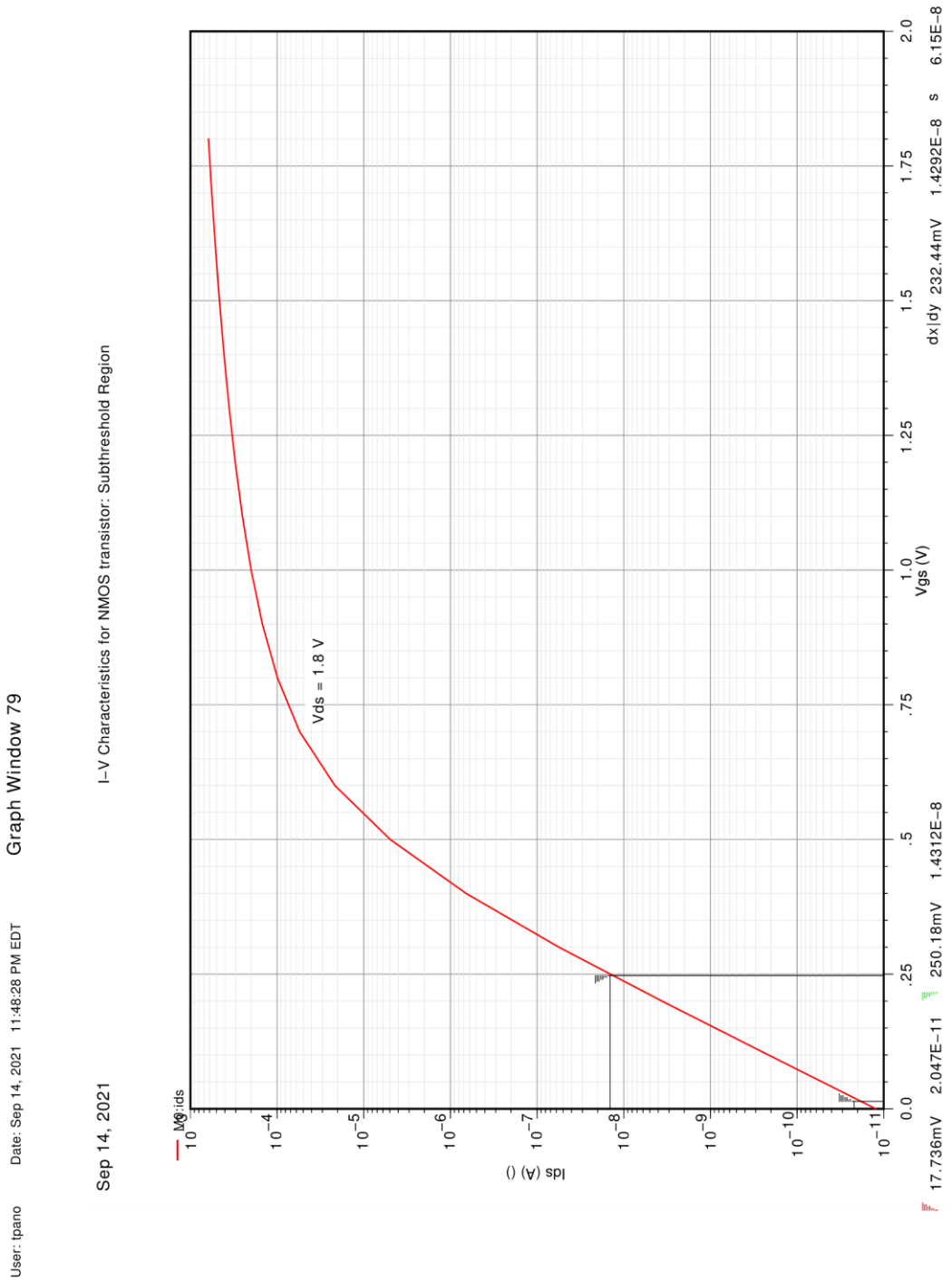


User: tpano Date: Sep 21, 2021 1:11:58 PM EDT lab1 pmos schematic : Sep 21 13:04:27 2021 27

Sep 21, 2021 I–V Characteristics for PMOS transistor: Transient Analysis with multiple Gate Voltages

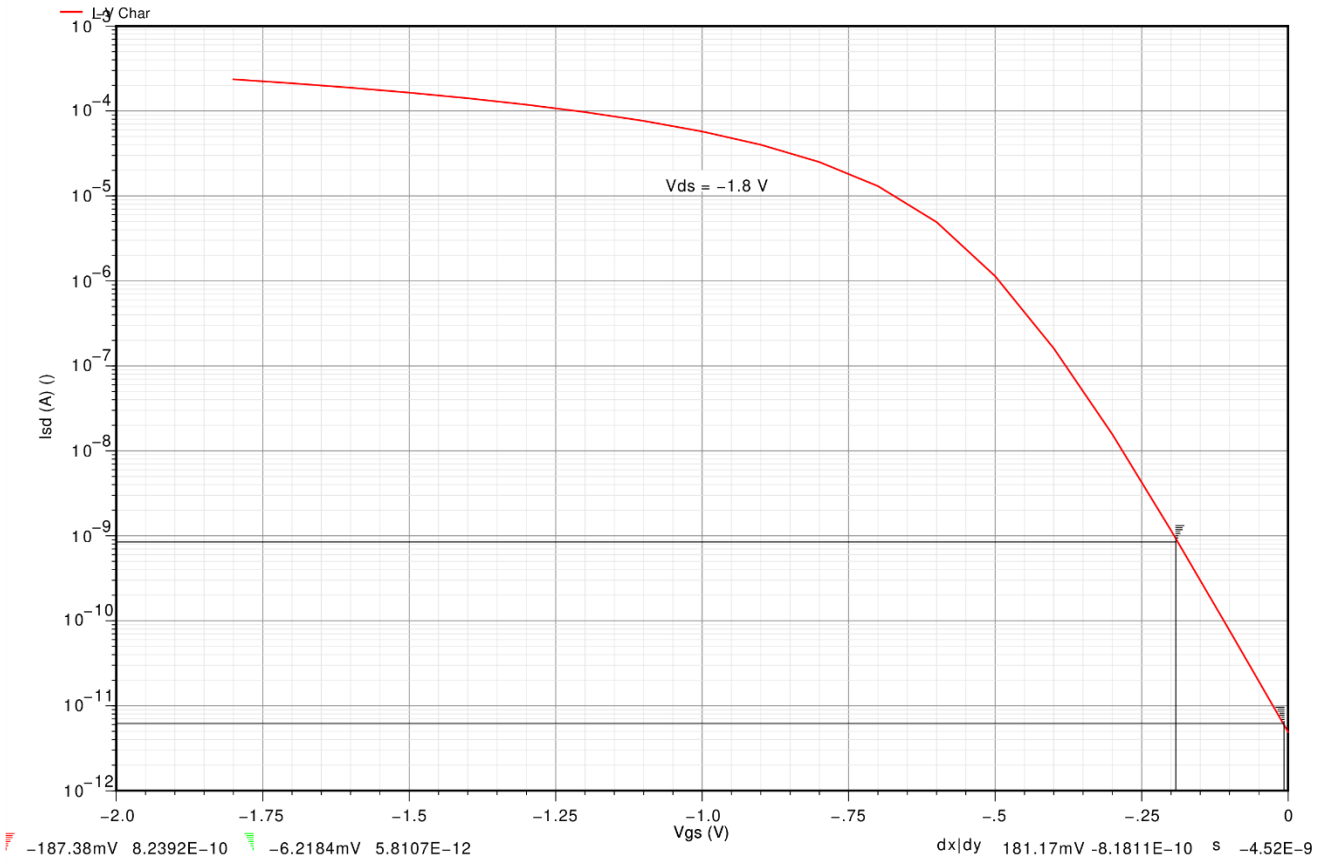


3. The Ids-Vgs curve used to obtain the subthreshold slope for both NMOS and PMOS devices.

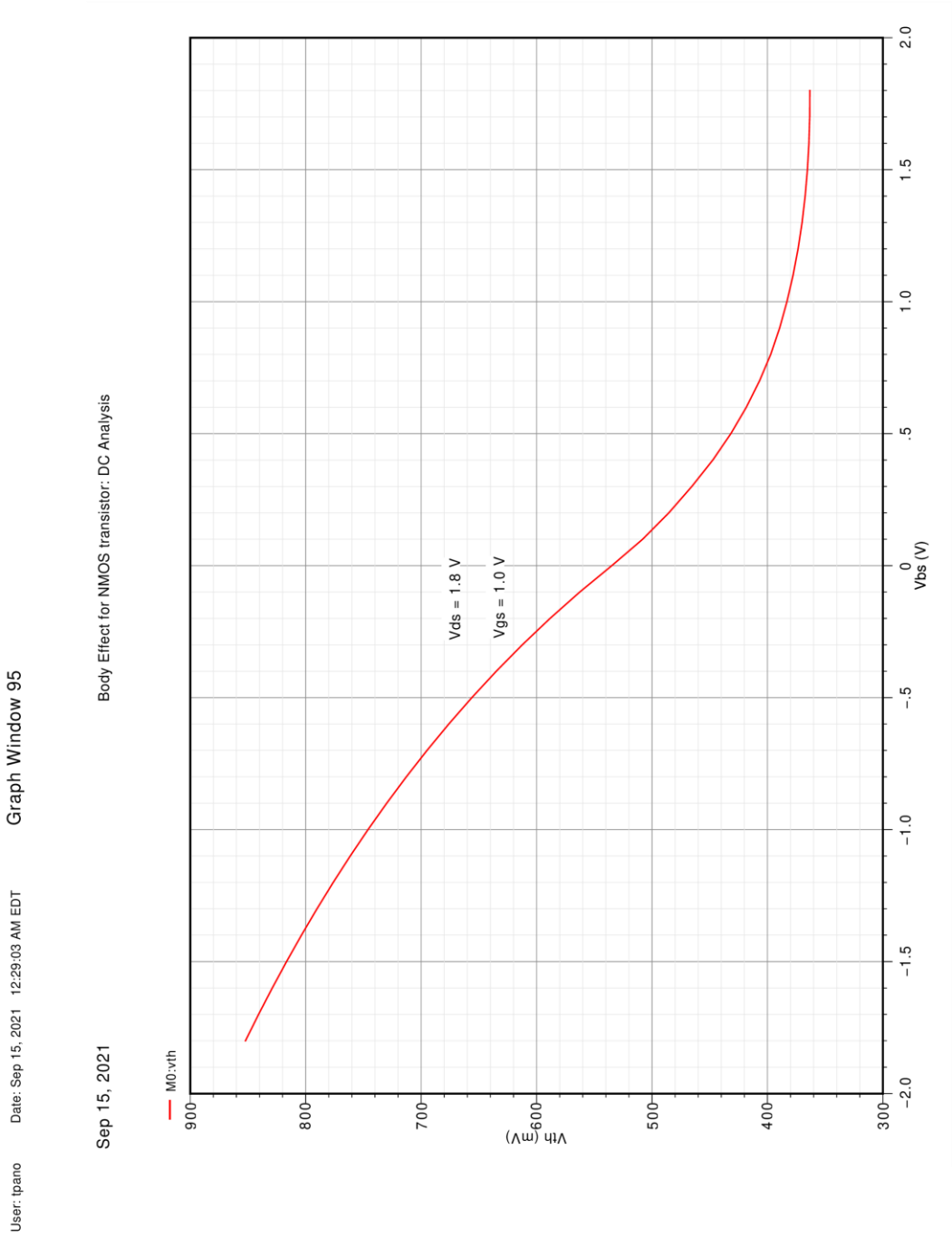


User: tpano Date: Sep 21, 2021 2:36:20 PM EDT lab1 pmos schematic : Sep 21 13:58:38 2021 42

Sep 21, 2021 I–V Characteristics for PMOS transistor: DC Analysis with single Drain Voltage

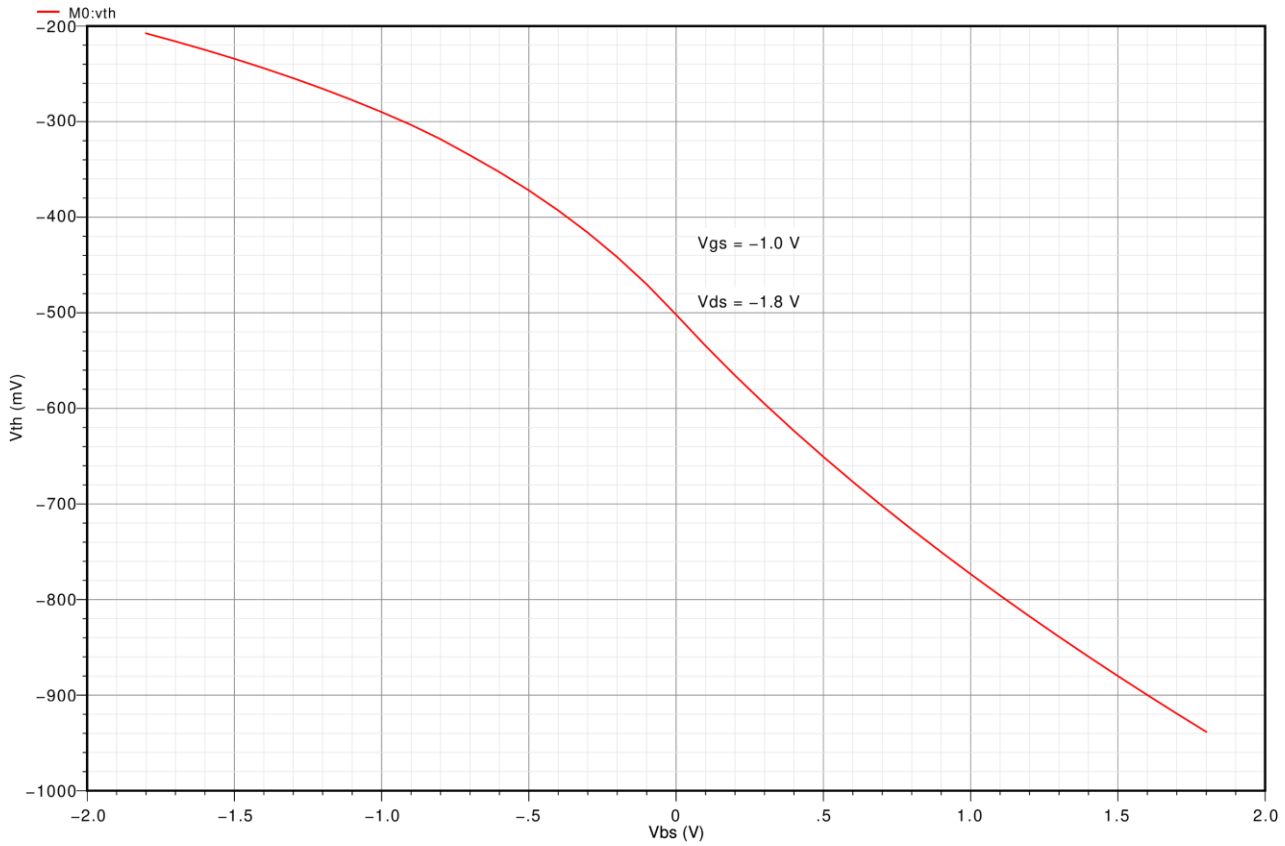


4. The Vth-Vgs curve used to analyse the body effect for both NMOS and PMOS devices.

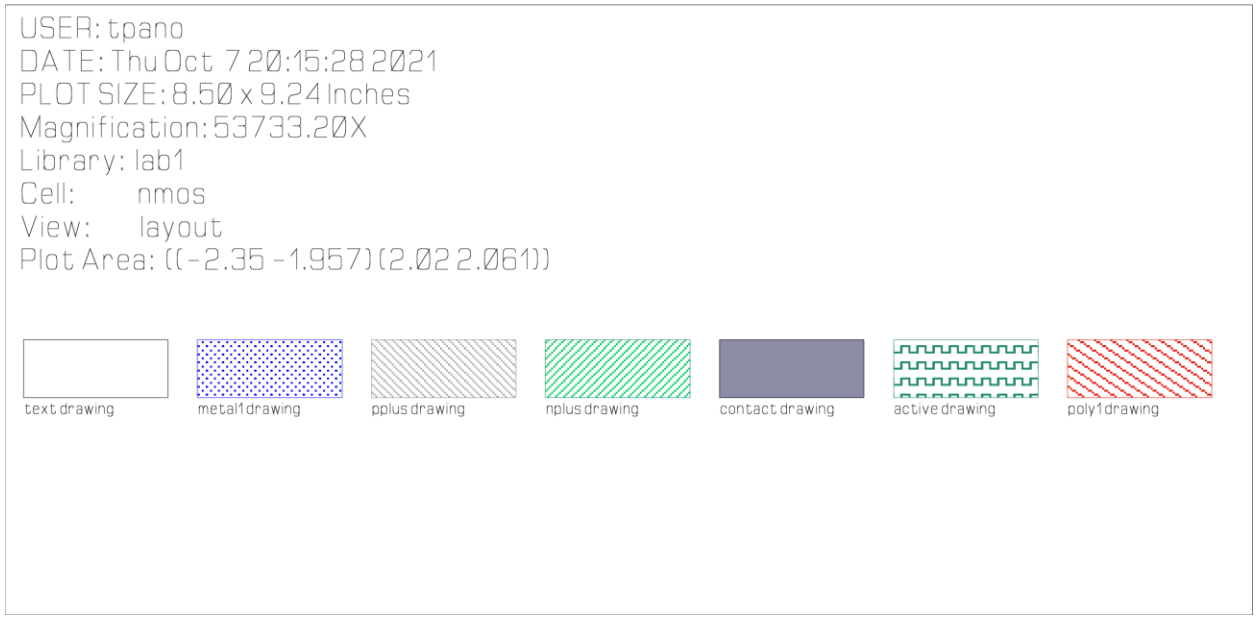


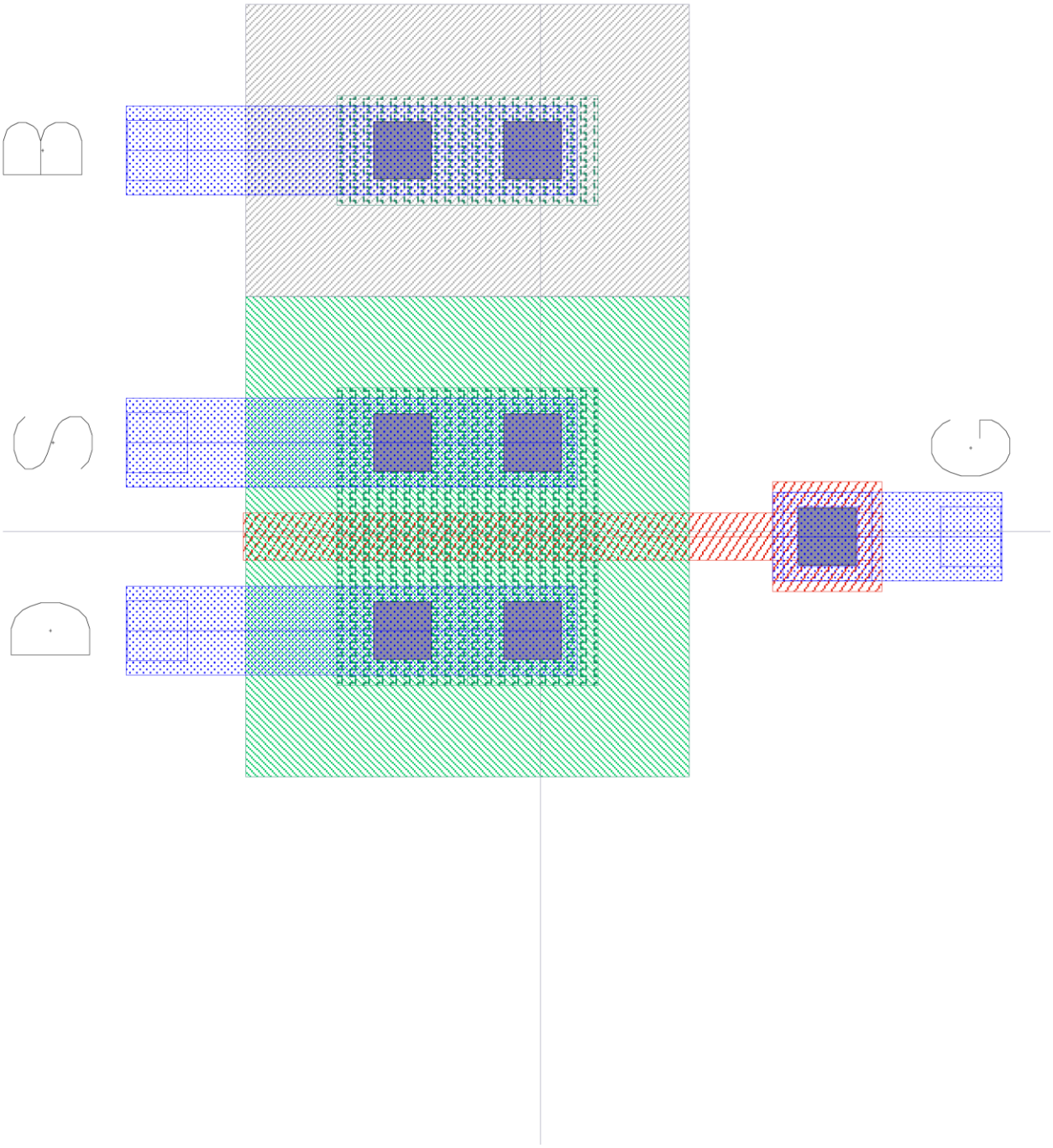
User: tpano Date: Oct 7, 2021 7:22:39 PM EDT Graph Window 10

Oct 7, 2021 Body Effect of PMOS transistor: DC Analysis

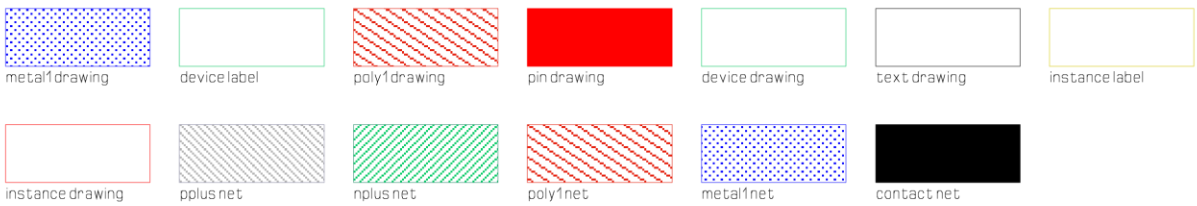


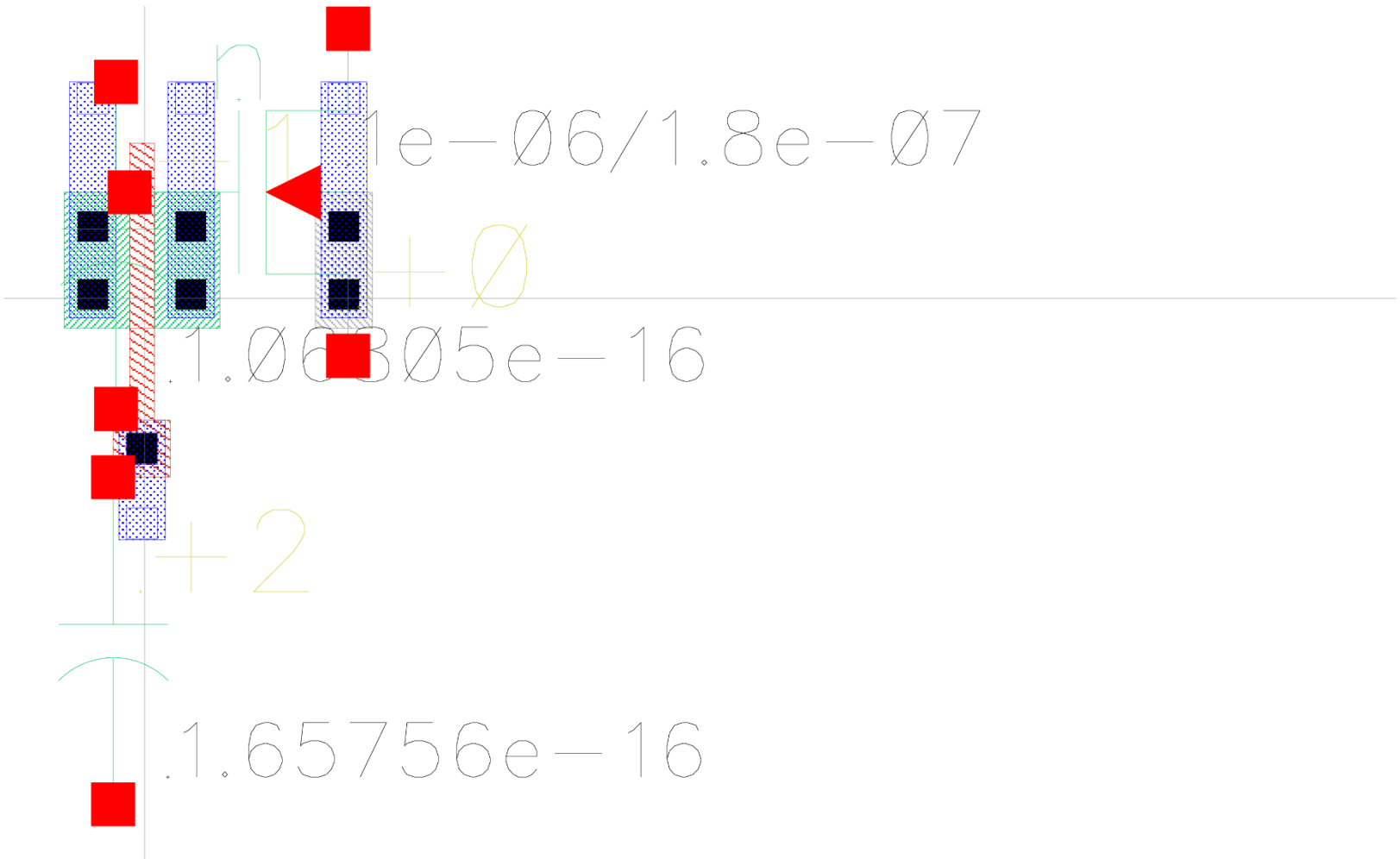
5. The layout and extended views of your NMOS transistor.




B
S
G
D

USER: tpano
DATE: Thu Oct 7 02:31:04 2021
PLOT SIZE: 6.74 x 10.98 Inches
Magnification: 27389.47X
Library: lab1
Cell: nmos
View: extracted
Plot Area: ((-1.03 -4.11) (9.17 12.14))




1e-06/1.8e-07
0
1.06305e-16
2
1.65756e-16

6. The family of I-V characteristic waveforms of the schematic and extracted NMOS transistor.