Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Outline (F2020)

ELE734: Low-Power Digital Integrated Circuits

This year classes will be delivered virtually through Zoom. Please follow the following regulations with regards to the virtually delivered classes:

1. Zoom link for each class would be shared on D2L prior to the class;
2. Zoom link should not be shared with others;
3. Video accessed via Zoom should not be recorded, for voice or video; without prior permission;

Please note the following for the Midterm and the Final Exam:

1. Online exam(s) within this course may use a virtual proctoring system. Please note that your completion of the exam may be recorded via the virtual platform and subsequently reviewed by your instructor. The virtual proctoring system provides recording of flags where possible indications of suspicious behaviour are identified only. Recordings will be held for a limited period of time in order to ensure academic integrity is maintained.
2. Access to a computer that can support remote recording is your responsibility as a student. The computer should have the latest operating system, at a minimum Windows (10, 8, 7) or Mac (OS X 10.10 or higher) and web browser Google Chrome or Mozilla Firefox. You will need to ensure that you can complete the exam using a reliable computer with a webcam and microphone available, as well as a high-speed internet connection. Please note that you will be required to show your Ryerson OneCard prior to beginning to write the exam. In cases where you do not have a Ryerson OneCard, government issued ID is permitted.
3. Information will be provided prior to the exam date by your instructor who may provide an opportunity to test your set-up or provide additional information about online proctoring. Since videos of you and your environment will be recorded while writing the exam, please consider preparing the background (room / walls) so that personal details are not visible, or move to a room that you are comfortable showing on camera.

Instructor	Dr. Andy Ye Office: ENG319 Phone: 416-979-5000 ext: 4901 E-mail: aye@ee.ryerson.ca Office Hours: TBD
Calendar Description	This course deals with the design of Digital CMOS integrated circuits. The course consists of three essential components: Theory, Laboratory, and project. Variety of design techniques, such as Static CMOS, Dynamic CMOS, and Transmission Gate are discussed in theory. These designs are studied on basic logic gates as well as combinational and sequential circuits. The lessons learned are applied to arithmetic building blocks such as adders, multipliers, and memory elements. A MOS transistor is studied using I-V equations, and the different areas of operations are modeled. The static (DC) are dynamic (transient) behaviors for an important building block, a CMOS inverter, are studied in depth.

Prerequisites	*COE538*
Compulsory Text(s):	1. *CMOS VLSI Design: A Circuit and Systems Perspective*, Neil H. E. Weste and David Harris, 4nd edition, Addison Wesley, 2010. 2. *ELE734 Low Power Digital Integrated Circuits Laboratory Manual,* by Adnan Kabbani and Tarek Khan
Reference Text(s)	
Learning Objectives (Indicators)	At the end of this course, the successful student will be able to: 1. Develop good understanding of the appropriate level of modeling used in VLSI design for area, performance and power optimization. (1c) 2. Use technical knowledge including CMOS layout, delay, and power estimation techniques to design reliable, high performance, and low power CMOS digital circuits and systems. (4a) 3. Apply the CMOS digital circuit design principles to define an accurate CMOS design problem statement. Recognize that good problem definition assists the CMOS design process. Describe differences between the various approaches that can be used to solve a CMOS digital circuit design problem. Select one specific approach to solve the problem. When the selected approach fails to solve the problem satisfactorily, analyze the cause of failure using the principles of CMOS digital circuit design. Based on the analysis, come up with new suggestions to improve the existing approach. Integrate the new suggestions into the existing design plan. Judge the completeness and quality of the generated solutions based on the principles of CMOS digital circuit design. (4b) 4. Use Cadence Tools to Implement CMOS digital circuit design and obtained experimental results. (5a) **NOTE**: *Numbers in parentheses refer to the graduate attributes required by the Canadian Engineering Accreditation Board (CEAB).*
Course Organization	3 hours of lecture per week for 13 weeks, in 1 section 2 hours of lab/tutorial per week for 13 weeks 7 Lab/tutorial sections of maximum 25 students each 2 Teaching Assistants, 3-4 sections per TA
Teaching Assistants	
Course Evaluation	Midterm Exam 25 % Lab 1 10 % Lab 2 7 % Lab 3 10 % Lab 4 8% Final Exam 40 % **TOTAL**: 100 %
Examinations	Midterm exam in Week 8, 1.5 hours, closed book (covers Weeks 1-6 of lecture and laboratory material – Chapters 1, 2, and 4). Final exam, during exam period, 3 hours, closed book (covers all the course material).

Other Evaluation and/or Information	• The mid-term test and final examination will be closed book. • In order to achieve a passing grade in this course, the student must achieve an average of at least 50% in both theoretical and laboratory components. • The written reports will be assessed not only on their technical or academic merit, but also on the communication skills of the author as exhibited through the reports.

Course Content and Laboratory/Tutorials

Week	Lecture Topic, description	Laboratory/Tutorials (ENG 412)
1 (Sep 7–13)	Chapter 1- Introduction (Sections 1.1, 1.3, 1.4, 1.5)	No Lab
2 (Sep 14–20)	Chapter 1- Introduction (Section 1.5) Chapter 2- MOS Transistor Theory (Sections 2.1, 2.2)	Characteristics of MOSFET Devices
3 (Sep 21–27)	Chapter 2- MOS Transistor Theory (Sections 2.5, 2.3, 2.4)	
4 (Sep 28–4)	Chapter 4- Delay (4.1, 4.2, 4.3, 4.4)	
5 (Oct 5–11)	***Week of Thanksgiving Monday: No Class and No Labs***	No Labs
6 (Oct 12–18)	Chapter 4- Delay (4.5) Chapter 5- Power (5.1)	CMOS Inverter Design
7 (Oct 19–25)	Chapter 5- Power (5.2, 5.3)	
8 (Oct 26–1)	***Midterm on November 1st during class hours***	CMOS Logic Families
9 (Nov 2–8)	Chapter 5- Power (5.3) Chapter 6- Interconnect (6.1, 6.2, 6.3, 6.4)	
10 (Nov 9–15)	Chapter 6- Interconnect (6.4) Chapter 8- Circuit Simulation (8.1, 8.2, 8.3, 8.4) Chapter 9- Combinational Circuit Design (9.1, 9.2)	
11 (Nov 16–22)	Chapter 9- Combinational Circuit Design (9.2)	1-bit CMOS Full Adder
12 (Nov 23–29)	Chapter 11- Datapath Subsystems (11.1, 11.2)	
13 (Nov 30–6)	Babbage Difference Engine – Carry Skip Adder Chapter 10- Sequential Circuit Design (10.1, 10.3, 10.2, 10.6)	

Important Notes

1. All of the required course-specific written reports will be assessed not only on their technical/academic merit, but also on the communication skills exhibited through these reports.

2. All assignment and lab/tutorial reports must have the standard cover page which must be signed by the student(s) prior to submission of the work. Submissions without the cover page **will not** be accepted. The cover page can be found on the departmental web site: Standard Assignment/Lab Cover Page

3. Should a student miss a mid-term test or equivalent (e.g. studio or presentation), with appropriate documentation, a make-up assessment ***may*** be scheduled. Alternatively, the weight of the missed work is placed on the final exam, or another single assessment. This may not cause that exam or assessment to be worth more than 70% of the student's final grade. If a student misses a scheduled make-up test or exam, the grade may be distributed over other course assessments even if that makes the grade on the final exam worth more than 70% of the final grade in the course. Make-up assessments cover the same material as the original assessment but need not be of an identical format.

4. Students who miss a final exam for a verifiable reason and who cannot be given a make-up exam prior to the submission of final course grades, must be given a grade of INC (as outlined in the *Grading Promotion and Academic Standing Policy)* and a make-up exam (normally within 2 weeks of the beginning of the next semester) that carries the same weight and measures the same knowledge, must be scheduled.

5. Medical or Compassionate documents for the missing of an exam must be submitted within 3 working days of the exam. Students are responsible for notifying the instructor that they will be missing an exam as soon as possible.

6. **If a student is requesting accommodation due to a religious, aboriginal and/or spiritual observance, he or she must submit a Request for Accommodation of Student Religious, Aboriginal, and Spiritual**

Observance AND an Academic Consideration form within the FIRST TWO WEEKS OF CLASS or, for a final examination, within two weeks of the posting of the examination schedule. If the required absence occurs within the first two weeks of classes, or the dates are not known well in advance as they are linked to other conditions, these forms should be submitted with as much lead time as possible in advance of the required absence.
Both documents are available at http://www.ryerson.ca/senate/forms/relobservforminstr.pdf. Full-time or part-time degree students must submit the forms to their own program department or school.

7. The results of the first test or mid-term exam will be returned to students before the deadline to drop an undergraduate course in good Academic Standing.

8. Students are required to adhere to all relevant University policies including:
   - Undergraduate Grading, Promotion and Academic Standing: http://www.ryerson.ca/senate/policies/pol46.pdf
   - Student Code of Academic Conduct: http://www.ryerson.ca/senate/policies/pol60.pdf
   - Student Code of Non-Academic Conduct: http://www.ryerson.ca/senate/policies/pol61.pdf
   - Undergraduate Academic Consideration and Appeals: http://www.ryerson.ca/senate/policies/pol134.pdf
   - Examination Policy: http://www.ryerson.ca/senate/policies/pol135.pdf
   - Course Management Policy: http://www.ryerson.ca/senate/policies/pol145.pdf
   - Accommodation of Student Religious, Aboriginal and Spiritual Observance: http://www.ryerson.ca/senate/policies/pol150.pdf
   - Establishment of Student E-mail Accounts for Official University Communication: http://www.ryerson.ca/senate/policies/pol157.pdf

9. Students are required to obtain and maintain a Ryerson e-mail account for timely communications between the instructor and the students.

10. Any changes in the course outline, test dates, marking or evaluation will be discussed in class prior to being implemented.

11. Assignments, projects, reports and other deadline-bound course assessment components handed in past the due date will receive a mark of ZERO. Marking information will be made available at the time when such course assessment components are announced.

12. If you have taken the course previously and are currently looking to get a laboratory exemption, then you must fill out this form: http://www.ee.ryerson.ca/guides/ECE-LabExemptionForm.pdf

Approved by: _____ Date _____
Course Instructor

Approved by: _____ Date _____
Associate Chair or Program Director