Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	Low Power Digital Integrated Circuits
Course Number:	ELE 734
Semester/Year (e.g.F2016)	F2021

Instructor:	Andy Ye

Assignment/Lab Number:	1
Assignment/Lab Title:	Characteristics of MOSFET Devices

Submission Date:	October 12, 2021
Due Date:	October 12, 2021

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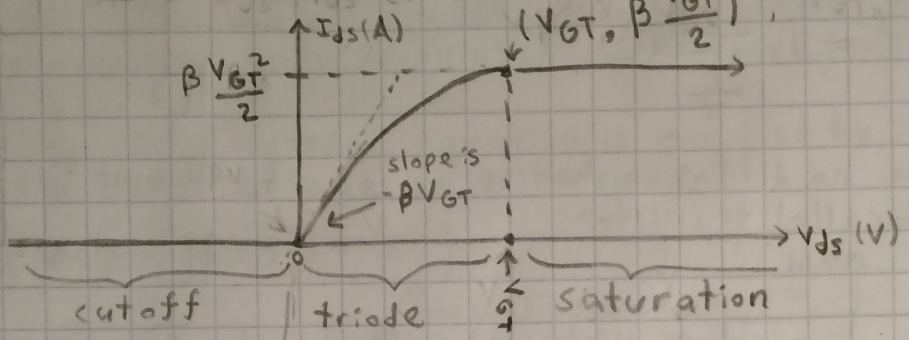
Lab 1 Prelab

NMOS I_{ds}-V_{ds} Curve

2.



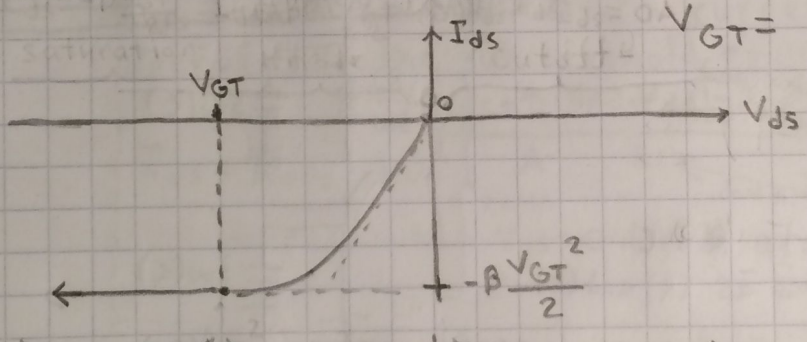
cutoff: $I_{ds} = 0A$ (if $V_{gs} < V_{tn}$)

triode: $I_{ds} = \beta(V_{GT} - \frac{V_{ds}}{2})V_{ds}$ (if $V_{tn} < V_{gs}$) (if $V_{ds} < V_{GT}$)

saturation: $I_{ds} = \beta\frac{V_{GT}^2}{2}$ (if $V_{tn} < V_{gs}$) (if $V_{GT} < V_{ds}$)

$V_{GT} = V_{gs} - V_{tn}$

PMOS I_{ds}-V_{ds} Curve



$V_{GT} =$

saturation: $I_{ds} = -\beta\frac{V_{GT}^2}{2}$ (if $V_{gs} < V_{tp}$) (if $V_{ds} < V_{GT}$)

triode: $I_{ds} = \beta(\frac{V_{ds}}{2} + V_{GT})V_{ds}$ (if $V_{gs} < V_{tp}$) (if $V_{GT} < V_{ds}$)

cutoff: $I_{ds} = 0A$ (if $V_{tp} < V_{gs}$)

$V_{GT} = V_{gs} - V_{tp}$

3. $V_t = V_{to} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right) - \eta V_{ds}$

γ: body effect; η: drain induced barrier lowering (DIBL)

$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2 q_e \varepsilon_{si} N_A}$, $\phi_s = 2 V_T \ln\left(\frac{N_A}{N_i}\right)$

The nominal threshold voltage, V_t, will increase as V_{sb} increases, and will decrease as V_{sb} decreases.

4. Channel-length modulation (CLM) occurs when changes in V_{ds} affect the length of the channel between the drain and the source. In triode and saturation mode, the drain and base form a diode in reverse bias mode. The diode's depletion region increases when V_{ds} increases, which decreases the channel length.

The drain current equation is modified by including the Early Voltage as a term (V_A).

$$I_{ds} = \frac{\beta}{2} V_{GT}^2 \left(1 + \frac{V_{ds}}{V_A}\right)$$

The effects of CLM are more important in short-channel devices than they are for long-channel devices.

5. Subthreshold conduction is current flow between the drain and source of a MOS transistor when it is in cutoff mode (i.e. off, $V_{gs} < V_{tn}$ for NMOS and $V_{gs} > V_{tp}$ for PMOS)

The expression for drain current when the transistor operates in the subthreshold region is:

$$I_{ds} = \underbrace{I_{off}}_{\text{current when } V_{gs}=0V \text{ and } V_{ds}=V_{DD}} \cdot 10^{\left(\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k_\gamma V_{sb}}{S}\right)} \cdot \left(1 - e^{-\left(\frac{V_{ds}}{V_T}\right)}\right)$$

S = subthreshold slope $= \left[\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right]^{-1} = nV_T \ln(10)$

↑ amount V_{gs} must drop to reduce I_{ds} by factor of 10

6.