Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	Low Power Digital Integrated Circuits
Course Number:	ELE 734
Semester/Year (e.g.F2016)	F2021

Instructor:	Andy Ye

Assignment/Lab Number:	2
Assignment/Lab Title:	CMOS Inverter

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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

Lab Report for Lab 2

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1. Schematic of the CMOS Inverter

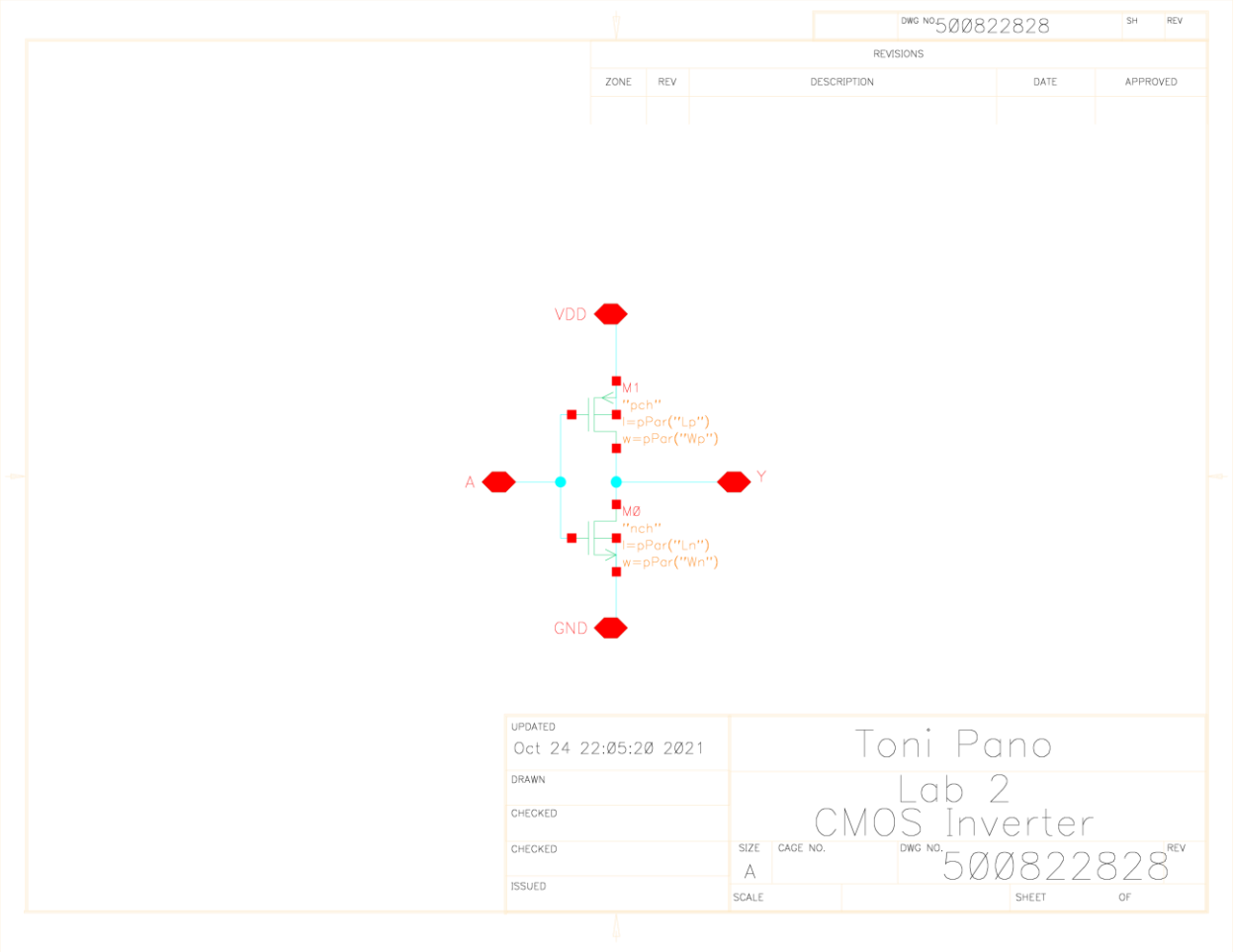

Figure 1.1. Schematic of the CMOS Inverter.

2. Schematic of the Testbench

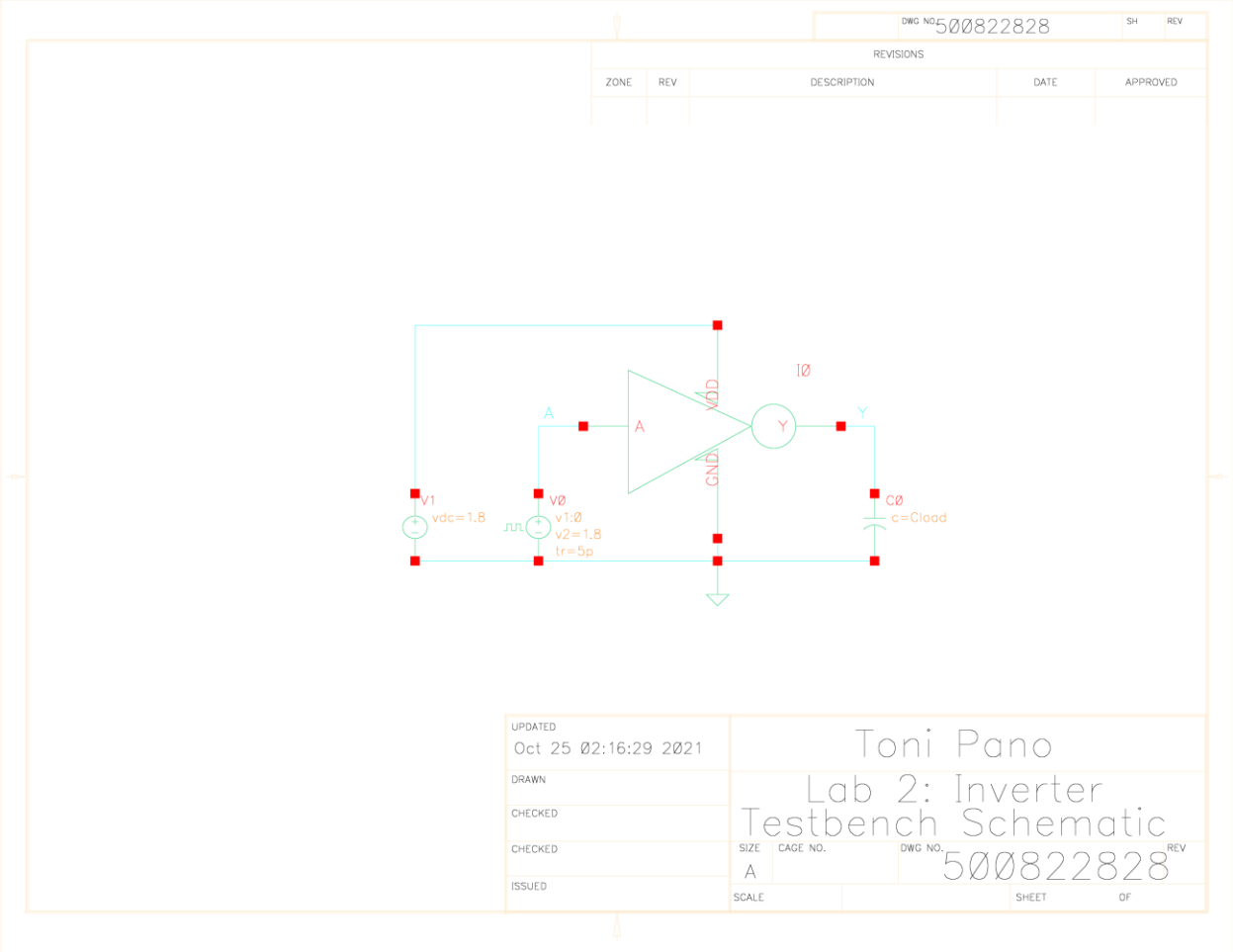

Figure 2.1. Schematic of the CMOS Inverter Testbench.

3. Results of the Static and Dynamic CMOS Inverter Simulations

a. Static Analysis

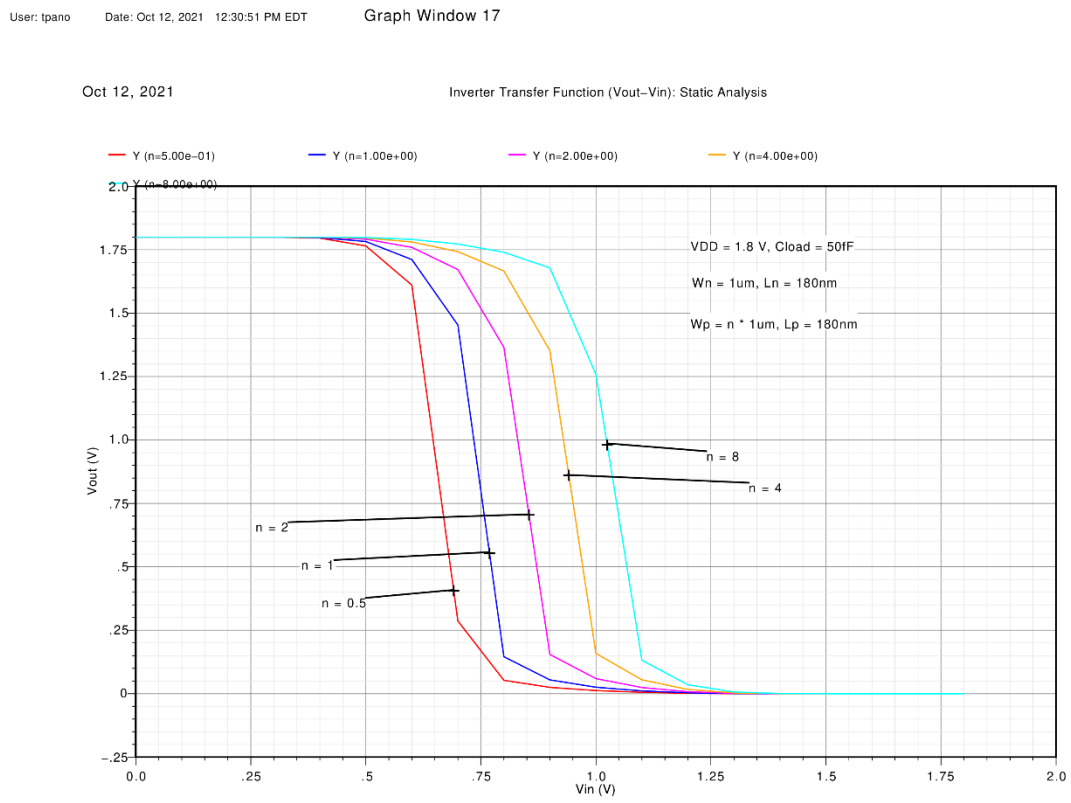

Figure 3.A.1. The transfer function of the inverter's input and output voltages for different values of the PMOS transistor width (n) in micrometers.

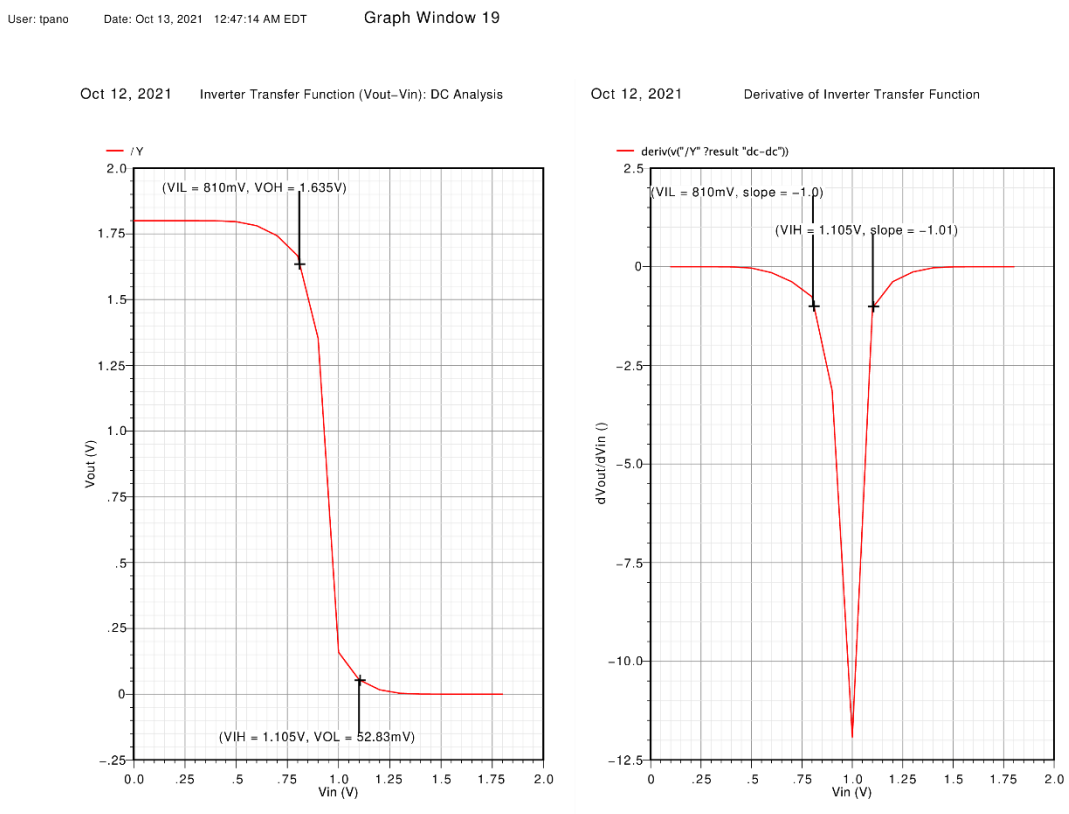

Figure 3.A.2. The location of the VIL, VIH, VOL and VOH noise margins boundaries. These boundaries are defined where the transfer function has a slope of -1.

b. Dynamic Analysis

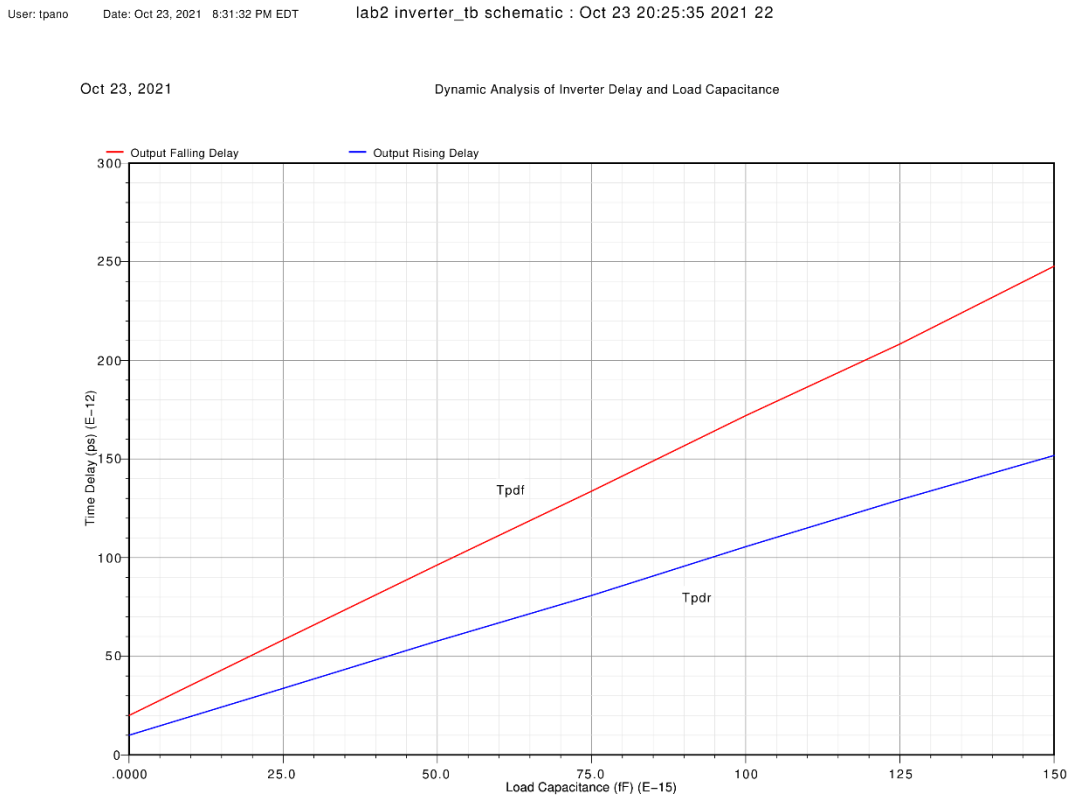

Figure 3.B.1. The falling (Tpdf) and rising (Tpdr) delay of the inverter when different capacitance loads are applied to the inverter's output.

4. Layout and Extracted Views of the CMOS Inverter

a. Layout View

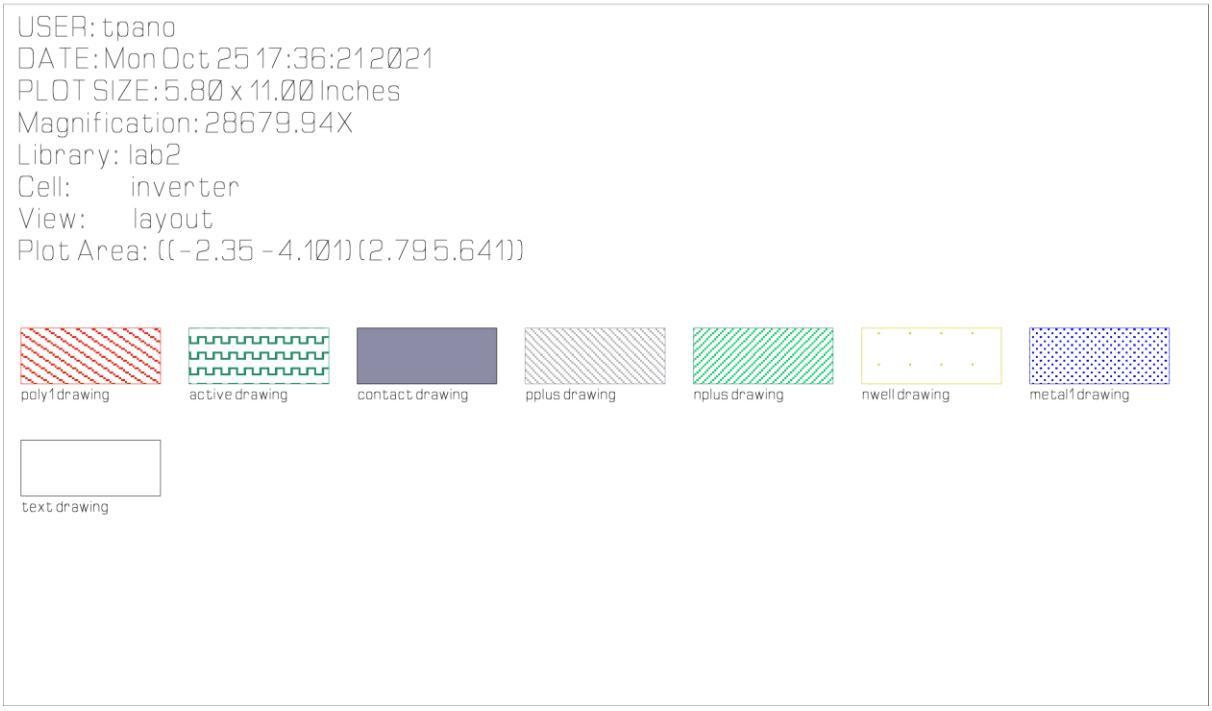

Figure 4.A.1. Legend for Layout view.

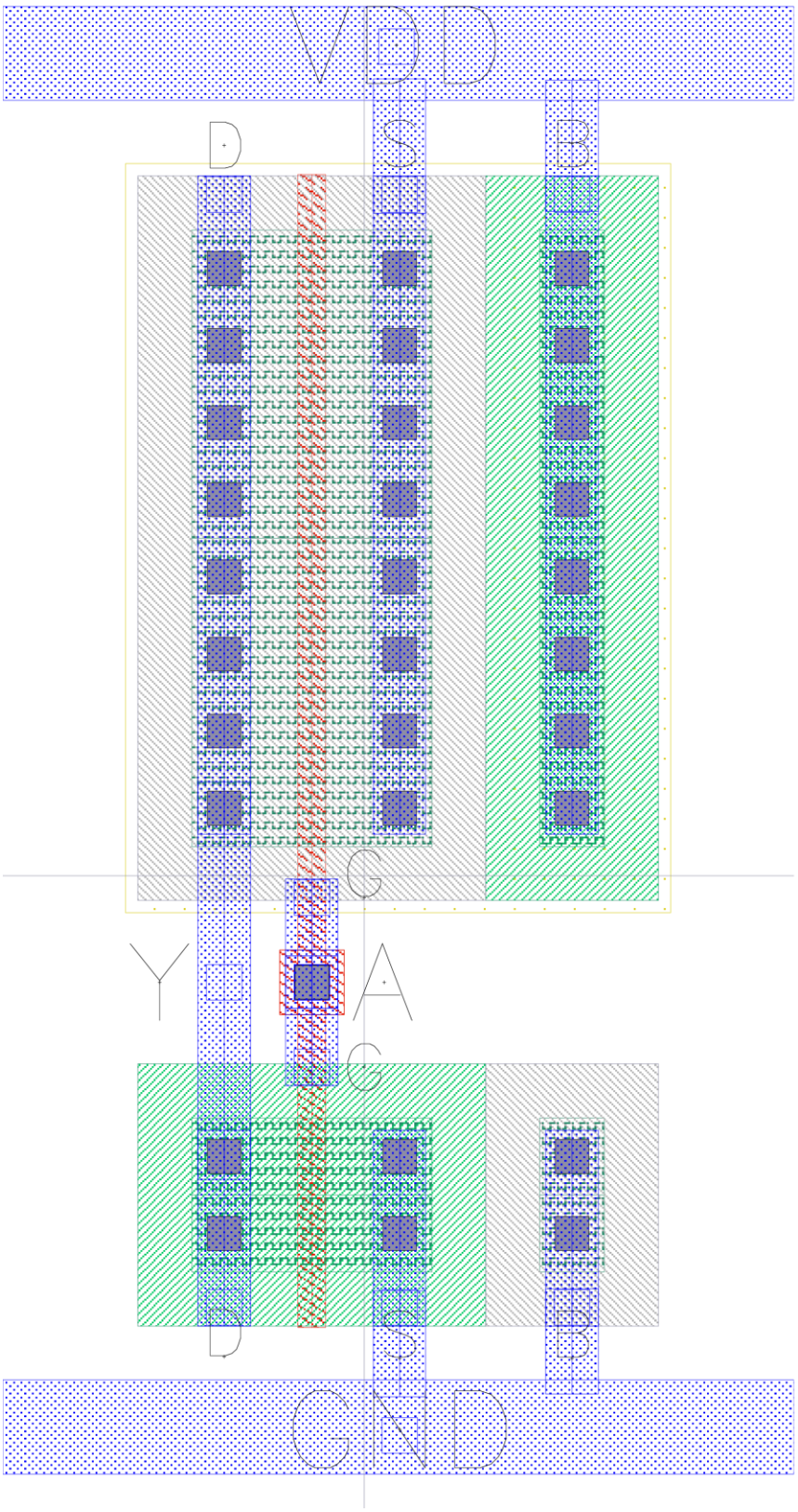

Figure 4.A.2. Layout of CMOS Inverter.

b. Extracted View

Figure 4.B.1. Legend for Extracted view.

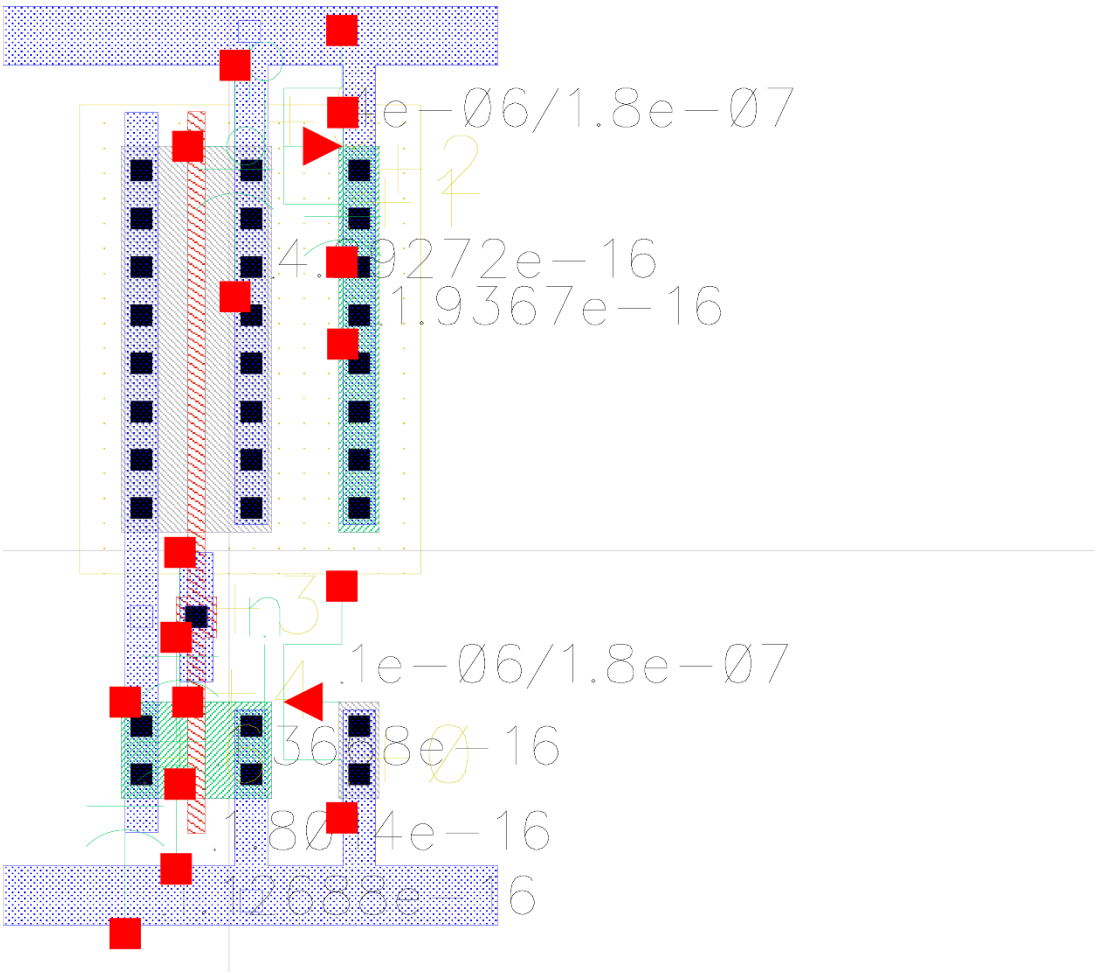

Figure 4.B.2. Extracted capacitance parameters from Layout of CMOS Inverter.

5. Post-Layout Simulation Results

a. Schematic of the Testbench

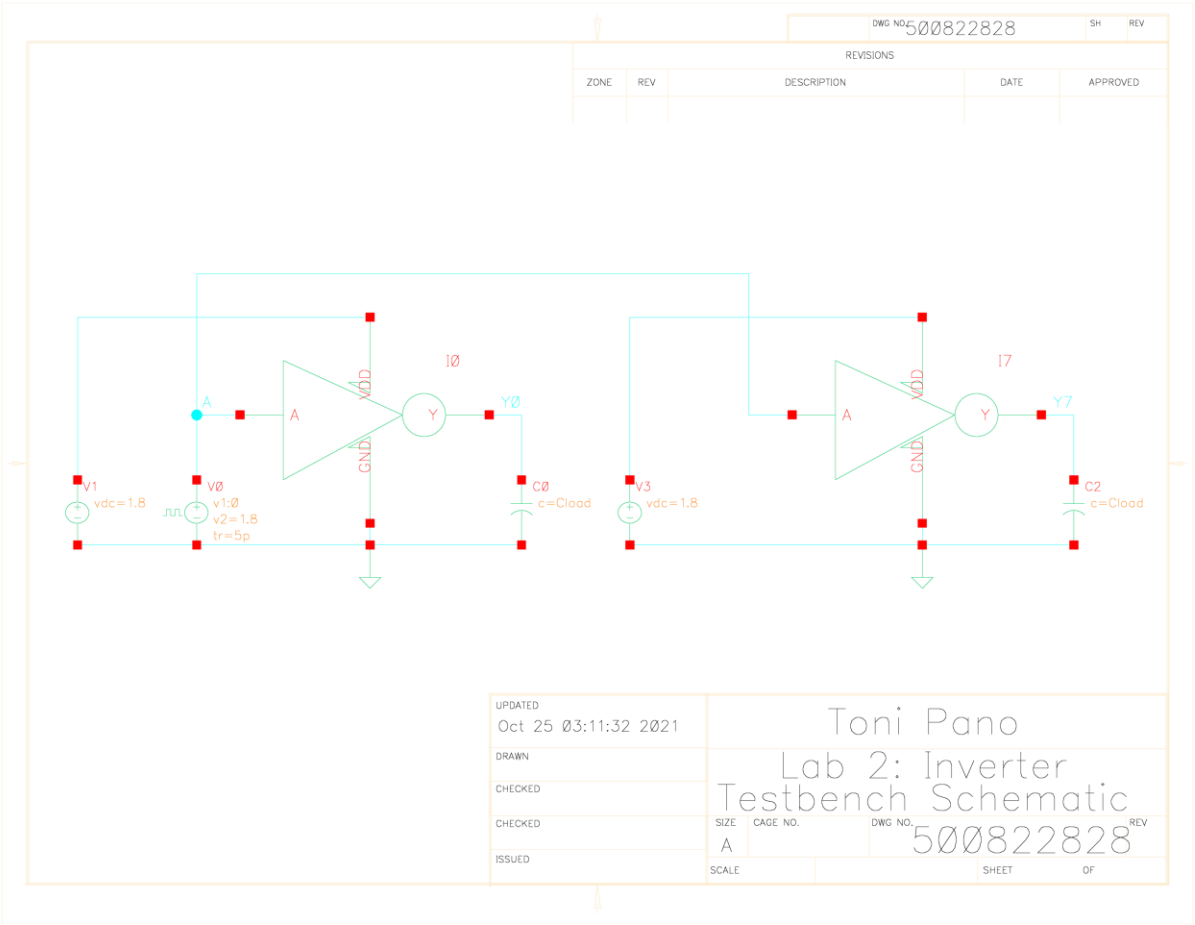

Figure 5.A.1. Schematic of the testbench for comparing the default schematic behaviour and extracted layout behaviour in the same simulation.

b. Results of the CMOS Inverter Static Analysis Simulations

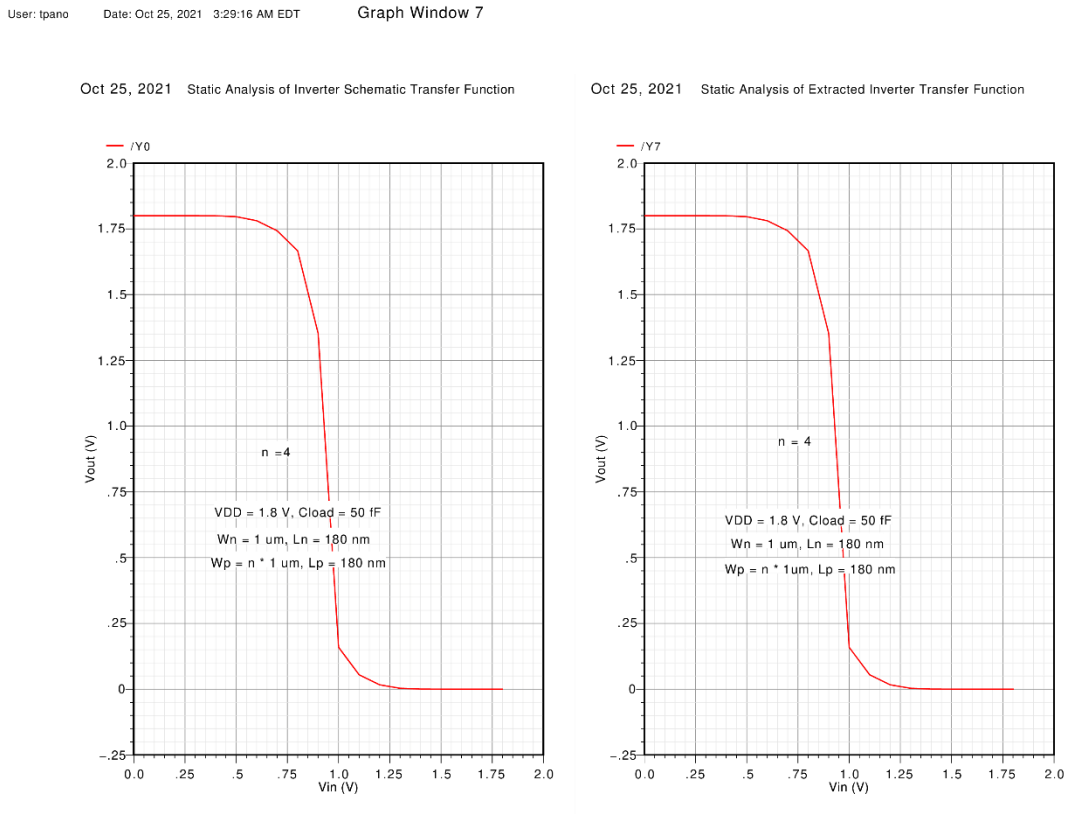

Figure 5.B.1. The inverter transfer function for n = 4 (PMOS width is 4um). The behaviour from the default schematic is on the left (Y0), and from the extracted layout behaviour is on the right (Y7).

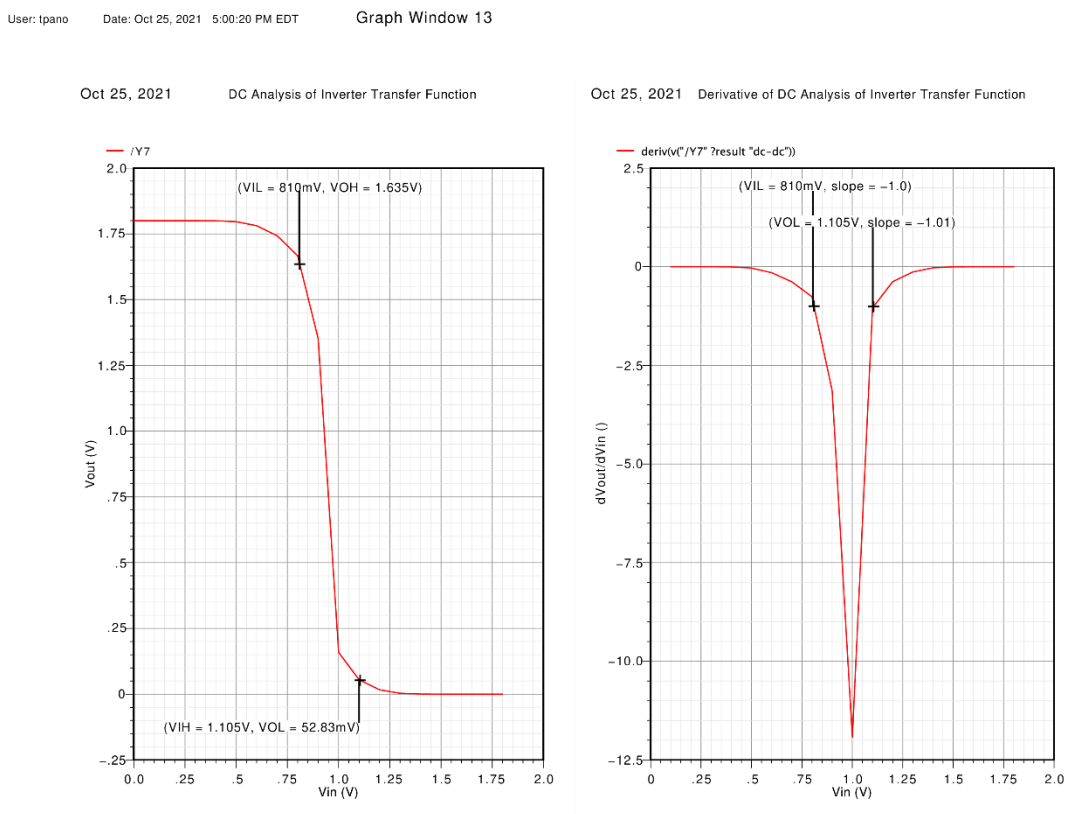

Figure 5.B.2. The location of the VIL, VIH, VOL and VOH noise margins boundaries on the extracted layout inverter's transfer function (Y7). These boundaries are defined where the transfer function has a slope of -1.

c. Results of the CMOS Inverter Dynamic Analysis Simulations

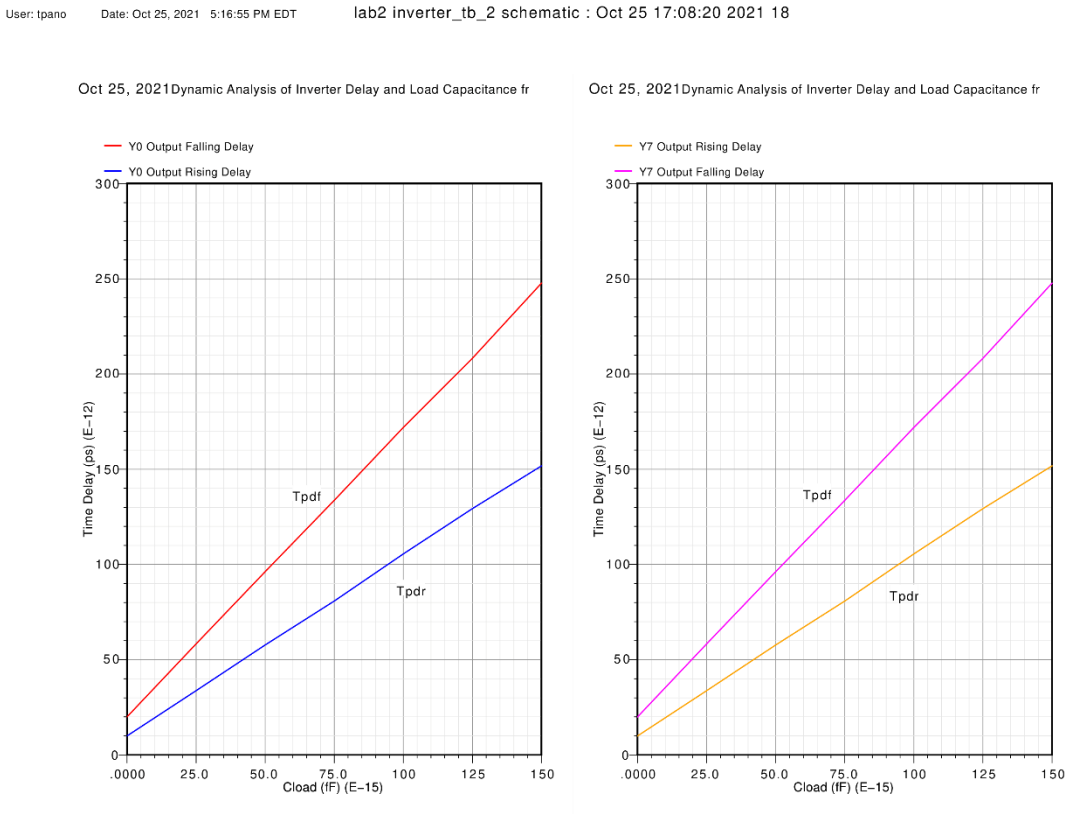

Figure 5.C.1. The inverter falling delay (Tpdf) and rising delay (Tpdr) for different load capacitances. The behaviour from the default schematic is on the left (Y0), and from the extracted layout behaviour is on the right (Y7).

6. Summary of Results

The results show that the CMOS Inverter's transfer curve (from the schematic) has VM = VDD/2 when n is between 2 and 4. If n = 4, then the available slopes on the derivative of the transfer function come closest to -1 when Vin = 810mV, and when Vin = 1.105V. This determines the noise margin boundaries as VIL = 810mV, VIH = 1.105V, VOL = 52.83mV, and VOH = 1.635V. The falling and rising delay from the schematic behaviour of the CMOS inverter shows both delays increasing as the load capacitance increases, however the falling delay is always greater than the rising delay.

The only deviation from the prelab was using 1.8V for VDD in the lab, instead of 5V for VDD as used in the prelab.

The behaviour of the CMOS inverter from the schematic and extracted layout match's each other's graphs. The transfer functions, transfer function slopes, falling delay and rising delay look very similar to each other.

Sizing the PMOS twice as wide as the NMOS (by setting n = 2) would only have set VM = VDD/2 if the ratio of the beta terms in the drain to source current were twice as big for NMOS than PMOS. Because the beta terms include the mobility of electrons in silicon (for NMOS), and the mobility of holes for silicon (in PMOS), this meant that the mobility of electrons should have been twice the mobility of holes in silicon. However, this assumption is a rough estimate of the actual mobility values in silicon. Measured experimental values [1] indicate that the ratio of the mobility of electrons to holes in silicon is closer to 3.1 (1400 $cm^2 V^{-1}s^{-1}$/ 450 $cm^2 V^{-1}s^{-1}$). This explains why VM = VDD/2 for values of n between 2 and 4, and not n =2, as observed in the transfer functions from the lab results.

References

[1] Mobility values in silicon: http://www.ioffe.ru/SVA/NSM/Semicond/Si/electric.html#Basic