

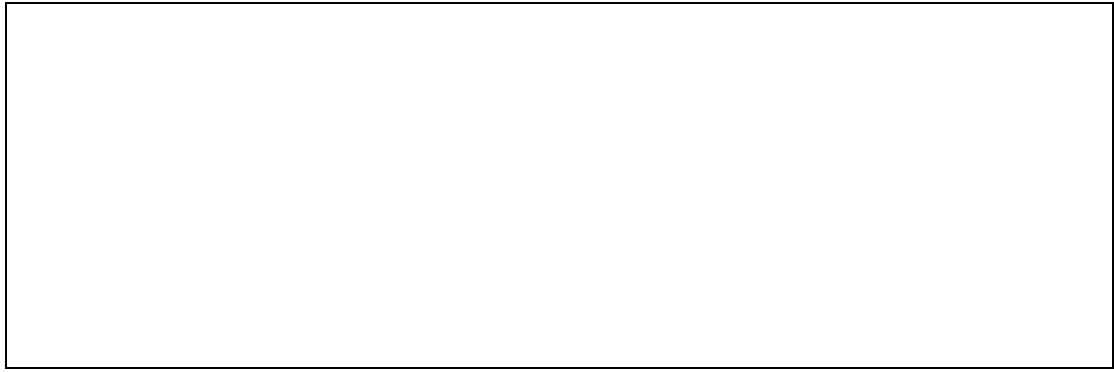


## 2023 Digital IC Design Homework 3

NAME	鄭旻軒		
Student ID	P76111628		
Simulation Result			
Functional simulation	100	Gate-level simulation	100
<pre># Expected answer: 9   get: 9 --&gt; Pass # Pattern 59 : ((1-1)^(c-a)+3-l= # Expected answer: 2   get: 2 --&gt; Pass # Pattern 60 : ((2-1)^(c-a))= # Expected answer: 2   get: 2 --&gt; Pass  #  #  #  # </pre>  <p>Congratulations!!! You past all patterns! Your score is 100. Total use 2248 cycles to complete simulation.</p> <pre>** Note: \$finish      : C:/Users/Tonr01/Verilog_HW/Verilog_HW3/RTL category/testfixture.sv(190) # Time: 26976 ns Iteration: 1 Instance: /testfixture # 1 # Break in Module testfixture at C:/Users/Tonr01/Verilog_HW/Verilog_HW3/RTL category/testfixture.sv line 190</pre>		<pre># Expected answer: 2   get: 2 --&gt; Pass # Pattern 60 : ((2-1)^(c-a))= # Expected answer: 2   get: 2 --&gt; Pass  #  #  #  # </pre>  <p>Congratulations!!! You past all patterns! Your score is 100. Total use 2248 cycles to complete simulation.</p> <pre>** Note: \$finish      : C:/Users/Tonr01/Verilog_HW/Verilog_HW3/RTL category/testfixture.sv(190) # Time: 26976 ns Iteration: 1 Instance: /testfixture</pre>	
Synthesis Result			
Total logic elements	720		
Total memory bits	0		
Embedded multiplier 9-bit elements	1		
Total cycle used	2248		
Clock width	12		
<p>我主要分成 5 個 state 來完成，In_Data 主要用於控制 state 的轉換</p> <p>State 0: 主要是一些變數的初始化</p> <p>State 1: 主要是將輸入的 ascii code 用陣列 temp 來儲存，我直接將 ascii code 轉成對應數字，所以 temp 可以只用 6 bits</p> <p>State 2: 將陣列 temp 的值轉換成 postfix，再存到陣列 postfix 中，步驟跟作業提供一樣</p> <p>State 3: 主要做後序的計算，步驟跟作業提供一樣</p> <p>State 4: 輸出答案，我將 stack pointer top 初始值設成 0 為空，所以 stack 剩下的最後一個值會在 top == 1 時</p>			
Description of your design			



*Scoring = Area cost \* Timing cost*

*Area cost = Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used \* Clock width*

**\* Total logic elements must not exceed 1500.**