2023 Digital IC Design Homework 3

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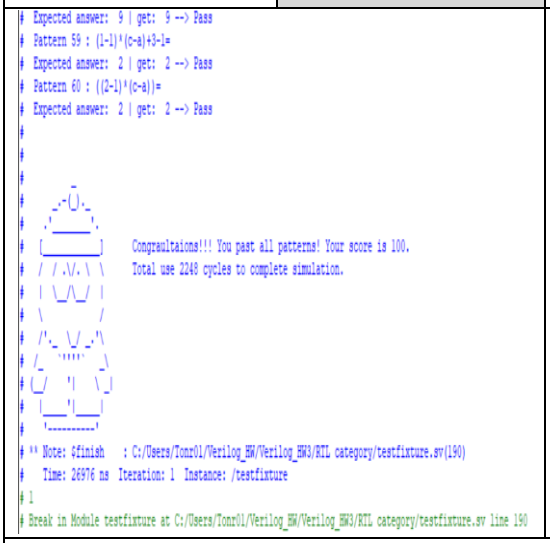
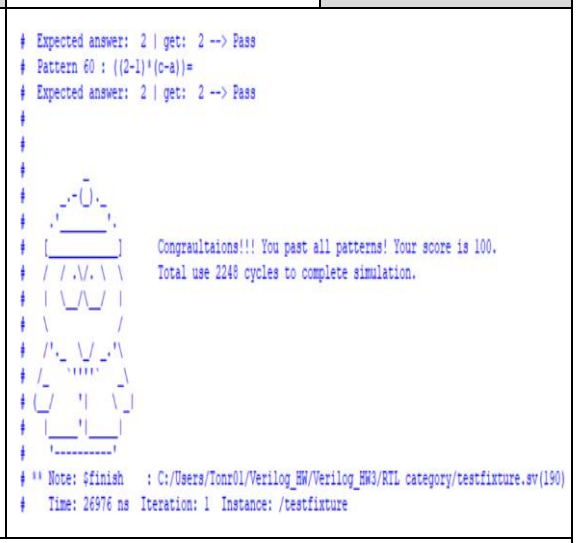
Simulation Result

Functional simulation	100	Gate-level simulation	100





Synthesis Result

Total logic elements	720
Total memory bits	0
Embedded multiplier 9-bit elements	1
Total cycle used	2248
Clock width	12

我主要分成 5 個 state 來完成， In_Data 主要用於控制 state 的轉換

State 0: 主要是一些變數的初始化

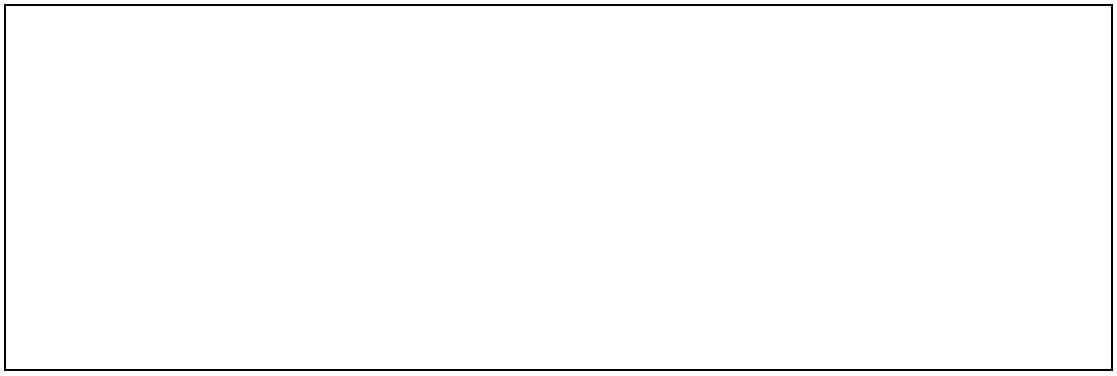
State 1: 主要是將輸入的 ascii code 用陣列 temp 來儲存，我直接將 ascii code 轉成對應數字，所以 temp 可以只用 6 bits

State 2: 將陣列 temp 的值轉換成 postfix，再存到陣列 postfix 中，步驟跟作業提供一樣

State 3: 主要做後序的計算，步驟跟作業提供一樣

State 4: 輸出答案，我將 stack pointer top 初始值設成 0 為空，所以 stack 剩下的最後一個值會在 top == 1 時

Description of your design



*Scoring = Area cost * Timing cost*

*Area cost = Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used * Clock width*

*** Total logic elements must not exceed 1500.**