

2023 Digital IC Design Homework 5

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Simulation Result			
Functional simulation	Completed	Gate-level simulation	Completed
<pre>VSDM 26> run -all ===== ** Simulation Start ** ===== ** Simulation completed successfully! ** ===== # Note: \$finish : C:/Users/Tom01/Verilog_HW/Verilog_HW5/RTL category/testfixture.v(145) # Time: 12721900 ns Iteration: 1 Instance: /testfixture # 1 # Break in Module testfixture at C:/Users/Tom01/Verilog_HW/Verilog_HW5/RTL category/testfixture.v line 145</pre>		<pre>VSDM 27> run -all ===== ** Simulation Start ** ===== ** Simulation completed successfully! ** ===== # Note: \$finish : C:/Users/Tom01/Verilog_HW/Verilog_HW5/RTL category/testfixture.v(145) # Time: 12721900 ns Iteration: 1 Instance: /testfixture # 1 # Break in Module testfixture at C:/Users/Tom01/Verilog_HW/Verilog_HW5/RTL category/testfixture.v line 145</pre>	
Evaluation Results			
test1.png	25.32	test2.png	24.82
test3.png	29.12	test4.png	20.95
test5.png	21.94	test6.png	25.21
Description of your design			
<p>我分成 6 個步驟，分別是 READDATA, COLOR, STORE9, BILINEAR, WRITEDATA, FINISH</p> <p>READDATA: 我把 input 分別暫存到三個 memory 裡面</p> <p>COLOR: 這裡主要用來決定現在的 bilinear interpolation 的 case，0~3 分別對應到題目提供的 a~d</p> <p>STORE9: 再來宣告大小為 9 的陣列 data，用來存現階段所需的 4 個 case 的九宮格的值，因為我用三個 memory 去暫存輸入資料，九宮格 0~4 可能會因為更新後的值會跟輸入不同而導致錯誤，所以會根據目前的顏色去對應的 memory 取值，九宮格的取值方法跟作業四助教提供的方法一樣，用 x, y 軸去當坐標取值</p> <p>BILINEAR: 做 bilinear interpolation</p> <p>WRITEDATA: 寫值到三個 memory 中</p> <p>FINISH: 將 done 設成 1</p> <p>最後花了 12721900 ns，end cycle 要設大一點</p>			

Scoring = average PSNR of the six test images

*** PSNR of all interpolation results should meet at least the baseline.**