Semiconductor Manufacturing Technology

Chapter 3

Device Technologies

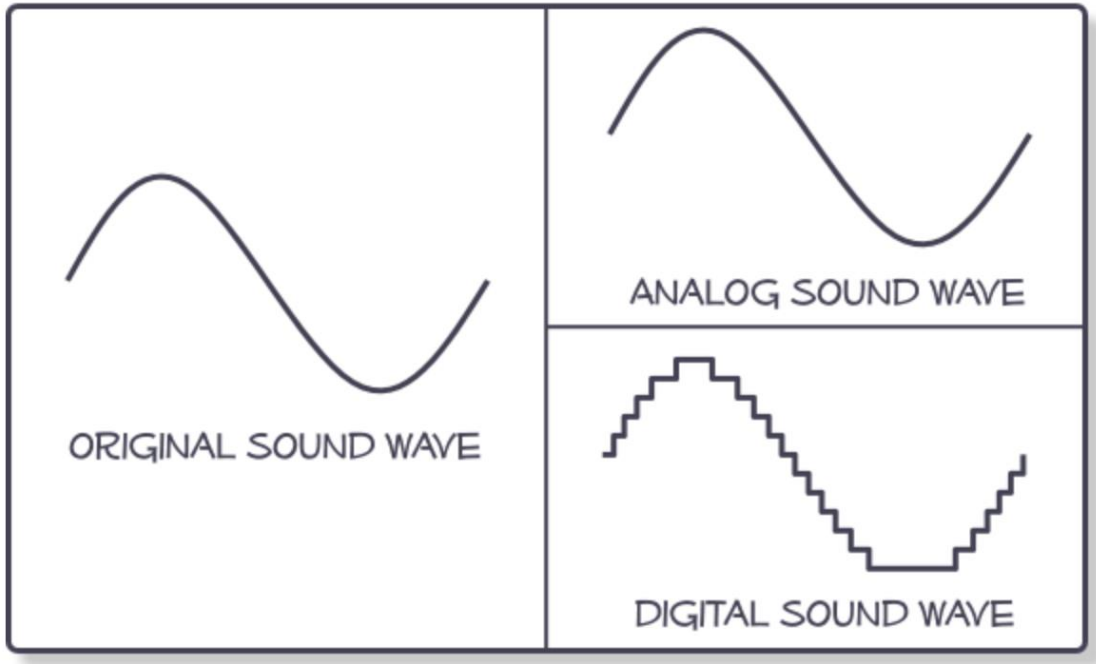
Objectives

After studying the material in this chapter, you will be able to:

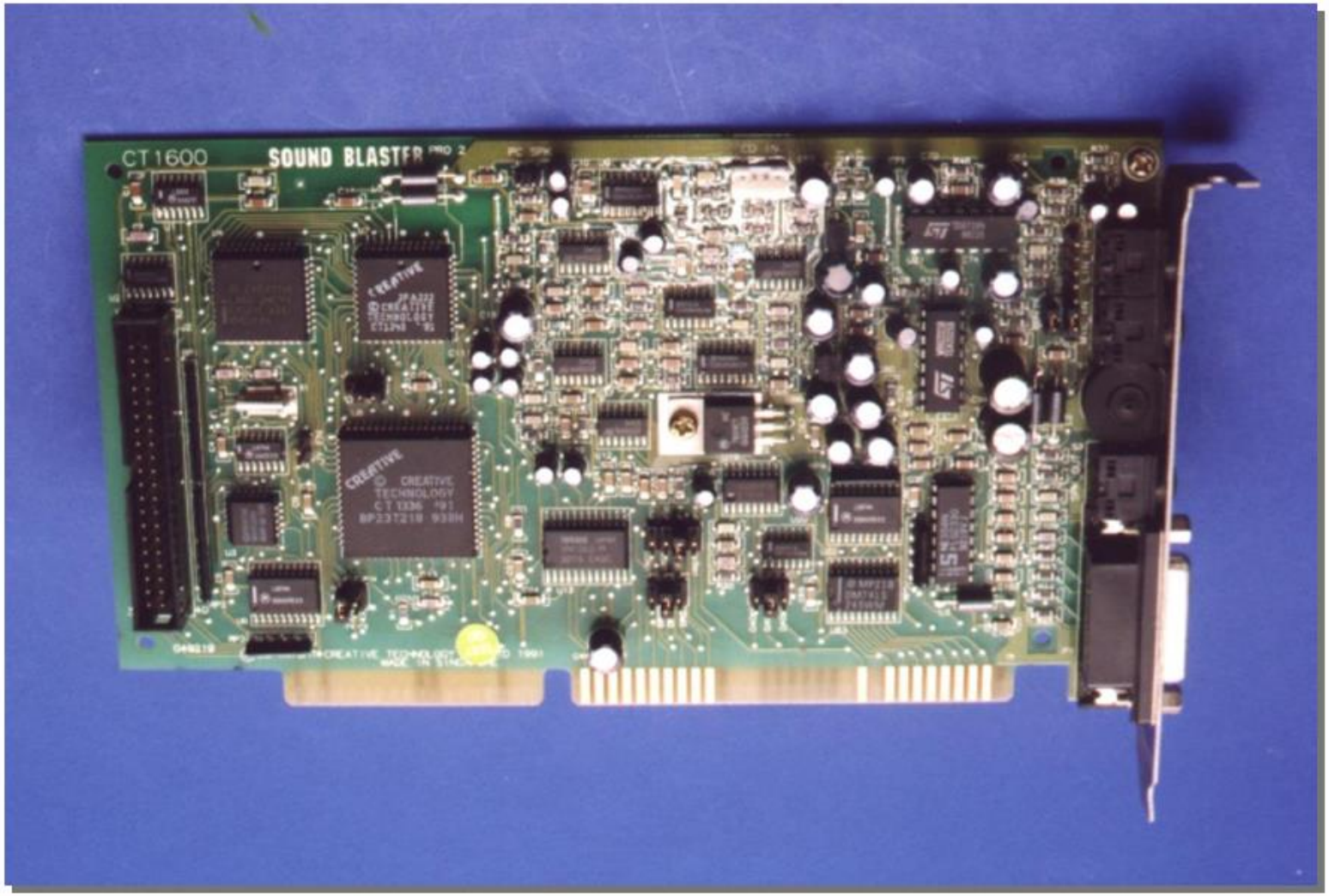
1. Identify differences between analog and digital devices and passive and active components. Explain the effects of parasitic structures in passive components.
2. Describe the PN junction, why it is important, and explain reverse and forward biasing.
3. State the characteristics of bipolar technology and the bipolar junction transistor in terms of function, biasing, structure and applications.
4. Explain the basic characteristics of CMOS technology, including the field effect transistor, biasing and the CMOS inverter.
5. Explain the difference between enhancement and depletion mode MOSFETs.
6. Explain the effects of parasitic transistors and the implications for CMOS latch up.

Circuit Types

- 數位 (Digital) IC是傳輸、處理和處理數位信號的IC且該電路是處理離散的訊號。 它是近年來應用最廣泛、增長最快（因先進製程節點的推進）的集成電路品種
- 類比 (Analog) IC是處理連續自然類比信號（如光、聲音、速度和溫度）的IC。如果按科技劃分，類比IC可以分為只處理類比信號的線性IC（如放大器 amplifier、運算放大器 operational amplifier、濾波器 filter等）和同時處理類比和數位信號的混合IC (如類比數位轉換器 analog-to-digital converter / ADC、數位類比轉換器 digital-to-analog converter / DAC)。



Components on Printed Circuit Board



	soc	sip
整合方式	單一晶片內整合所有模組（一個晶片）	多晶片封裝於一個模組內（多個晶片 / 晶片仍是分開）
製程依賴性	所有模組使用相同製程	不同晶片可以使用不同製程
設計彈性	靈活性較低，需要完整重新設計	靈活性高，可重用現有晶片
成本	高	低
性能	更高的效能和能效	性能略低於 SoC，且功耗稍高
應用	手機處理器	穿戴式設備

Active & Passive Component

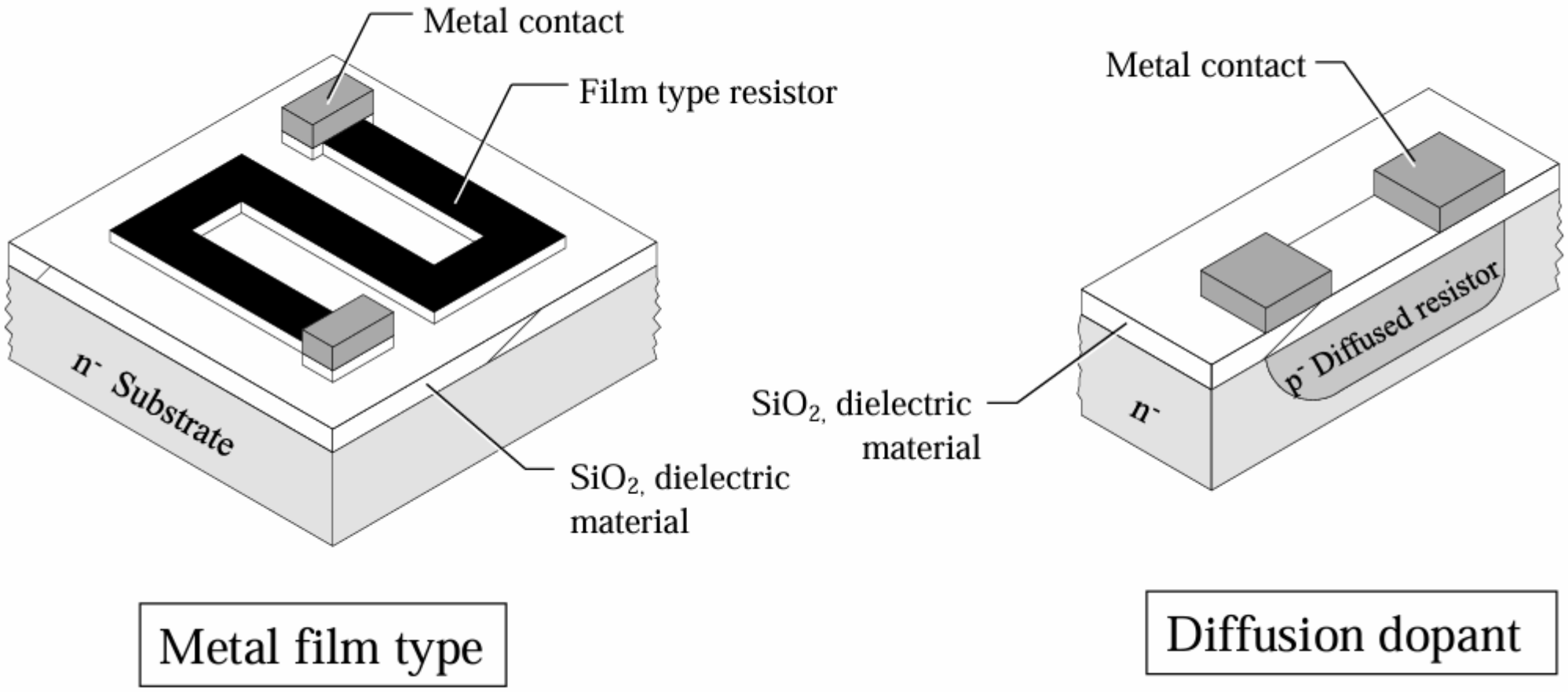
- **主動元件（Active Components）：**
  - **定義：** 主動元件能夠控制電流並提供增強功能，通常依賴於外部電源來操作。這些元件能夠放大訊號或作為開關。
  - **應用：** 主動元件應用於放大訊號、數據處理、電流控制等。

- **被動元件（Passive Components）：**
  - **定義：** 被動元件不需要外部電源即可工作，不能主動控制電流流動。這些元件只會消耗能量或儲存能量。
  - **應用：** 被動元件多用於電壓分配、濾波電路、阻抗匹配等。

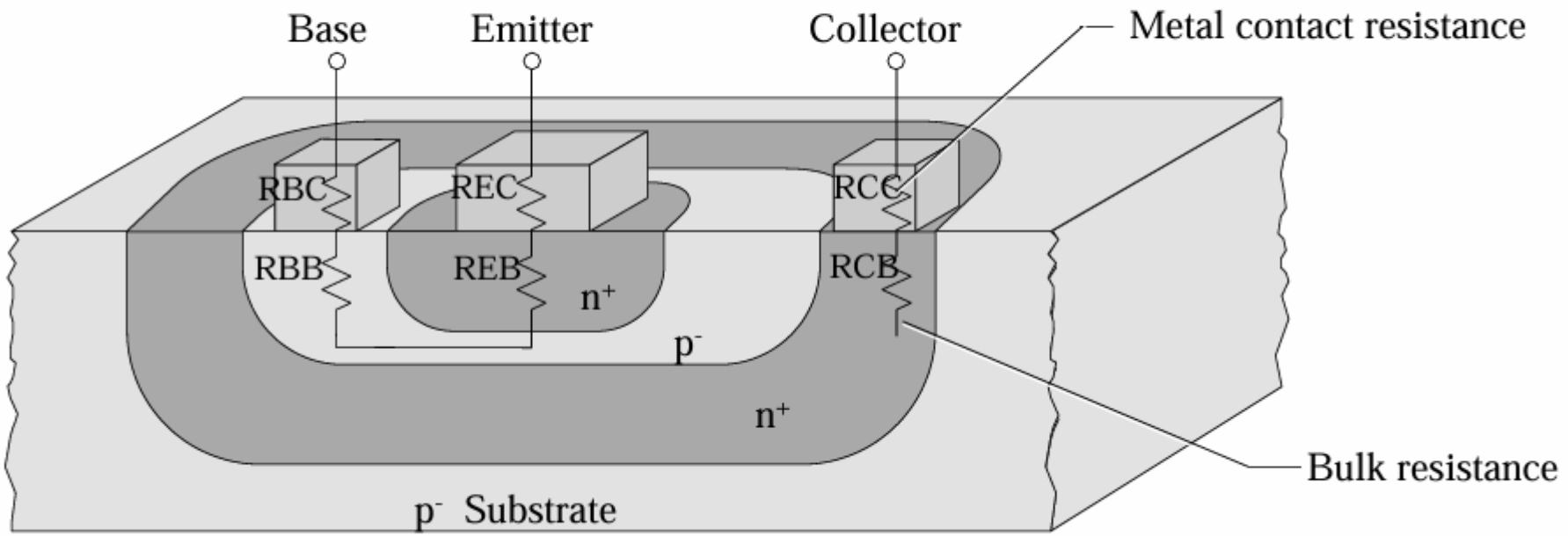
Passive Component Structures

- IC Resistor Structures (R)
  - ➢ Parasitic Resistor Structures
- IC Capacitor Structures (C)
  - ➢Parasitic Capacitance Structures
- IC Inductor Structures (L)

Resistor Structures in IC

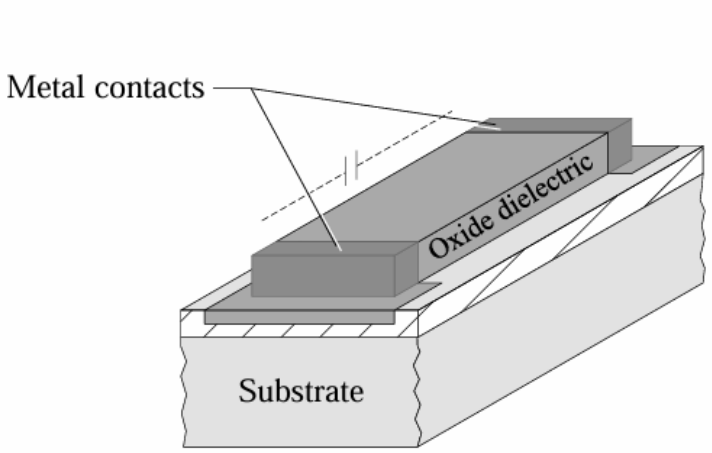


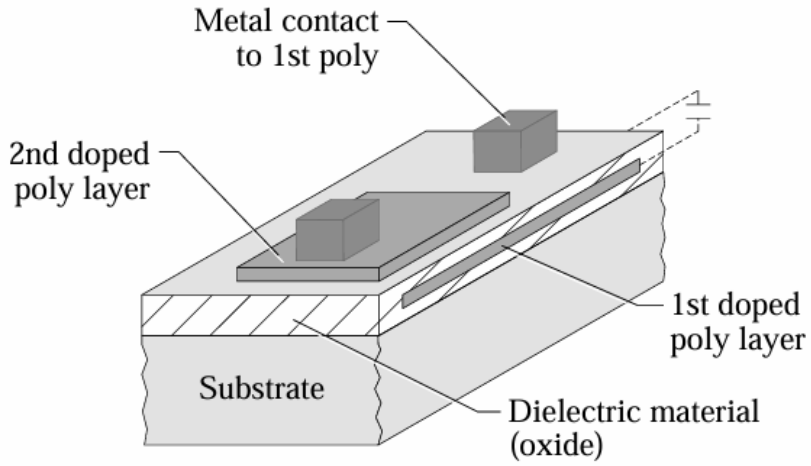
Parasitic Resistances in a Transistor

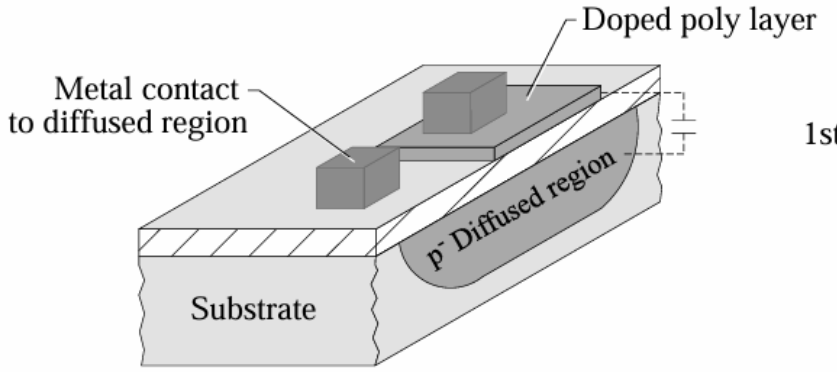


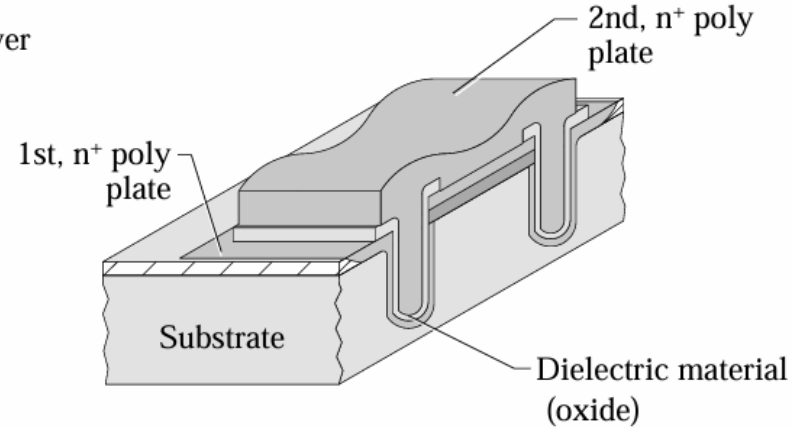
- It reduces the operational performance of IC devices
- Higher density comes higher resistance

Capacitors Structures in IC

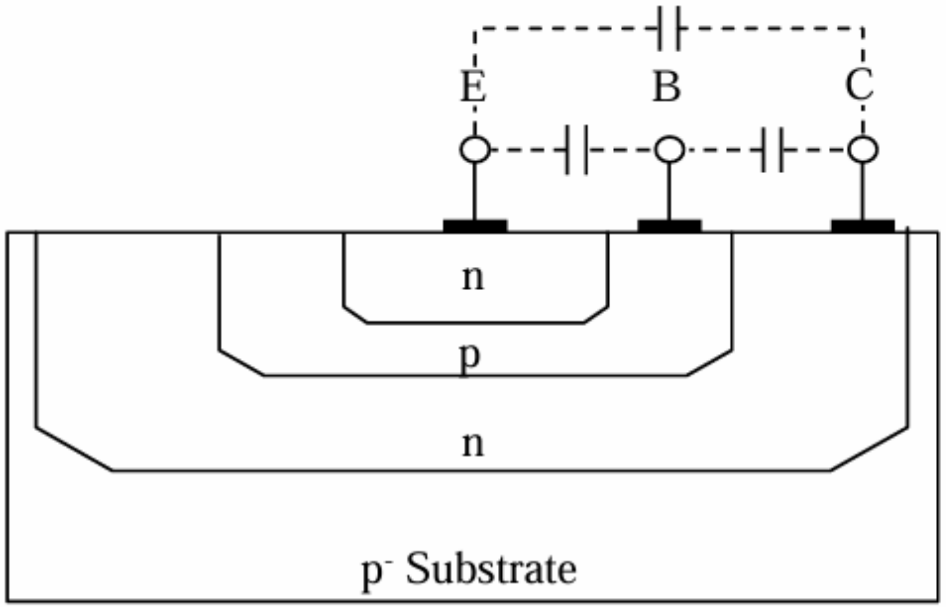




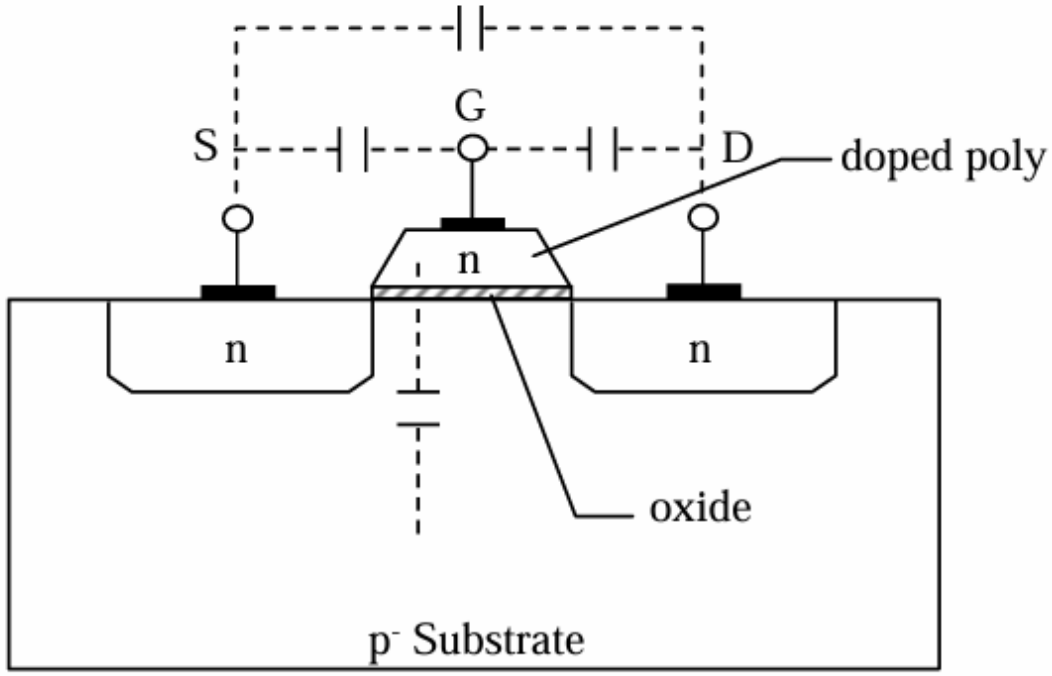




Parasitic Capacitances in a Transistor



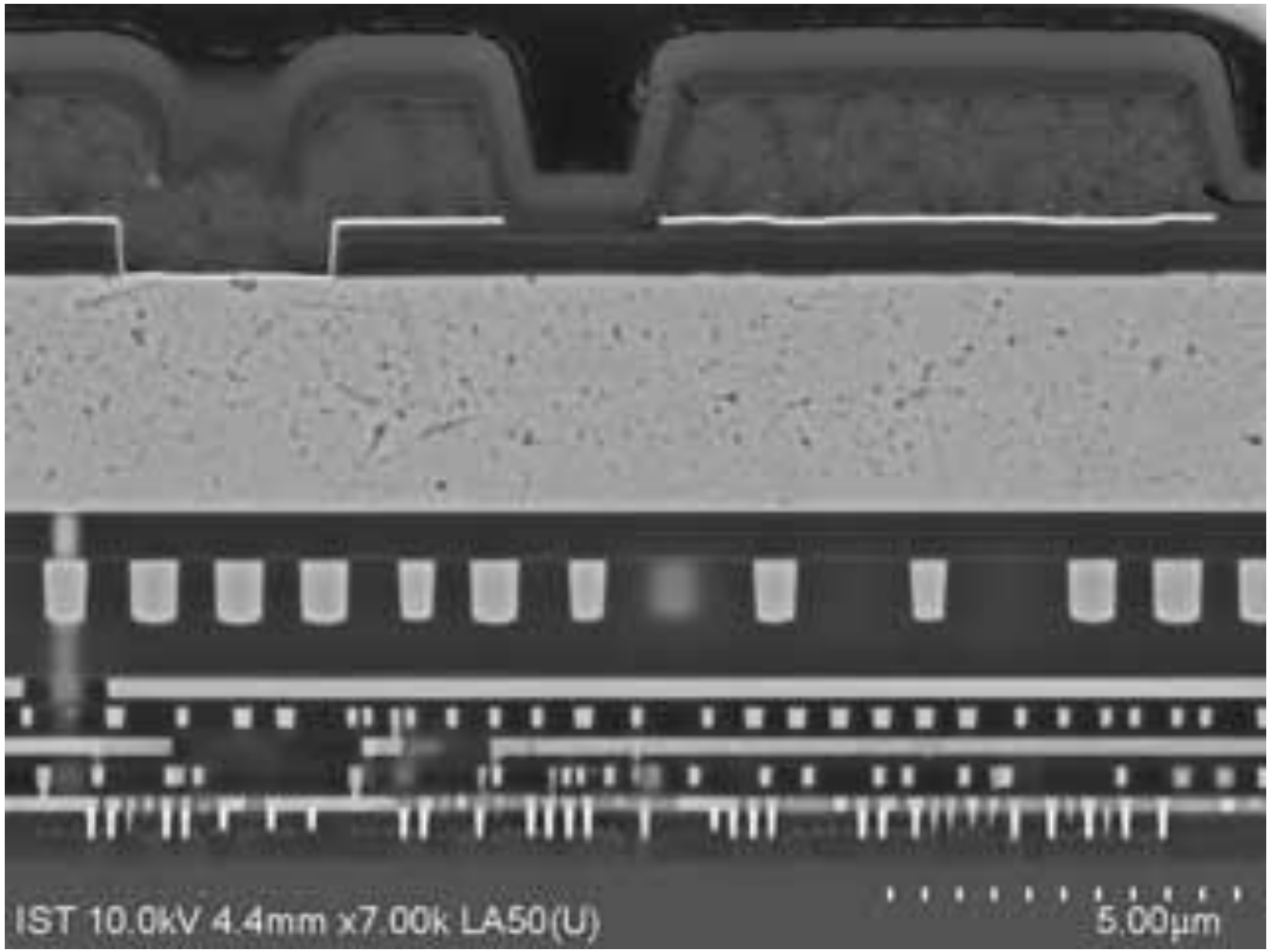
Bipolar junction transistor

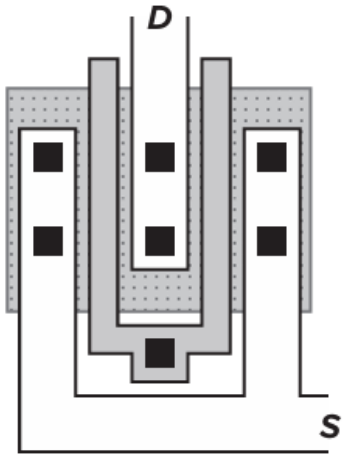


Field effect transistor

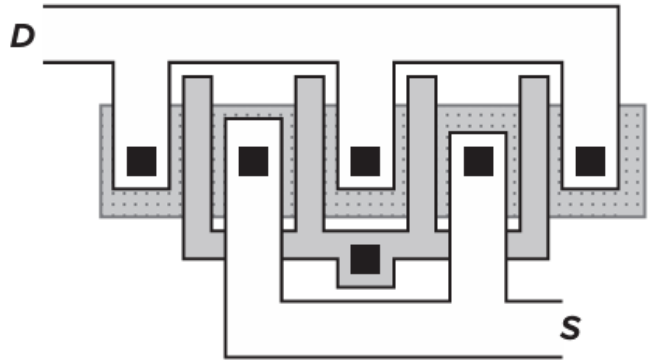
- Parasitic capacitance may create instability in circuits, even short-circuit paths for AC signals where they are not need

Parasitic Resistances & Parasitic Capacitances in a Transistor





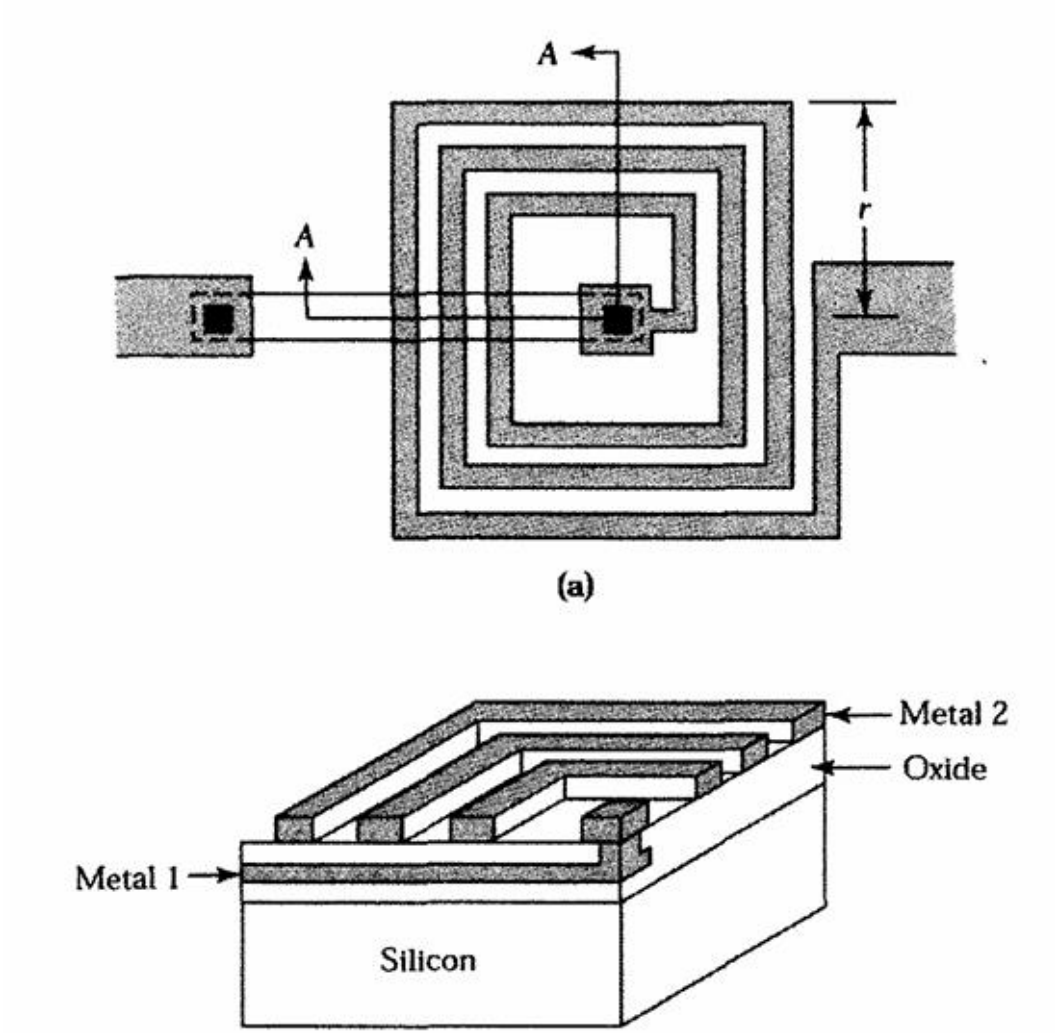
(a)



(b)

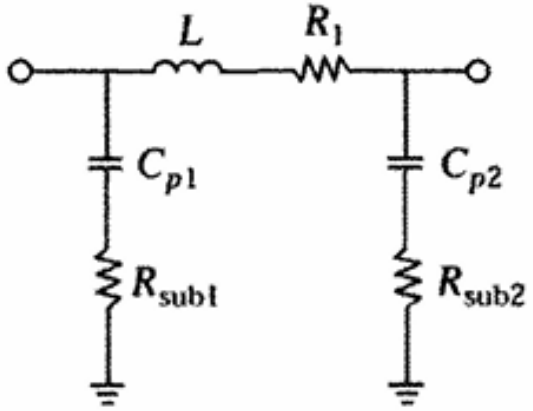
Source: iST、Design of Analog CMOS Integrated Circuit

Integrated-Circuit Inductor



$$\mathcal{E} = -N\frac{\mathrm{d}\Phi}{\mathrm{d}t} = -N\frac{\mathrm{d}\Phi}{\mathrm{d}i}\,\frac{\mathrm{d}i}{\mathrm{d}t}$$

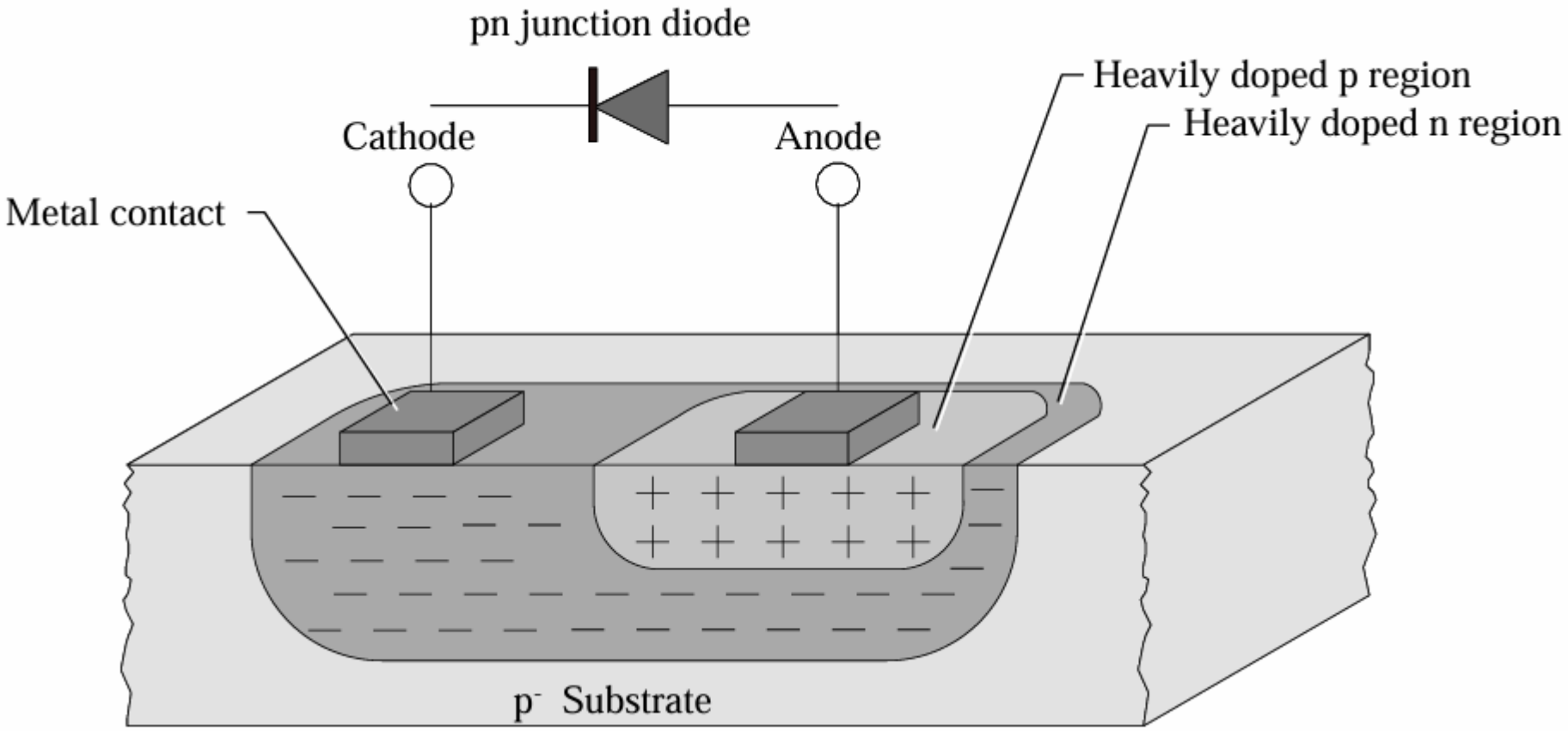
$$L = N\frac{\mathrm{d}\Phi}{\mathrm{d}i}$$



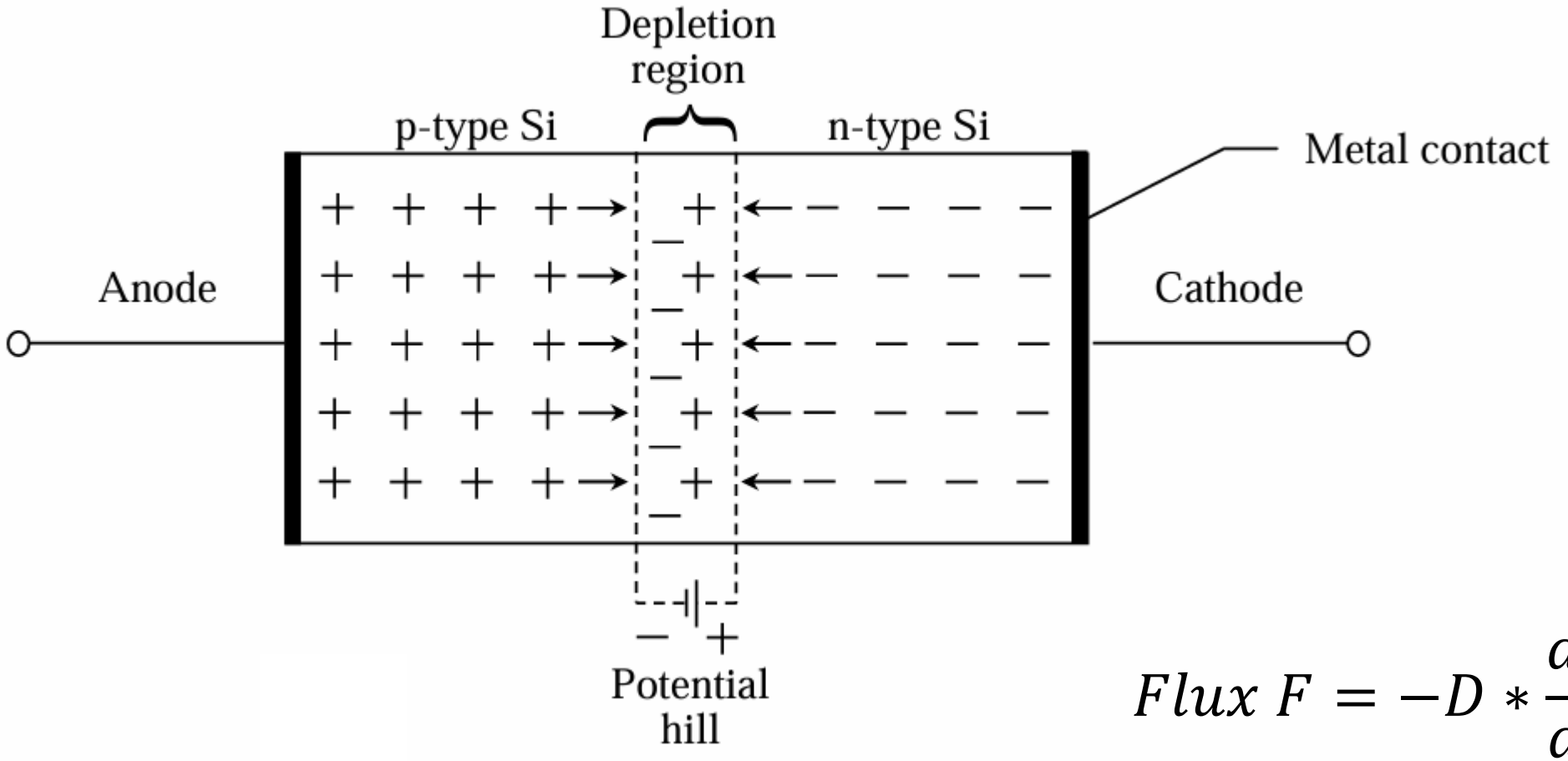
Active Component Structures

- The pn Junction Diode
- The Bipolar Junction Transistor
- Schottky Diode
- Bipolar IC Technology
- CMOS IC Technology
- Enhancement and Depletion-Mode MOSFETs

Basic Symbol and Structure of the pn Junction Diode

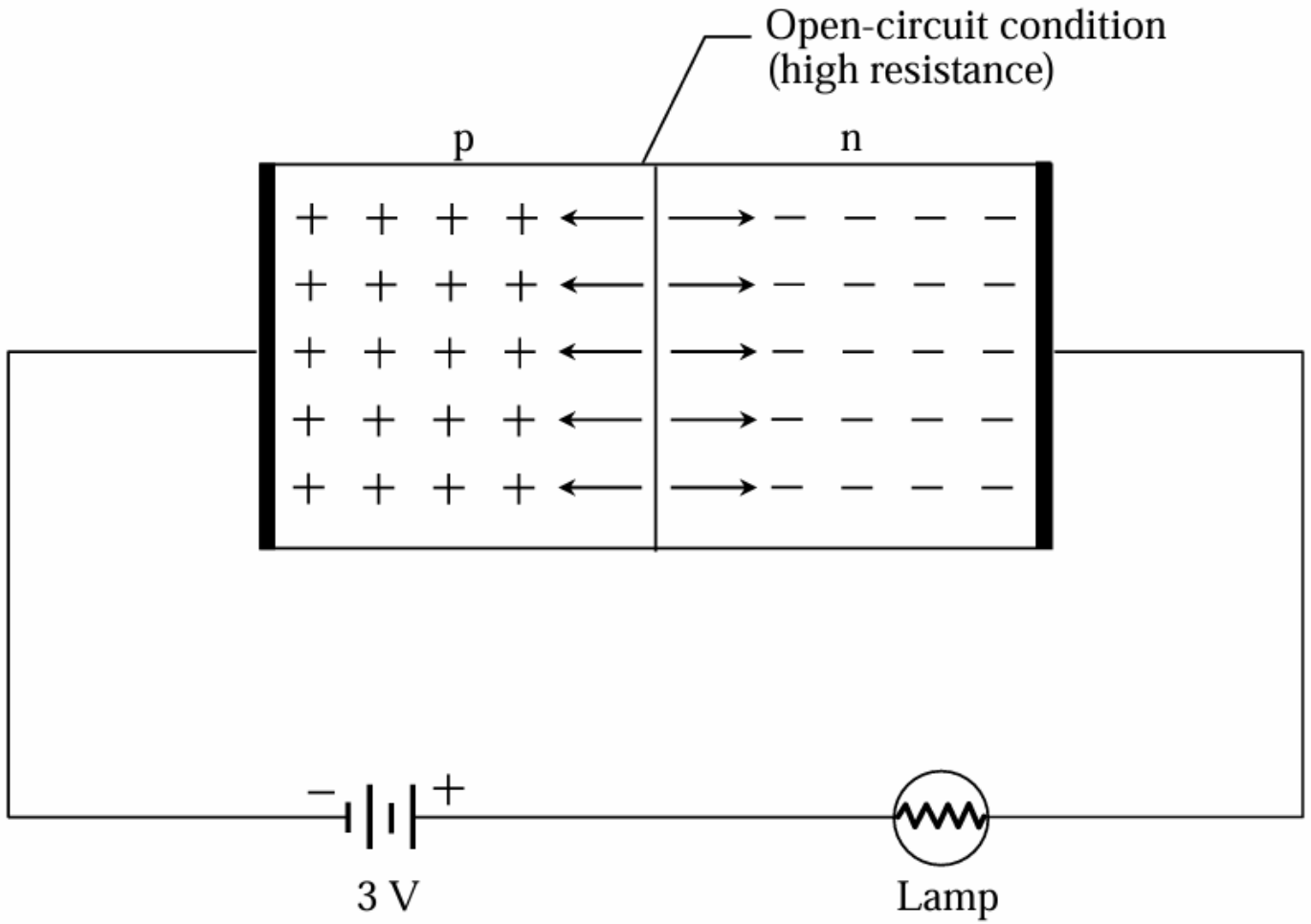


Basic Concept for pn Junction Diode

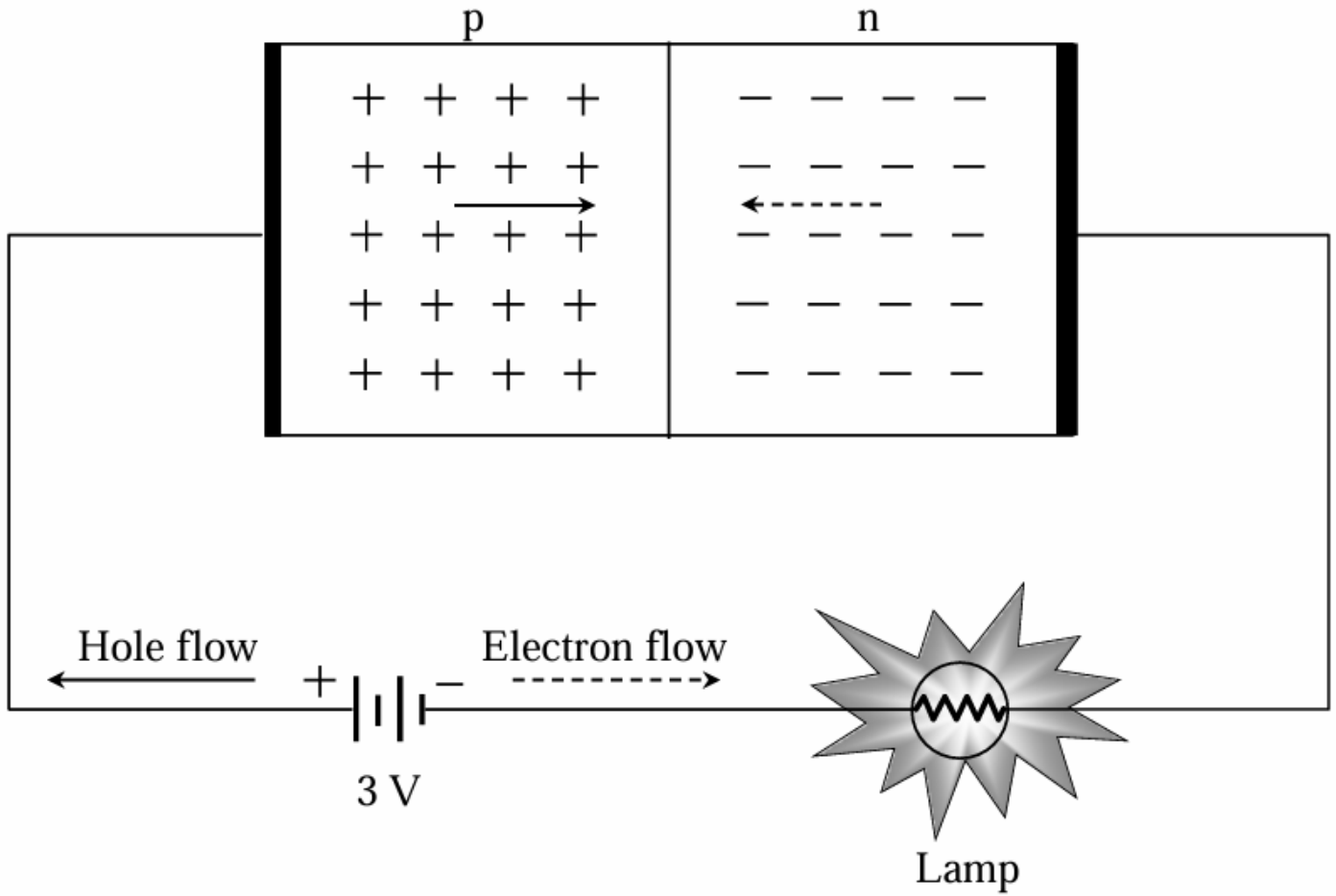


$$Flux\ F = -D * \frac{dn}{dx}$$

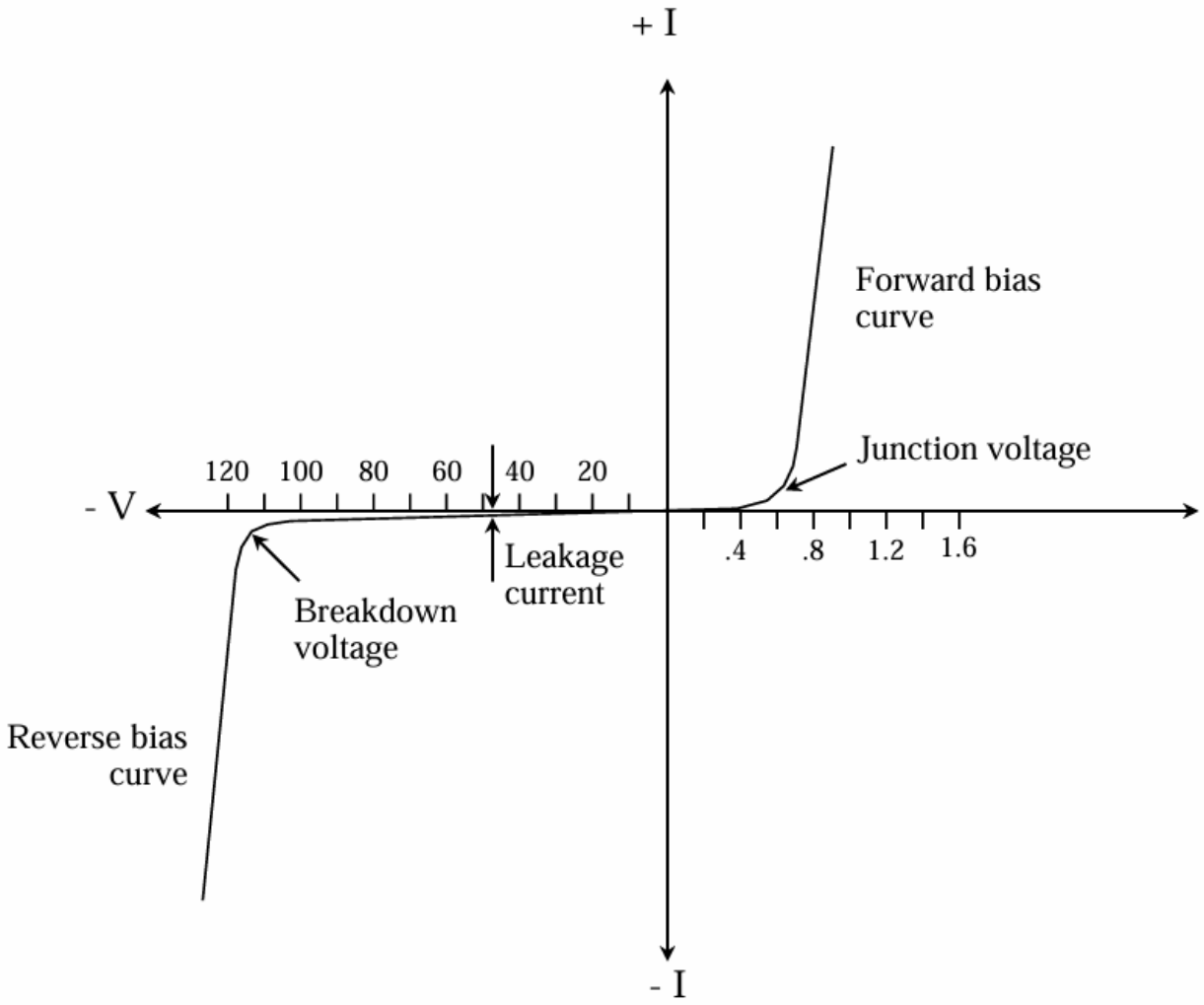
Reverse-Biased PN Junction Diode



Forward-Biased PN Junction Diode

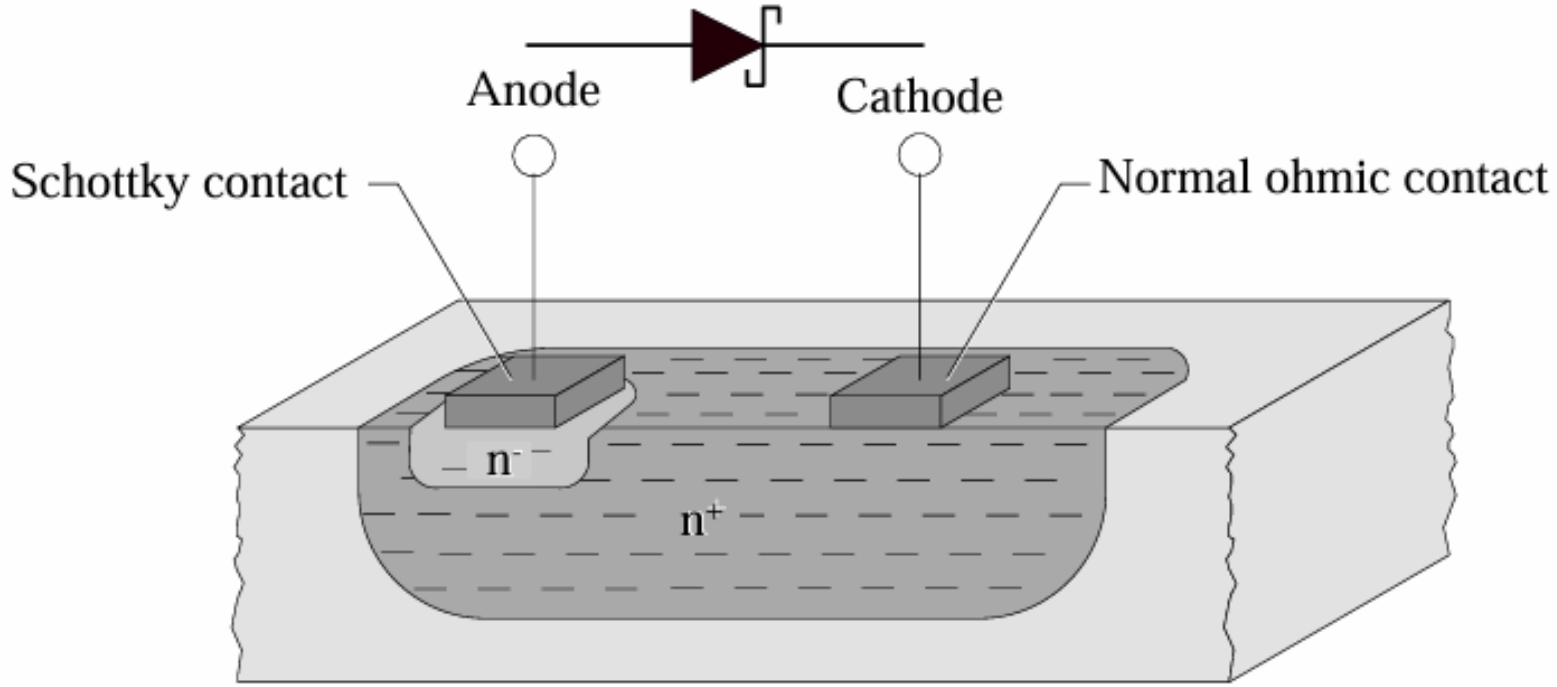


Bias Voltage Characteristics of a Silicon Diode



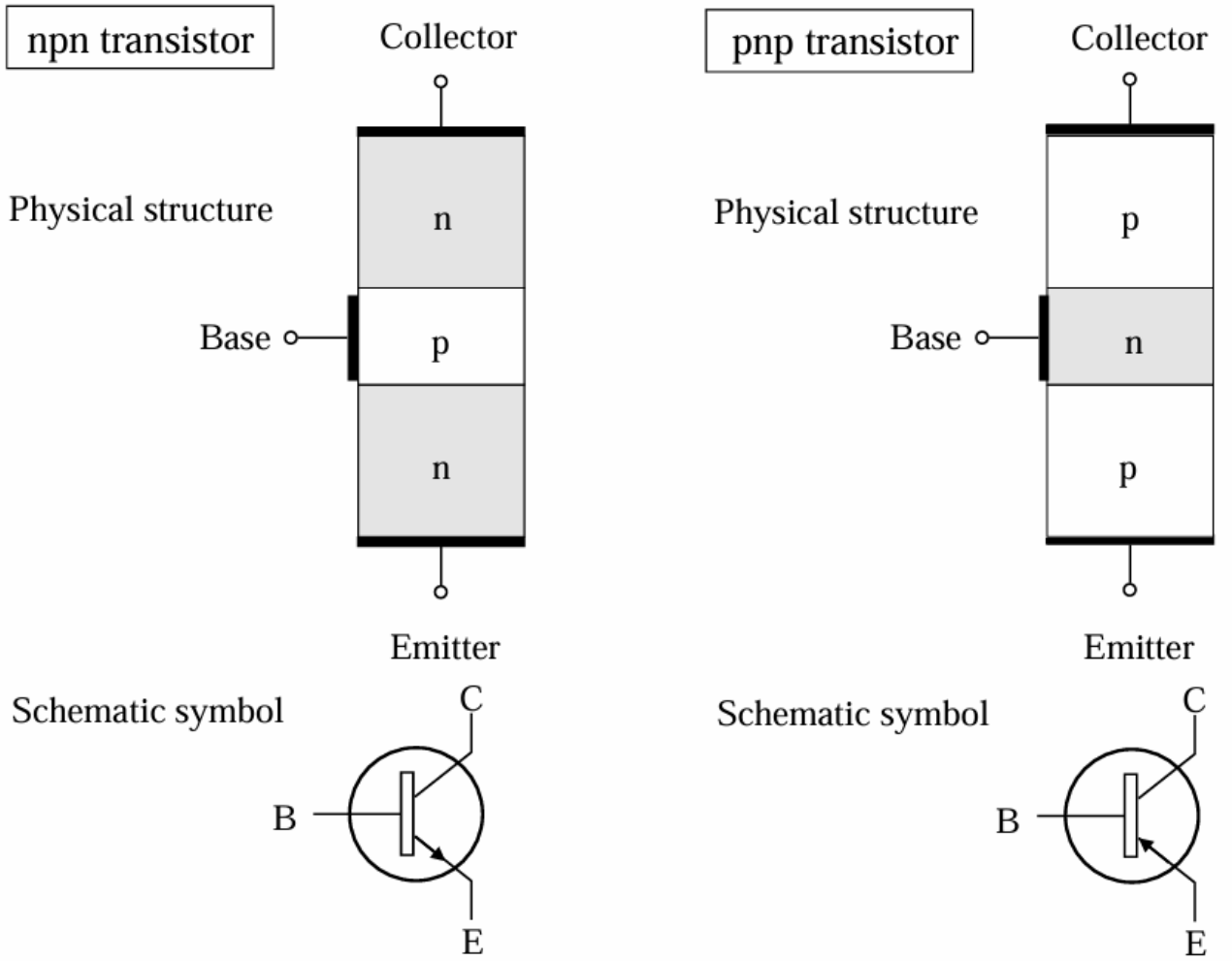
	Si	Ge
I_s（逆向飽和電流）	較小 (10 - 20 nA)	較大 (1 – 2 uA)
V_D（導通電壓）	0.6 – 0.7 V	0.2 – 0.3 V
崩潰電壓	較大 (-250 V)	較小 (-40 - -50 V)

Basic Symbol and Structure of the Schottky Diode

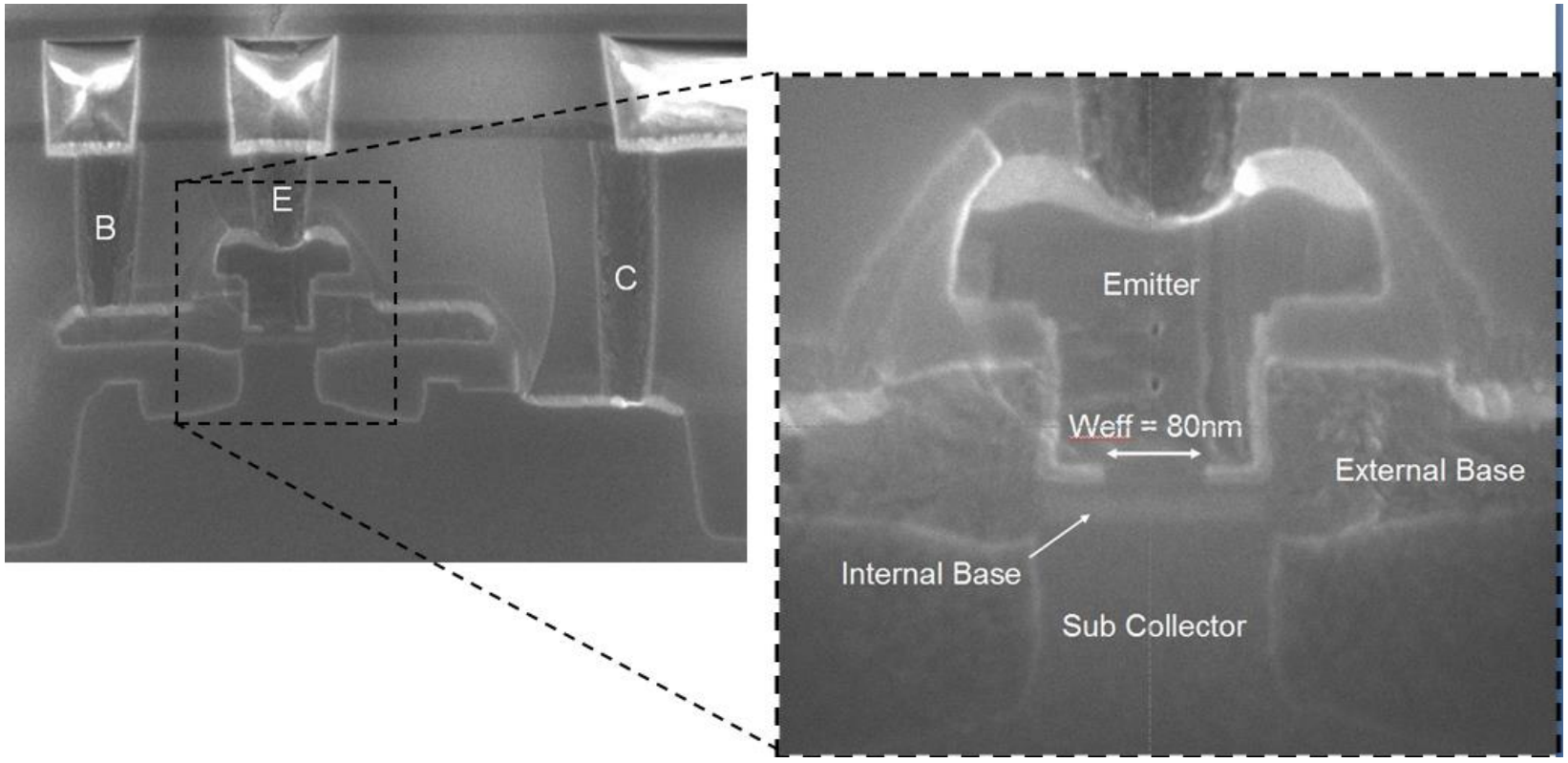


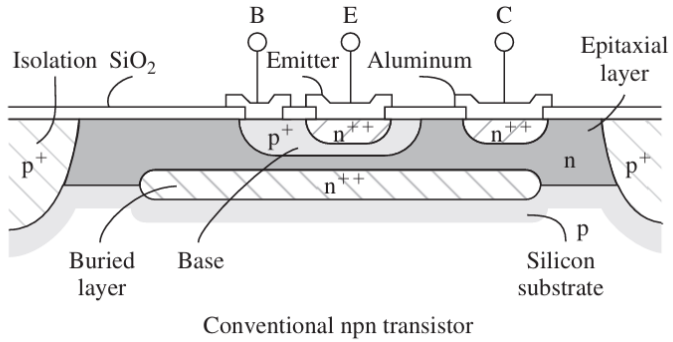
- The forward junction voltage drop 0.3~0.5 V is nearly half that of pn-junction 0.6~ 0.8V.
- It formed when metal is brought in contact with lightly doped n-type semiconductor materials.
- Faster switching than pn diode, no minority.

Basic Symbol and Structure of Two Types of Bipolar Junction Transistors



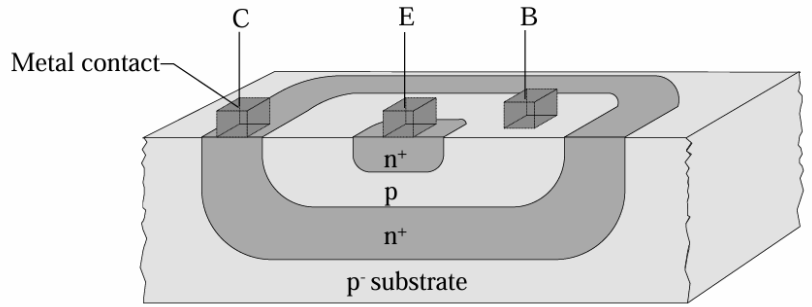
Cross Section of an NPN BJT





Conventional npn transistor

(a)

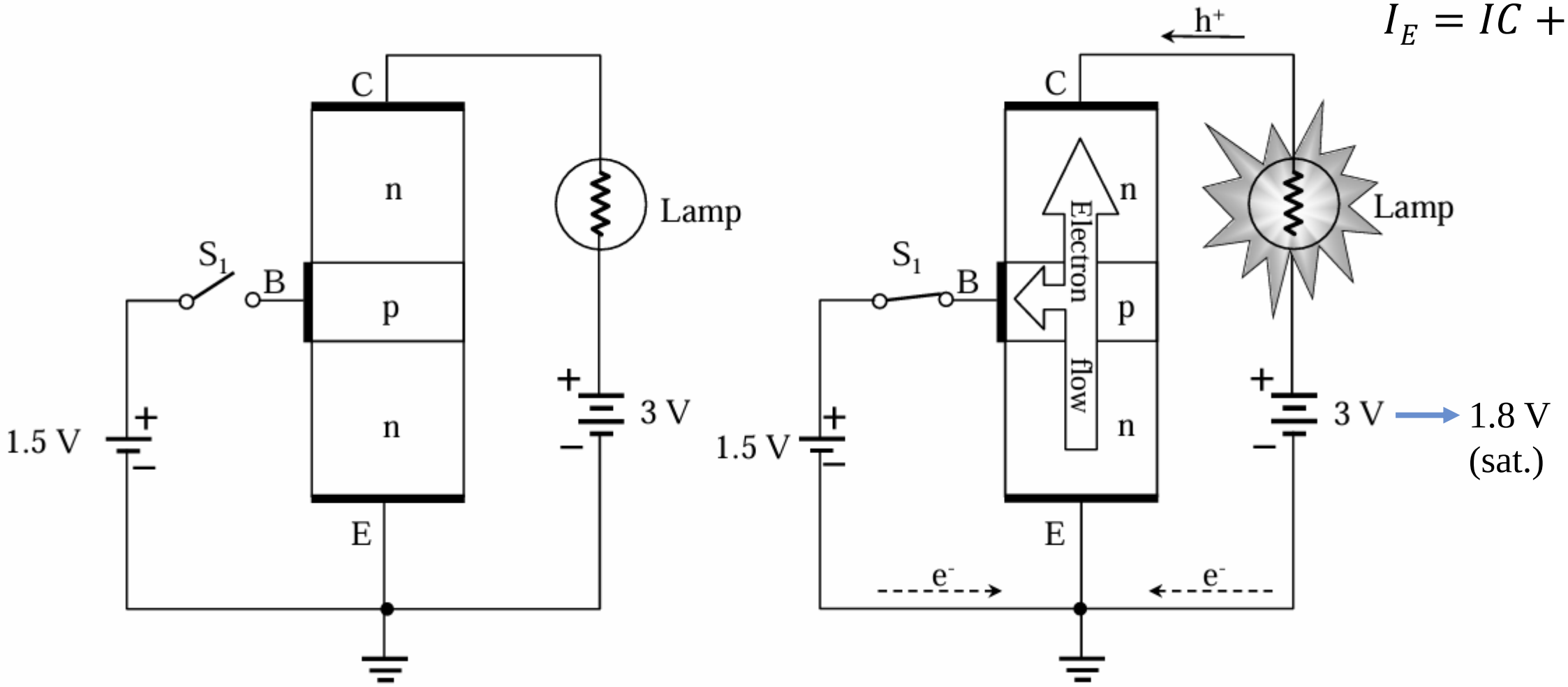


Source: imec

NPN Transistor Biasing Circuit

$$\beta = \frac{I_C}{I_B}$$

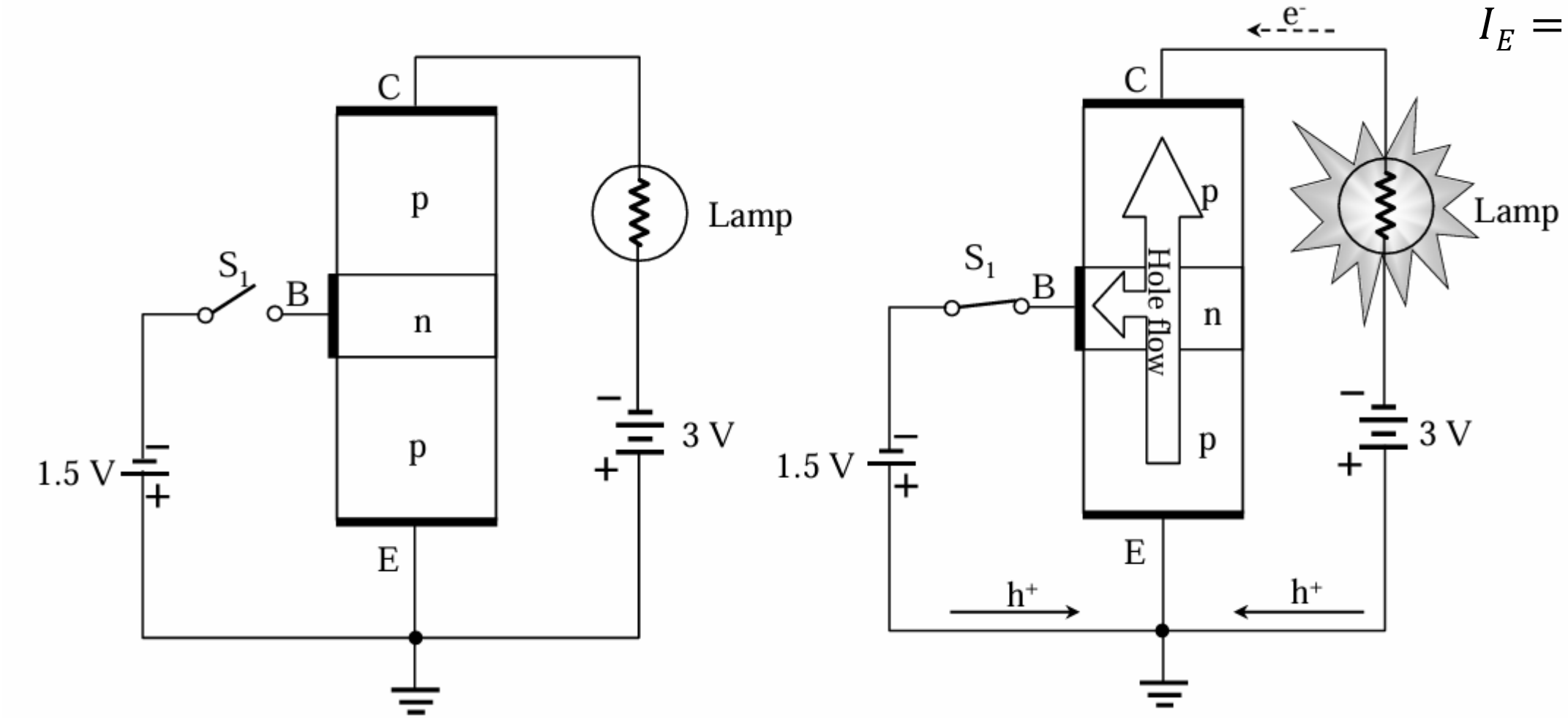
$$I_E = IC + IB$$



PNP transistor biasing circuit

$$\beta = \frac{I_C}{I_B}$$

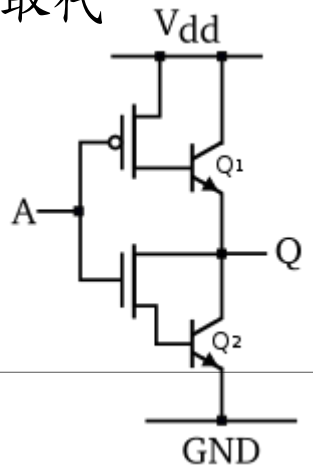
$$I_E = IC + IB$$

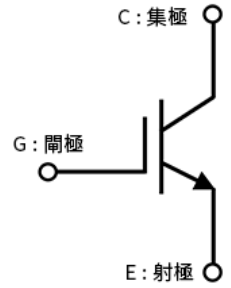


The Comparison Between npn and pnp Bipolar Junction Transistors

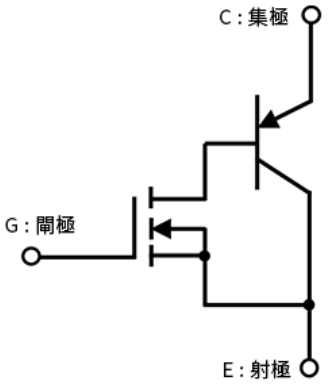
	npn	pnp
導通條件（BE兩端所施加的偏壓）	基極施加正電壓（指基極電位高於射極）	基極施加負電壓（指基極電位低於射極）
傳輸載子	主要載子（電子）	主要載子（電洞）
導通速度 / 開關速度	較快	較慢
飽和電壓（CE兩端所施加的偏壓）	較低（若使用Si，常見0.2 V）	較高（若使用Si，常見0.3 V）
熱穩定	較好	較差

- **1950-1980年代：**BJT的主流地位
- **1980年代以後：** MOSFET逐漸取代了BJT（因為BJT功耗較高、密度限制、熱穩定問題、成本高），但BJT在一些特定應用仍不會被取代





N溝道型IGBT的電路圖符號

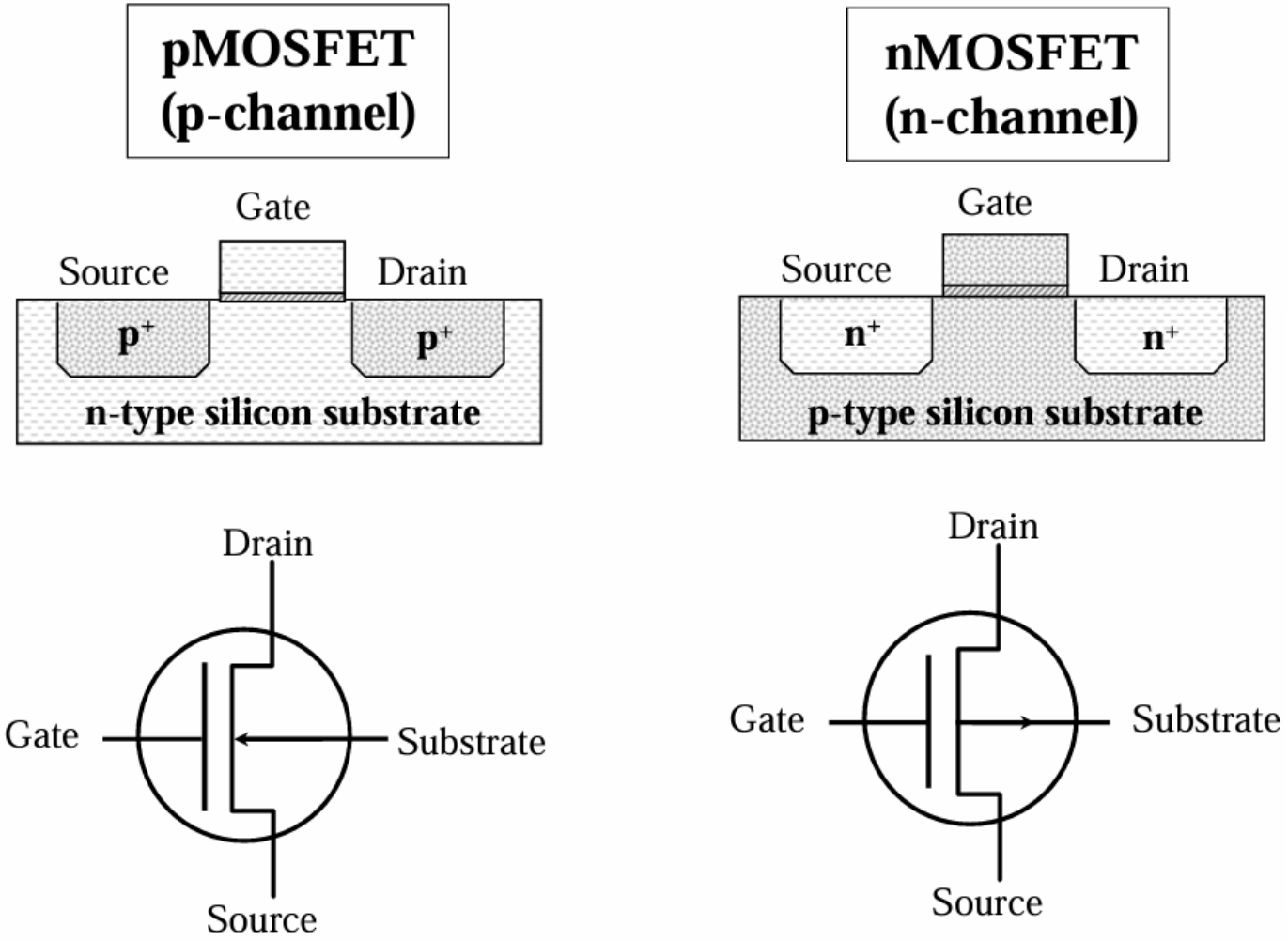


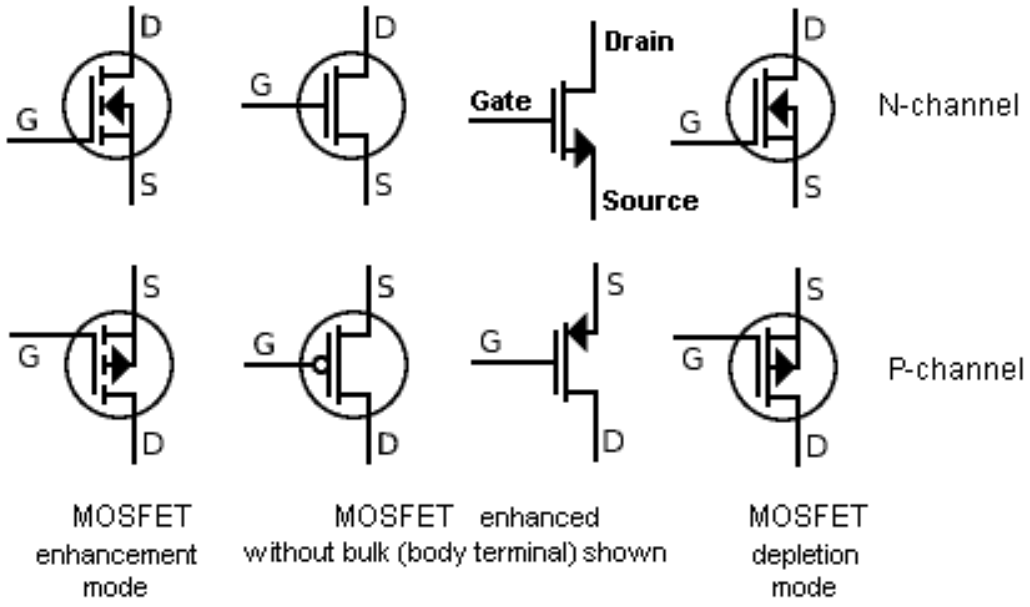
N溝道型IGBT的等效電路範例

BJT vs. MOSFET

- FET is a voltage-amplifying device, BJT is a current-amplifying device
- Greatest advantage: low voltage and low power operation
- BJT requires input current to turn on, FET as a result of electric field created by gate voltage- thus the name field-effect transistor
- It has infinite R_{in} and moderate gain make it an excellent device for use in instrumentation and communications

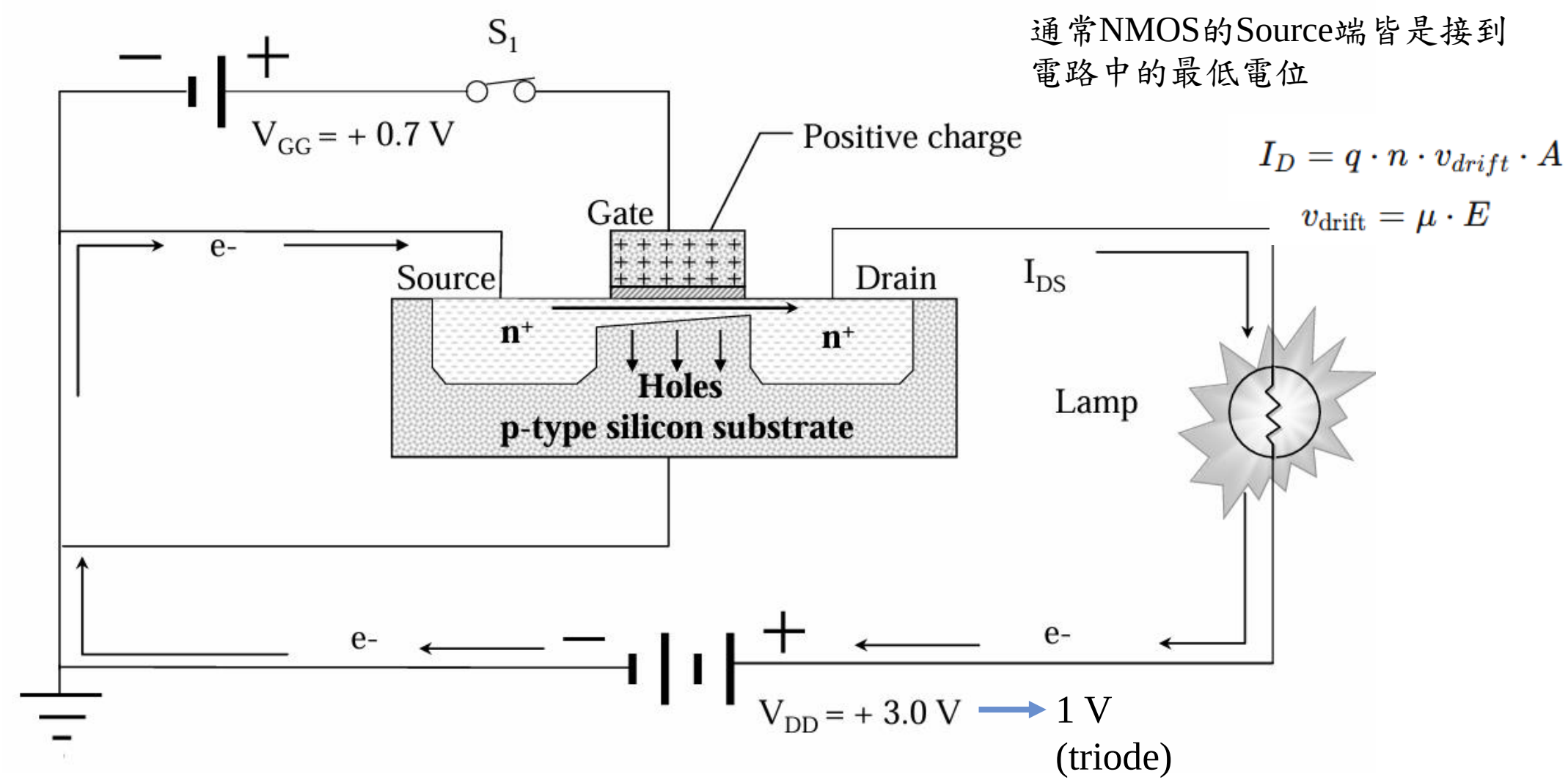
Basic Symbol and Structure of Two Types of Metal-Oxide-Semiconductor Field Effect Transistors



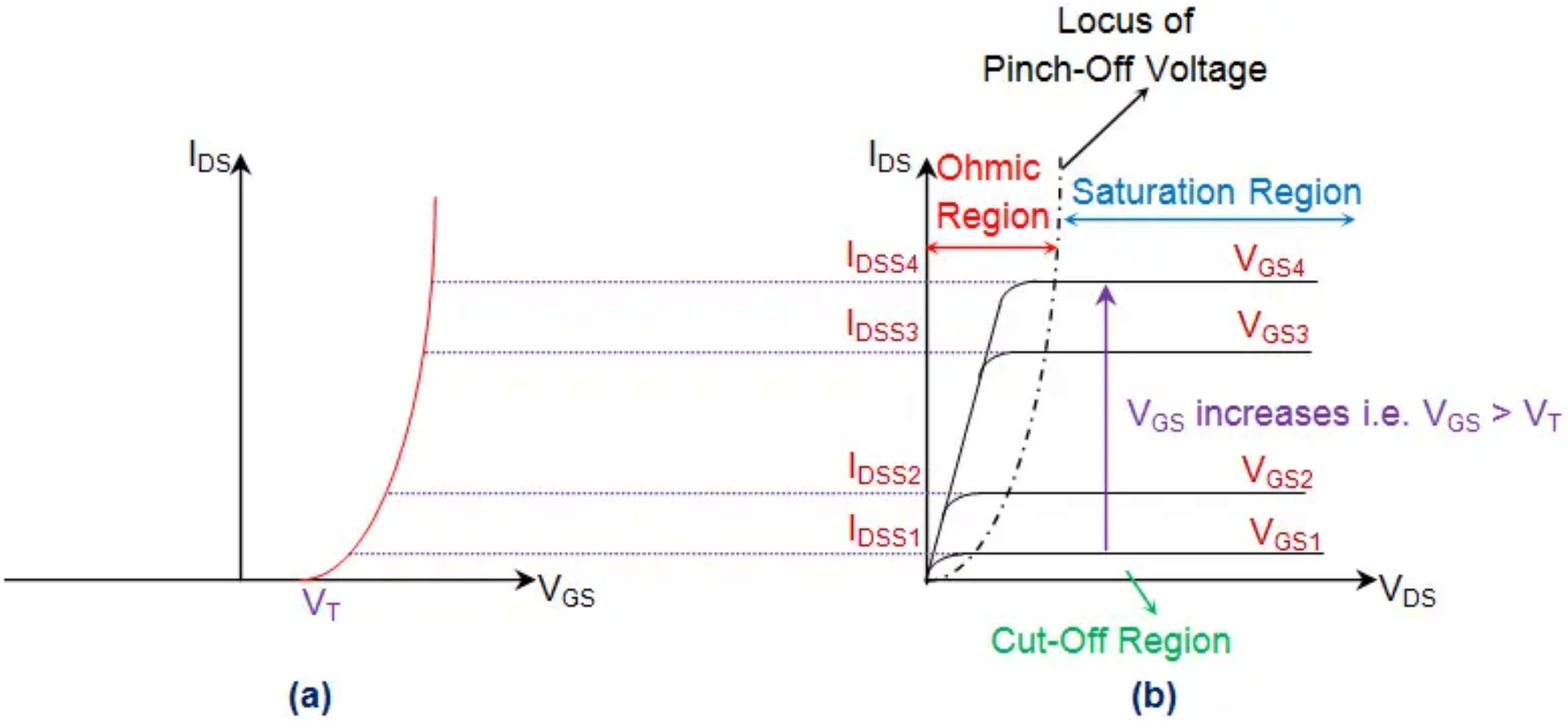


Source: quora

Biasing Circuit for an NMOS Transistor

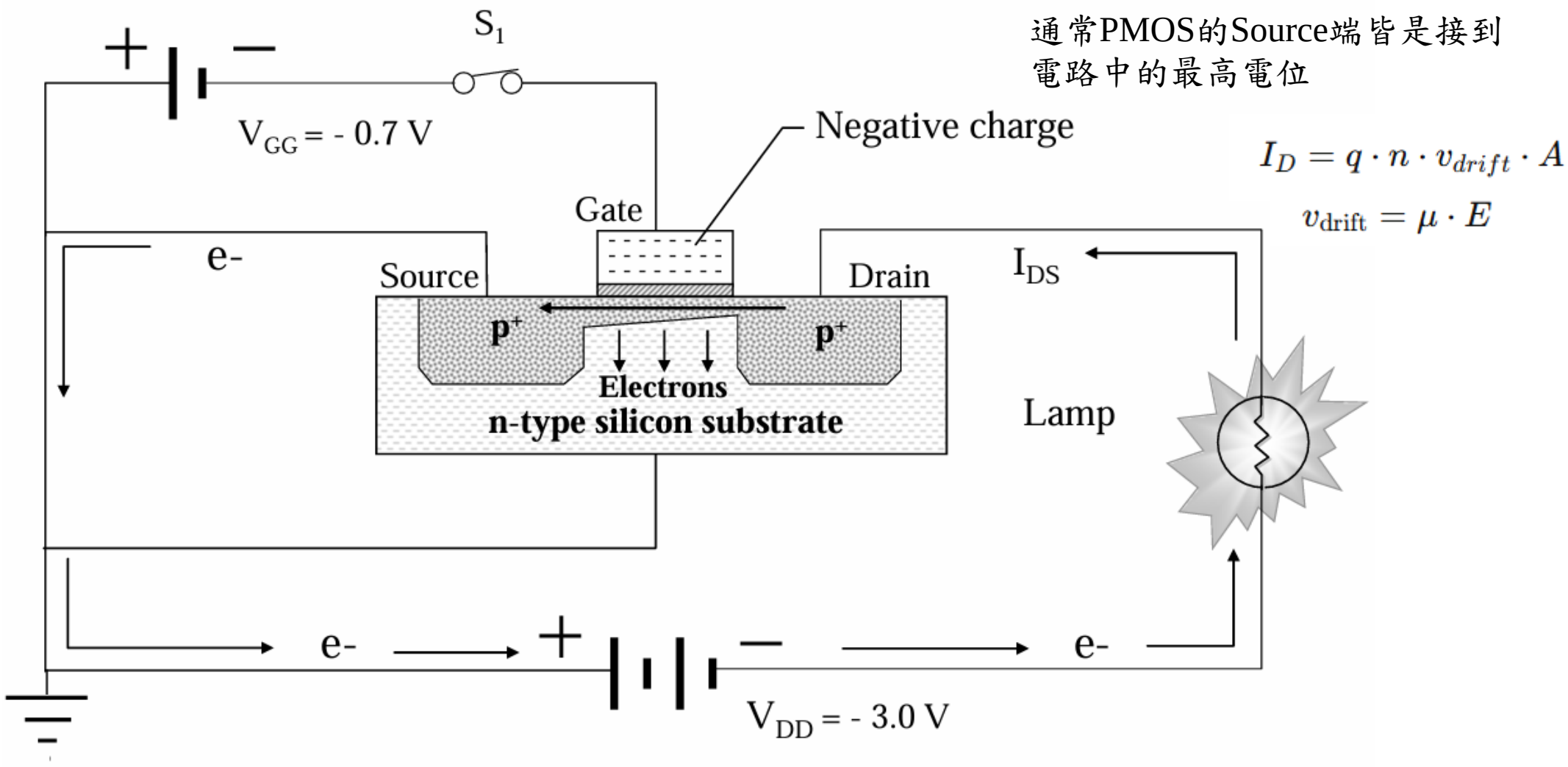


Example of Characteristics Curves of an N-channel MOSFET



n-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

Biasing Circuit for a P-Channel MOSFET

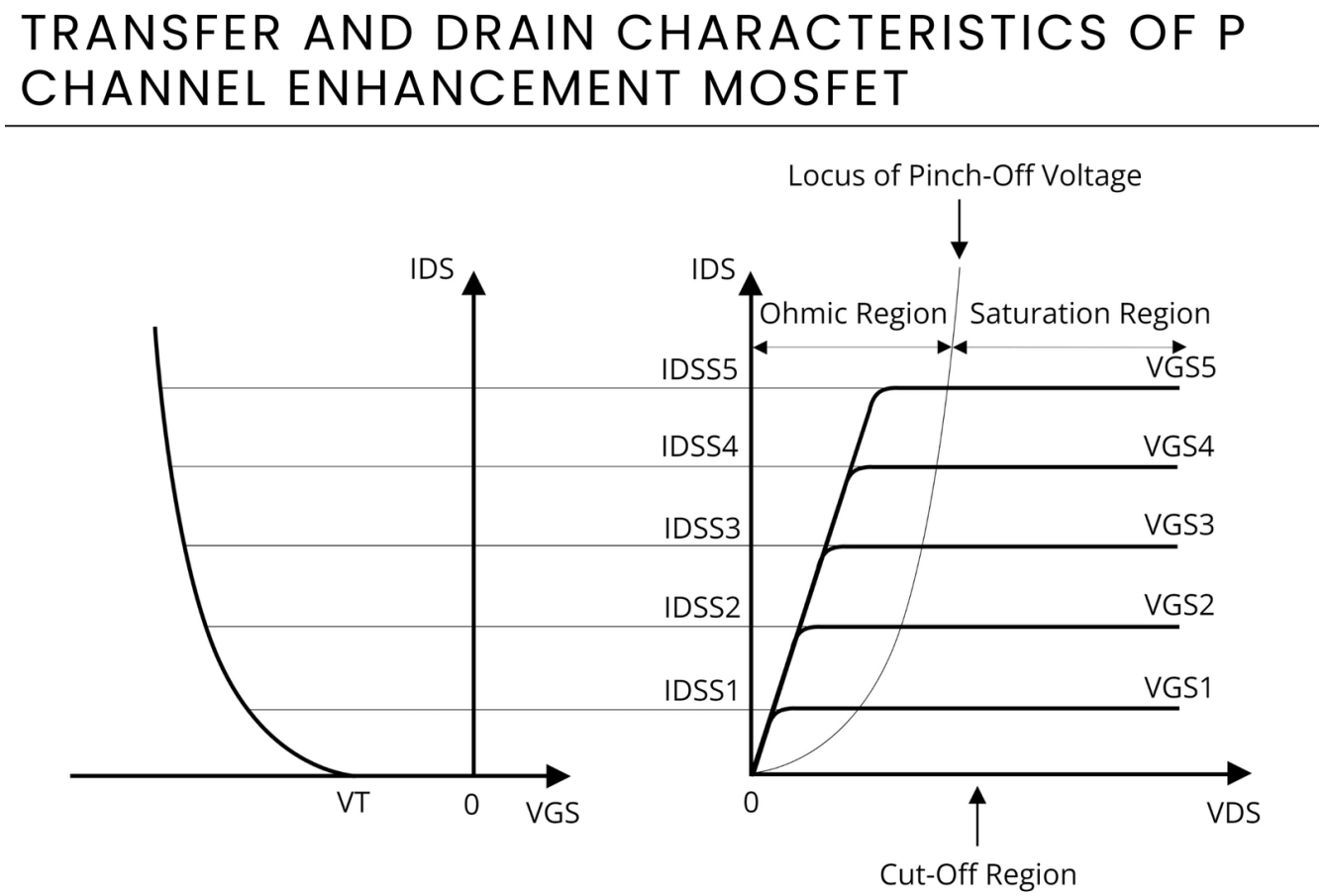


通常PMOS的Source端皆是接到電路中的最高電位

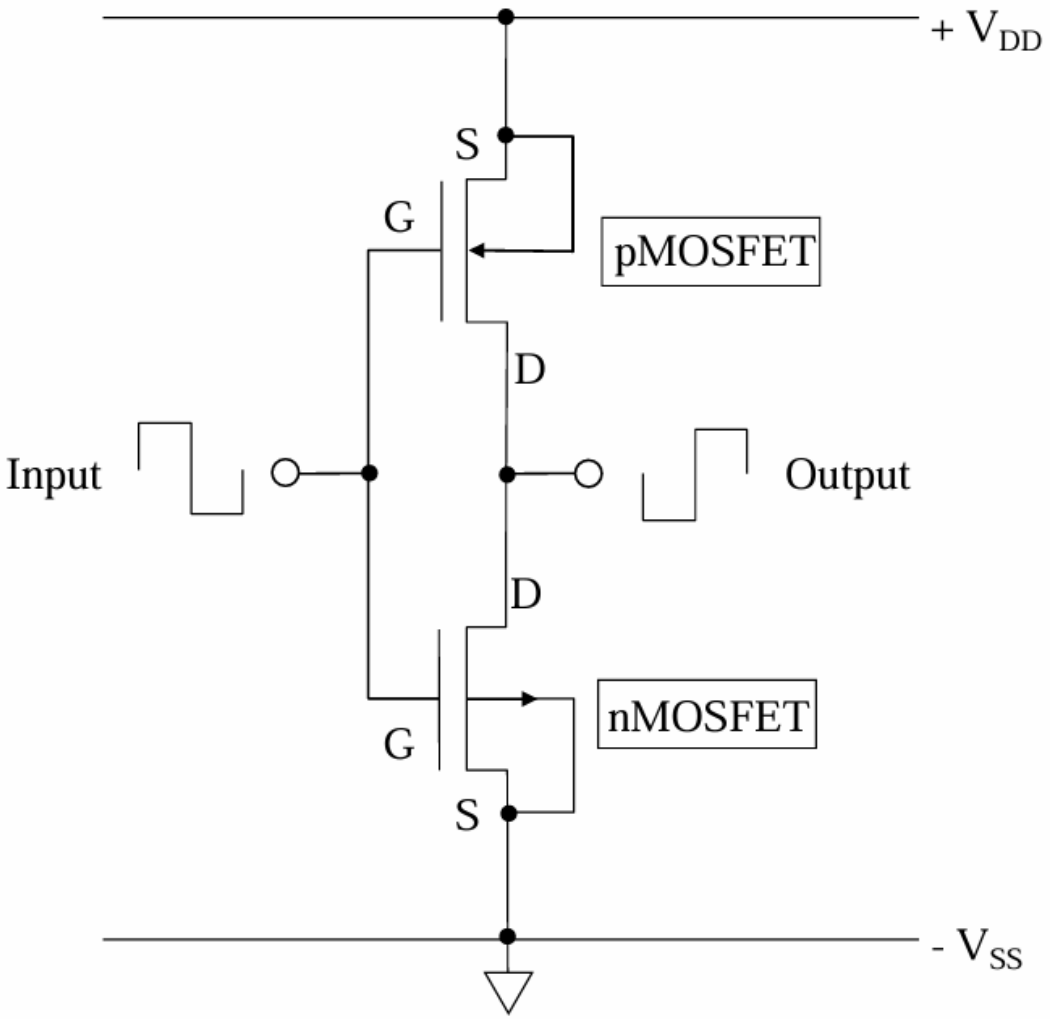
$$I_D = q \cdot n \cdot v_{drift} \cdot A$$

$$v_{\text{drift}} = \mu \cdot E$$

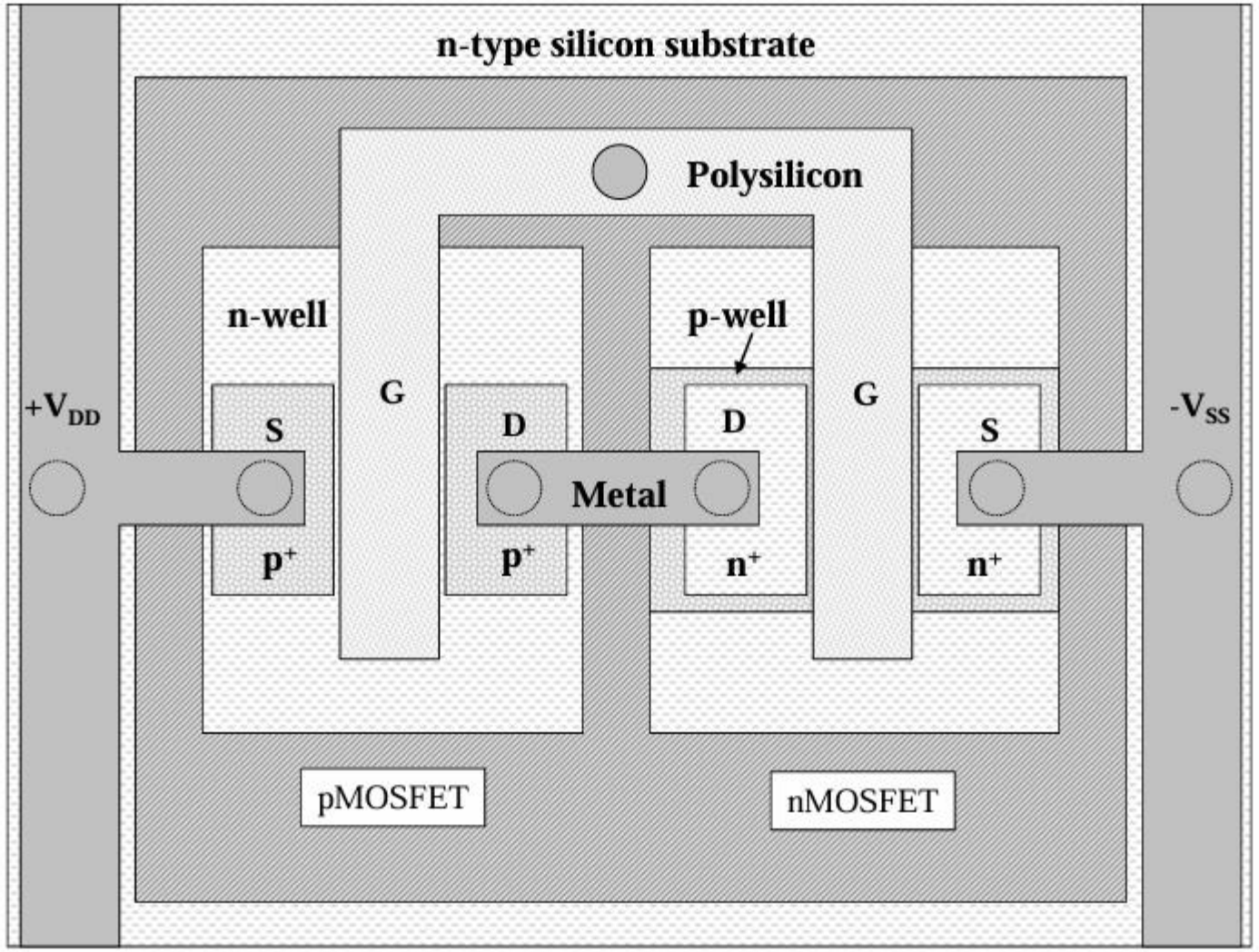
Example of Characteristics Curves of an P-channel MOSFET



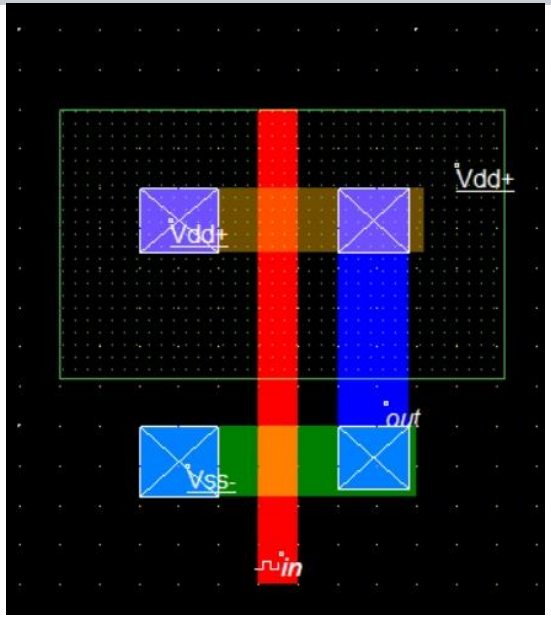
Schematic of a CMOS Inverter

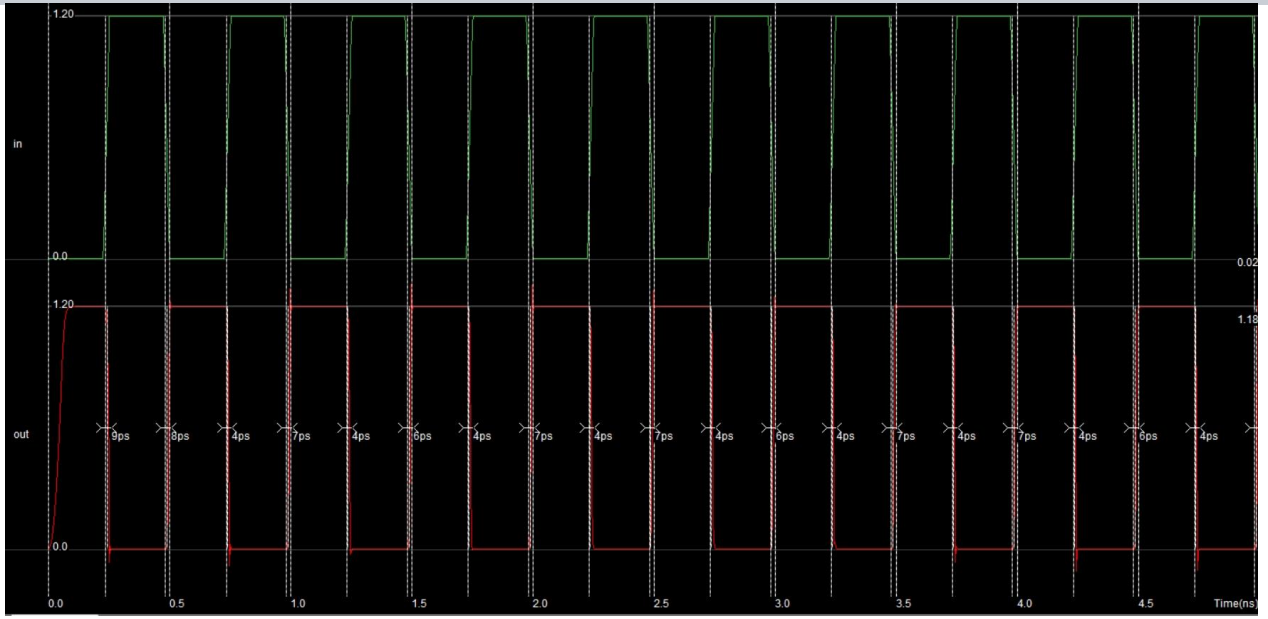


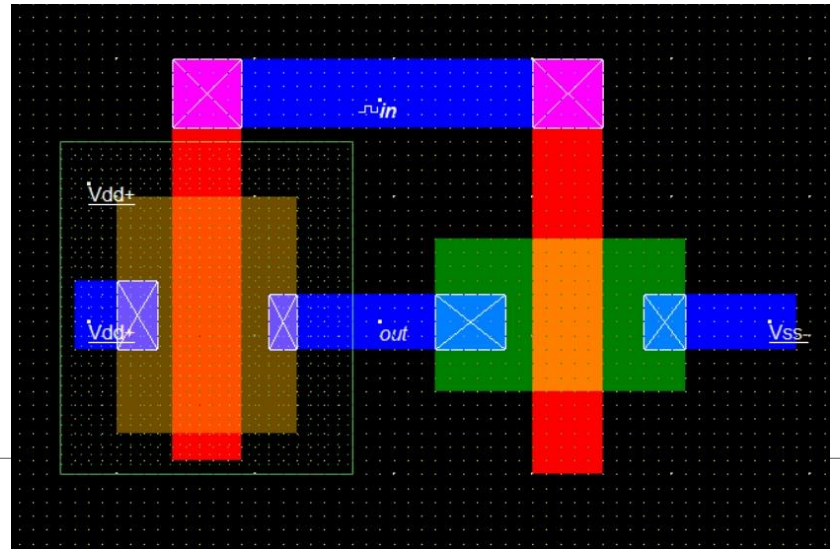
Schematic of a CMOS Inverter

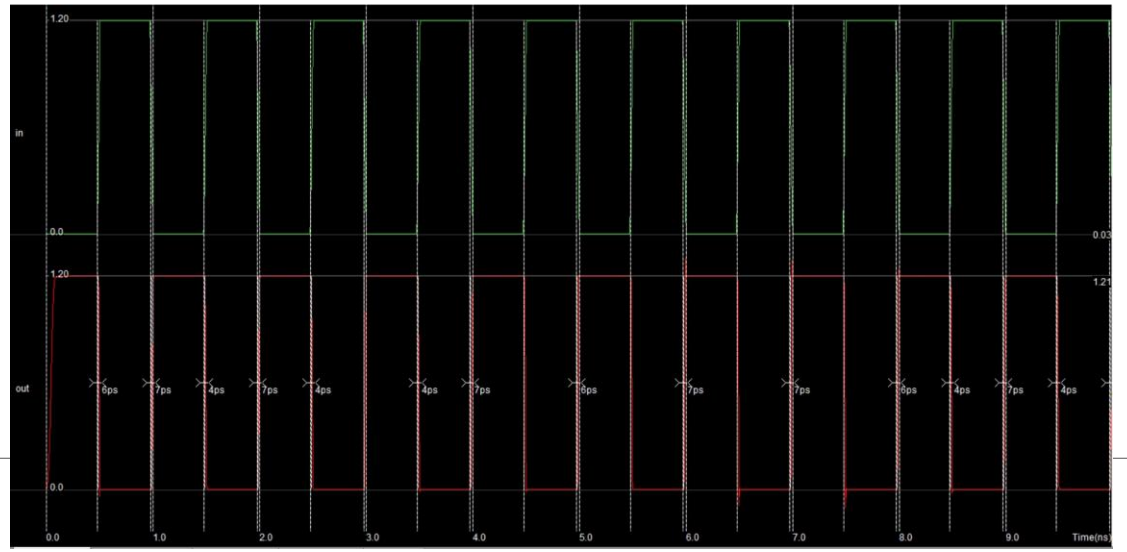


CMOS Inverter layout

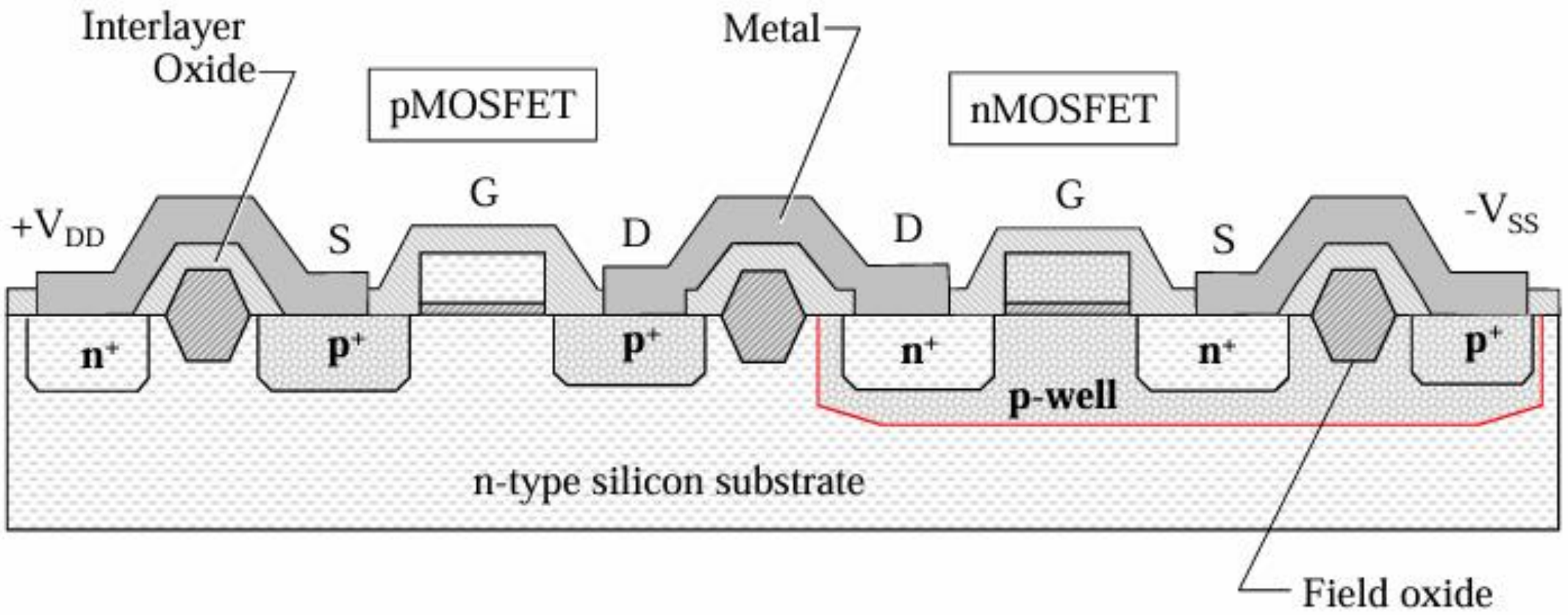




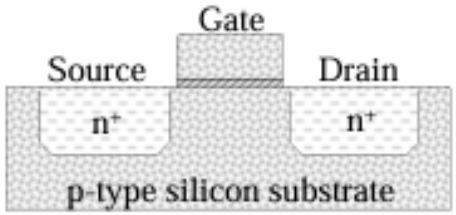
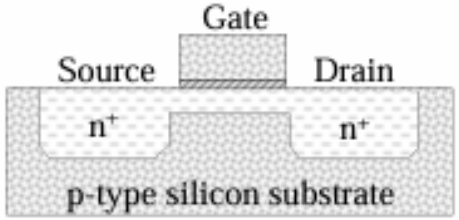
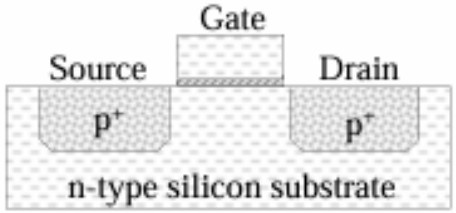
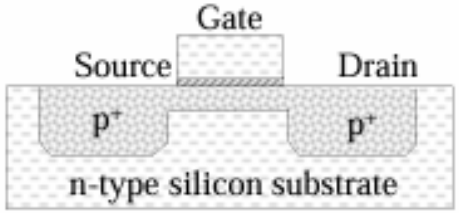




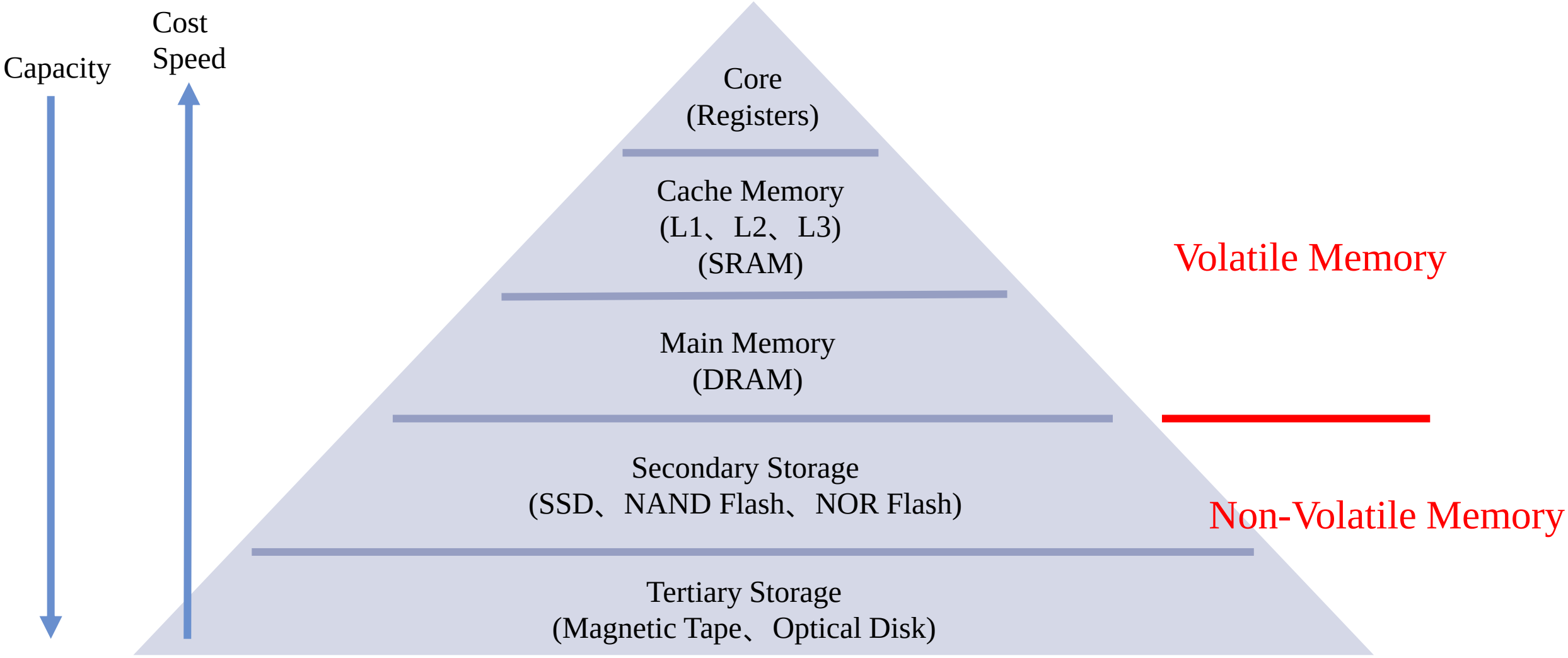
Cross-section of CMOS Inverter



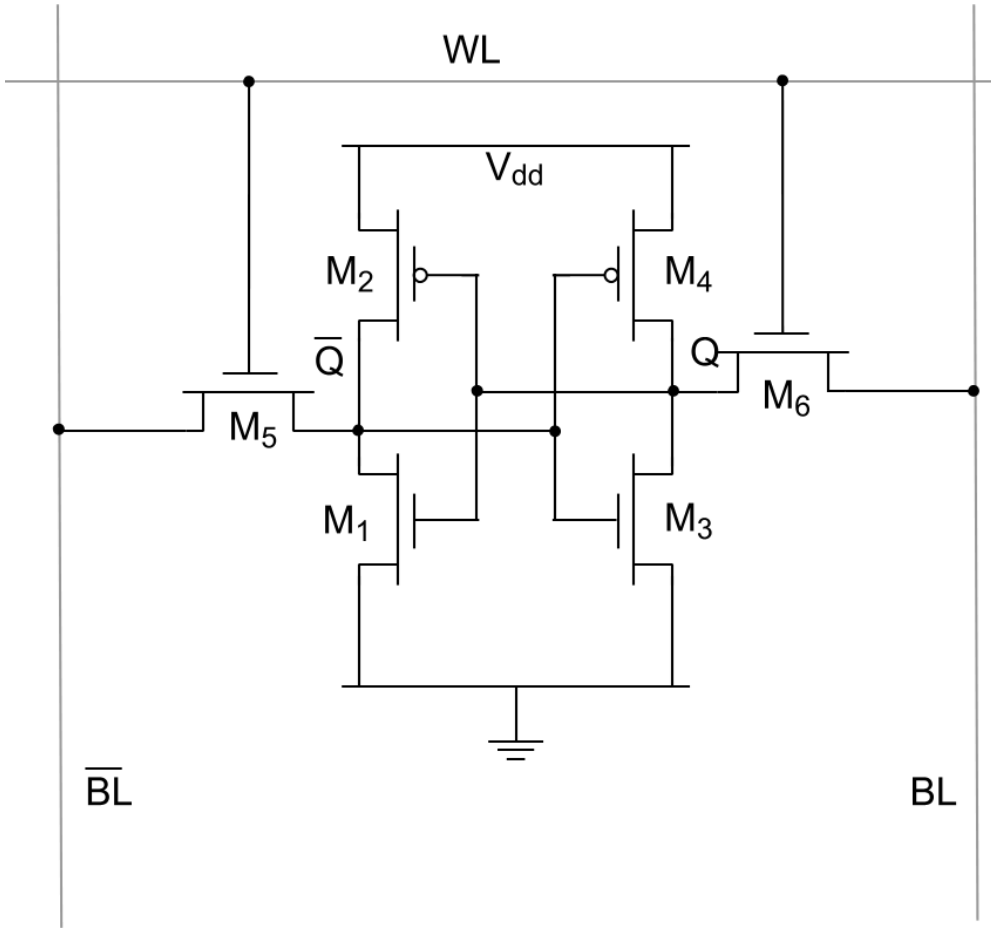
Comparison of Enhancement and Depletion Mode MOSFETs

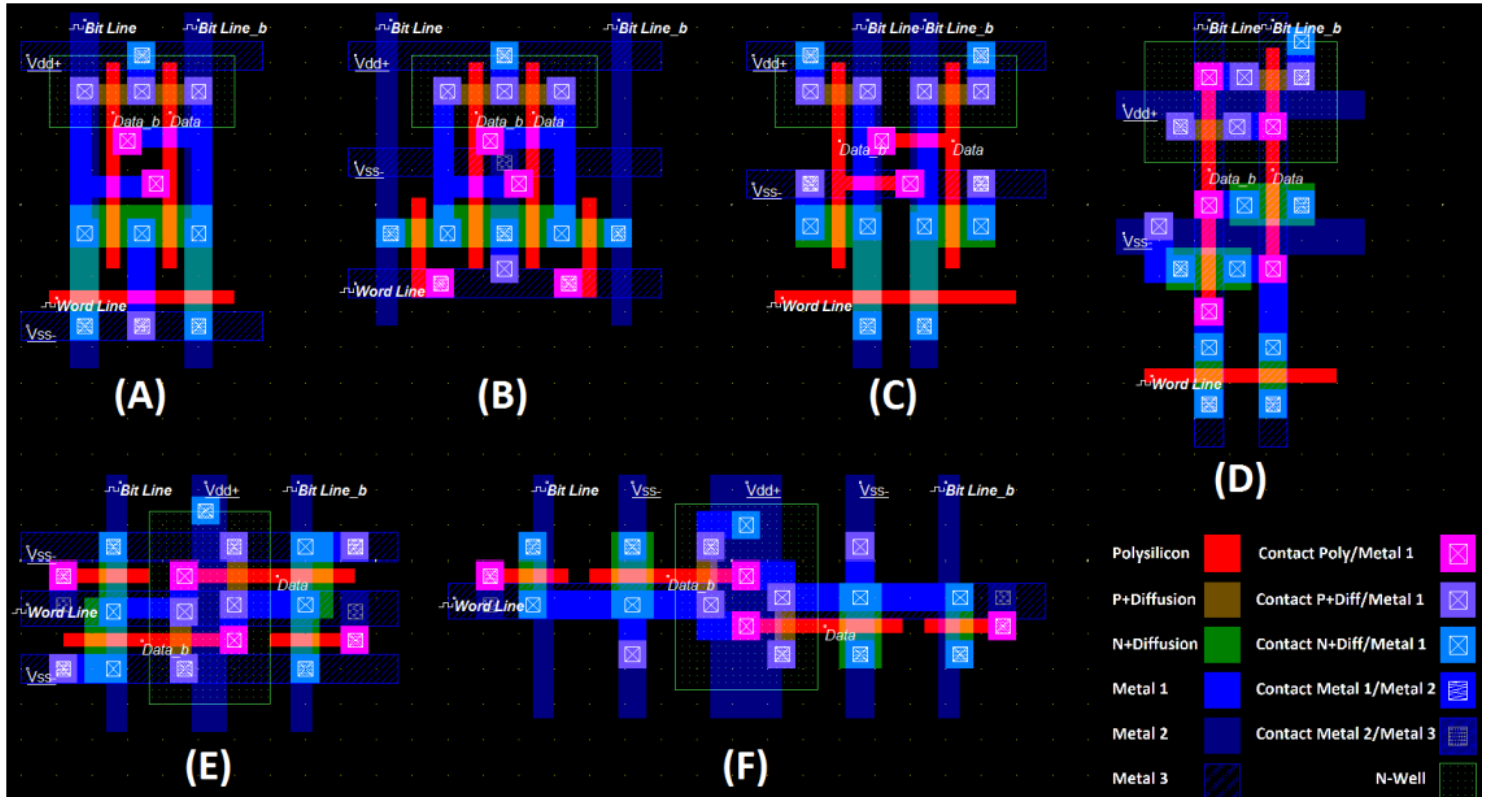
MOSFET Type	Mode	Standby Condition	V_{GG} Switching Requirements	Physical Structure
nMOS	Enhancement	Off	+	
nMOS	Depletion	On	-	
pMOS	Enhancement	Off	-	
pMOS	Depletion	On	+	

Memory Hierarchy



SRAM





6T-SRAM

Source: Wikipedia

The Key Parameter for The Semiconductor Device

Major Customer Care-abouts (= Technology driving forces) for Electronic Products

- **Appeal** (screen (LCD or OLED), size, color, metallic) , **User Friendliness** (OS, UI), **Camera functions, Ergonomic, ...** ➔ **beyond EE**

- **Functionality (or Chip Area)**
  - e.g. single/dual/quad/octa-core AP (or CPU) + n-in-1 wifi (802.11ax/ac/n/g…) + all-in-1 modem (5G sub-6GHz/mm Wave, 4G LTE, TD-LTE, 3G CDMA, TDSCDMA, TDMA2000, 2G GSM, …)
- **Cost**
  -- Die size (= chip area), process cost (technology scaling), ***yield***, ..

- **Performance**
  - clock speed…
- **Power Consumption**
  - Packaging and cooling options
  - **Battery run time !**

- Pure scaling (i.e. if without new features) has some performance improvement, but cannot reduce power consumption by much.
- **Performance and power**: main focus of this course !.

- **These factors are often referred to as : "PPAC" (Power/Performance/Area/Cost)**

The Key Parameter for The Semiconductor Device

How to generate more functions from a given chip (or package) area ?
(How to continue the Moore's Law as device dimension is approaching atomic limit?) -- must go from 2D to 3D IC

Multi-chip 3D (incl. 2.5D) stacking **using TSV**
(in mass production)

-- many variations
-- TSMC is leading
-- also referred to as "heterogeneous integration" or "chiplet(s) 小晶片"

Single-chip Sequential (or Monolithic) 3D integration
(R&D phase)

Layer transfer (and bonding)

(similar to "smart cut" for SOI wafer)
-- Si, Ge, GaN … all possible (Intel)

Monolithic 3D integration (thin film deposition)

-- Poly-Si → crystalline FET (TSRI)
-- BEOL Metal-oxide FET (e.g. IGZO, UMC)
-- others (e.g. CNT, TSMC)

Via density (/mm^2)	10^3	10^5	10^7
upper-layer FET proc. Temp.	no limit	< 400-500C	< 400-500C

- Higher via density ➔ higher band-width and versatility (better)
- Higher FET process Temp ➔ higher FET Idsat / performance / lower junc. leakage (better)
- Cost is another major factor to be considered (later..)

The Key Parameter for The Semiconductor Device

Moore's Law and Cost Reduction

- Cost reduciton: It's easy to explain through a fixed function application, e.g. WiFi 802.11 a/b/g/n/ac (5th) /ax(6th) combo chip (by BRCM or Realtek). Designers can use either 40nm or 28nm) CMOS.

  ➔ assume: 1) 28nm wafer price / 40nm wafer price = 1.6 (roughly true)
  2) same yield for both processes = assumed 100% (will examine yield later)
  28nm GDW (gross die per wafer) / 40nm GDW = $1/(28/40)^2 = 2.04$
  ∴ 28nm cost per die / 40nm cost per die = 1.6/2.04 *100% = 78%

  ➔ But market price for this WiFi chip is pretty much the same for either processes.

  ➔ So whoever can scale from 40nm to 28nm *first* can enjoy a larger profit margin, or can *lower the market price to drive the laggard competitors (using 40nm) out of business*! *(so in order to survive, everybody needs to keep up the cut-throat scaling pace ➔ Moore's Law !)*

  ➔ This is particularly true for memory markets, because memory functions are very standard (e.g. PC-grade or Mobile-grade DDR1/2/3/4 DRAM, or MLC/TLC 128/256Gbit 3D- NAND Flash) -- so-called "commodity products".

  ➔ To scale faster than everybody else is the key (and perhaps only) memory strategy for Samsung (and Hynix) 三星記憶體 的 最主要戰略 . Big companies like Hitachi, NEC, Mitsubishi, Matsushita, Toshiba, Elpida, Intel, TI, IBM, Siemens, Infineon, STM, Qimonda, Vanguard, ... were all driven out of DRAM business over time!