Semiconductor Manufacturing Technology

Chapter 4

Silicon and Wafer Preparation

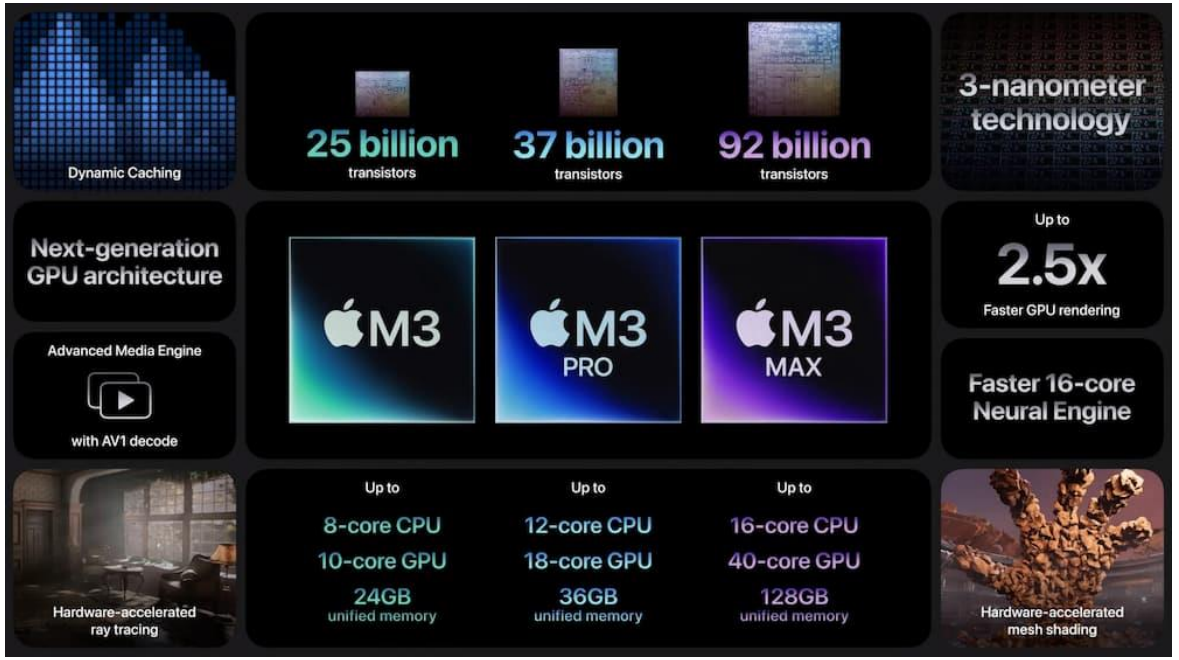
Objectives

- Describe the advantage and challenge for silicon.
- Describe how raw silicon is refined into semiconductor grade silicon.
- Explain the crystal structure and growth method for producing monocrystal silicon.
- Discuss the major defects in silicon crystal.
- Outline and describe the basic process steps for wafer preparation, starting from a silicon ingot and finishing with a wafer.
- State and discuss seven quality measures for wafer suppliers.
- Explain what is epitaxy and why it is important for wafers.

Advantage of Si technology

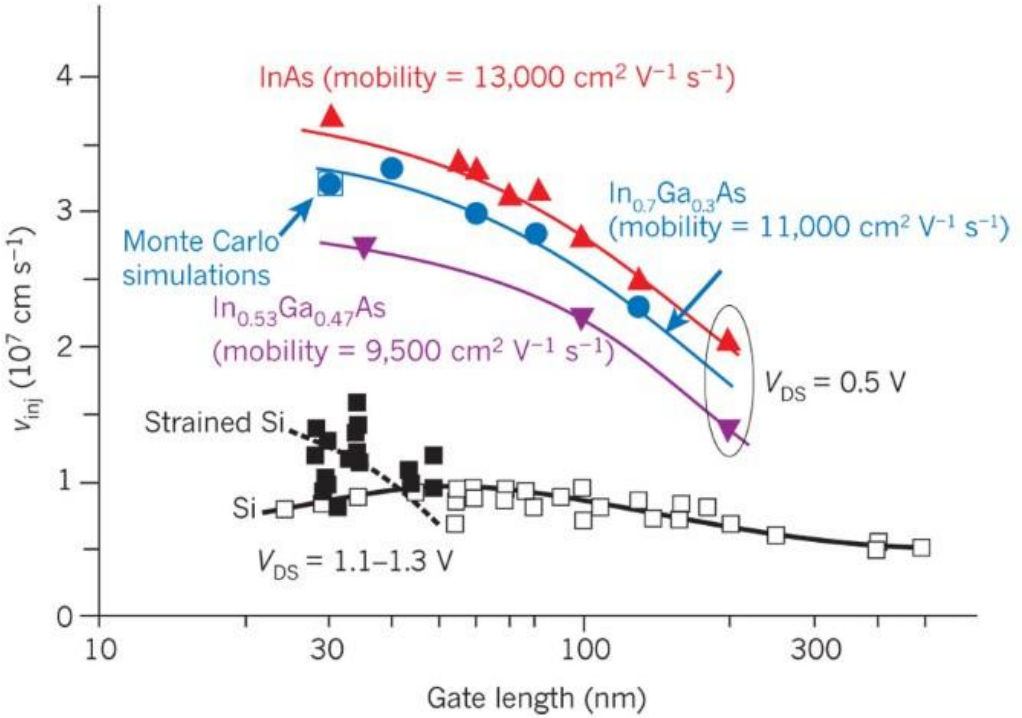
- Scalable
- Operation frequency
- Complementary metal-oxide-semiconductor design
- Low power (turn-on power)
- Low cost

目前手機晶片還說動則150億顆電晶體起跳，若是專門給HPC、AI、挖擴等需要更強算力的應用來說，必然電晶體數量會更高



The main challenge for Si technology

- There is no perfect material in nature, so silicon still exist some disadvantage, likewise
  - Indirect bandgap (optoelectrical application)
  - Narrow bandgap (high power application)
  - Operation frequency still not enough (communication application)
- But the main challenge for Si is not the characteristics mentioned above, scalable problem is.

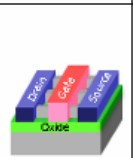
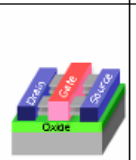
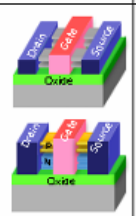
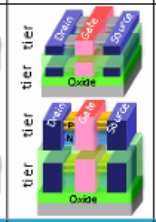
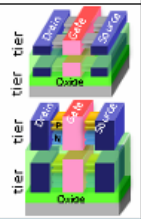
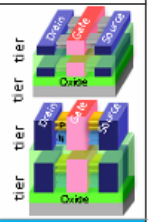


Source: Jesús A. del Alamo, Nanometre-scale electronics with III–V compound semiconductors, Nature 479, pages317–323 (2011)

The main challenge for Si technology

Table MM-7 Device Architecture and Ground Rules Roadmap for Logic Devices.

Note: GxxMxx/Tx notation refers to Gxx: contacted gate pitch, Mxx: tightest metal pitch in nm, Tx: number of tiers. This notation illustrates the technology pitch scaling capability. On top of pitch scaling there are other elements such as cell height, number of stacked devices, DTCO constructs, 3D integration, etc. that define the target area scaling (gates/mm^2).

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length – HP (nm)	16	14	12	12	12	12
Lg: Gate Length – HD (nm)	18	14	12	12	12	12
Channel overlap ratio – two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) – finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency – finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) – HP		30	30	20	15	15
LGAA width (nm) – HD		15	10	10	6	6
LGAA width (nm) – SRAM		7	6	6	6	6
Footprint drive efficiency – lateral GAA – HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) – HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) – HD	101.0	126.0	96.0	128.0	88.0	80.0
PN seperation width (nm)	45	40	20	15	15	10

Acronyms used in the table (in order of appearance): LGAA—lateral gate-all-around-device (GAA), CFET (Complementary Field Effect Transistor), 3DVLSI—fine-pitch 3D logic sequential integration.

Source: IEEE, More Moore, 2022 International roadmaps devices and system

The main challenge for Si technology

power

Performance

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
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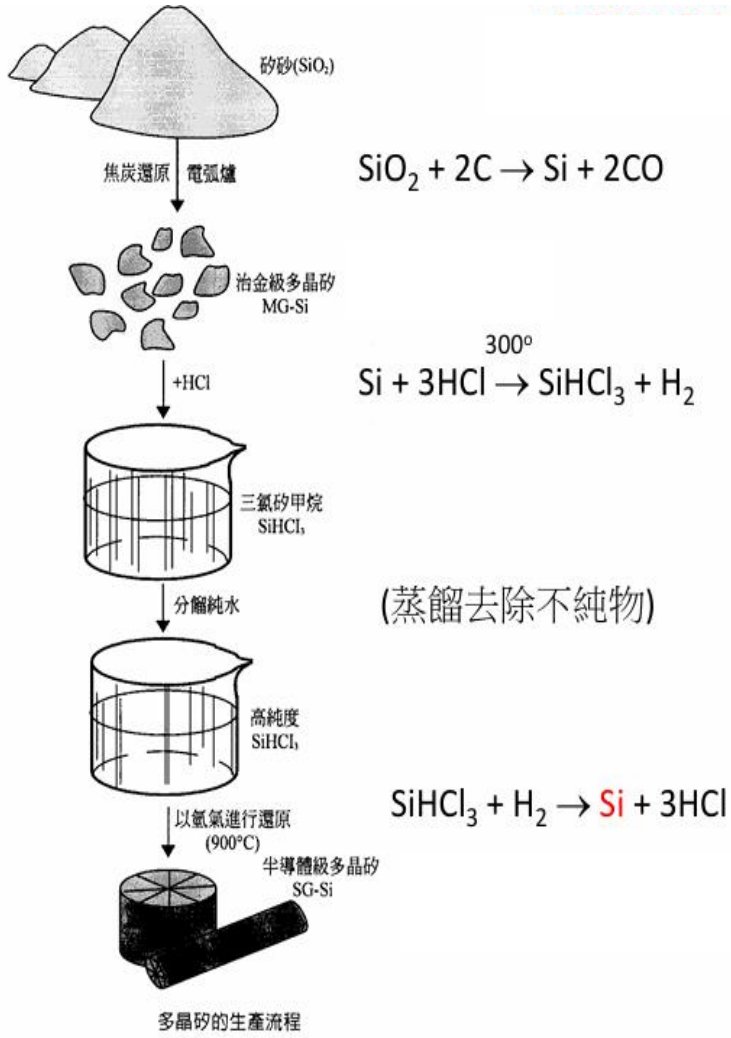
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
LOGIC DEVICE ELECTRICAL SPECS						
Power Supply Voltage - Vdd (V)	0.70	0.65	0.65	0.60	0.60	0.60
Subthreshold slope (mV/dec) - HP (mV/dec)	82	72	70	70	70	70
Subthreshold slope (mV/dec) - HD (mV/dec)	75	67	67	65	65	65
Capacitive equivalent thickness (CET) (nm) [2]	1.00	1.00	0.90	0.90	0.90	0.90
Vt,sat at Ioff=10nA/um - HP (mV)	156	165	165	164	156	154
Vt,sat (mV) at Ioff=100pA/um - HD (mV) [3][4]	288	271	268	268	258	255
Effective mobility (cm2/V.s)	125	100	80	60	40	40
Rsd (Ohms.um) [5]	271	257	245	232	221	210
Ballisticity,Injection velocity (cm/s)	9.00E+06	9.00E+06	9.00E+06	9.00E+06	9.00E+06	9.00E+06
Vdsat (V) - HP	0.092	0.101	0.108	0.144	0.216	0.216
Vdsat (V) - HD	0.104	0.101	0.108	0.144	0.216	0.216
Ion (uA/um) at Ioff=10nA/um - HP [6]	874	787	851	753	737	753
Ion (uA/device) at Ioff=10nA/um - HP [7]	88	170	184	157	118	115
Ion (uA/um) at Ioff=100pA/um - HD [8]	644	602	656	551	532	547
Ion (uA/device) at Ioff=100pA/um - HD [9]	65	130	142	115	85	83
Cch,total (fF/um2) - HP/HD [8]	34.52	34.52	38.35	38.35	38.35	38.35
Gate height over fin (nm)	20	15	10	10	10	10
Cch (fF/um) - HP [8]	0.44	0.39	0.37	0.37	0.37	0.37
Cch (fF/um) - HD [8]	0.50	0.39	0.37	0.37	0.37	0.37
CV/I (ps) - FO3 load, HP [9]	1.06	0.96	0.84	0.88	0.90	0.88
I/(CV) (1/ps) - FO3 load, HP [10]	0.94	1.04	1.18	1.14	1.11	1.14
Energy per switching (CV2) (fJ/switch) - FO3 load, HP	0.65	0.49	0.47	0.40	0.40	0.40
ANALOG SPECIFICATIONS OF LOGIC DEVICE						
Transconductance - gm (µS/µm)	1605	1621	1751	1725	1653	1684
High-current gain cut-off frequency - fT (GHz)	261	304	358	411	403	411
Maximum oscillation frequency - fmax (GHz)	169	175	166	210	233	240
1/f-noise (µV²-µm²/Hz)	16	16	13	13	13	13
Analog gain (dB)	42	40	36	38	39	39
Minimum noise figure - Nfmin (60GHz) (dB)	1.6	1.4	1.3	1.1	1.1	1.1
Maximum stable gain - MSG (60GHz) (dB)	11.1	10.0	13.5	14.3	14.2	14.3

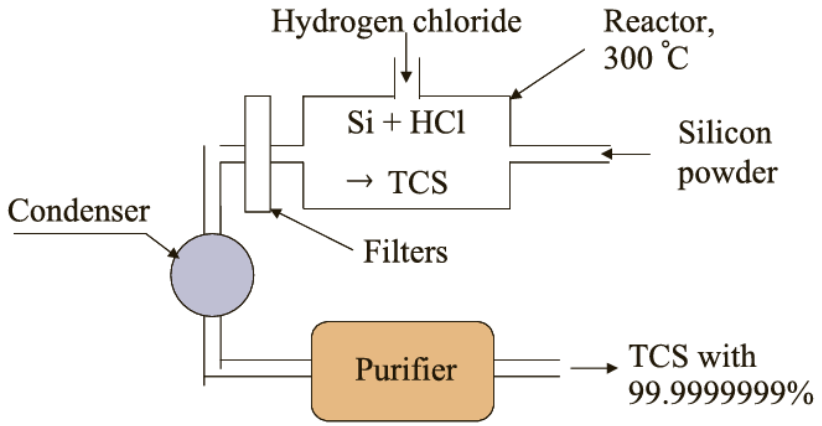
Source: IEEE, More Moore, 2022 International roadmaps devices and system

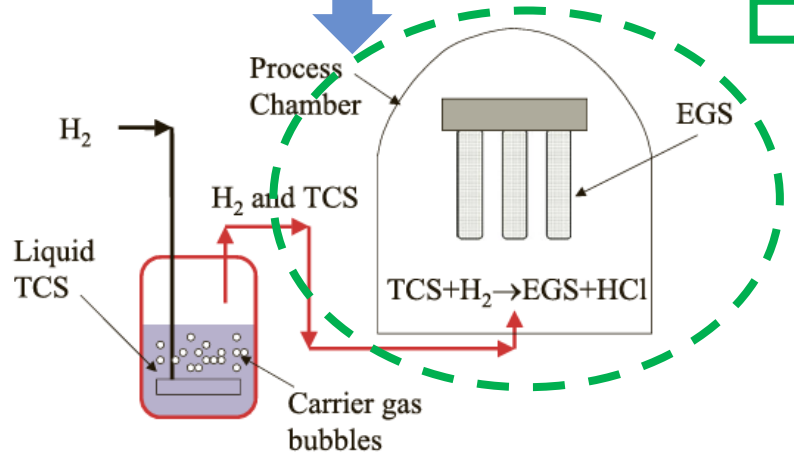
Semiconductor-Grade Silicon

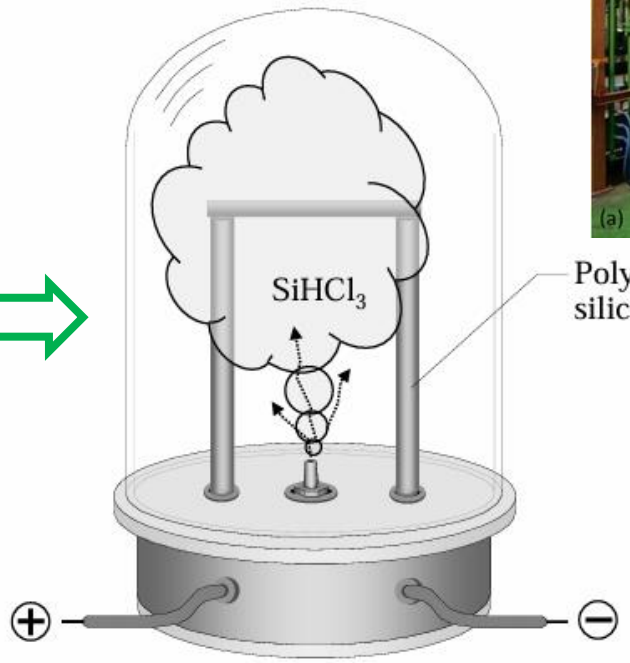
Steps to Obtaining Semiconductor Grade Silicon (SGS)		
Step	Description of Process	Reaction
1	Produce metallurgical grade silicon (MGS) by heating silica with carbon	SiC or C (s) + SiO2 (s) → Si (l) + SiO(g) + CO (g)
2	Purify MG silicon through a chemical reaction to produce a silicon-bearing gas of trichlorosilane ($SiHCl_3$)	Si (s) + 3HCl (g) → $SiHCl_3$ (g) + H_2 (g) + heat
3	$SiHCl_3$ and hydrogen react in a process called Siemens to obtain pure semiconductor- grade silicon (SGS)	2$SiHCl_3$ (g) + 2H_2 (g) → 2Si (s) + 6HCl (g)



Siemens Reactor for SG Silicon





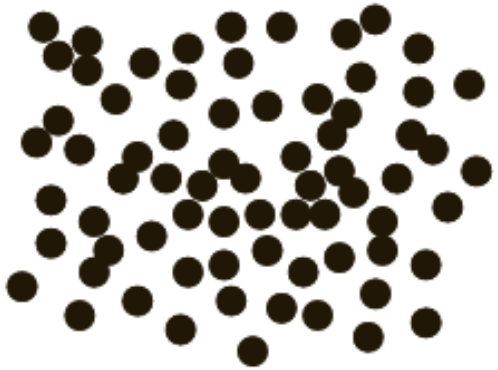


Crystal Structure

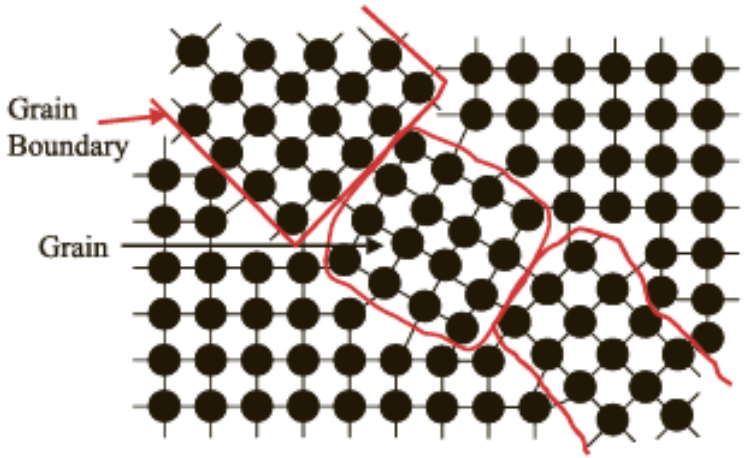
- Amorphous
  - ➢No repeated structure
- Polycrystalline
  - ➢Some repeated structure
- Single crystal
  - ➢One repeated structure

	Amorphous	Polycrystal	Single crystal
Mobility	低	次之	高
Cost	便宜	次之	最貴

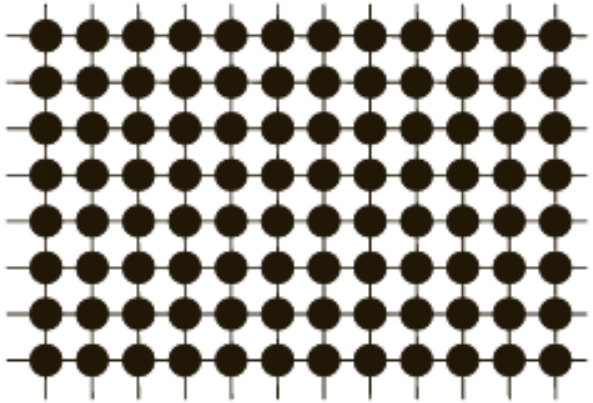
Amorphous structure



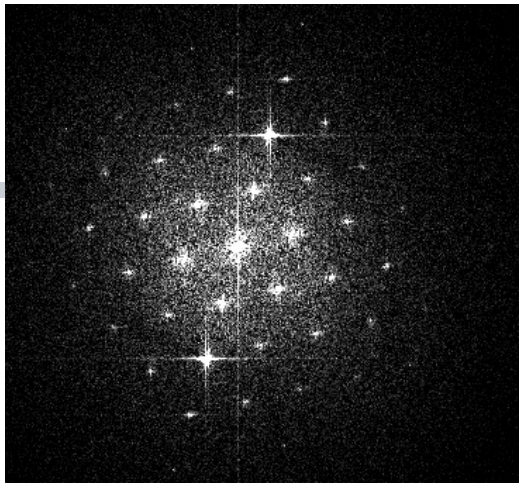
Polycrystalline Structure



Single crystal structure

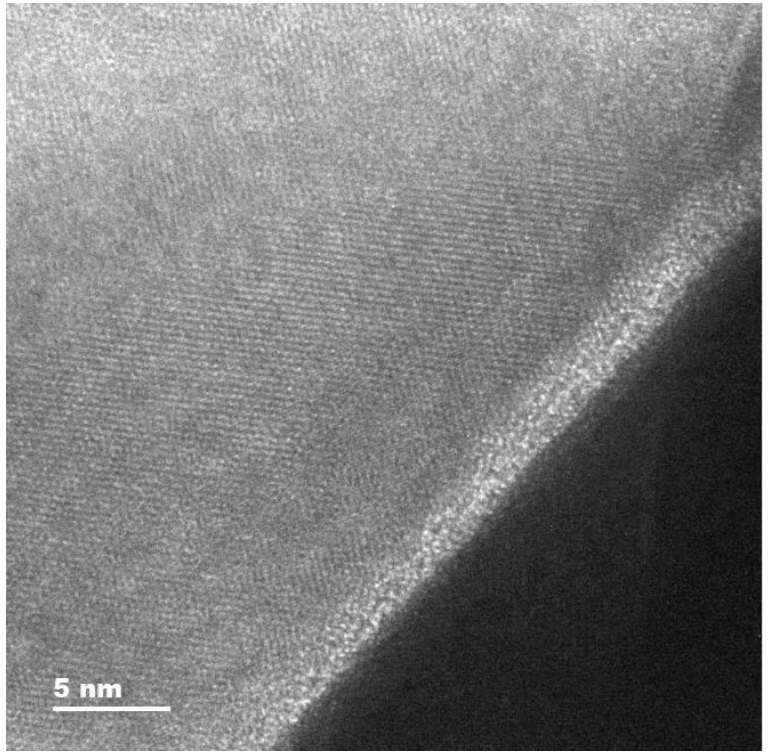


Crystal Structure (HRTEM image)

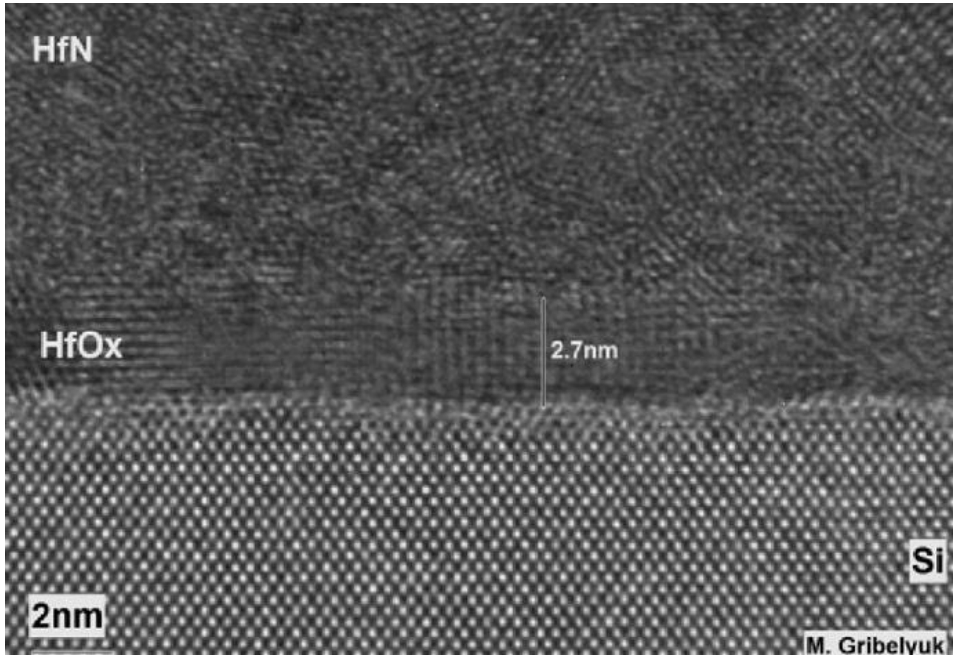


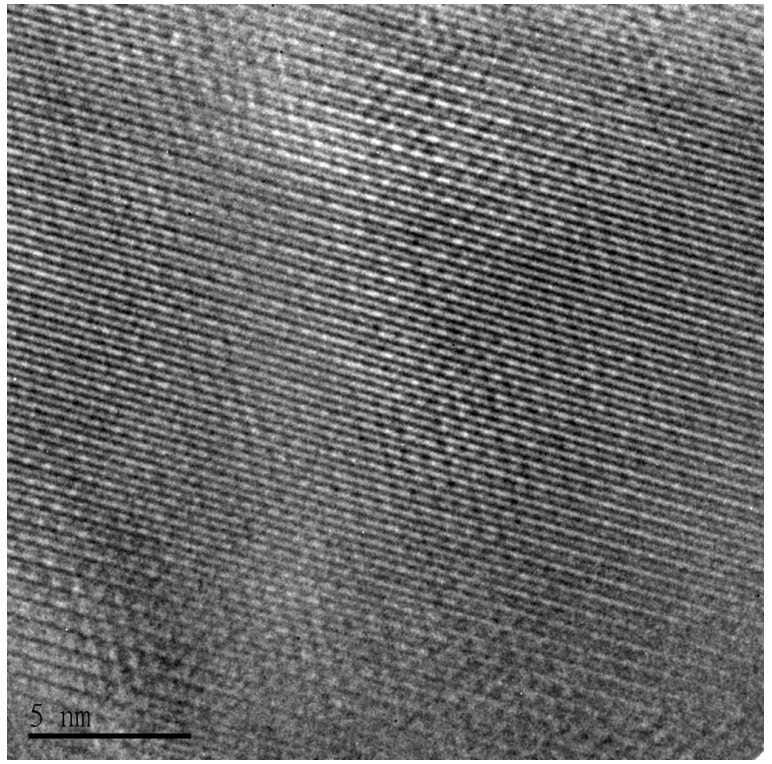
2D material

Low-k material



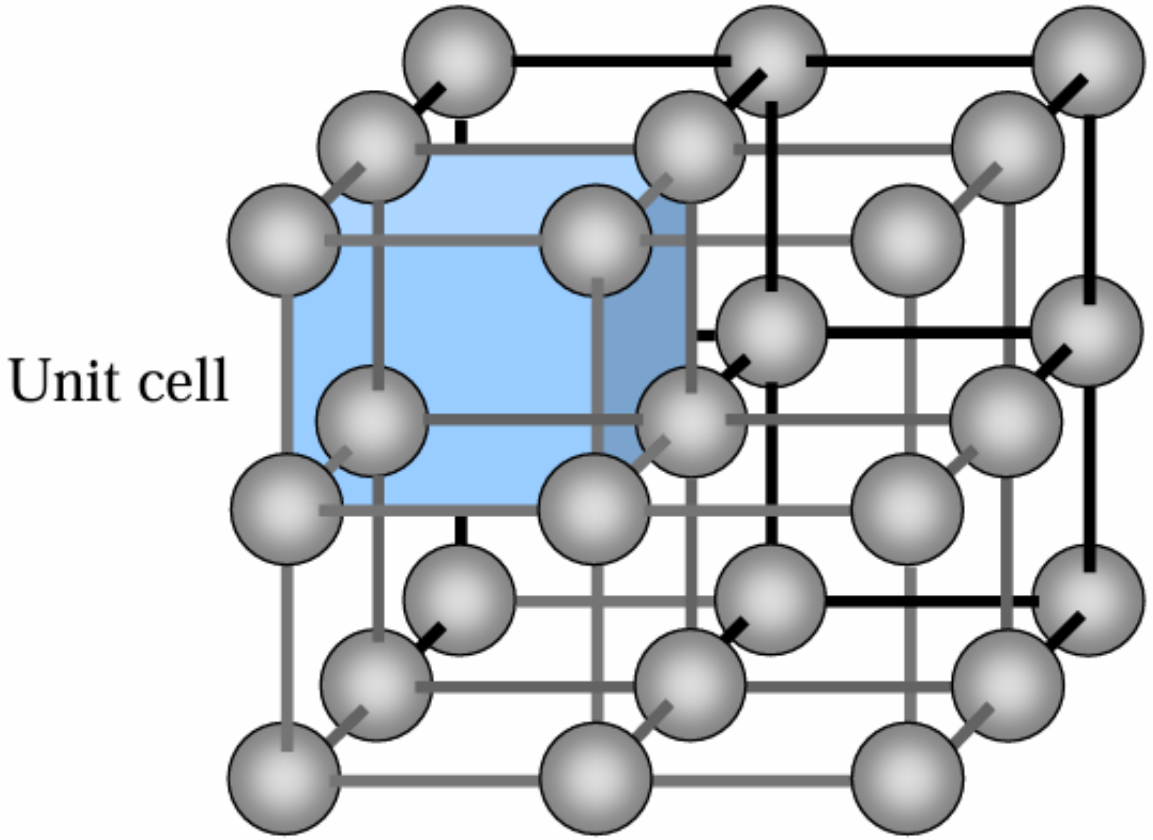
High-k material





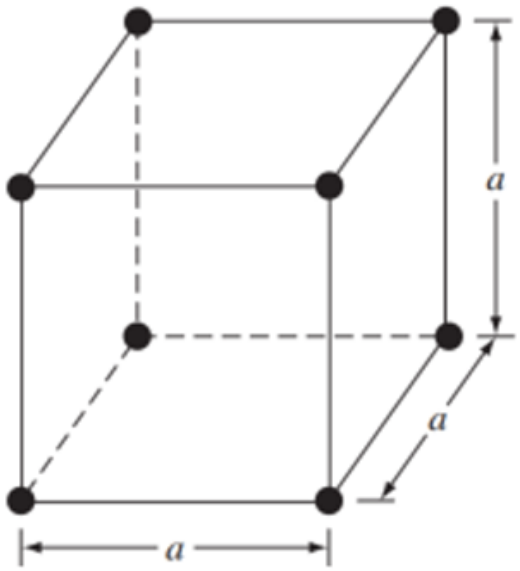
Unit cell

- Because the materials with a single crystal structure are arranged neatly and periodically, they can be described by the concept of unit cell

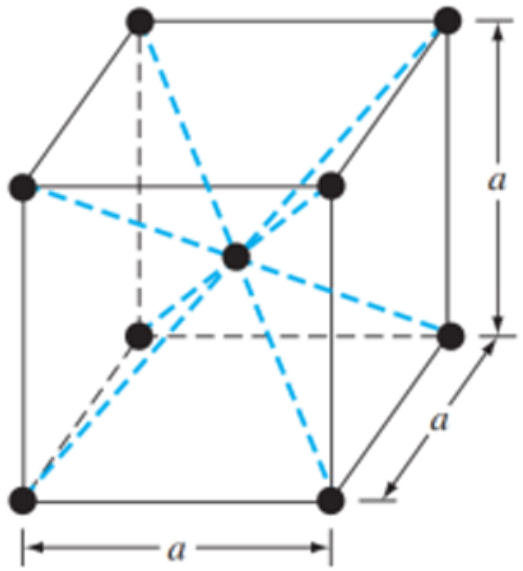


Some examples of unit cells (cubic structure)

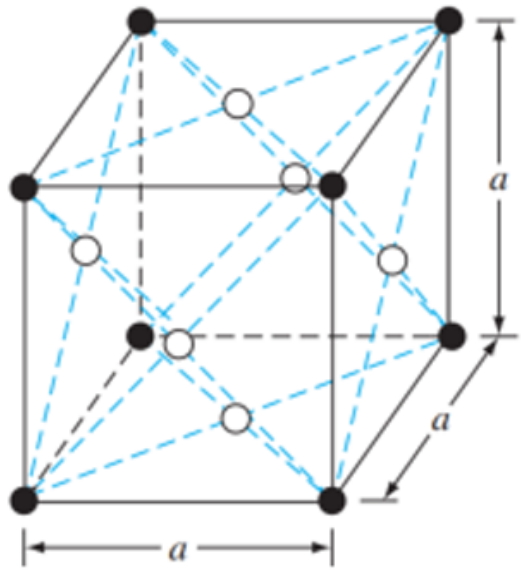
Simple cubic
(SC)
簡單立方



Body-centered cubic
(BCC)
體心立方

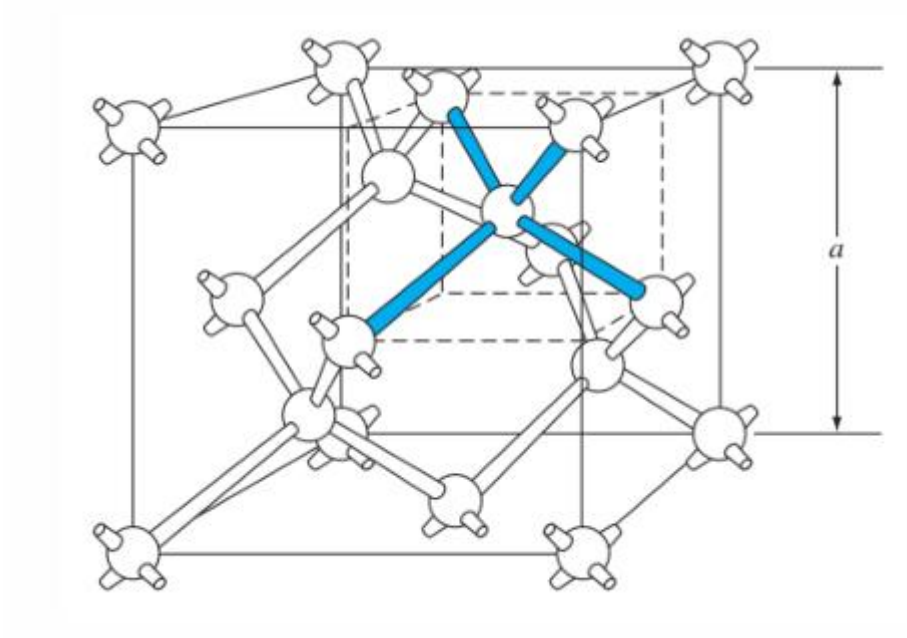


Face-centered cubic
(FCC)
面心立方

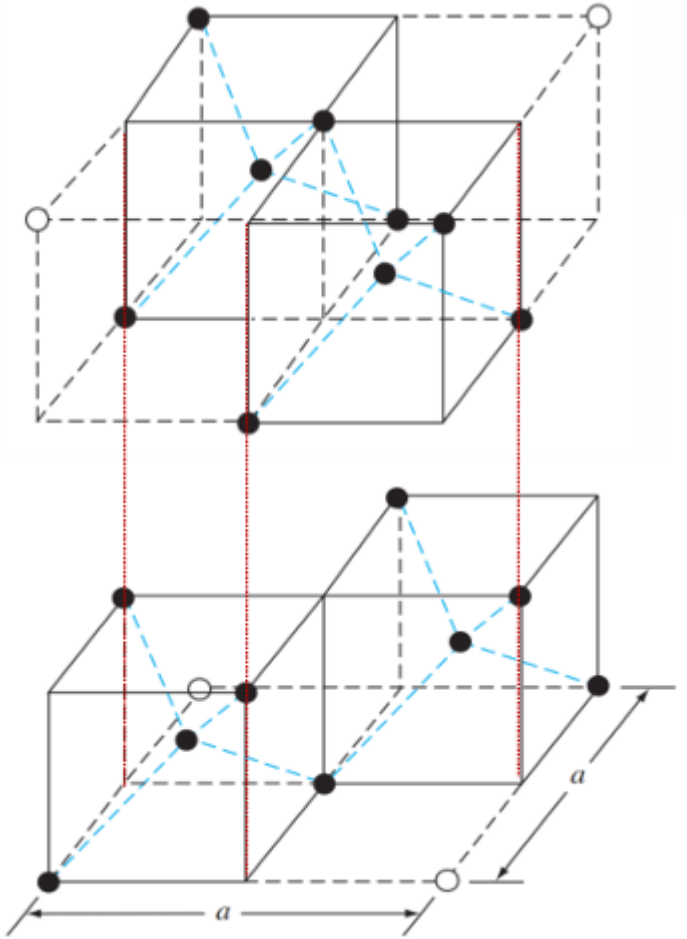


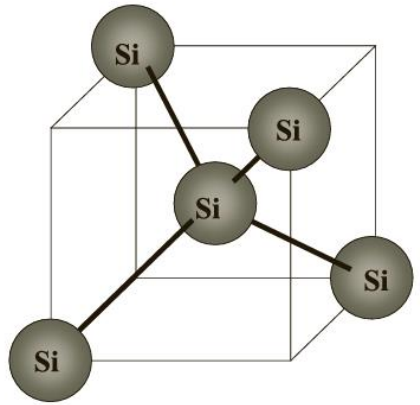
Silicon Unit Cell

FCC Diamond Structure



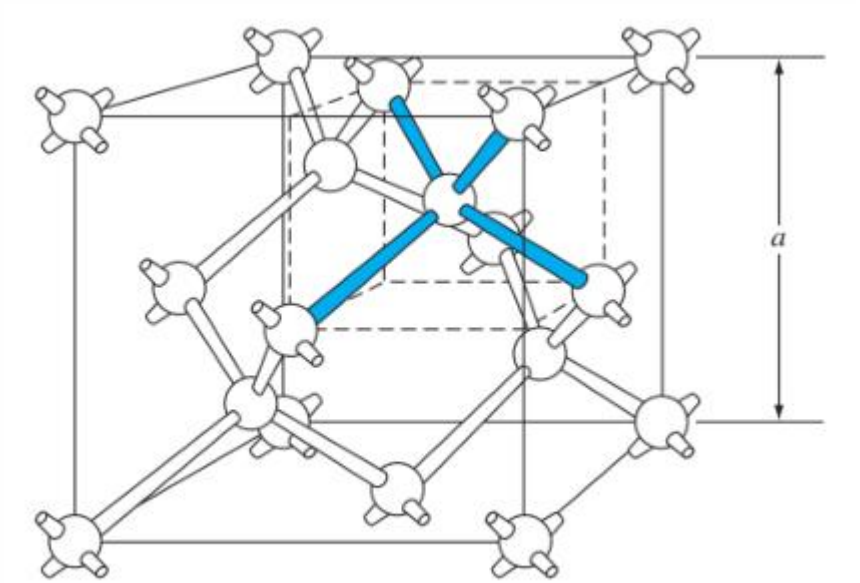
$$8 * \frac{1}{8} + 6 * \frac{1}{2} + 4 = 8\ atoms$$

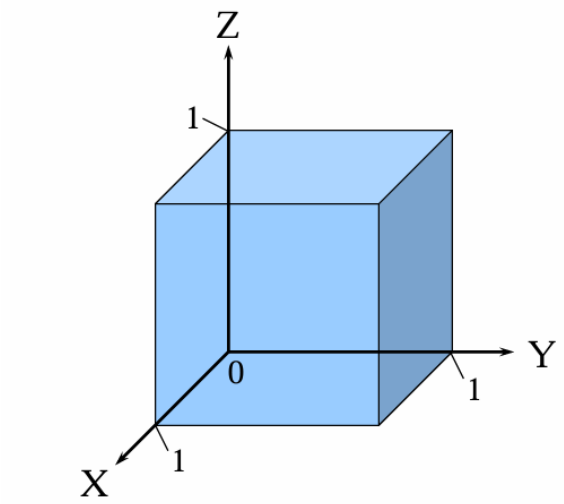




Description the orientation for unit cell

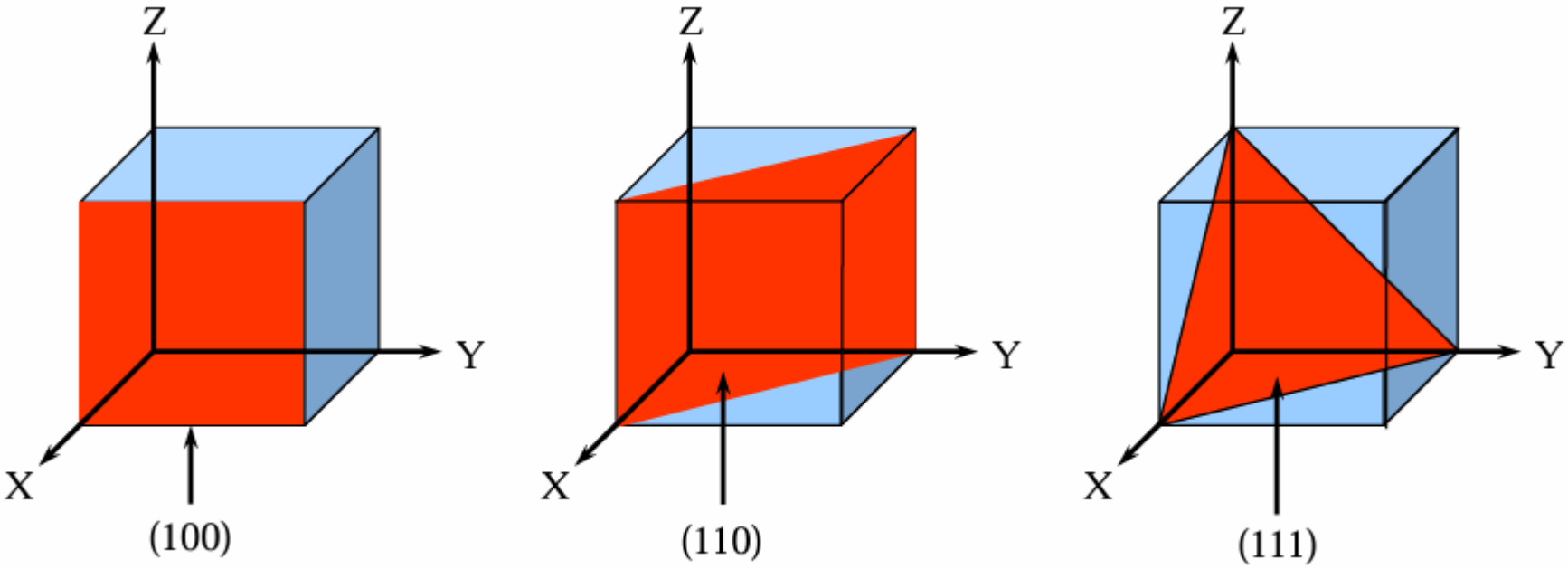
- This is the structure of Si in bulk, but it is not useful.
- Because semiconductor manufacturing process is essentially a planar process.





Miller index

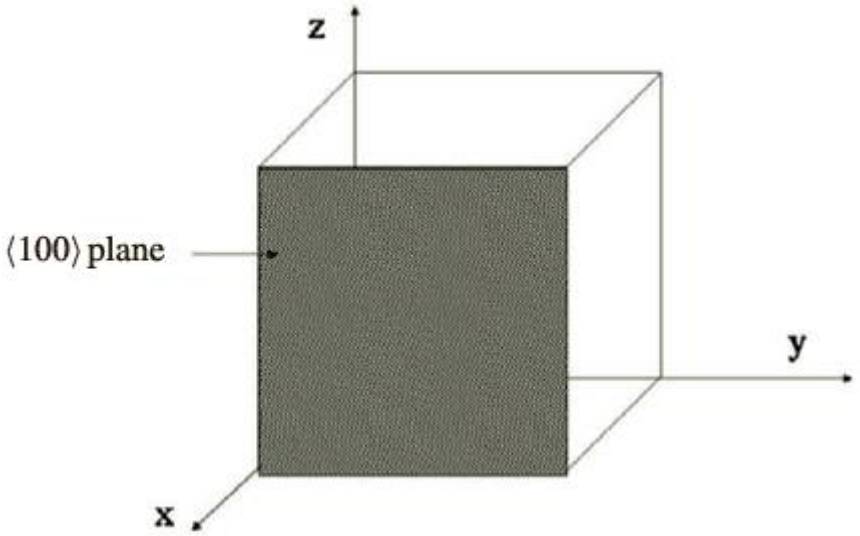
Miller Indices of Crystal Planes

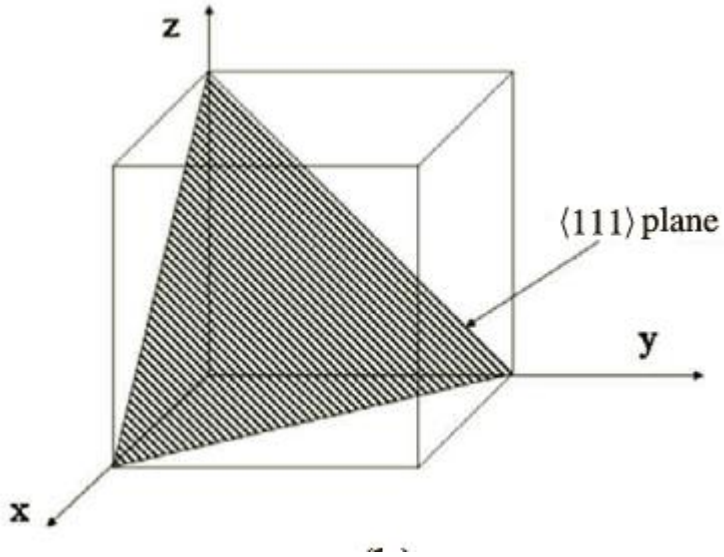


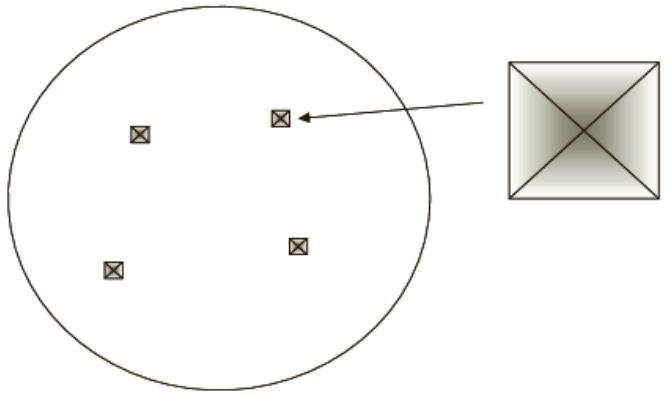
Indexing Procedure for Planes

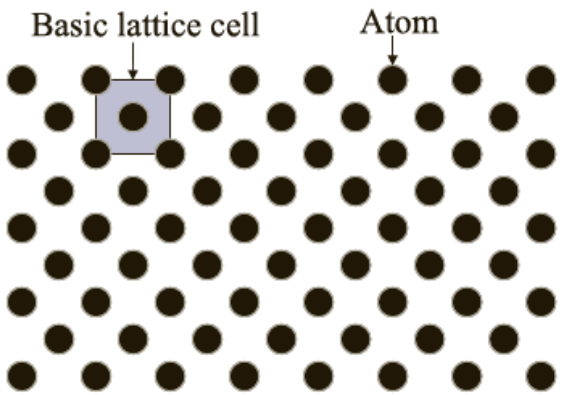
1. Record where the plane intercepts the axes in the unit of the unit cell length
2. Invert the intercept values
3. Convert to the smallest possible set of whole numbers
4. Enclose the whole-number set in parentheses

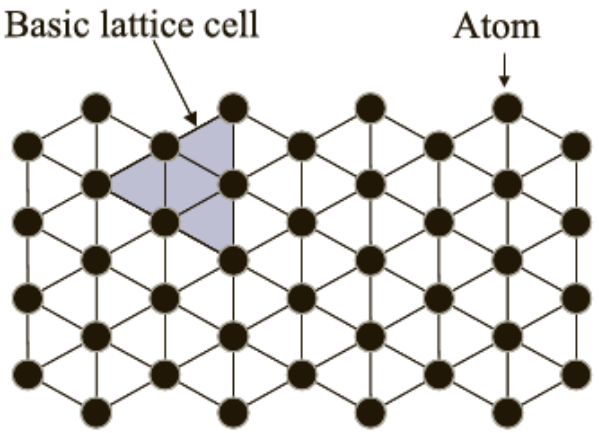
Most common use for Si plane

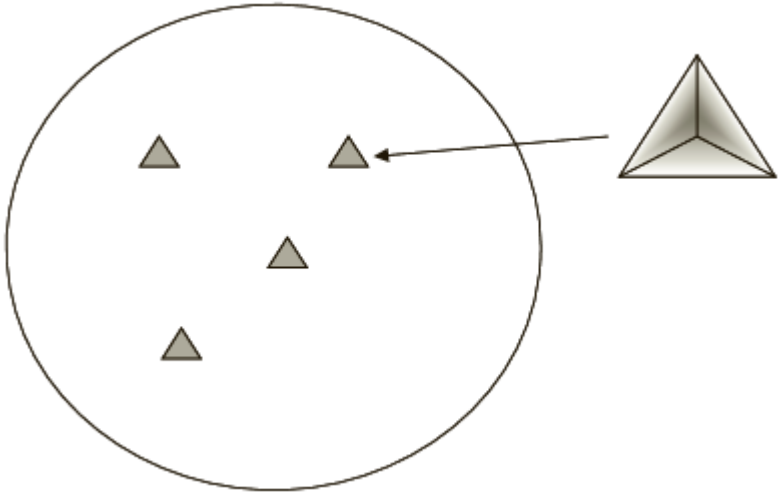








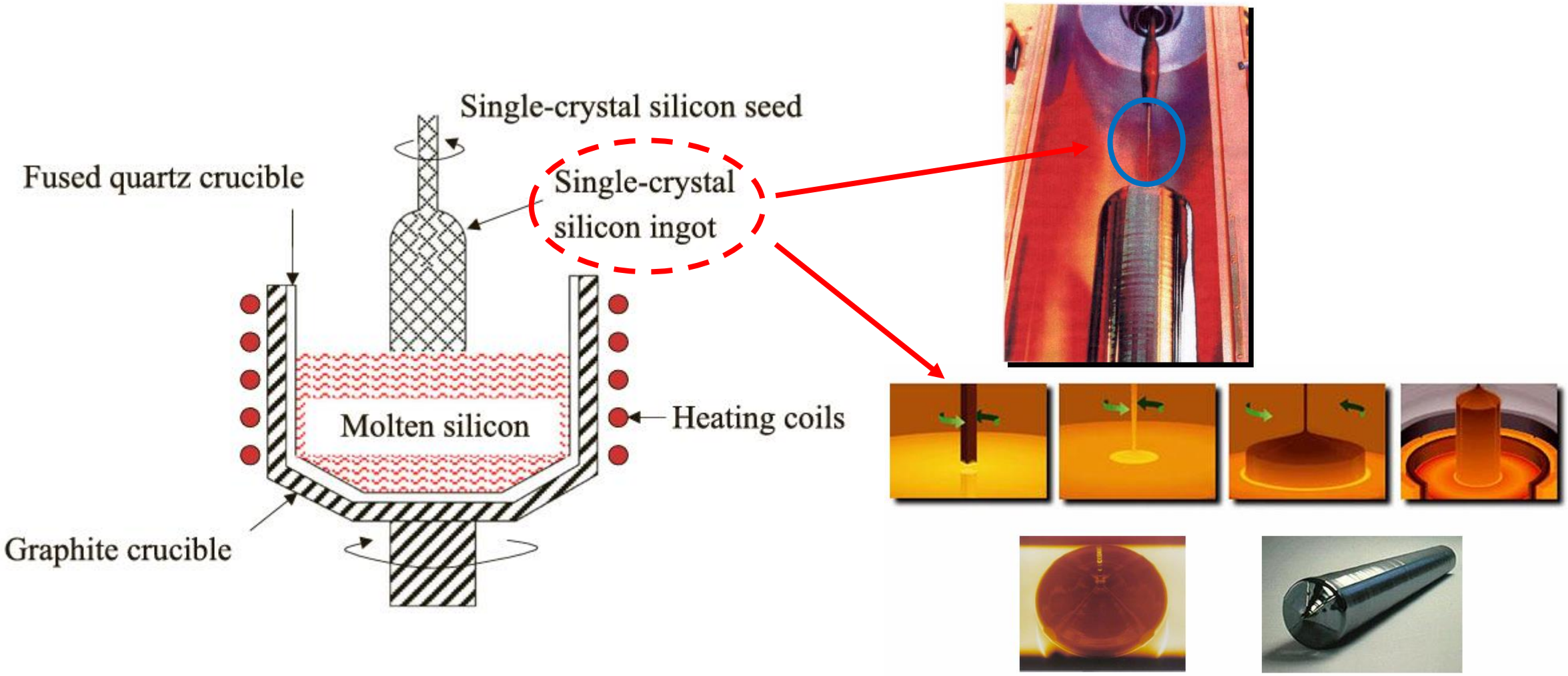




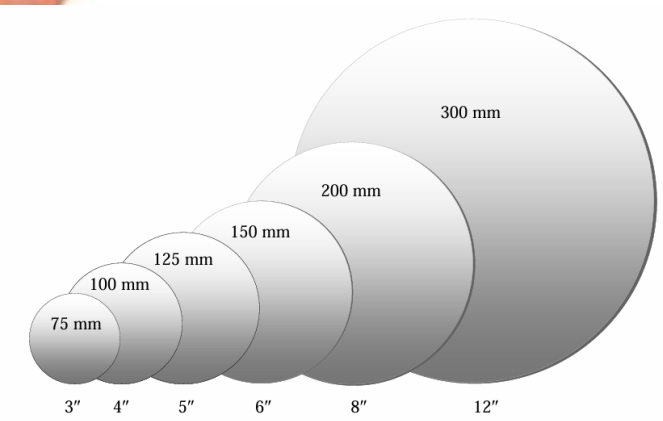
Monocrystal Silicon Growth (from SGS to crystal)

- CZ Method (Czochralski)
  - CZ Crystal Puller
  - Doping
  - Impurity Control
- Float-Zone Method
- Reasons for Larger Ingot Diameters

Czochralski (CZ) Crystal Growth



The size of Si wafer



The size of Si wafer

Wafer Size	2” (50.8mm)	3” (76.2mm)	4” (100mm)	5” (125mm)	6” (150mm)	8” (200mm)	12” (300mm)	18” (450mm)
Thickness	279 ± 25 um	381 ± 25 um	525 ± 20 um	625 ± 20 um	675 ± 20 um	725 ± 20 um	775 ± 20 um	925 ± 25 um
Weight	1.32 g	4.05 g	9.67 g	17.87 g	27.82 g	52.98 g	127.62 g	342.77 g
Primary Flat Length	15.88 ± 1.65 mm	22.22 ± 3.17 mm	32.5 ± 2.5 mm	42.5 ± 2.5 mm	57.5 ± 2.5 mm	Notch	Notch	Notch
Secondary Flat Length	8 ± 1.65 mm	11.18 ± 1.52 mm	18 ± 2 mm	27.5 ± 2.5 mm	37.5 ± 2.5 mm	NA	NA	NA
Secondary Flat Location	90 ± 5 degree clockwise from primary flat					NA	NA	NA
	45 ± 5 degree clockwise from primary flat							
	180 ± 5 degree clockwise from primary flat							

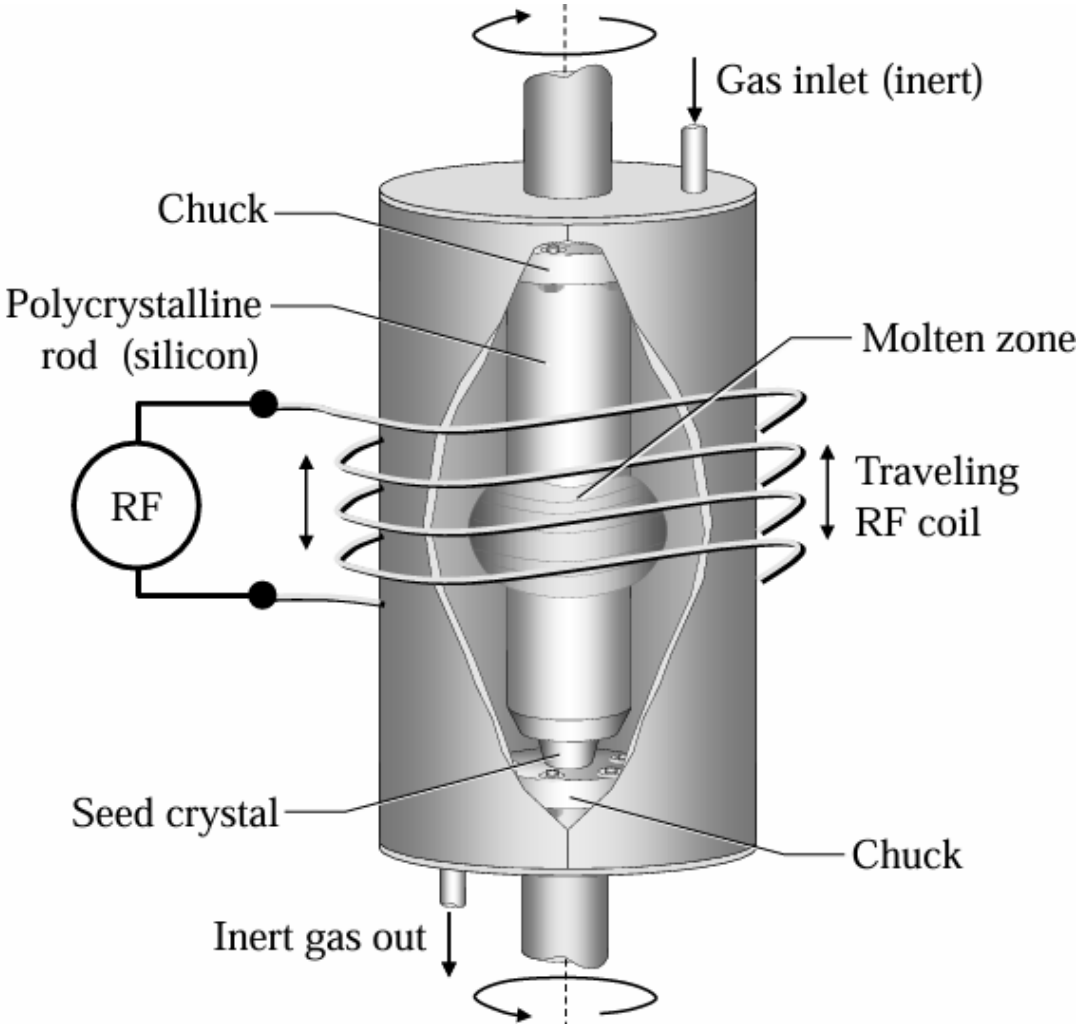
- Although the cost per individual chip decreases for design houses as wafer size increases, the yield actually decreases. Therefore, an 18-inch wafer is not as cost-effective as the market might assume.

Dopant Concentration Nomenclature

- In the single crystal silicon rods pulled using the Czochralski (CZ) method, the burning of the crucible introduces trace impurities of oxygen and carbon into the finished silicon rods.
- The oxygen content in these silicon rods is usually around 20 to 30 ppm.
- To achieve a uniform dopant distribution in silicon rods or wafer, high pulling speeds and low crucible rotation speeds can be utilized.

	Concentration (Atoms/cm^3)			
Dopant	$< 10^{14}$ (Very Lightly Doped)	10^{14} to 10^{16} (Lightly Doped)	10^{16} to 10^{19} (Doped)	$>10^{19}$ (Heavily Doped)
Pentavalent	n^{--}	n^{-}	n	n^{+}
Trivalent	p^{--}	p^{-}	p	p^{+}

Float Zone (FZ) Crystal Growth



- Smaller diameter (4-6 inch)
  - Since the silicon polycrystalline rods are vertically suspended in the machine, there will be gravity-related issues when growing larger-sized wafers
  - If the wafers are too large, there will also be issues related to thermal conductivity and melting
- High purity silicon wafer
- It is still necessary to use opposite rotation directions at the top and bottom to obtain high-quality silicon wafers

Crystal Defects in Silicon

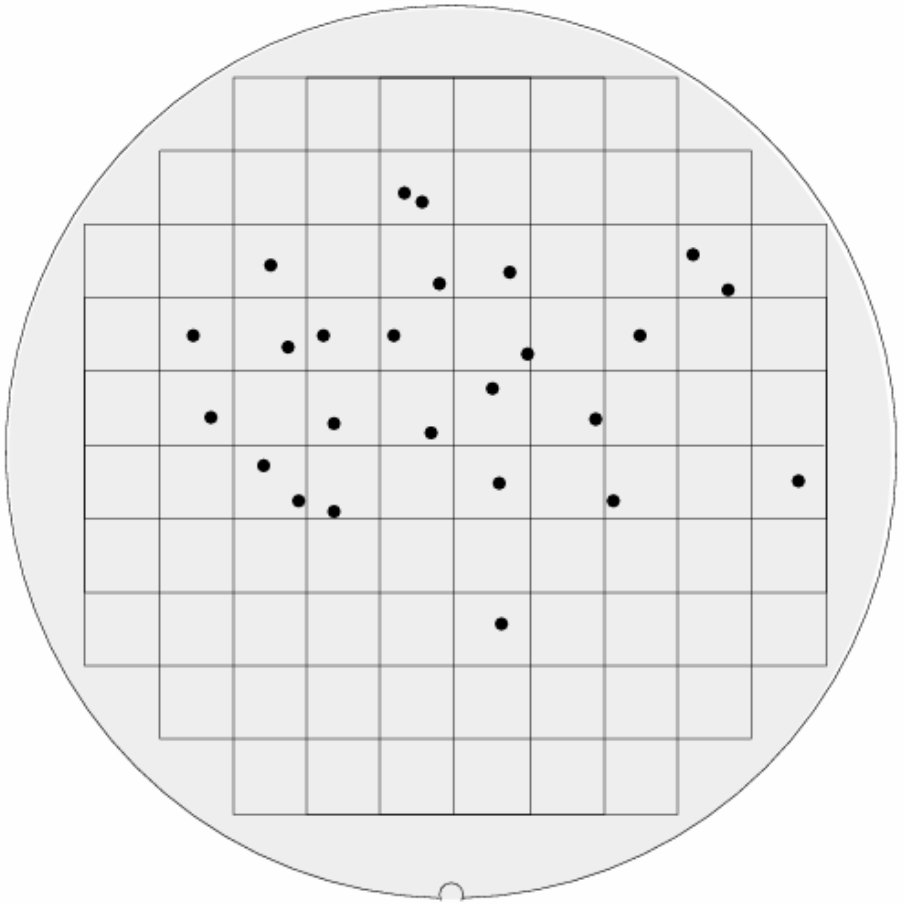
- A crystal defect (microdefect) is any interruption in the repetitive nature of the unit cell crystal structure

Three general types of crystal defects in silicon:

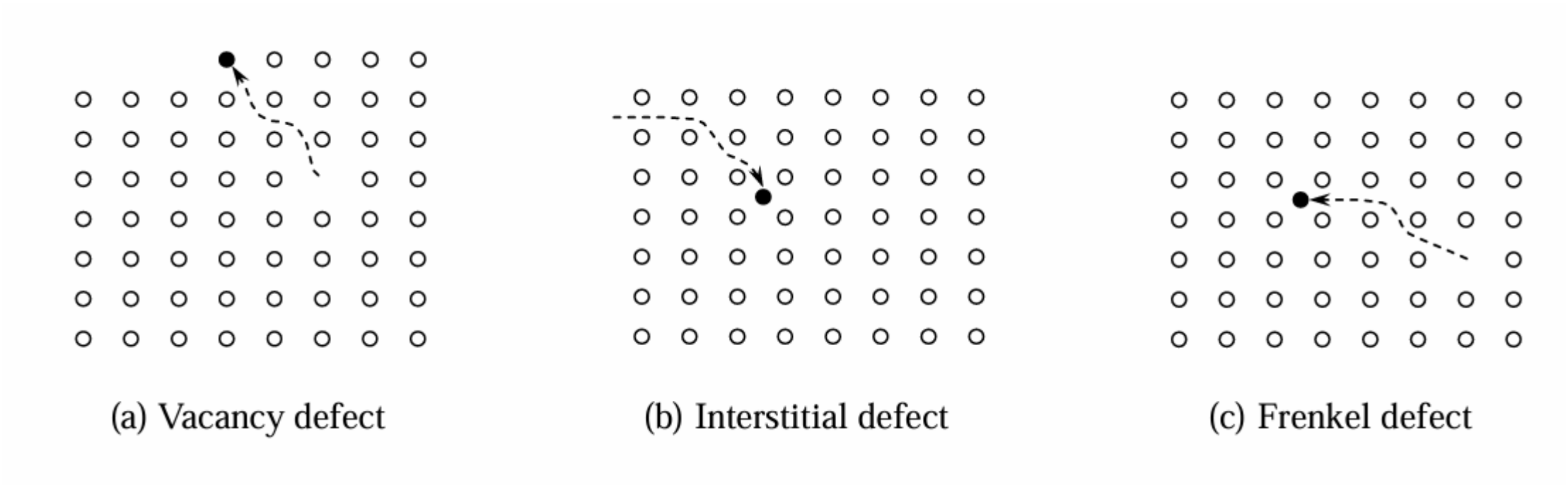
1. Point defects（點）
   - ➢ Localized crystal defect at the atomic level
2. Dislocations（線）
   - ➢ Displaced unit cells
3. Gross defects（面）
   - ➢ Defects in crystal structure

Yield of a Wafer

$$\text{Yield} = \frac{66 \text{ good die}}{88 \text{ total die}} = 75\%$$

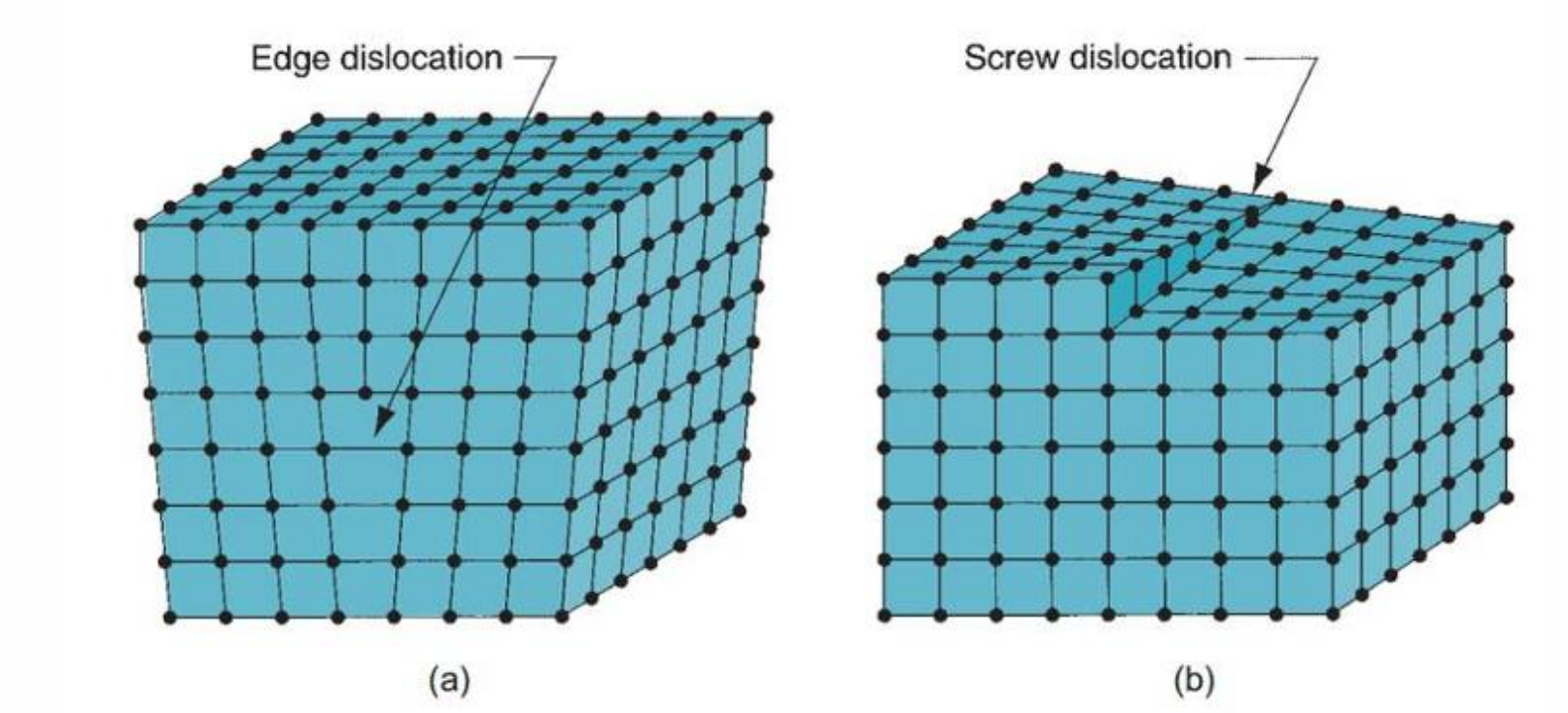


Point Defects

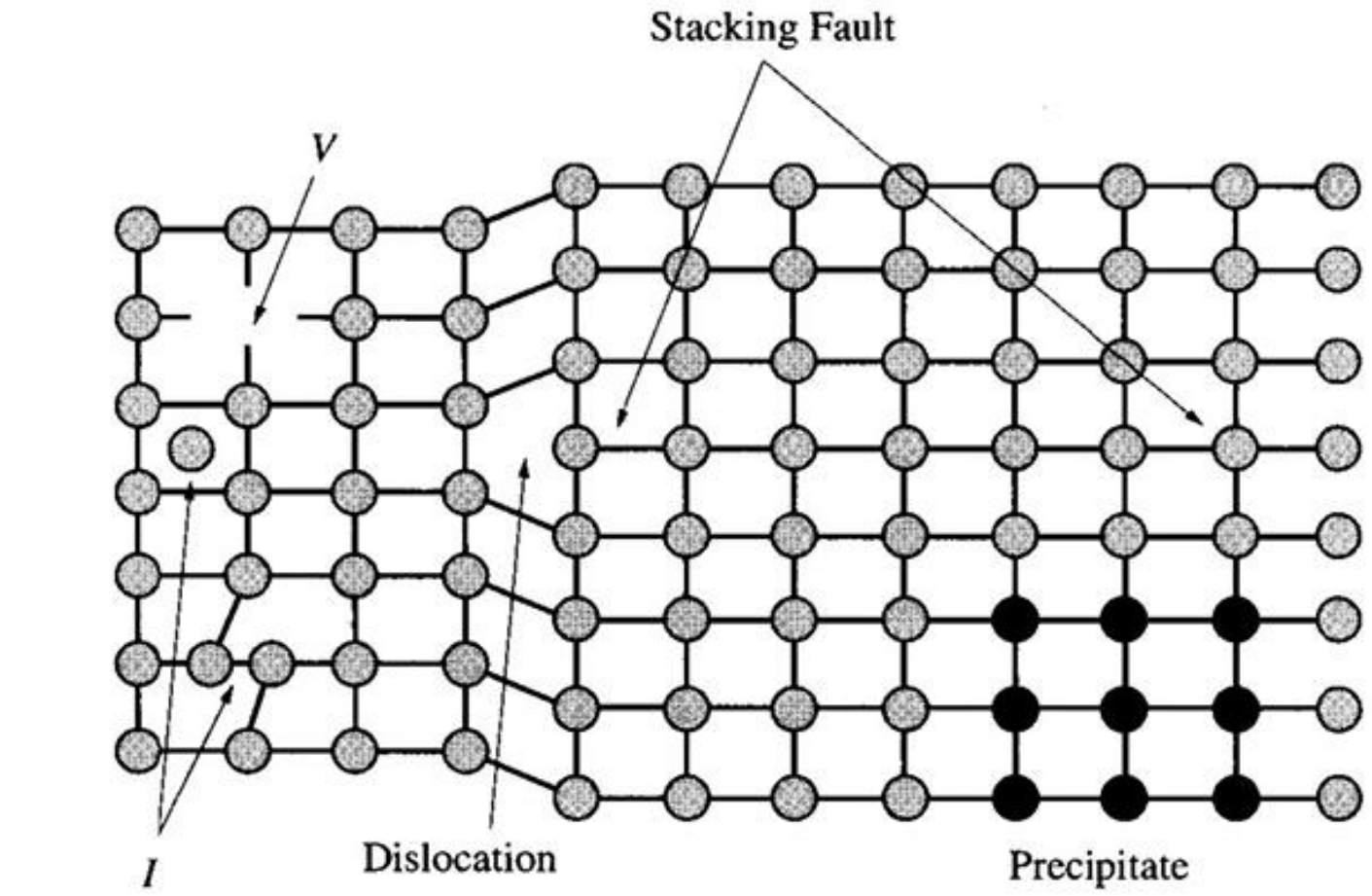


Dislocation / Line Defects

- 線缺陷（Line Defects），也稱為位錯（Dislocations），是晶體材料中一種重要的晶格缺陷類型。它們是一維的缺陷，沿著一條線存在於晶體中
- 由於應力的累積，可能來自溫度梯度（拉晶）、雜質元素、界面不匹配、機械力（如拉伸、壓縮、彎曲、切削或夾取wafer所造成力的不均勻）等因素，導致該缺陷

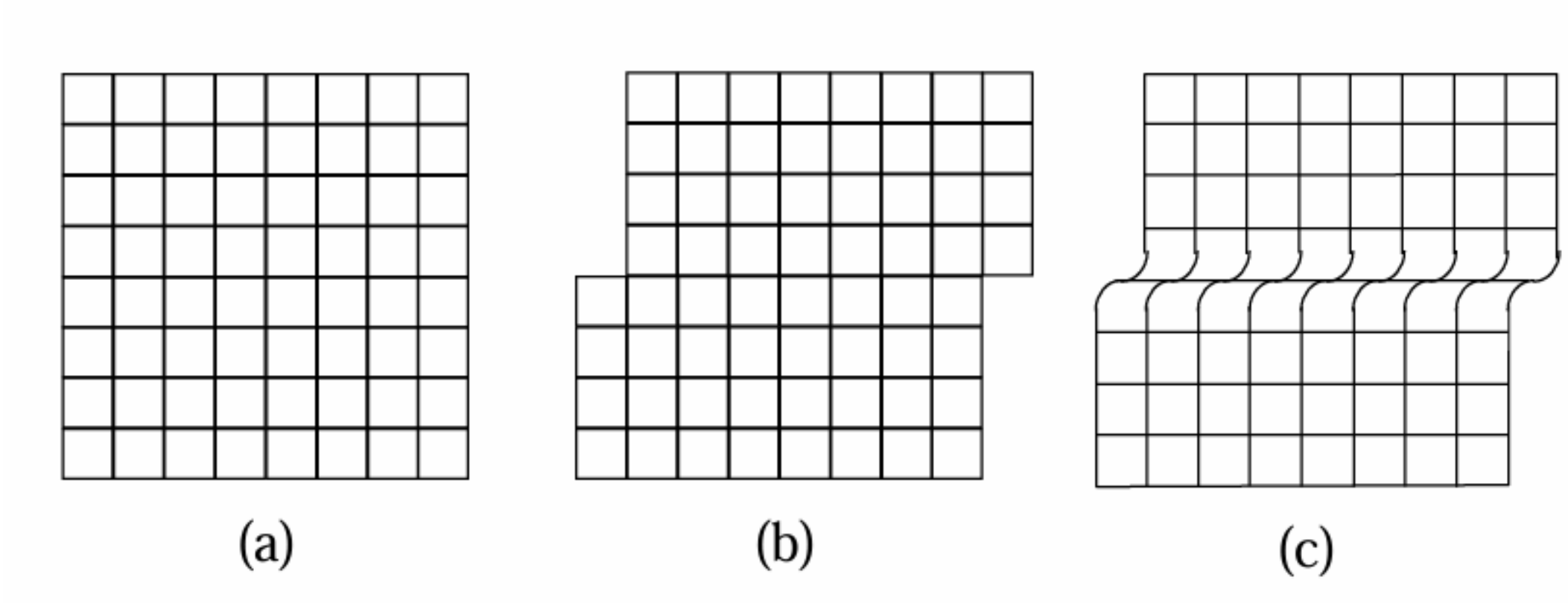


The mixture of Point and Line Defect in Crystal

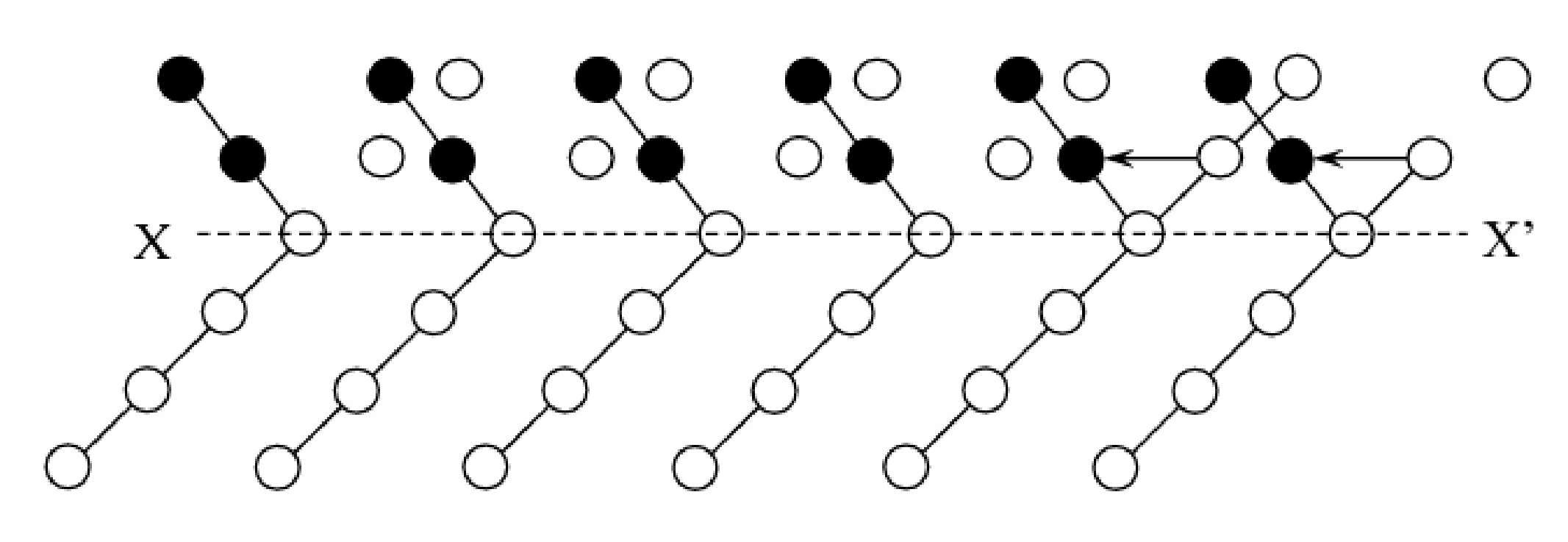


- Necking down in the beginning of the pull at high speed so that high vacancy densities remove the edge dislocation

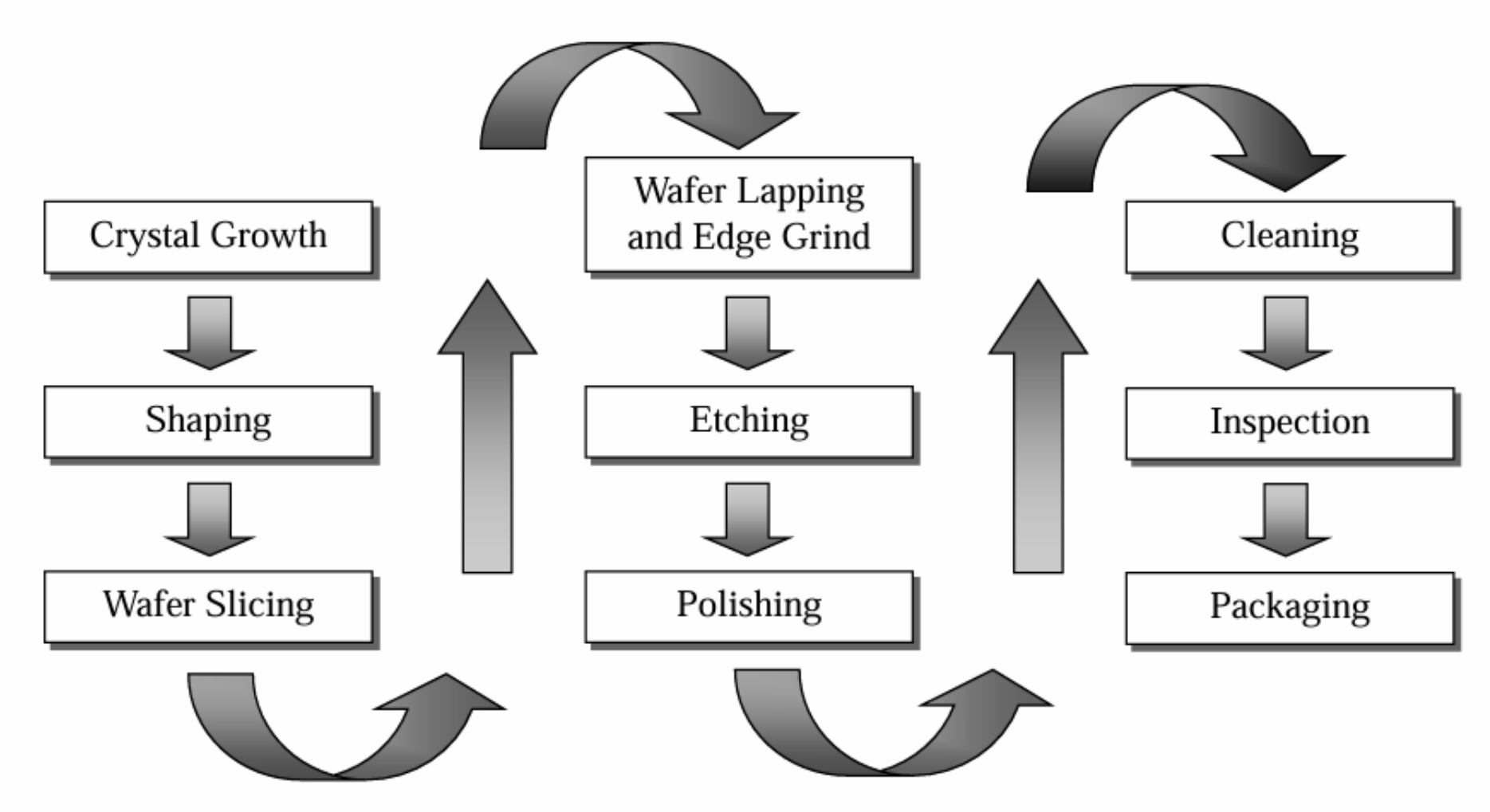
Crystal Slip



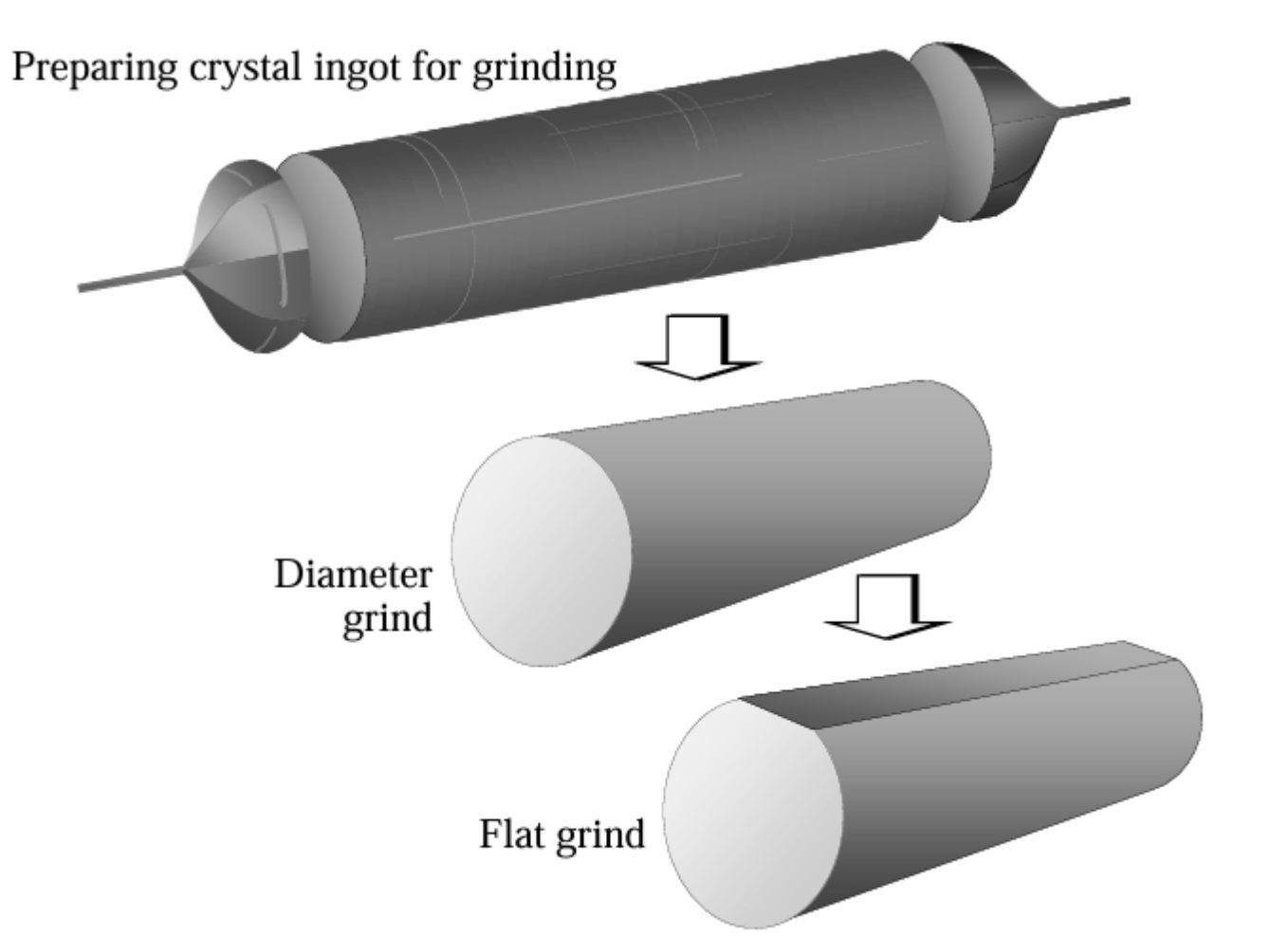
Crystal Twin Planes



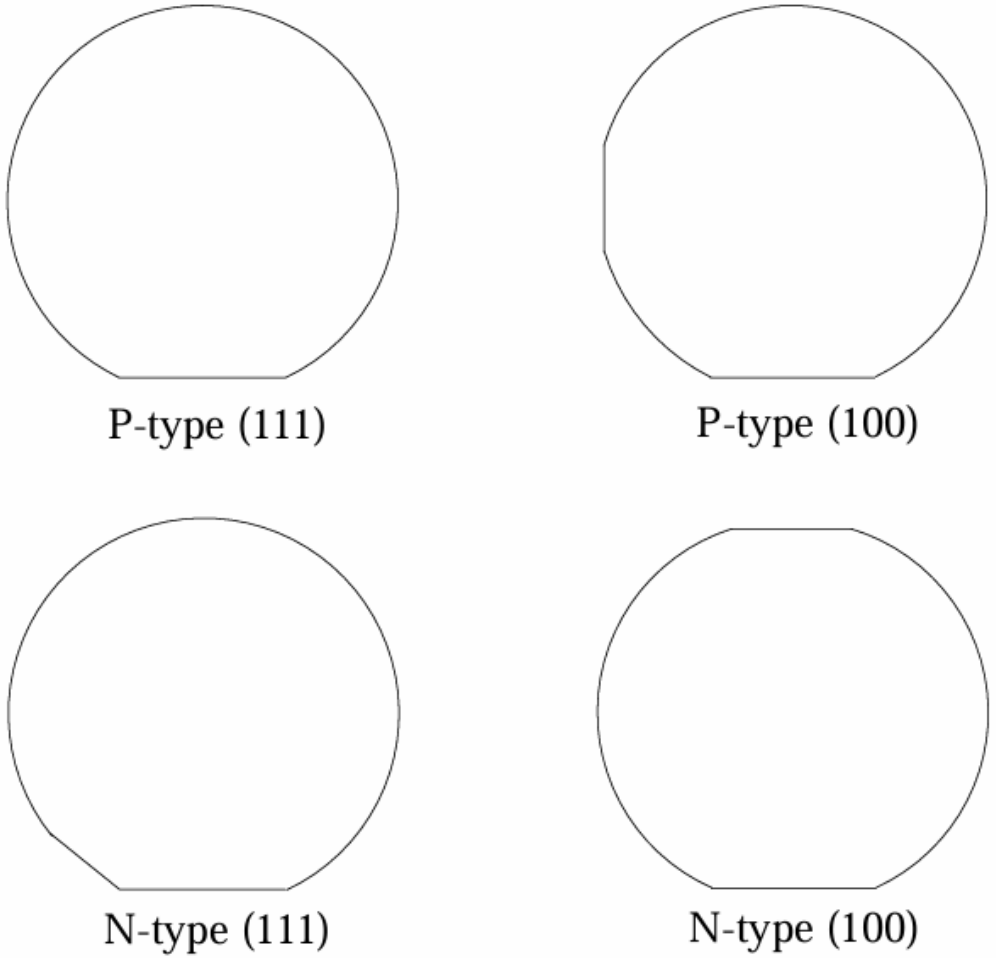
Basic Process Steps for Wafer Preparation



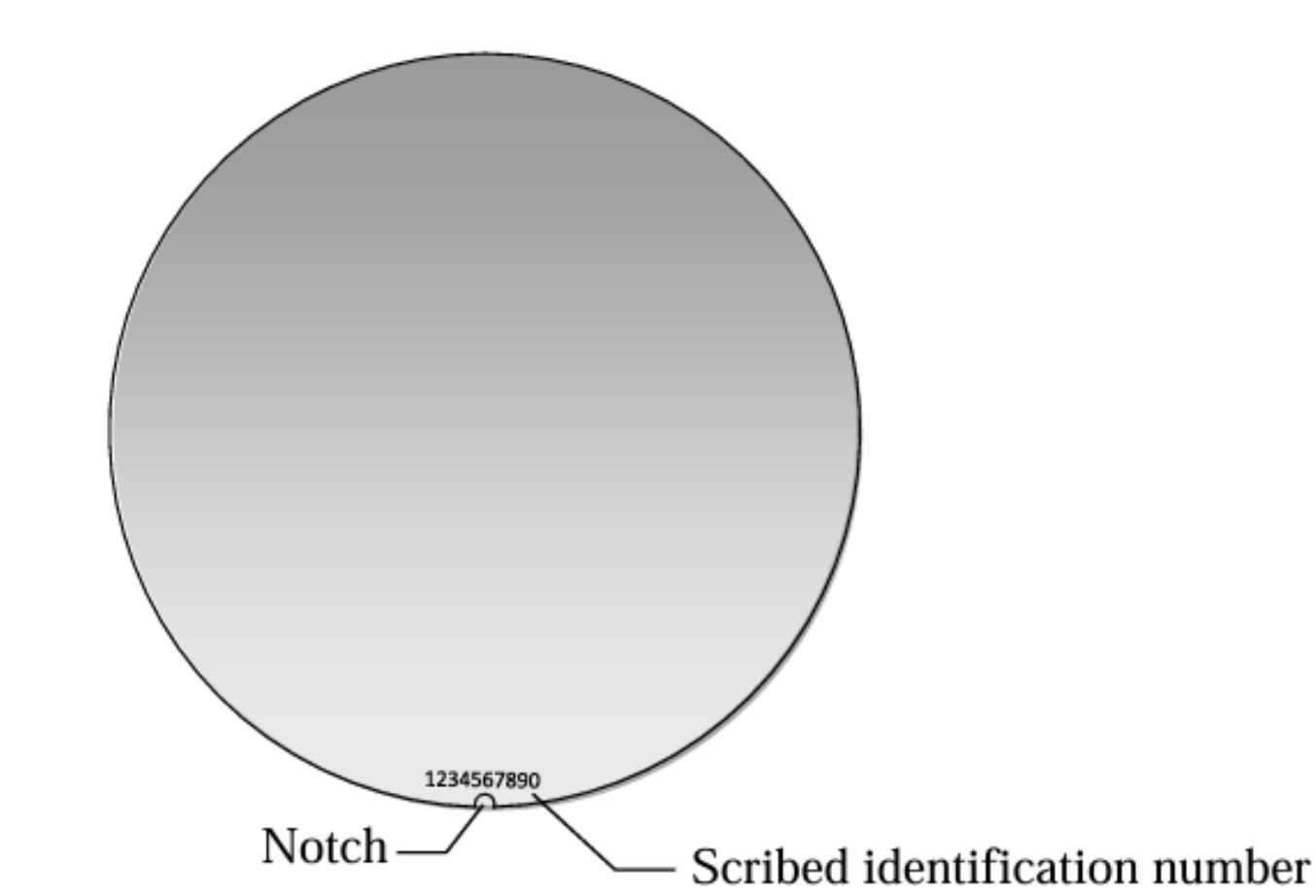
Ingot Diameter Grind



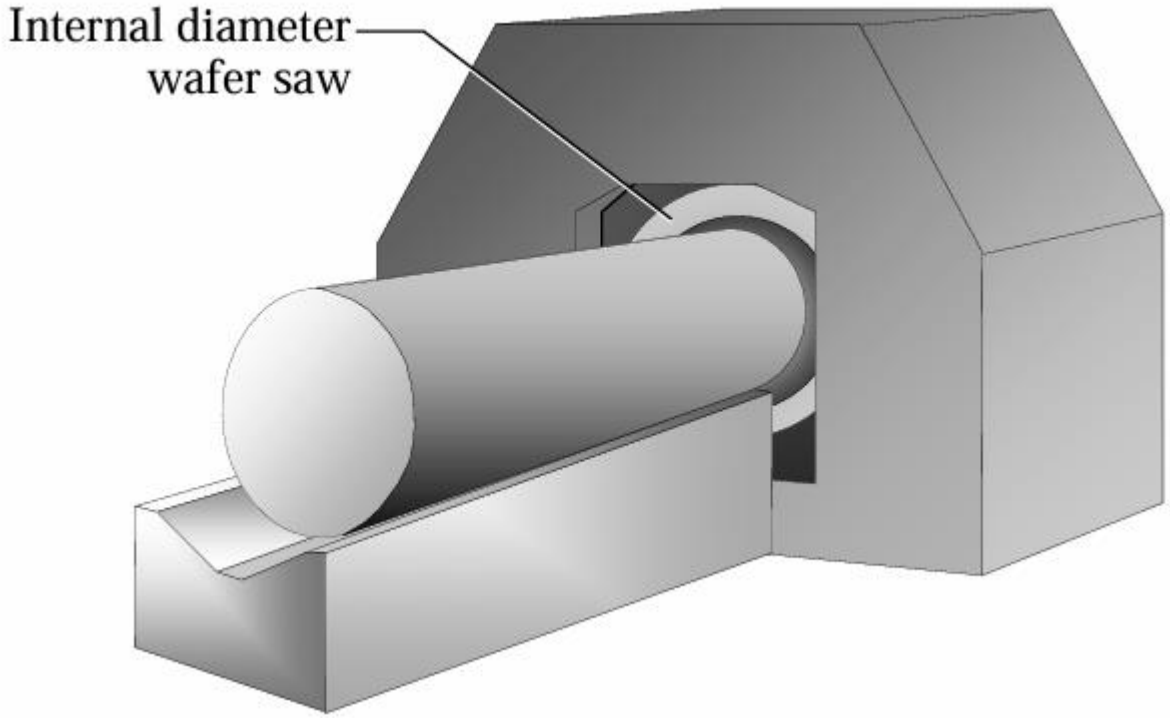
Wafer Identifying Flats

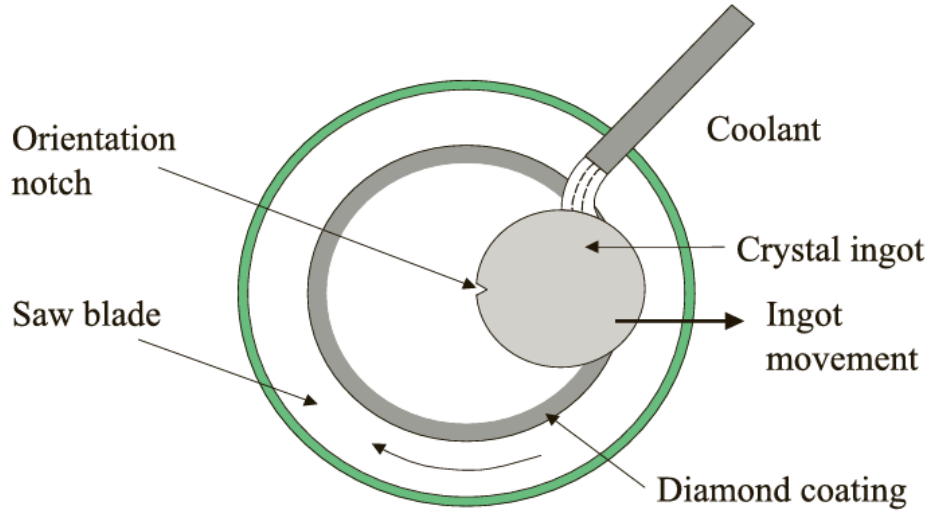


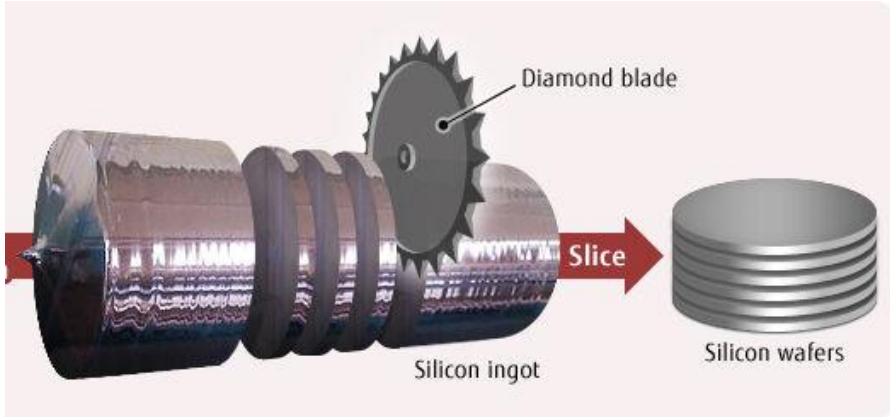
Wafer Notch and Laser Scribe



Wafer Slicing (Internal Diameter Saw / Diamond Wire Saw)

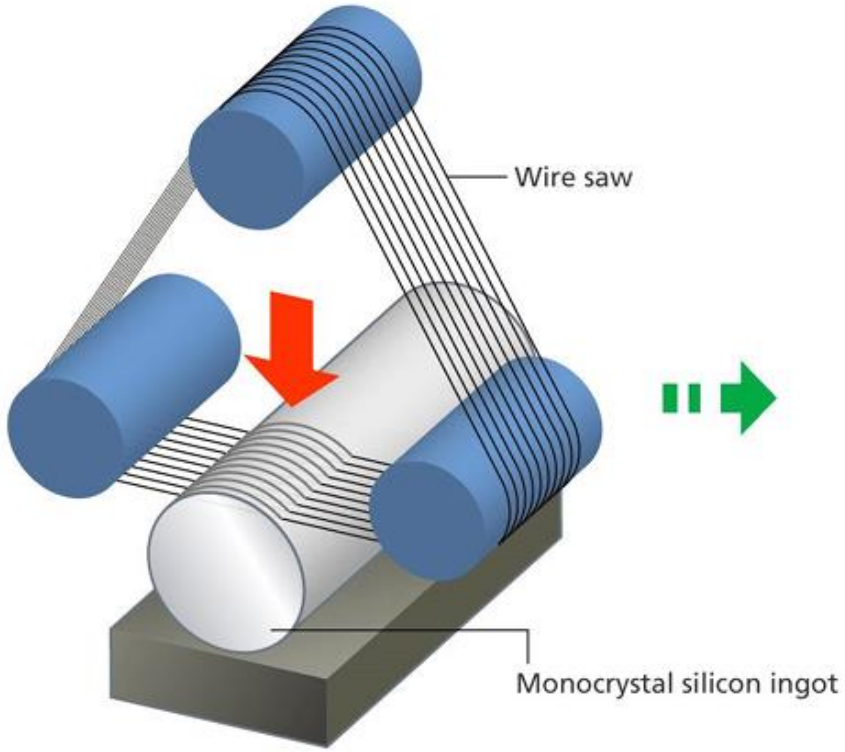


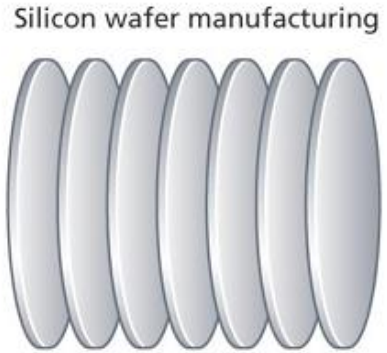


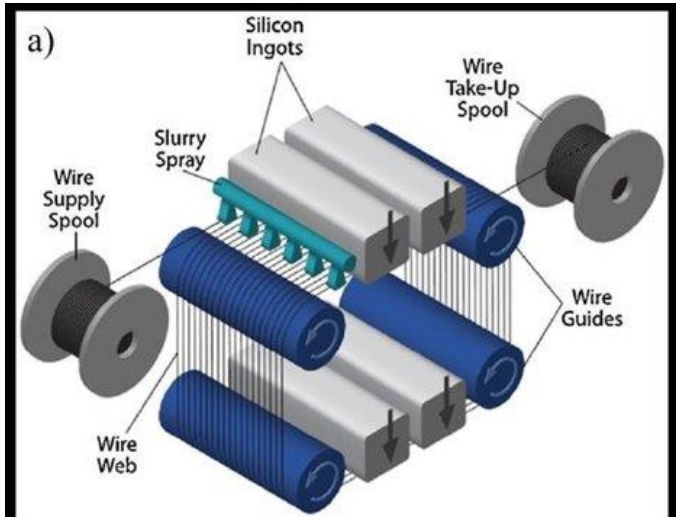


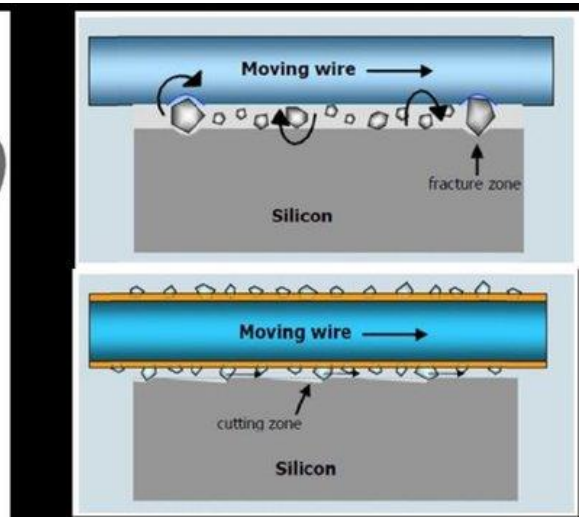
Source: fujitsu.com

Wafer Slicing (Internal Diameter Saw / Diamond Wire Saw)





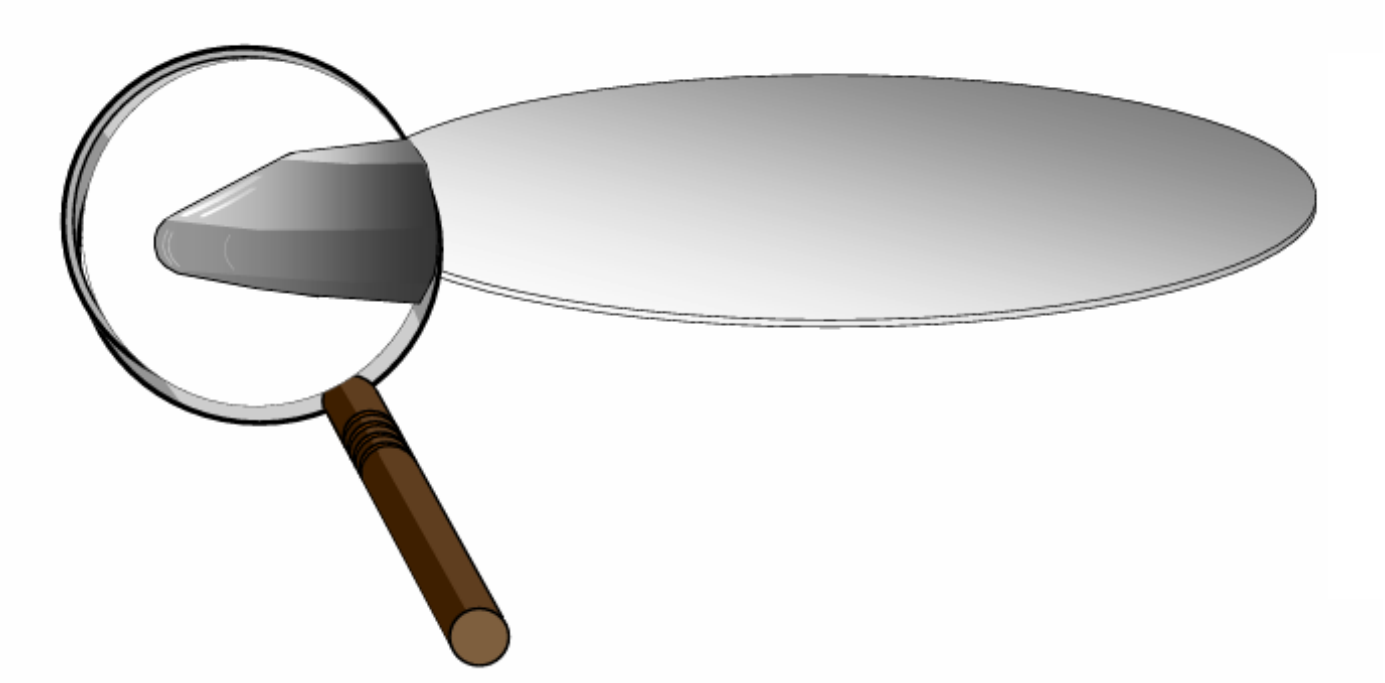


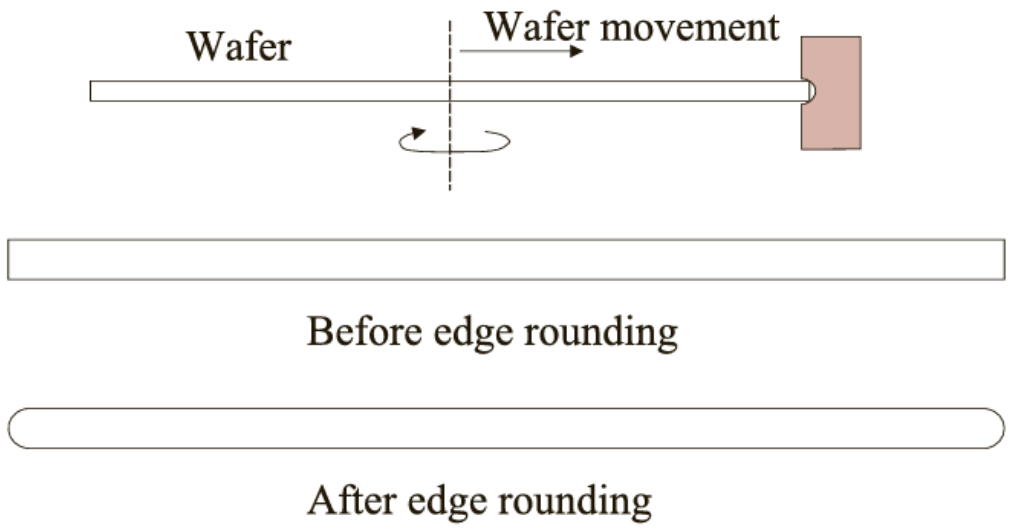


Source: Nikon、Erick Cardoso Costa, Influence of diamond wire sawing parameters on subsurface microcracks formation in monocrystalline silicon wafer, Conference Paper, Oct 2019

Polished Wafer Edge

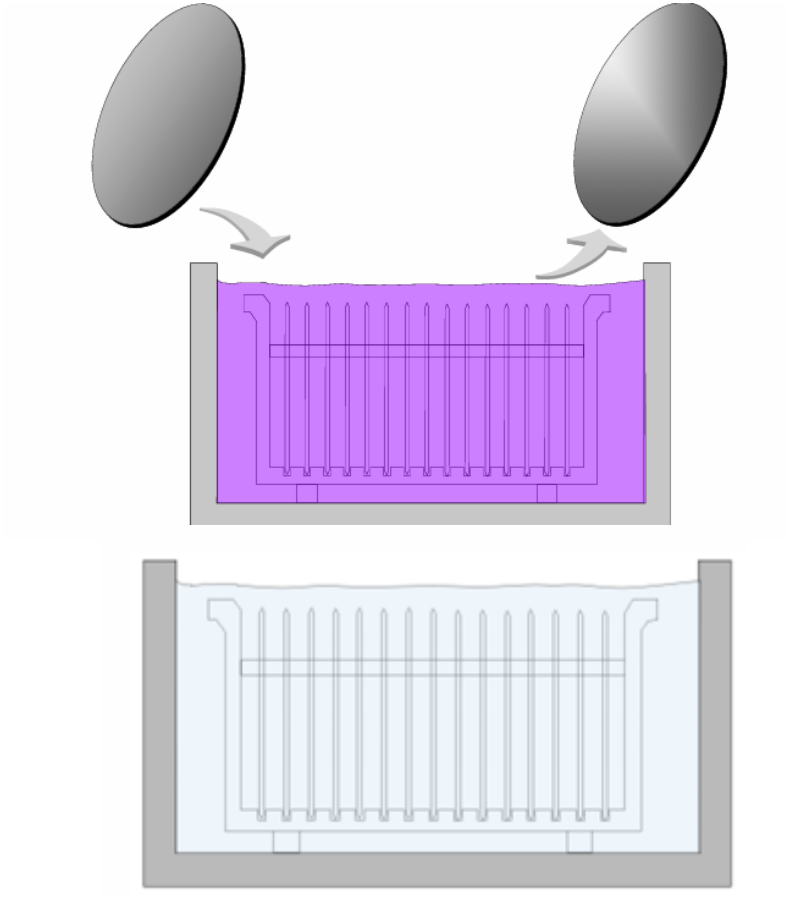
- 經過線鋸或鏈鋸之後，wafer的邊緣會變得非常鋒利，可能會將人員刮傷或者放置cassette中時，可能也會造成破損甚至破裂，從而產生不必要的汙染

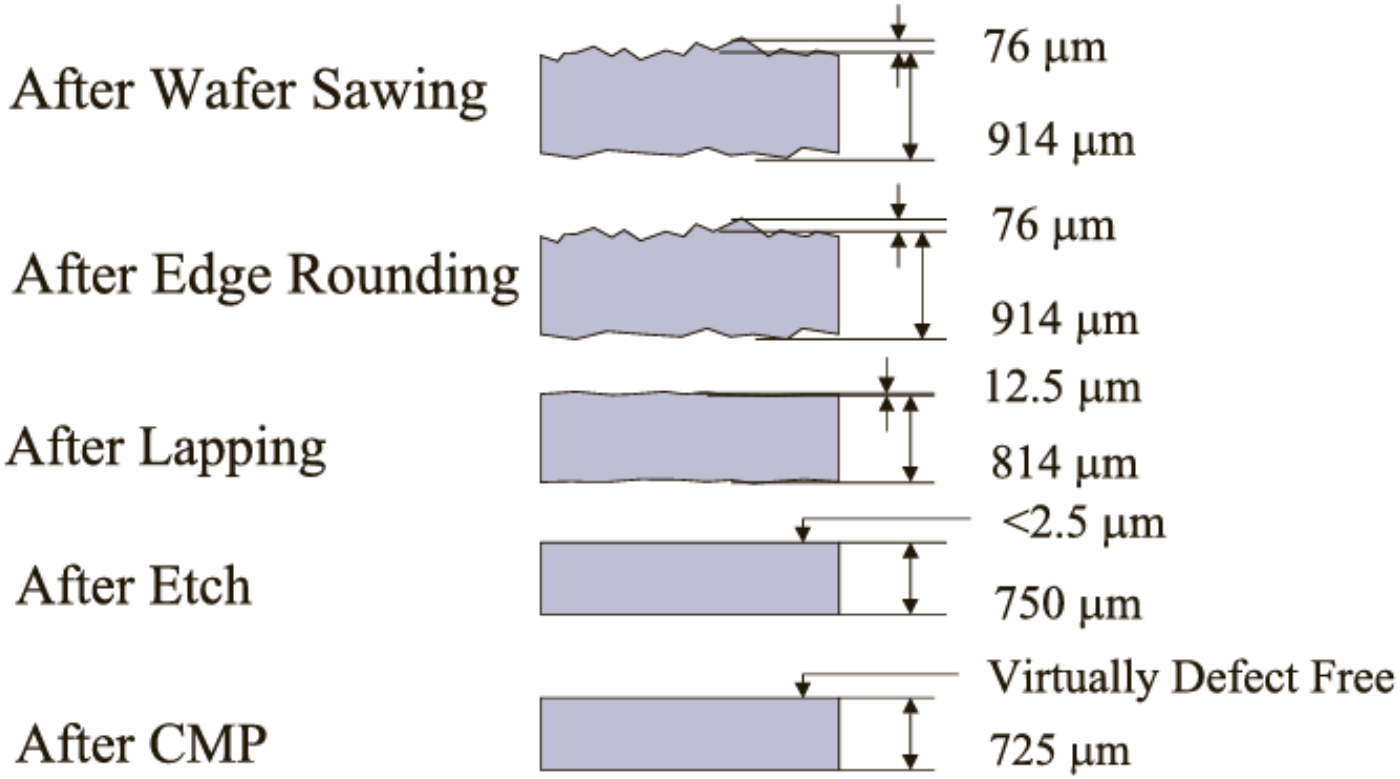




Chemical Etch of Wafer Surface to Remove Damage

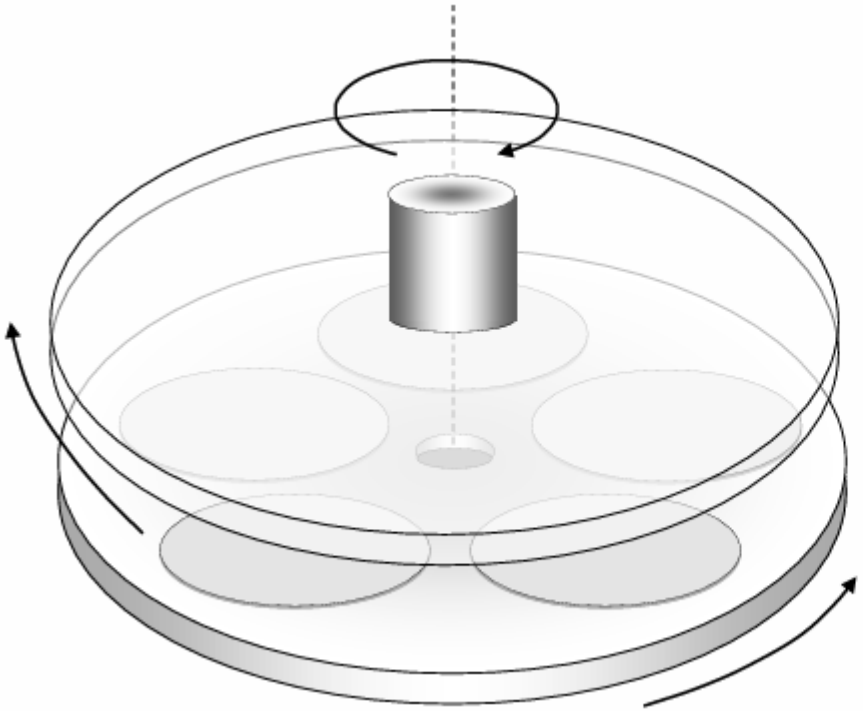
- 濕式蝕刻：去除由切片過程、邊緣磨削和研磨中造成的微粒和損傷，所以常常利用具有酸性或鹼性的蝕刻液將其去除

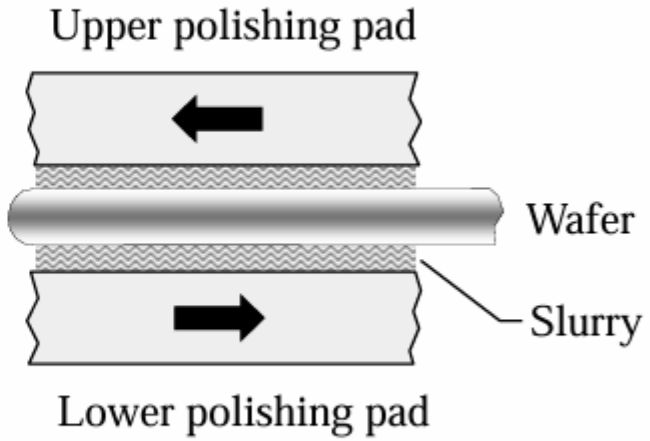




Single / Double-Sided Wafer Polish

- 粗磨：快速去除多餘的材料，並達到接近目標的厚度範圍，採用機械雙面研磨過程在均勻加壓下完成
- 細磨 (CMP)：使用更細緻的研磨漿和研磨墊，進一步減少表面粗糙度





Wafer Cassette

- 晶圓的盒子通常由鐵氟龍Teflon製成，抗腐蝕性、高溫穩定性、低微粒產生、抗靜電
- 裝入防潮袋(Moisture Barrier Bag)，通入氮氣防止運輸過程氧化
- #300mm Silicon #Wafer Manufacturing Process

Quality Measures

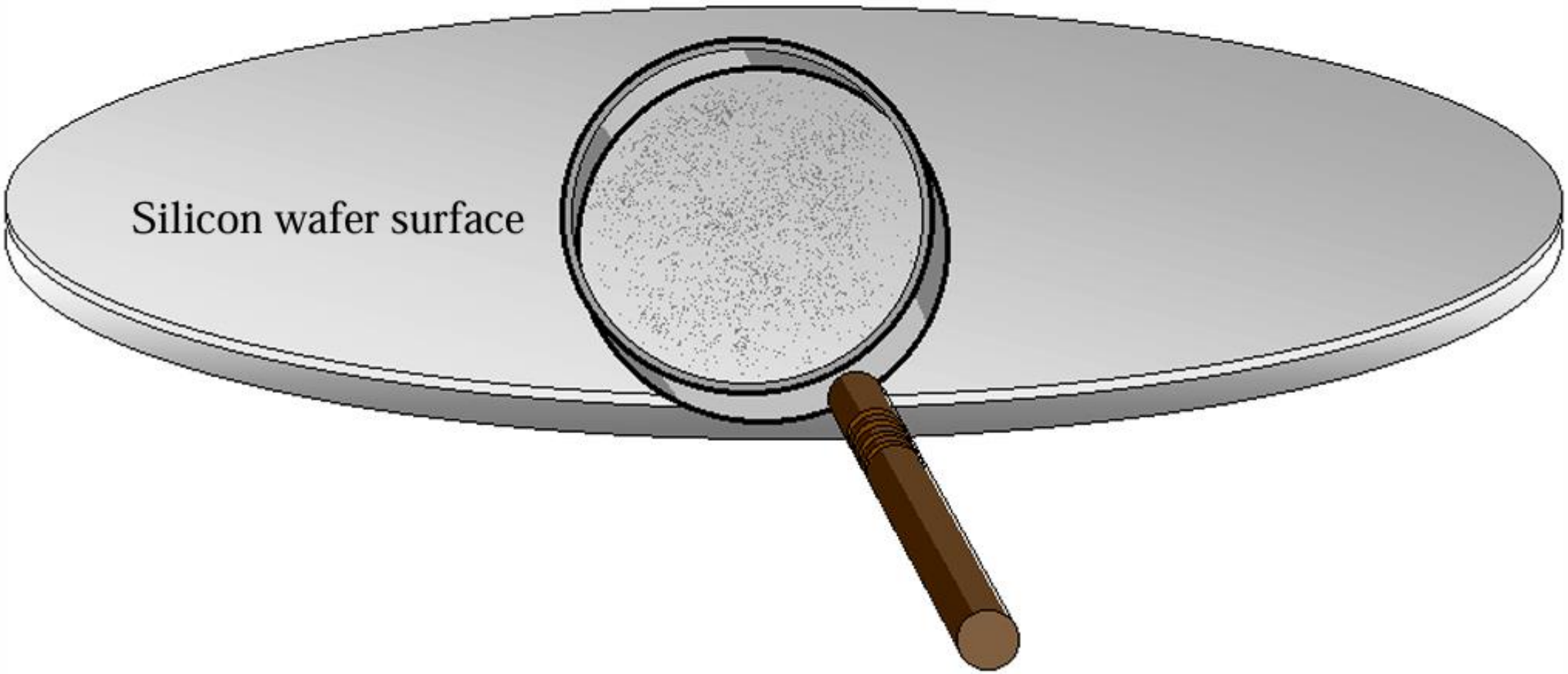
- Physical dimensions
- Flatness
- Microroughness
- Oxygen content
- Crystal defects
- Particles
- Bulk resistivity

Improving Silicon Wafer Requirements

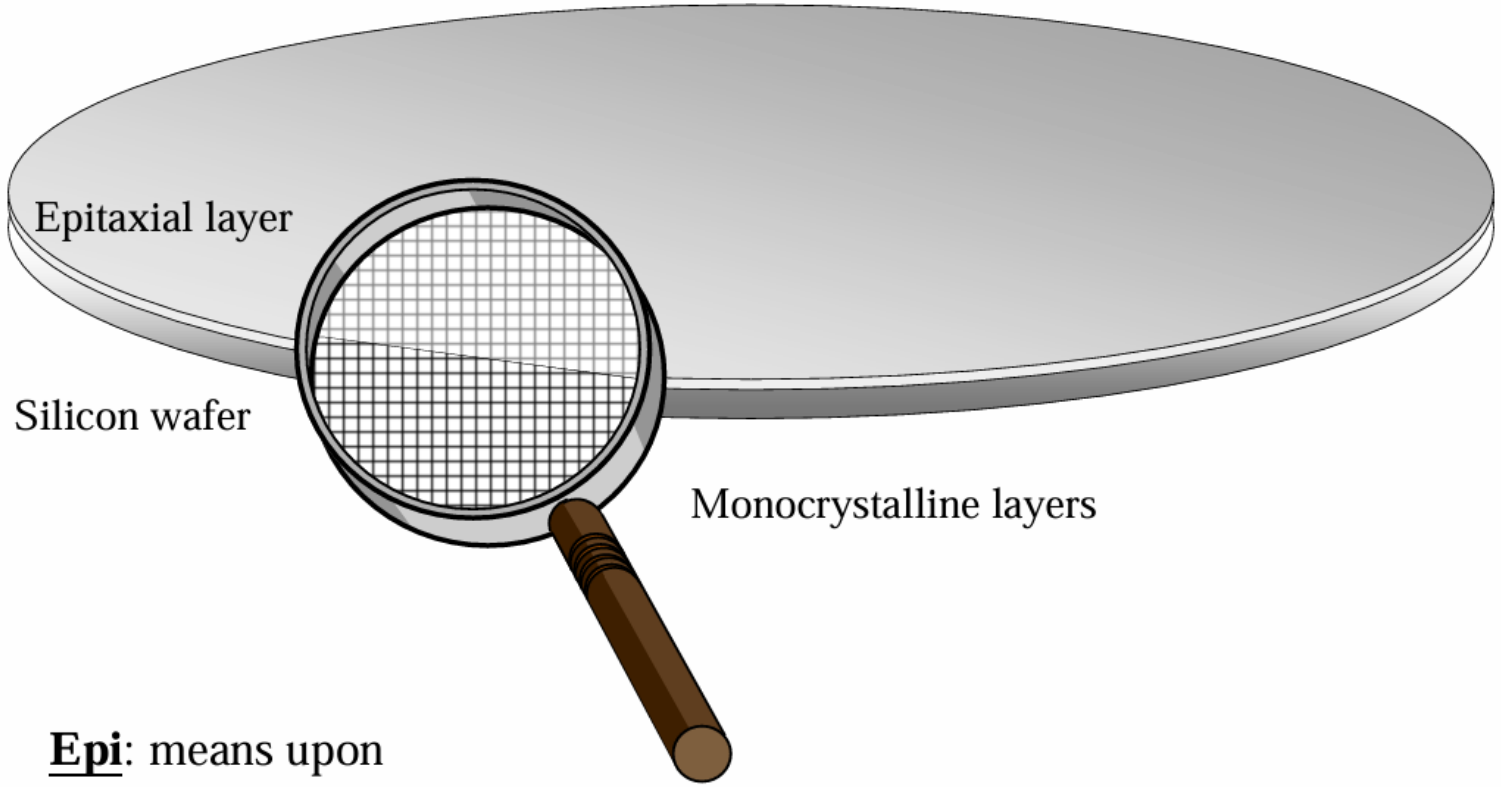
	Year (Critical Dimension)			
	1995 (0.35 µm)	**1998 (0.25 µm)**	**2000 (0.18 µm)**	**2004 (0.13 µm)**
Wafer diameter (mm)	200	200	300	300
Site flatness[A] (µm) Site size (mm x mm)	0.23 (22 x 22)	0.17 (26 x 32)	0.12 26 x 32	0.08 26 x 36
Microroughness[B] of front surface (RMS)[C] (nm)	0.2	0.15	0.1	0.1
Oxygen content (ppm)[D]	$\leq 24 \pm 2$	$\leq 23 \pm 2$	$\leq 23 \pm 1.5$	$\leq 22 \pm 1.5$
Bulk microdefects[E] (defects/cm^2)	≤ 5000	≤ 1000	≤ 500	≤ 100
Particles per unit area (#/cm^2)	0.17	0.13	0.075	0.055
Epilayer[F] thickness (± % uniformity) (µm)	3.0 (± 5%)	2.0 (± 3%)	1.4 (± 2%)	1.0 (± 2%)

Adapted from K. M. Kim, "Bigger and Better CZ Silicon Crystals," *Solid State Technology* (November 1996), p. 71.

Flatness of Wafer Front Surface



Formation of Epitaxial Silicon Layers



- **Epi**: means upon
- **Taxis**: means ordered
- In epitaxial silicon, the base wafer is used as a seed crystal to grow a thin layer of silicon on wafer
- The epi-layer can be n- or p-type and is **independent** of the initial wafer type

Epitaxy film thickness (橢偏儀)

- 每當工程師做完有關於鍍膜或磊晶相關的製程之後，他們為了監控所沉積的膜厚以判斷機台當天狀況時，其中一種常見的量測是利用橢偏儀去做膜厚的測量 (Ellipsometry）
- 基本原理:
  - 利用偏振光照射樣品，根據反射後光的偏振態變化來反推材料的光學常數與膜層厚度
- 優點:
  - 非接觸式
  - 非破壞式

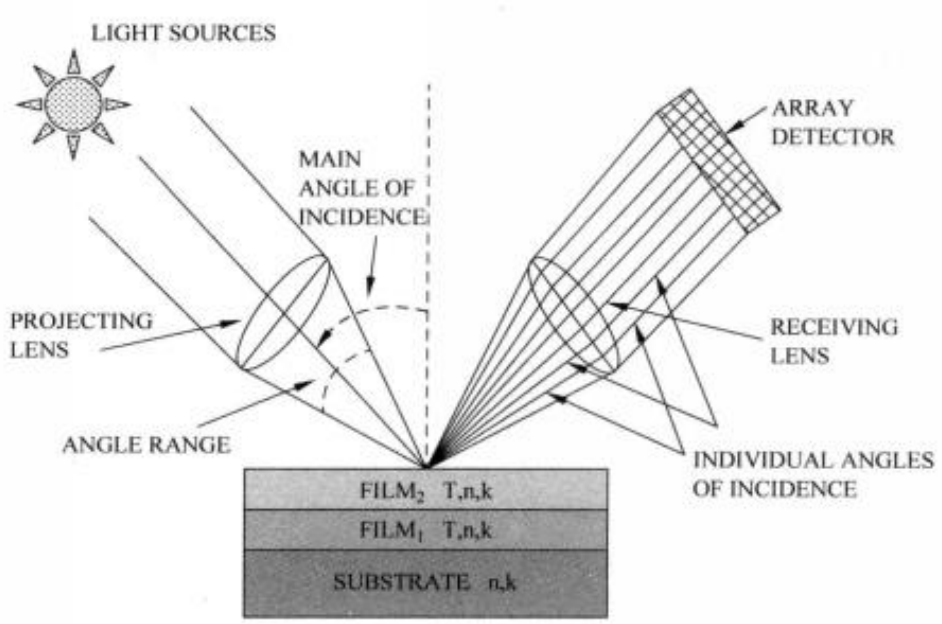
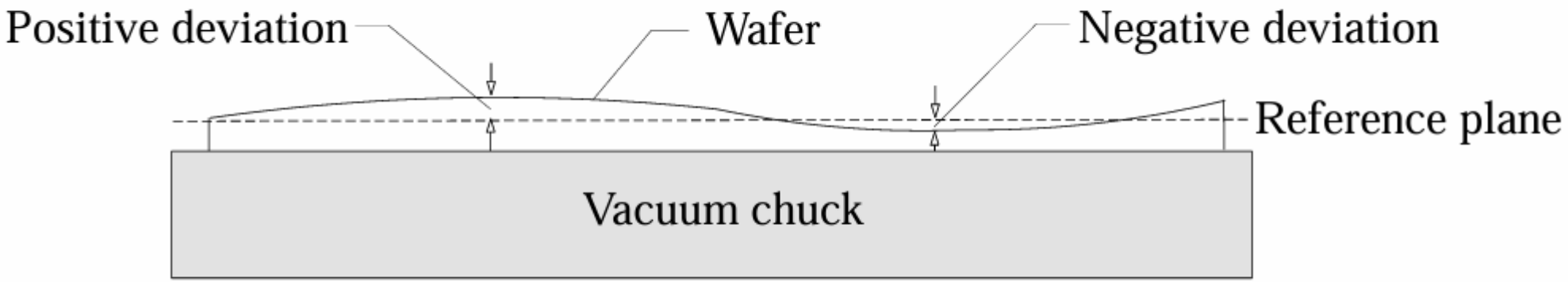


图 16.8 偏振差椭圆率测量仪的组件

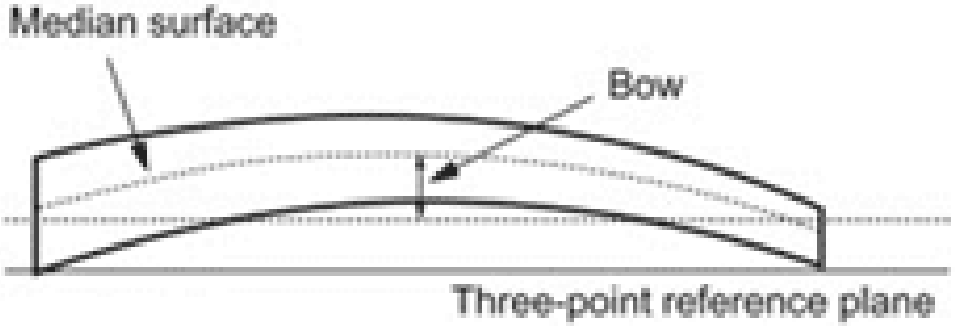
Source: HORIBA

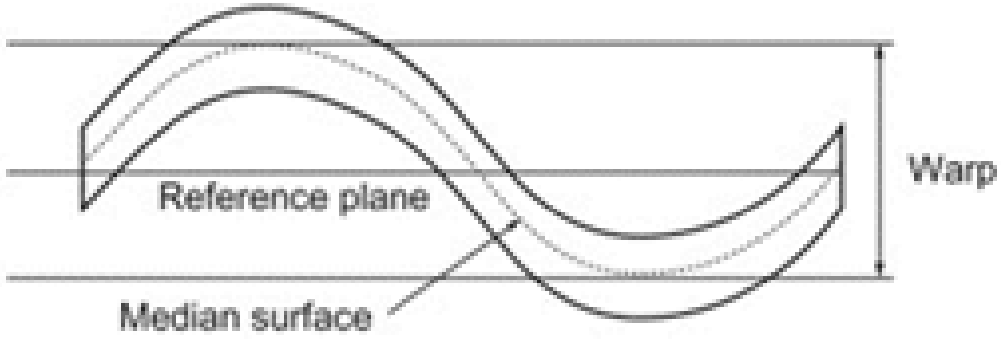
Wafer Deformation



Flatness

- TTV（Total Thickness Variation，總厚度變化）
  - TTV = Max(Ti) − Min(Ti) (Ti為各測量點厚度)
  - 先進製程（如 5nm 以下）要求 TTV ≤ 1 μm，一般製程可放寬至 3–5 μm
- Bow（弓形彎曲量）
  - Bow = Max(Zi) − Min(Zi) (Zi為表面高度值)
  - 300mm (12”) 晶圓通常要求 Bow ≤ 50 μm 或更低
- Warp（扭曲程度）
  - Warp = Max(Zi − Zfit)(Zfit為擬合平面高度)
  - 300mm (12”) 晶圓 Warp 通常需 ≤ 30 μm 或更低（先進封裝要求更嚴格）

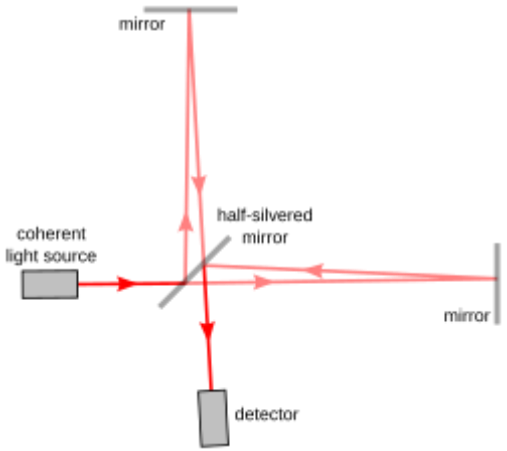


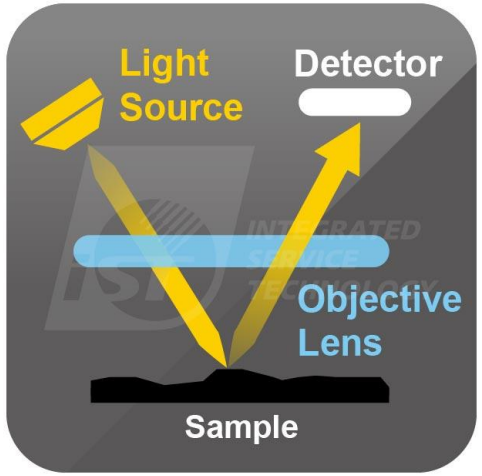


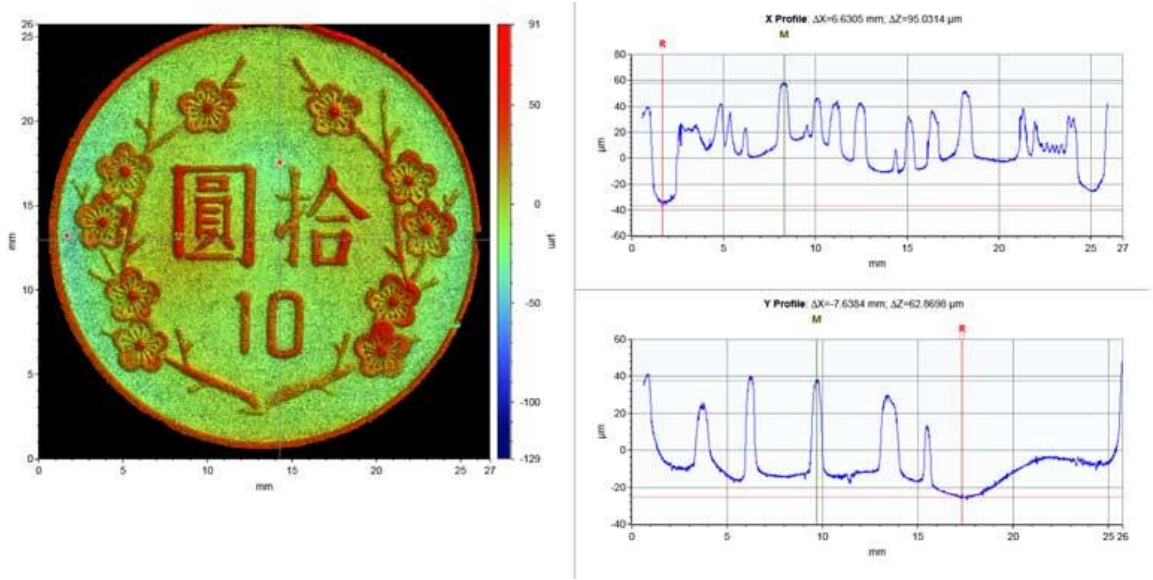
Source: VIRTEK

Flatness (光學干涉儀 Interferometry)

- 光學干涉儀利用光源發出的光經過分束、反射及重組後，在檢測器上形成干涉條紋。這些條紋對應於樣品表面各點的光程差，進而反映了表面形狀的微小變化
- 利用分光器將入射光分成兩路：一束作為參考光，另一束照射到樣品表面。被測光在反射後與參考光重新合併，產生具有相位差的干涉圖樣。再利用電腦軟體，重構出樣品表面的資訊，利用這些資訊進一步計算得出TTV、BOW、Warp
- 優點:
  - ➢ 非接觸式測量
  - ➢ 快速數據獲取與處理



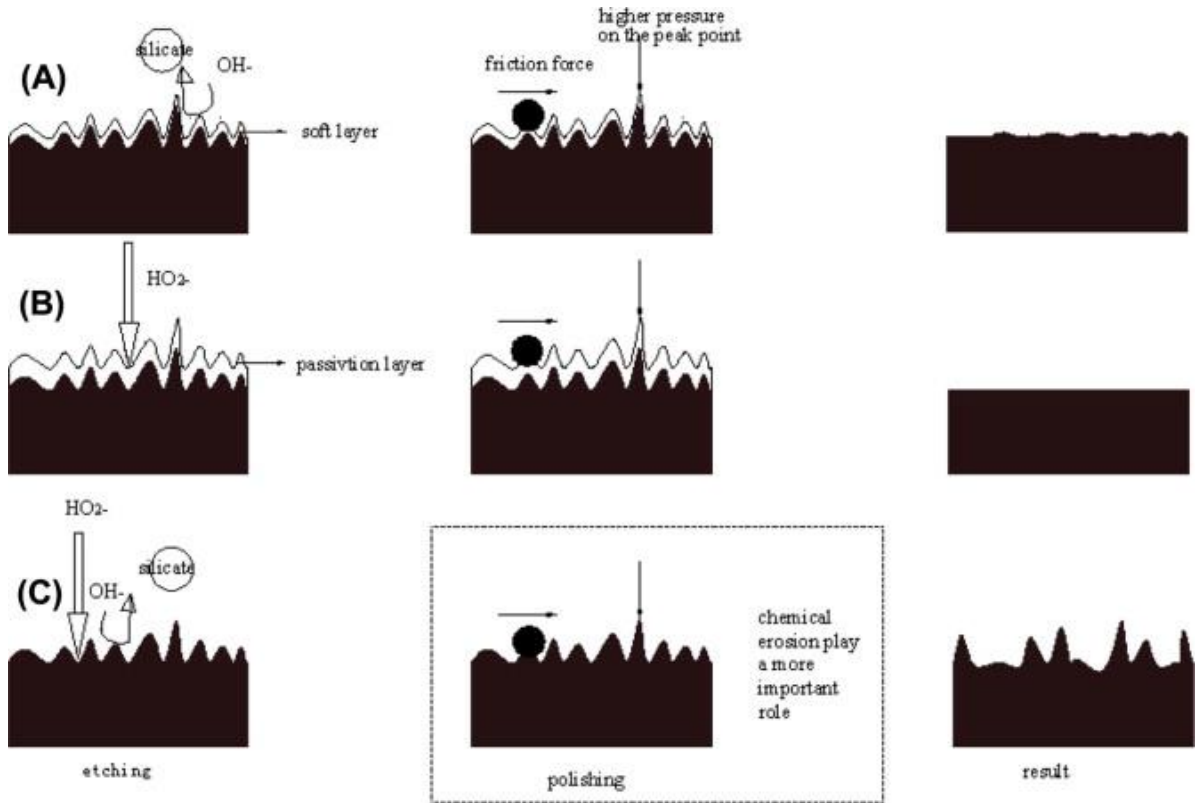




Source: Wikipedia、IST

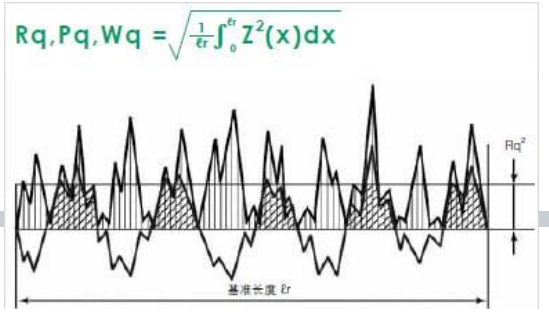
Microroughness

- 微粗糙度指晶圓或材料表面在微米或奈米尺度上的起伏，與平坦度不同，平坦度偏向大尺度（整片晶圓）形變的量測，微粗糙度則是觀察局部表面的粗糙情形
- 在量測分析中，最常見的方法是利用AFM（Atomic Force Microscopy，原子力顯微鏡）



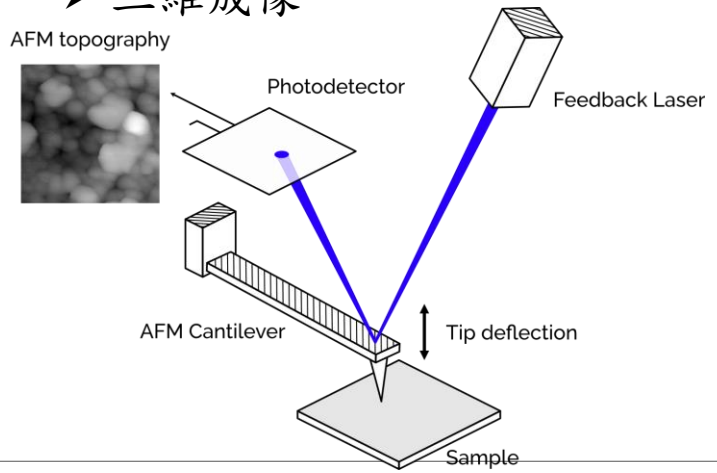
Source: Haibo Wang, Effect of hydrogen peroxide concentration on surface micro- roughness of silicon wafer after final polishing, Microelectronic Engineering, Volume 88, Issue 6, June 2011, Pages 1010-1015

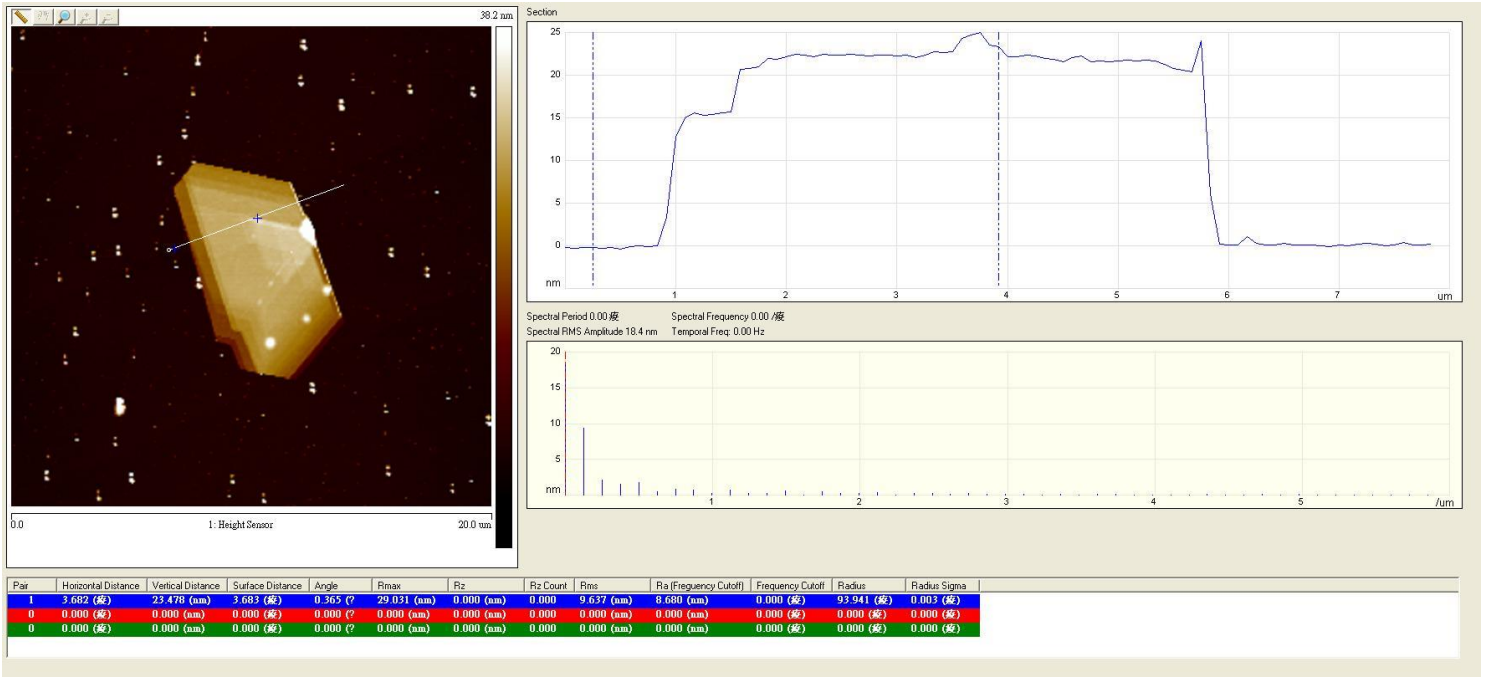
Microroughness



- AFM（Atomic Force Microscopy，原子力顯微鏡）
  - 一種利用探針與樣品表面間的相互作用力進行成像和測量的先進顯微技術。它能夠達到奈米甚至原子級的分辨率
  - AFM 的核心是位於微小懸臂（cantilever）末端的尖銳探針，其尖端半徑通常只有幾納米。當探針靠近或接觸樣品表面時，兩者之間會產生范德華力、靜電力等相互作用力。這些微弱力會引起懸臂彎曲或振動。

- 優點:
  - 高解析度
  - 多功能測量
  - 三維成像

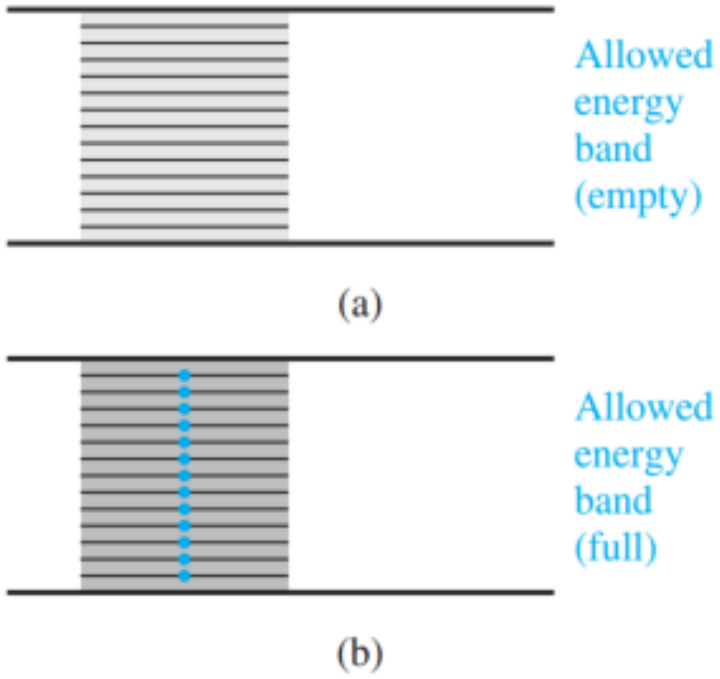


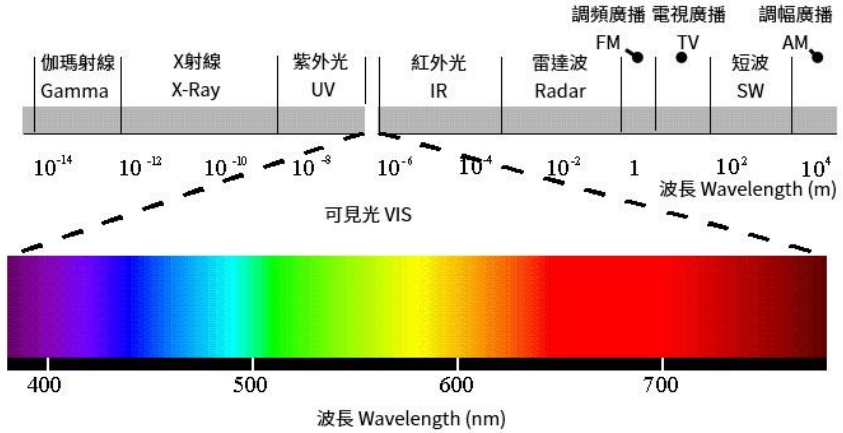


Source: molecular vista

Oxygen content

- 在矽晶圓中，最常見且標準化的含氧量量測方法是 **FTIR（Fourier Transform Infrared Spectroscopy，傅立葉轉換紅外光譜）（當然還有其他種元素類的材料分析工具）**
- 紅外線光譜(Infrared spectroscopy)，是藉由樣品分子對不同波長紅外線的吸收所產生的特徵光譜，來進行材質的鑑別及研究。

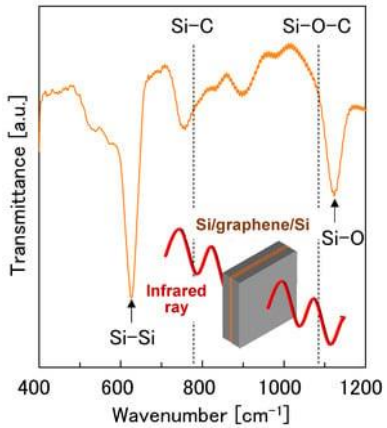


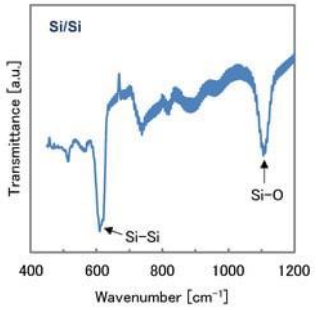


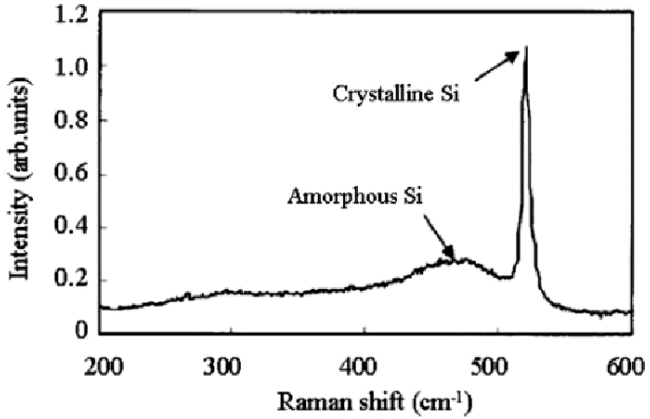
Region	Wavelength (um)	Wavenumber (cm^{-1})
Near IR	0.75 – 2.5	13300 – 4000
Mid IR	2.5 – 25	4000 – 400
Far IR	25 - 1000	400 – 10

Oxygen content (FTIR)

- 基本原理:
  - 分子震動與紅外吸收
  - 當紅外光照射至樣品上，樣品分子中的化學鍵會因為吸收能量而發生震動。不同的化學鍵會對特定的紅外光波長進行吸收，因此不同的物質會產生不同的紅外吸收光譜
- 優點:
  - 量測快
  - 高靈敏性
  - 非破壞性
- FTIR是一種吸收光譜技術，除了吸收光譜，當然還有放射光譜的技術，如Raman spectrum等



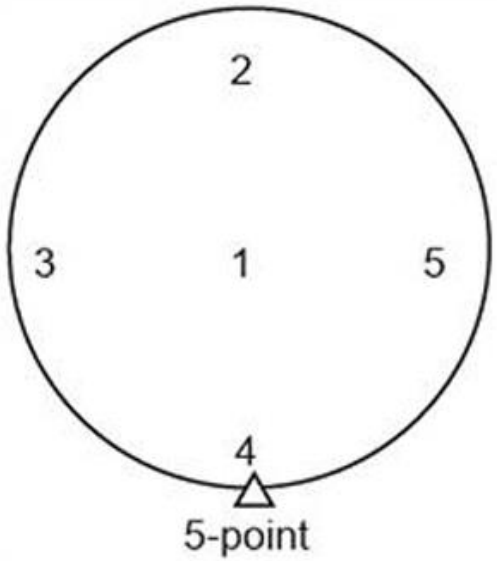




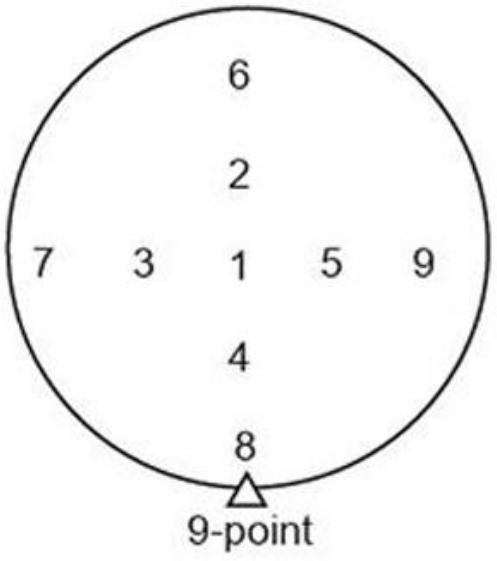
Source: TSRI、Takenori Naito, Fabrication of Si/graphene/Si Double Heterostructures by Semiconductor Wafer Bonding towards Future Applications in Optoelectronics, Nanomaterials 2018, 8(12), 1048

Bulk resistivity

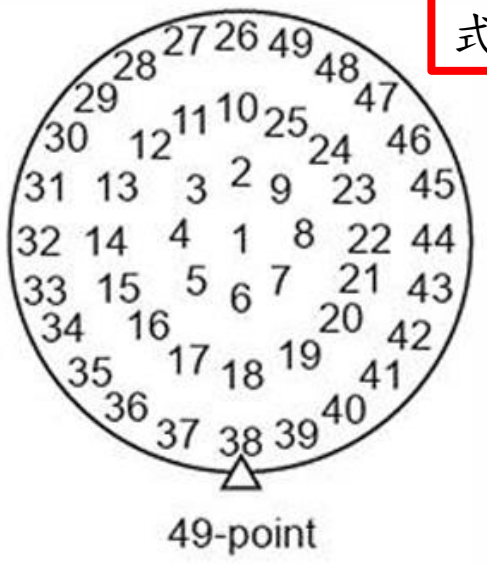
- **Bulk resistivity（體電阻率）** 是描述晶圓或半導體材料內部固有導電性的參數，通常以歐姆-公分（Ω·cm）為單位。這項參數與材料中的摻雜濃度直接相關，對於後續元件的電性表現至關重要。
- 在晶圓中，常見的量測電阻率的方法之一為四點探針量測（Four-point Probe measurement, 俗稱4pp）



5-point



9-point



49-point

此圖所描述的量測取點方式也可應用於其他量測

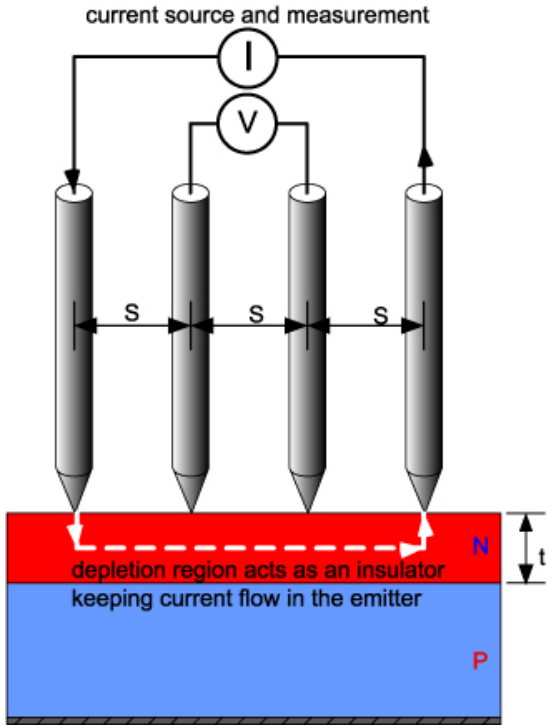
$$\rho = \frac{1}{q * n * \mu}$$

Bulk resistivity (4pp)

- 基本原理:
  - 四探針通常沿一條直線等間距排列，其中外側兩個探針用於施加電流，而內側兩個探針則負責測量電壓降。
- 優點:
  - 消除接觸電阻影響
  - 非破壞性測量
  - 操作與數據處理快速

$$V(x) = \frac{I R_s}{2\pi}\left[\ln\left|x-\left(-\frac{3s}{2}\right)\right| - \ln\left|x-\frac{3s}{2}\right|\right]$$

$$\rho = \frac{\pi}{\ln(2)}\left(\frac{V}{I}\right)t = 4.532\left(\frac{V}{I}\right)t$$



Source: Everbeing Int'l Corp.、PVEducation

ULSI requirement

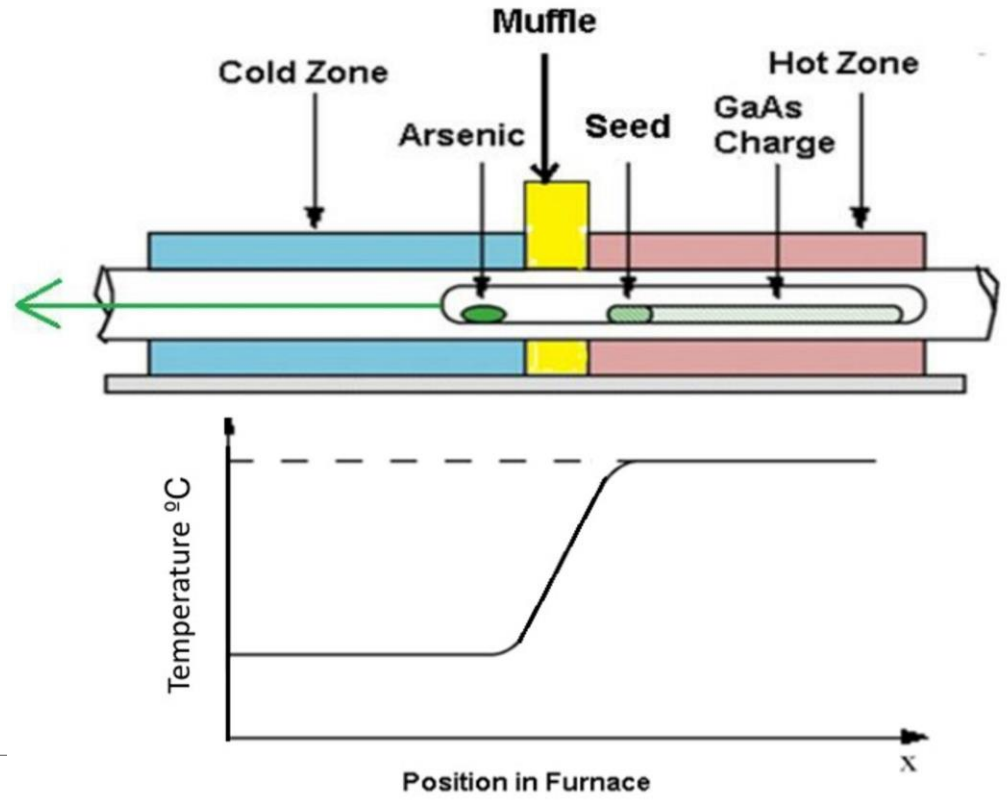
特性			
性質	CZ法	Float zone	ULSI requirement
電阻係數 n-type (ohm-cm)	1 – 50	1 – 300 以上	5 – 50 以上
電阻係數 p-type (ohm-cm)	0.005 – 50	1 – 300	5 – 50 以上
電阻係數梯度 (4pp) (%)	5 – 10	20	小於1
少數載子生命週期 (us)	30 – 300	50 – 500	300 – 1000
氧 (ppm)	5 – 25	NA	均勻且可控
碳 (ppm)	1 – 5	0.1 – 1	小於0.1
差排 (per cm^2)	小於500	小於500	小於1
直徑 (mm)	達到200	達到100	達到300
晶圓彎曲度 (um)	小於25	小於25	小於5
晶圓傾斜度 (um)	小於15	小於15	小於5
表面平坦度 (um)	小於5	小於5	小於1

GaAs Growth Technique

- 有兩種常見的可成長砷化鎵單晶的晶圓技術:
  - ➢ CZ法: 長大尺寸的晶錠
  - ➢ 布里吉曼技術 (Bridgman technique):
- 布里吉曼法主要透過梯度溫控與定向凝固來生長單晶，適用於 GaAs 及其他 III-V 族化合物半導體（如 InP、GaP）
- 步驟:

1. 原料準備
2. 高溫熔解
3. 控制冷卻和晶體成核

砷在高溫下極易揮發，所以熔融的 GaAs 會因為砷的快速揮發而導致砷含量不足，因此，需要額外補充固體砷



Schematics of the furnace and crucible used for GaAs growth.