Chapter 9

Metal-Semiconductor and Semiconductor Heterojunctions

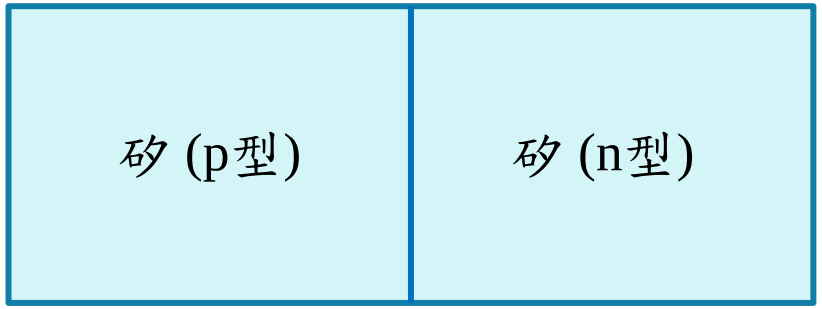
Outline

In this chapter, you may learn:

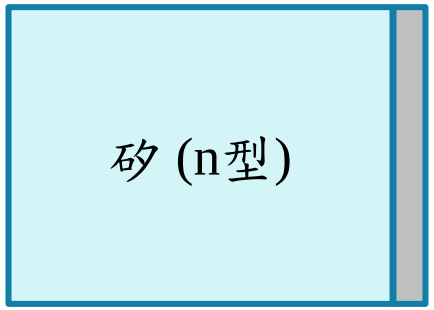
- The Schottky Barrier Diode
- Metal – semiconductor Ohmic Contacts
- Heterojunction

同質介面與異質介面

兩邊材料基質相同時稱之為同質介面 Homojunction



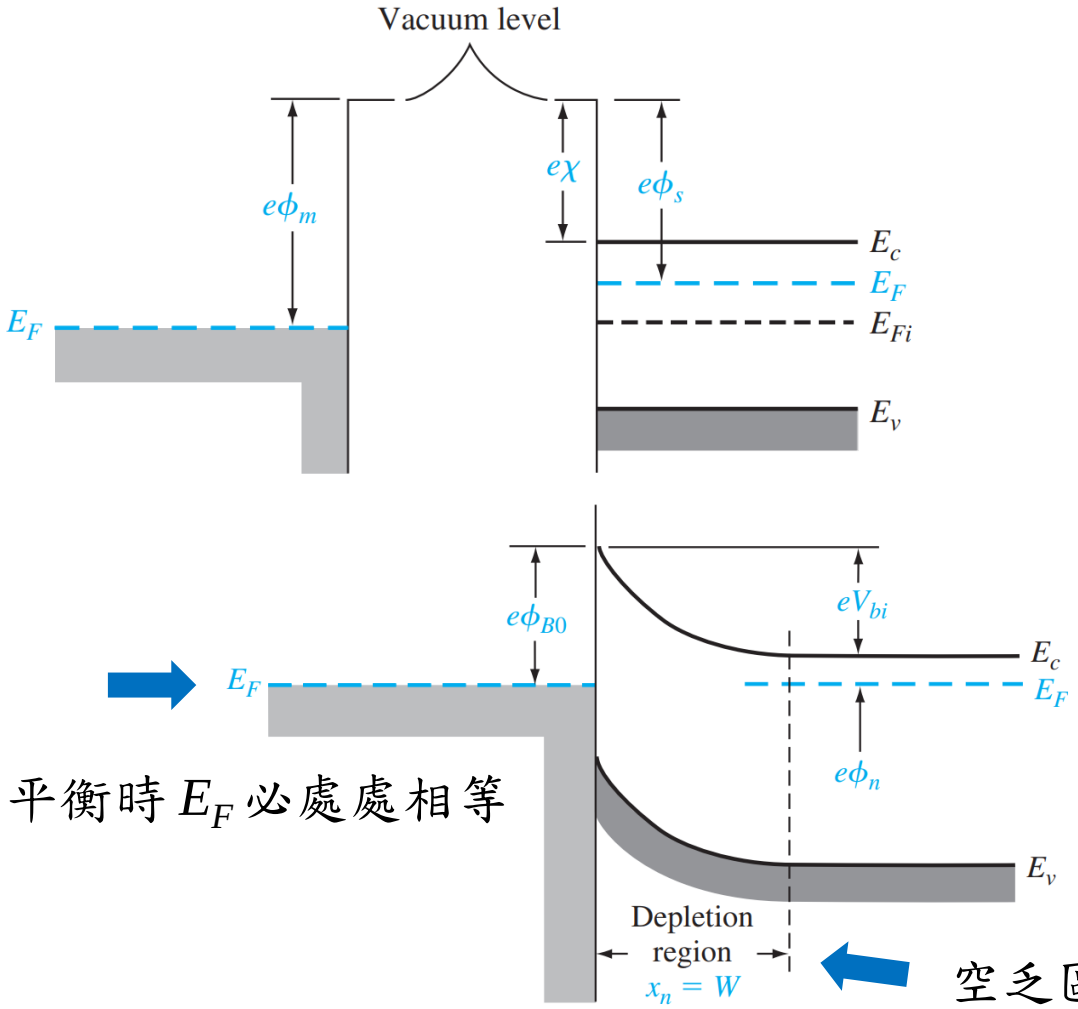
兩邊材料基質不同時稱之為異質介面 Heterojunction



- Schottky Diode
- Ohmic contact
- Tunneling Barrier

Schottky Diode

Metal-semiconductor contact, or Schottky barrier diode is mostly made on **n-type** semiconductor.



平衡時 E_F 必處處相等

ϕ_m 金屬功函數 work function：

使電子脫離金屬所需能量

ϕ_s 半導體功函數 semiconductor work function：

使電子脫離費米能階所需能量

χ 電子親和能 electron affinity：

使電子脫離傳導帶所需能量

假設：$\phi_m > \phi_s$

空乏區(電子擴散至金屬)

金屬功函數與電子親和能

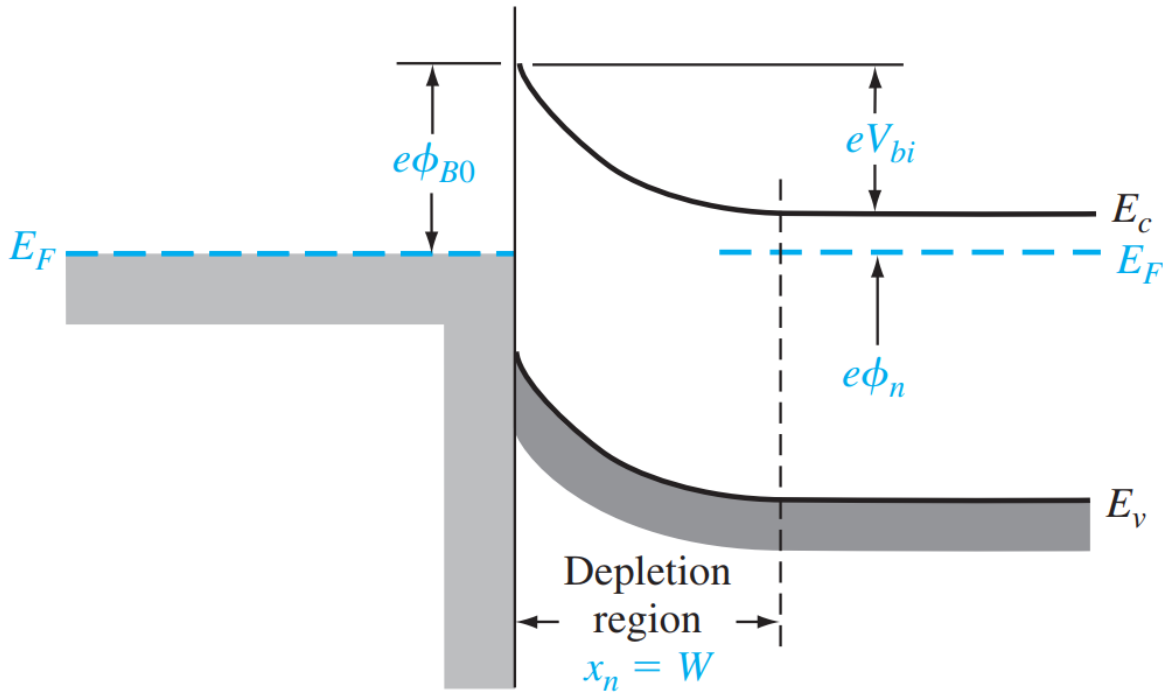
Table 9.1 | Work functions of some elements

Element	Work function, ϕ_m
Ag, silver	4.26
Al, aluminum	4.28
Au, gold	5.1
Cr, chromium	4.5
Mo, molybdenum	4.6
Ni, nickel	5.15
Pd, palladium	5.12
Pt, platinum	5.65
Ti, titanium	4.33
W, tungsten	4.55

Table 9.2 | Electron affinity of some semiconductors

Element	Electron affinity, χ
Ge, germanium	4.13
Si, silicon	4.01
GaAs, gallium arsenide	4.07
AlAs, aluminum arsenide	3.5

Schottky Diode (平衡時)



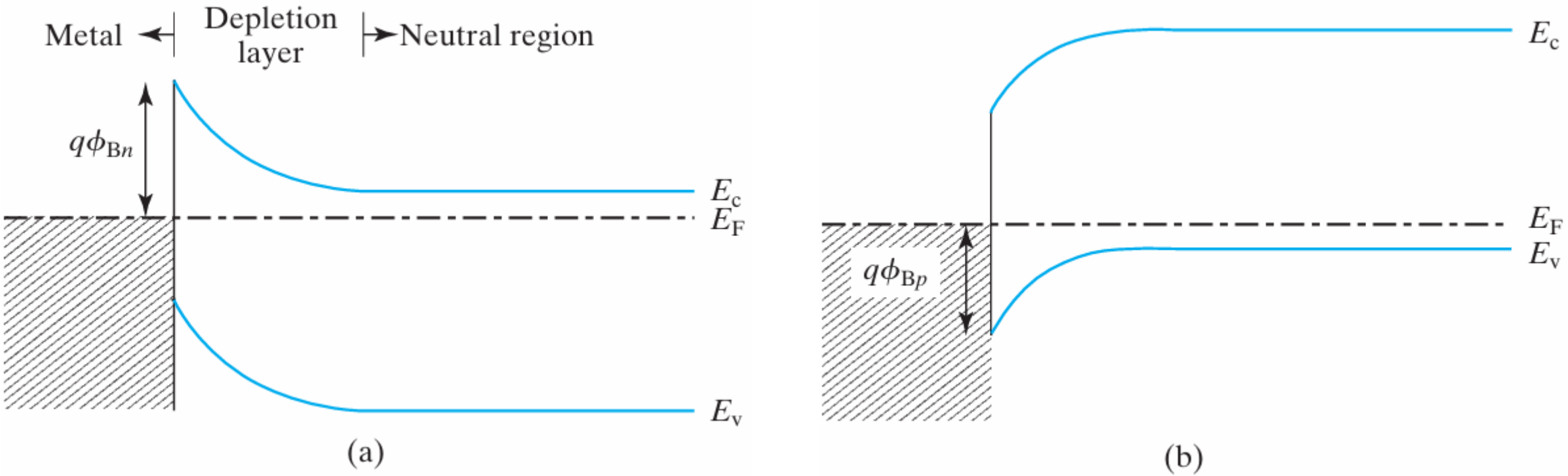
$$\phi_{B0} = \phi_m - \chi$$

$$V_{bi} = \phi_{B0} - \phi_n$$

$$\phi_n = E_c - E_F$$

與摻雜濃度有關，濃度愈高，差值愈小

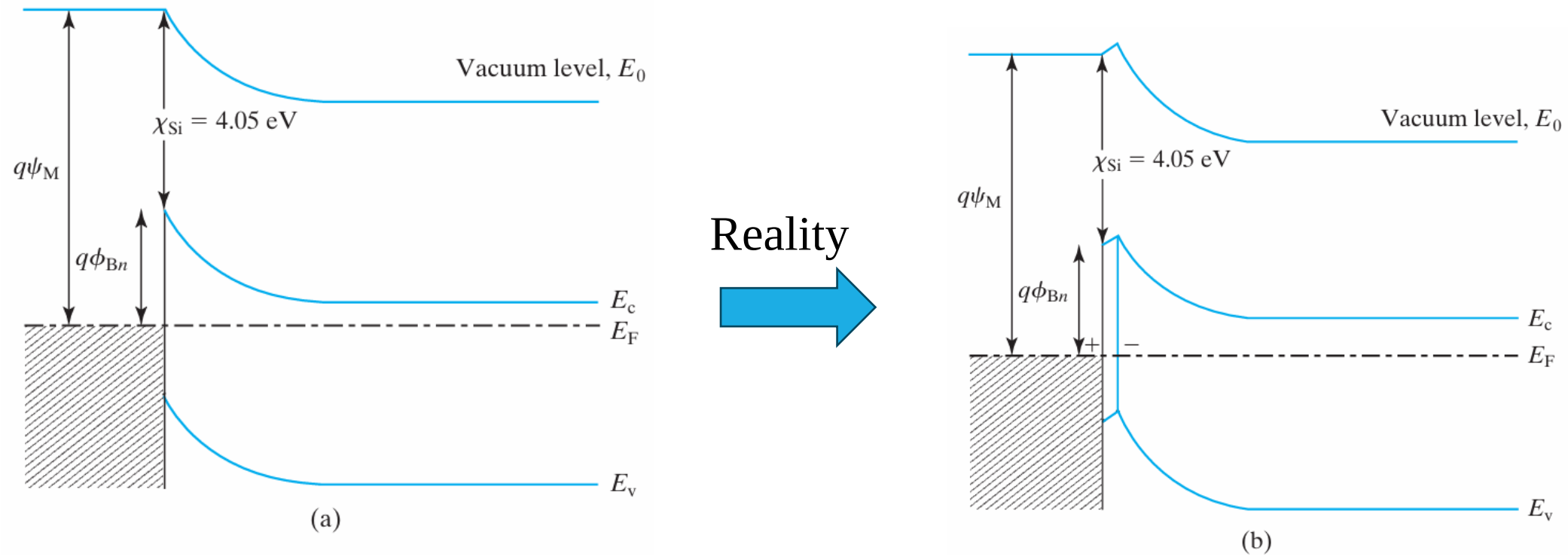
Energy band diagram of metal–semiconductor contact



$$\phi_{Bn} + \phi_{Bp} \approx E_g$$

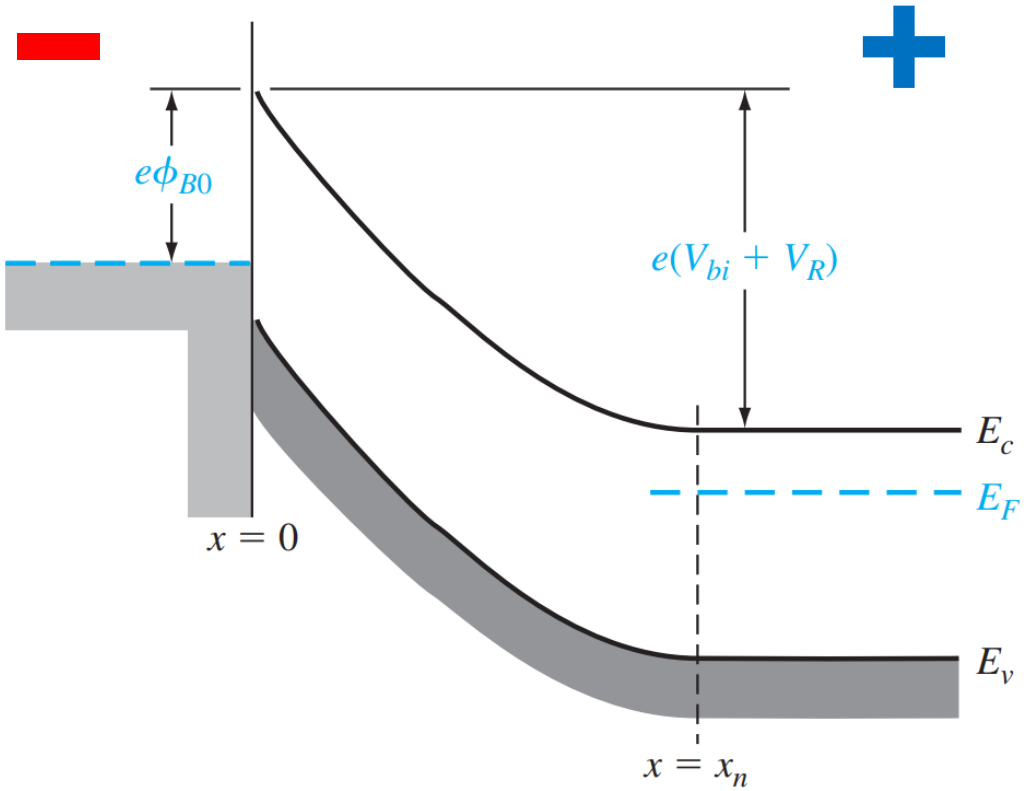
Fermi-level pinning

- Fermi-level pinning是一個在金屬–半導體界面上發生的現象，指的是半導體中的費米能級在接觸金屬後被固定在一個特定的能量位置上，不再受到金屬的功函數影響
- Fermi-level pinning主要由界面間隙狀態（interface gap states）引起，這些狀態會在金屬和半導體之間形成電荷分布，使得費米能級被固定

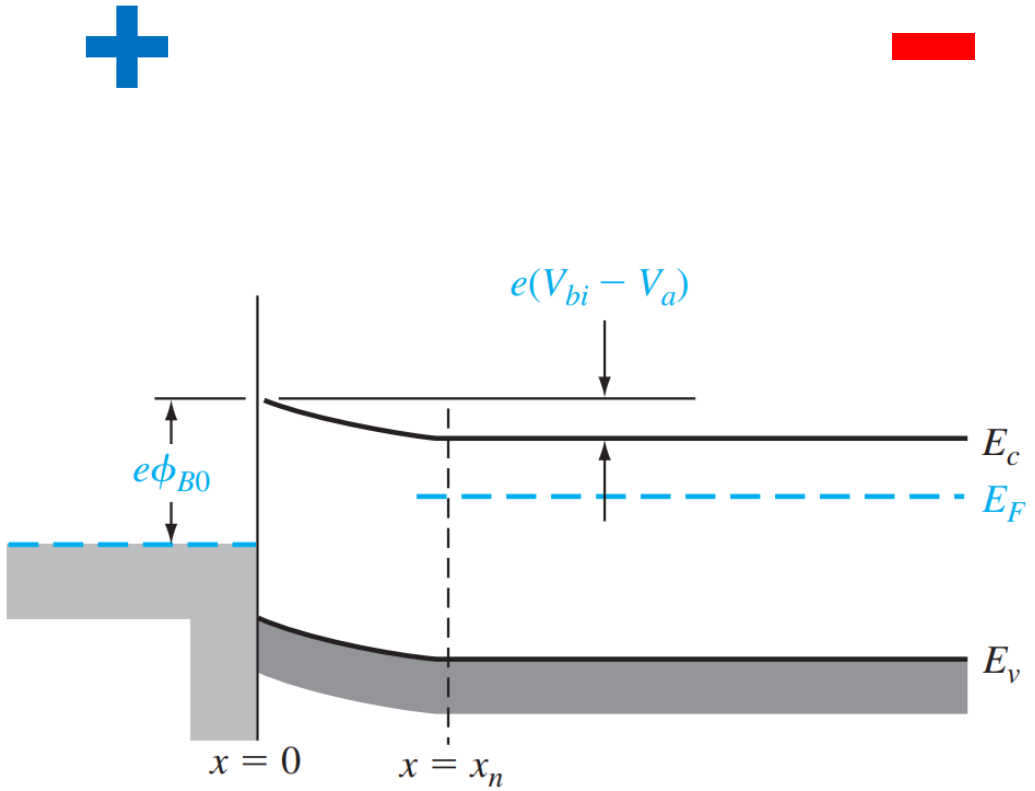


Schottky Diode (加偏壓)

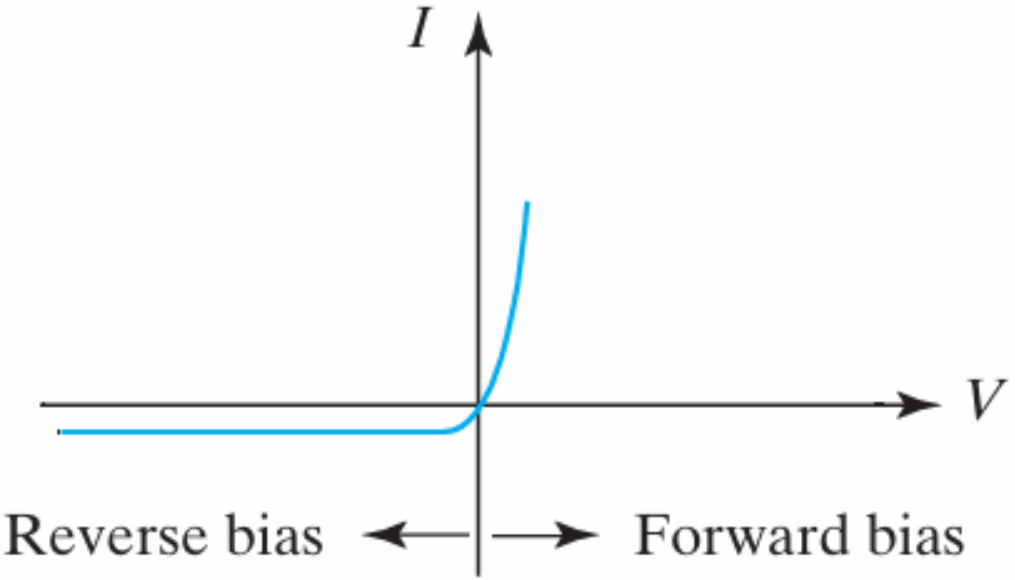
逆向偏壓
(無電流)



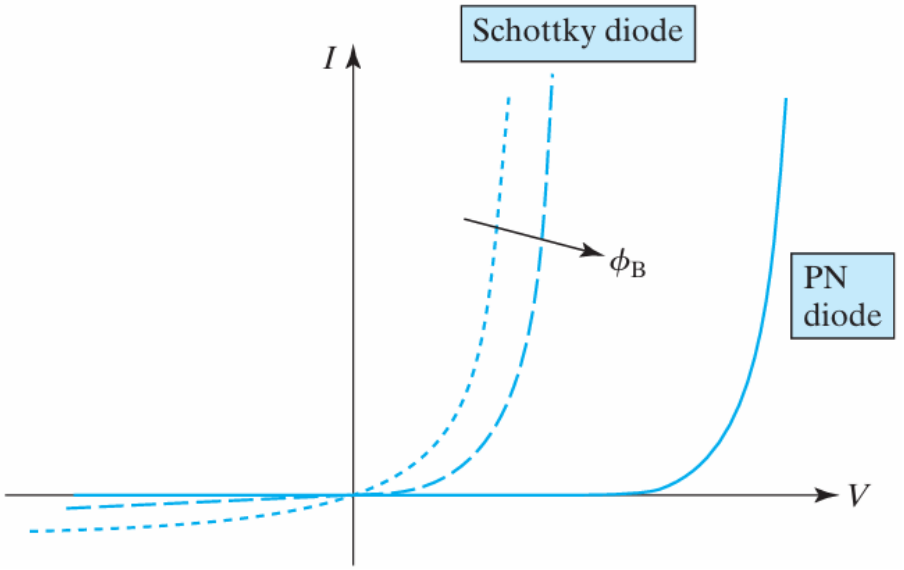
順向偏壓
(有電流)



Schottky Diode (加偏壓)

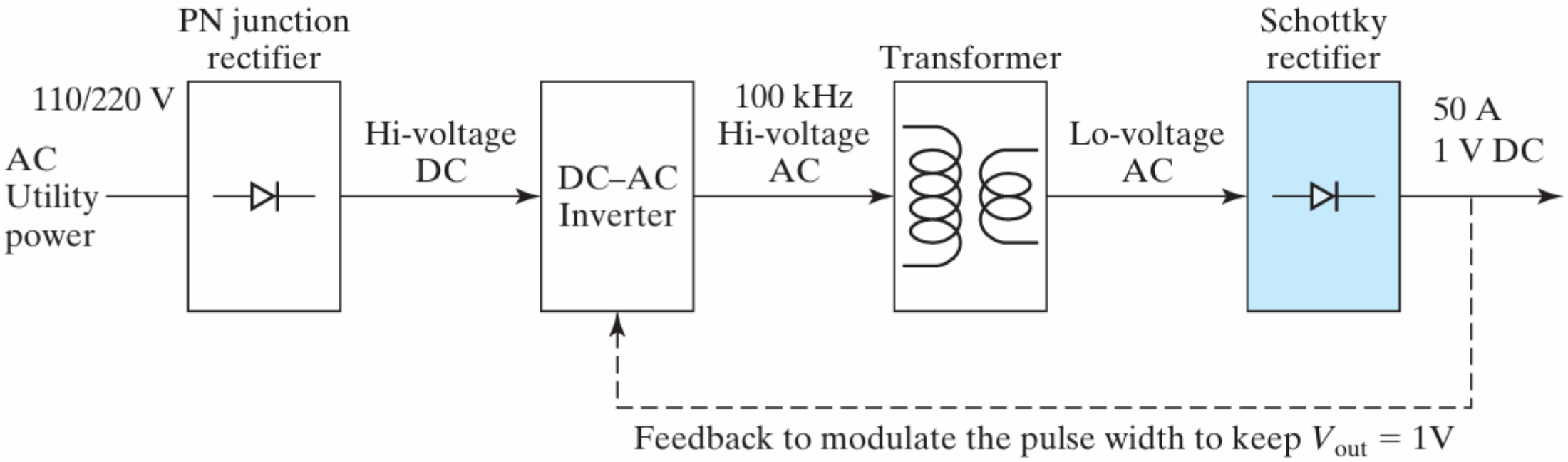


(d) Schottky diode *IV*.

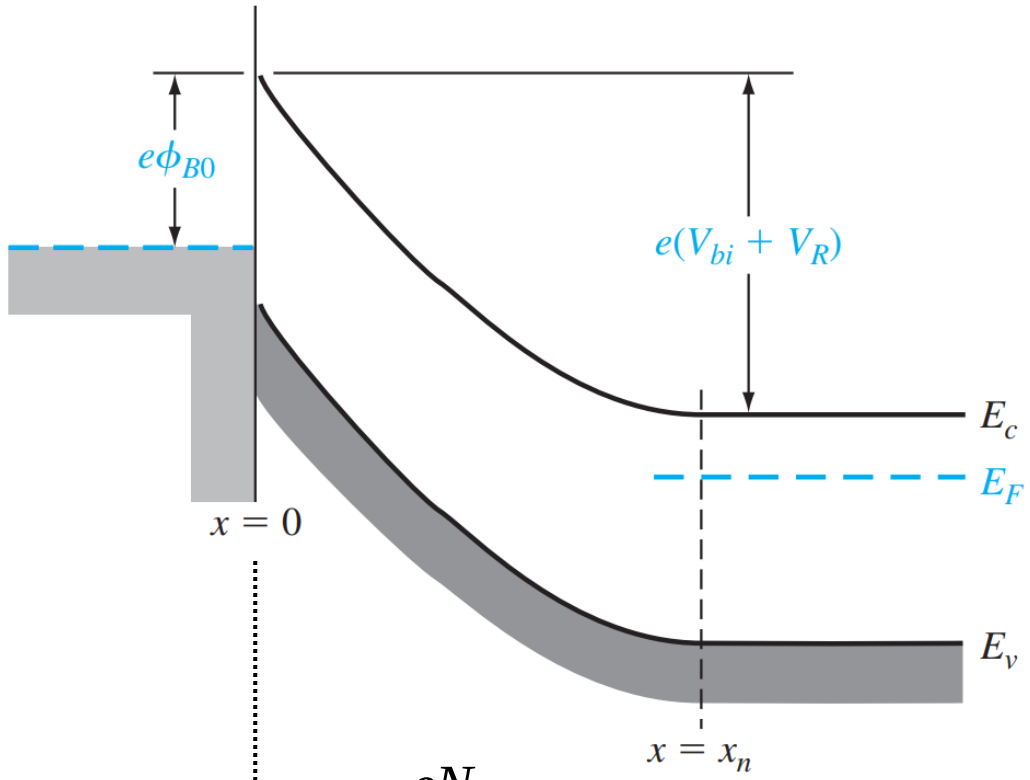


- Schottky diode has a lower "turn-on" voltage than that of a p-n junction diode (~0.6-0.8V)
- On the other hand, the breakdown voltage is lower than p-n junction diode
- The main tactic to pick up the diode is application, for instance, switch, high voltage field and so on.

Schottky Diode + PN Diode



電場與空乏區寬度



$$E = 0 \qquad E = -\frac{eN_d}{\varepsilon_s}(x_n - x) \qquad E = 0$$

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} + V_R)}{eN_d}}$$

和 p^+n 介面完全一樣

The depletion width for pn junction

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon_s (V_{bi} + V_R)}{e}\left[\frac{N_a + N_d}{N_a N_d}\right]}$$

Example 9.1

Objective: Determine the theoretical barrier height, built-in potential barrier, and maximum electric field in a metal–semiconductor diode for zero applied bias.

Consider a contact between tungsten and n-type silicon doped to $N_d = 10^{16}$ cm^{-3} at $T = 300$ K.

Example 9.1

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Consider a contact between tungsten and n-type silicon doped to $N_d = 10^{16}$ cm^{-3} at $T = 300$ K.

$$\phi_{B0} = \phi_m - \chi = 4.55 - 4.01 = 0.54 \text{ V}$$

$$\phi_n = \frac{kT}{e} \ln\left(\frac{N_c}{N_d}\right) = 0.0259 \ln\left(\frac{2.8 \times 10^{19}}{10^{16}}\right) = 0.206 \text{ V}$$

$$V_{bi} = \phi_{B0} - \phi_n = 0.54 - 0.206 = 0.334 \text{ V}$$

$$x_n = \left[\frac{2\epsilon_s V_{bi}}{eN_d}\right]^{1/2} = \left[\frac{2(11.7)(8.85 \times 10^{-14})(0.334)}{(1.6 \times 10^{-19})(10^{16})}\right]^{1/2}$$

$$x_n = 0.208 \times 10^{-4} \text{ cm}$$

$$|E_{max}| = \frac{eN_d x_n}{\epsilon_s} = \frac{(1.6 \times 10^{-19})(10^{16})(0.208 \times 10^{-4})}{(11.7)(8.85 \times 10^{-14})}$$

$$|E_{max}| = 3.21 \times 10^4 \text{ V/cm}$$

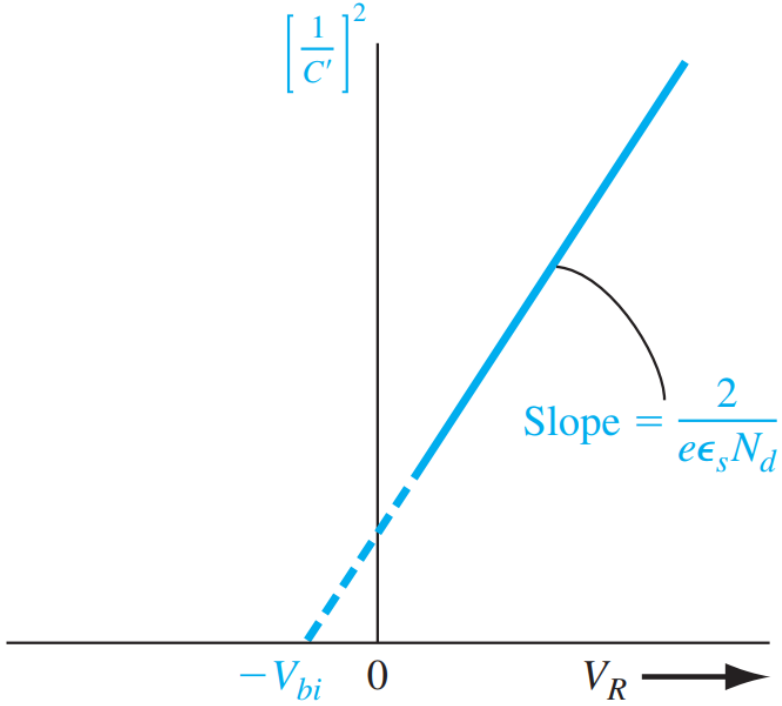
Junction Capacitance

- 和 p^+n 介面完全一樣
- 實驗上可得知材料的內建電位差 V_{bi} 以及摻雜濃度

$$Q' = eN_d x_n$$

$$C' = \frac{dQ'}{dV_R} \approx \sqrt{\frac{\varepsilon_s e N_d}{2(V_{bi} + V_R)}}$$

$$\left(\frac{1}{C'}\right)^2 = \frac{2(V_{bi} + V_R)}{\varepsilon_s e N_d}$$

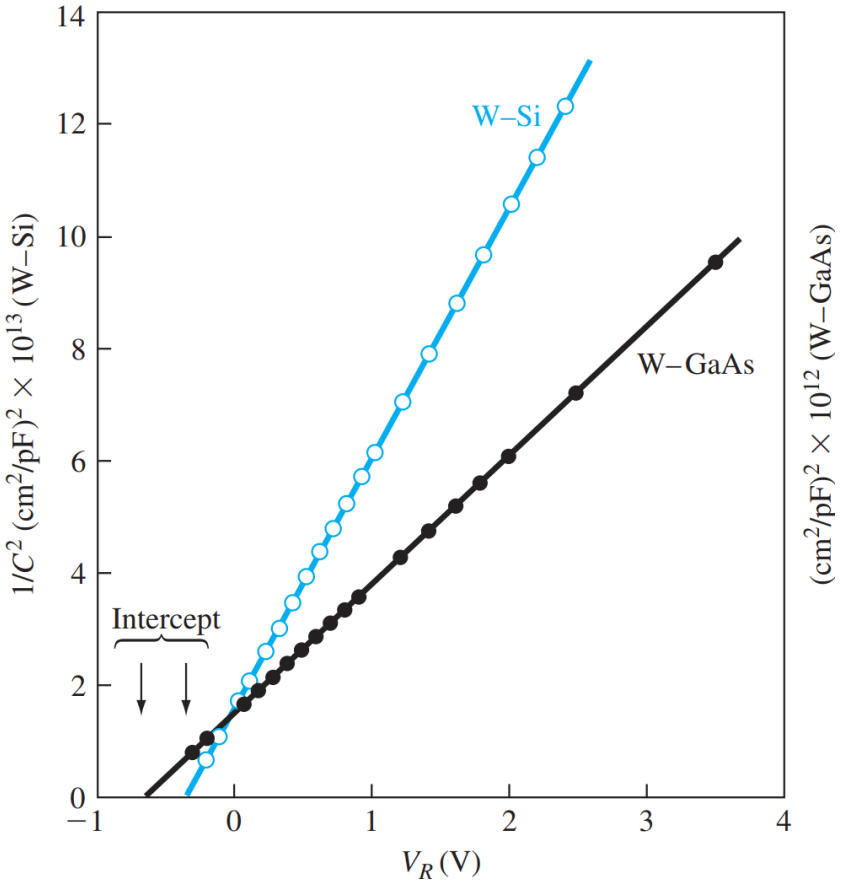


The junction capacitance for pn junction

$$C' = \left\{\frac{e\epsilon_s N_a N_d}{2(V_{bi} + V_R)(N_a + N_d)}\right\}^{1/2}$$

Example 9.2

Objective: To calculate the semiconductor doping concentration and Schottky barrier height from the silicon diode experimental capacitance data shown in Figure 9.3. Assume $T = 300$ K.



Example 9.2

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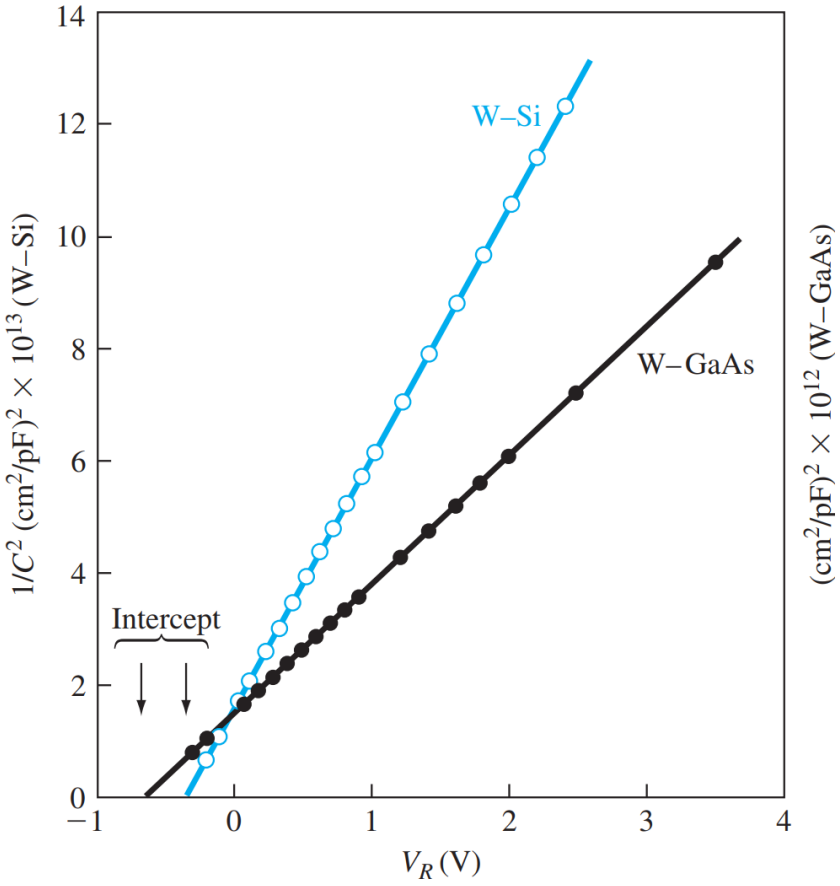
$$\frac{d(1/C')^2}{dV_R} \approx \frac{\Delta(1/C')^2}{\Delta V_R} = \frac{2}{e\epsilon_s N_d} \approx 4.4 \times 10^{13}$$

$$N_d = \frac{2}{(1.6 \times 10^{-19})(11.7)(8.85 \times 10^{-14})(4.4 \times 10^{13})} = 2.7 \times 10^{17}\ \text{cm}^{-3}$$

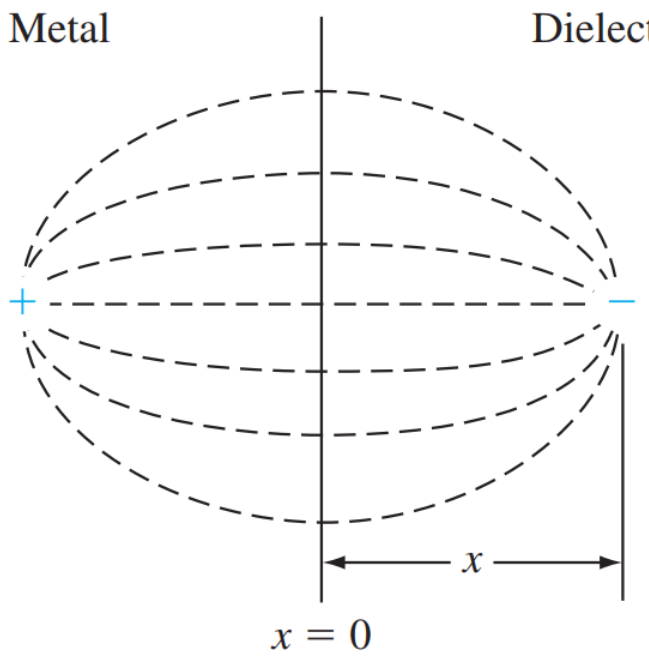
$$\phi_n = \frac{kT}{e} \ln\left(\frac{N_c}{N_d}\right) = (0.0259) \ln\left(\frac{2.8 \times 10^{19}}{2.7 \times 10^{17}}\right) = 0.12\ \text{V}$$

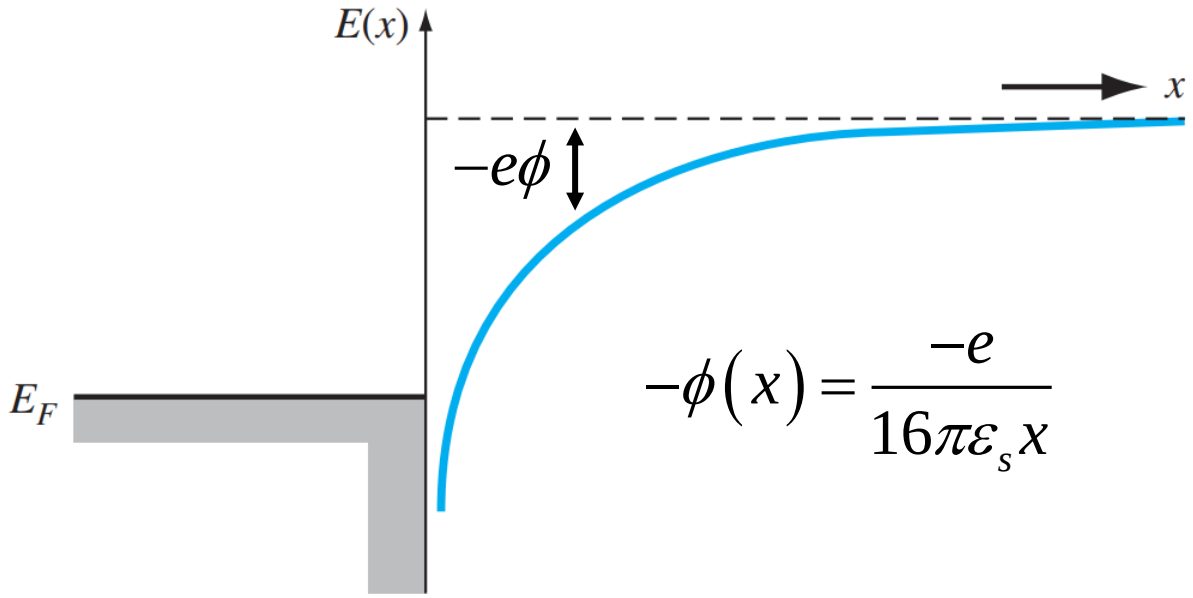
$$\phi_{Bn} = V_{bi} + \phi_n = 0.40 + 0.12 = 0.52\ \text{V}$$



位能障壁上的非理想效應

效應1：Schottky Effect / image-force-induced lowering

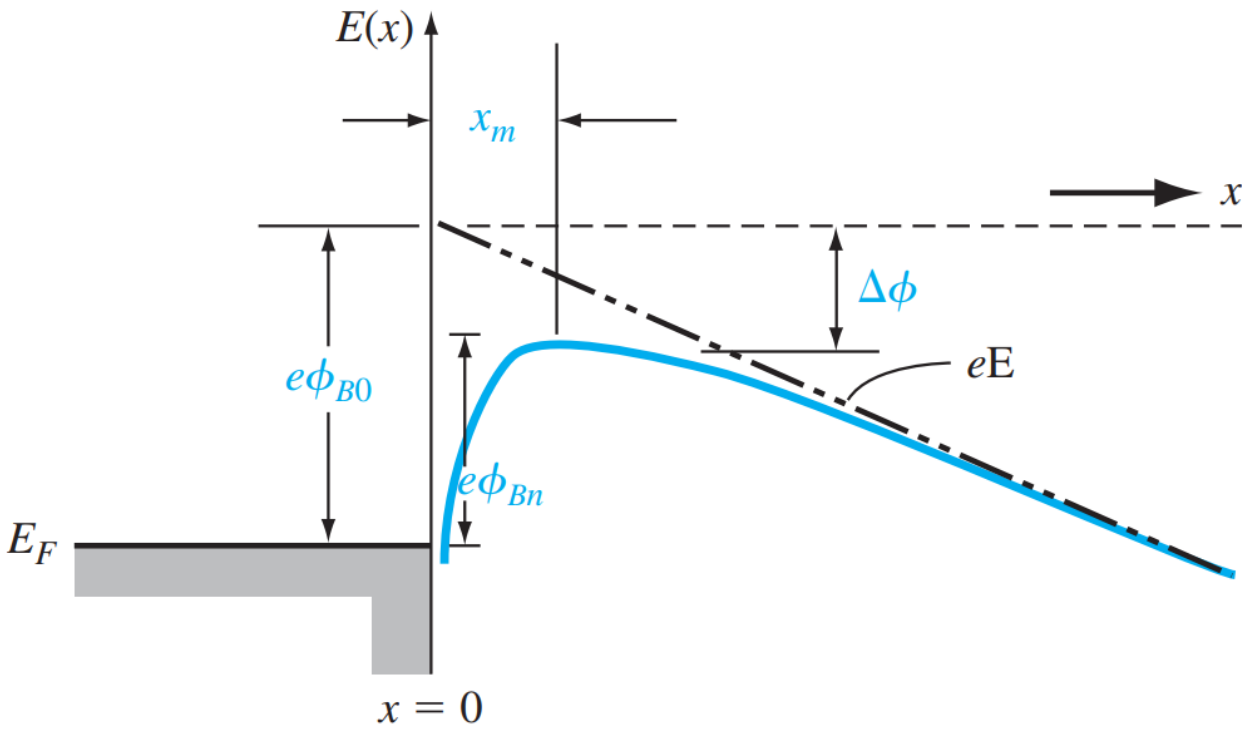




$$-\phi(x) = \frac{-e}{16\pi\varepsilon_s x}$$

$$F = \frac{-e^2}{4\pi\epsilon_s(2x)^2} = -e\mathrm{E}$$

位能障壁上的非理想效應



$$-\phi(x) = +\int_x^{\infty} \mathrm{E}\, dx'$$

$$-\phi(x) = \frac{-e}{16\pi\varepsilon_s x} - \mathrm{E}x$$

$$x_m = \sqrt{\frac{e}{16\pi\varepsilon_s \mathrm{E}}}$$

$$\Delta\phi = \sqrt{\frac{eE}{4\pi\varepsilon_s}}$$

$$\phi_{Bn} = \phi_{B0} - \Delta\phi$$

Example 9.3

Objective: Calculate the Schottky barrier lowering and the position of the maximum barrier height.

Consider a gallium arsenide metal–semiconductor contact in which the electric field in the semiconductor is assumed to be $E = 6.8 \times 10^4$ V/cm.

$$\Delta\phi = \sqrt{\frac{eE}{4\pi\epsilon_s}} = \sqrt{\frac{(1.6 \times 10^{-19})(6.8 \times 10^4)}{4\pi\,(13.\,1)(8.85 \times 10^{-14})}} = 0.0273 \text{ V}$$

$$x_m = \sqrt{\frac{e}{16\pi\epsilon_s E}} = \sqrt{\frac{(1.6 \times 10^{-19})}{16\pi(13.1)(8.85 \times 10^{-14})(6.8 \times 10^4)}}$$

$$x_m = 2 \times 10^{-7} \text{ cm} = 20 \text{ Å}$$

位能障壁上的非理想效應

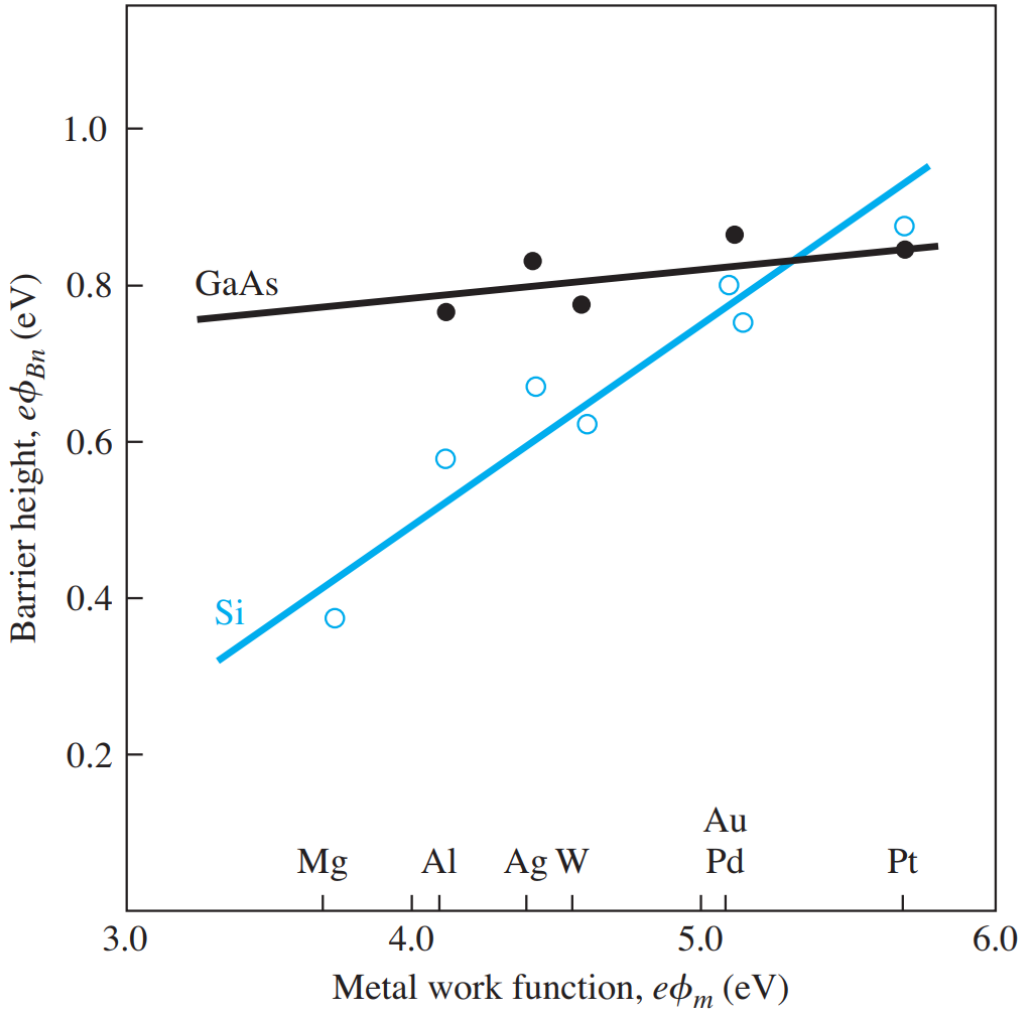
效應2：Interface States

理論上障壁的高度應該要滿足下式：

$$\phi_{B0} = \phi_m - \chi$$

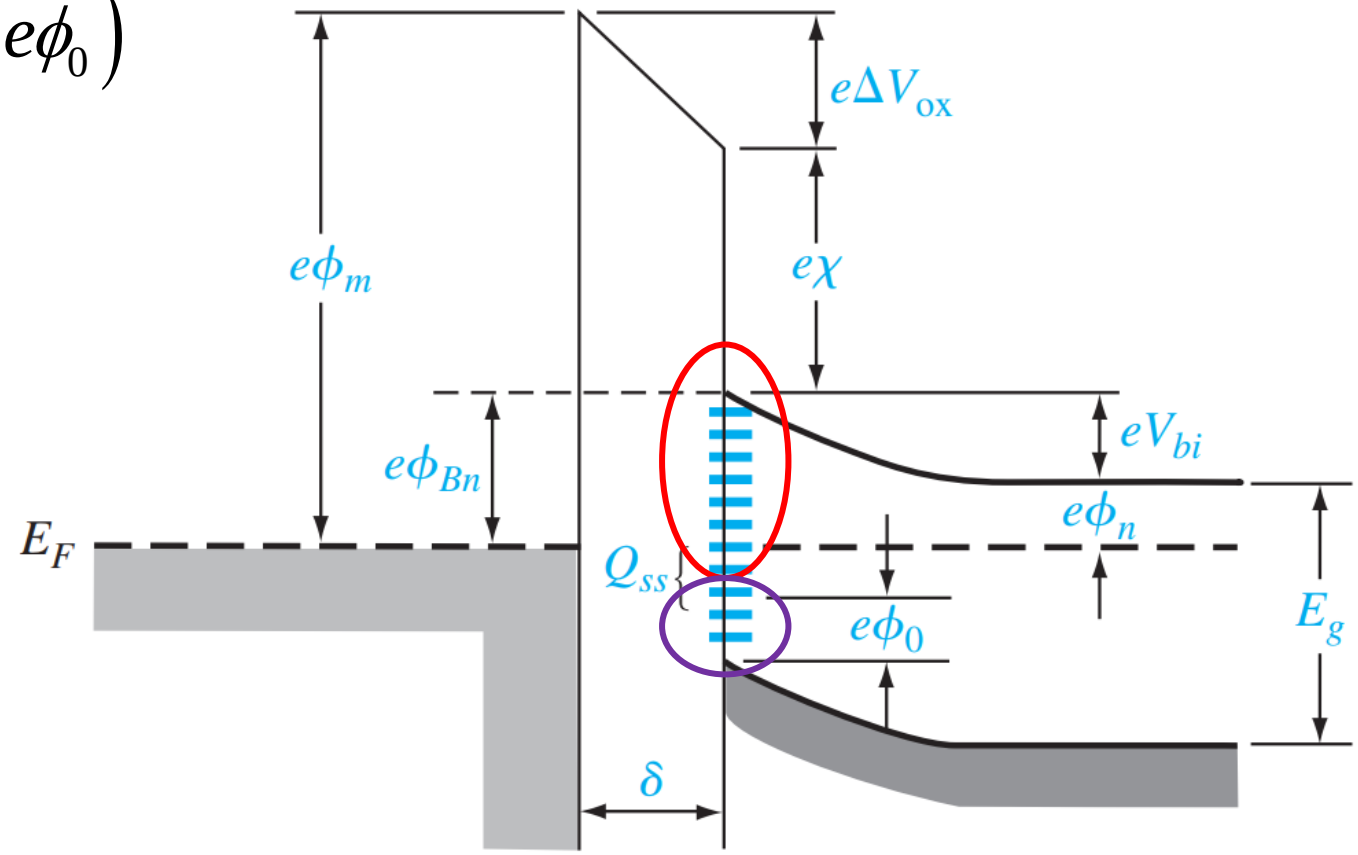
但實驗結果顯示 GaAs 卻是符合下式：

$$\phi_{Bn} = \frac{1}{e}\left(E_g - e\phi_0\right)$$



位能障壁上的非理想效應

$$\phi_{Bn} = \frac{1}{e}\left(E_g - e\phi_0\right)$$



Acceptor state / Donor state

位能障壁上的非理想效應

	Schottky Effect	Interface State
起因	半導體材料中電子靠近金屬時誘導的鏡像電荷效應	接面處的結構缺陷、晶格不匹配
作用機制	鏡像電荷對電子產生吸引，產生庫倫利核電場，從而降低能障	局域化能級捕獲/釋放載流子改變局部電荷分佈，導致 Fermi level pinning
對位能障的影響	位能障降低	Fermi level pinning
對元件影響	降低正向偏壓的導通電壓，但同時增加反向漏電流，影響元件穩定性	可能導致漏電流增加、元件操作不穩定

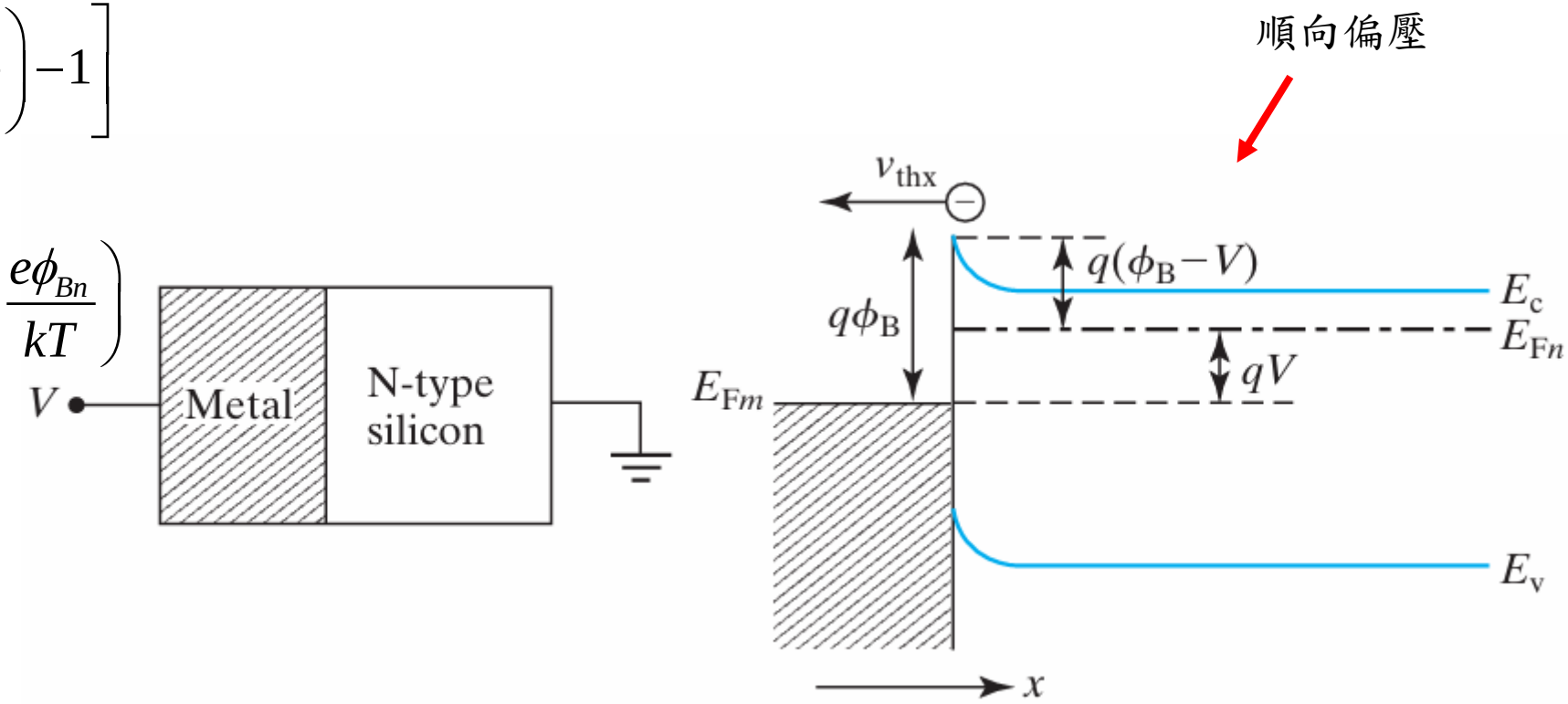
Thermionic Emission Theory

- 在Schottky二極體中，金屬和n型半導體直接接觸後，會在界面處形成一個能量障，稱為Schottky barrier
- 根據熱電子發射理論，在一定溫度下部分電子會獲得足夠能量，克服這一能障，從而從半導體側進入金屬側，產生電流。

$$J = J_{sT}\left[\exp\left(\frac{eV_a}{kT}\right) - 1\right]$$

$$J_{sT} = A^* T^2 \exp\left(-\frac{e\phi_{Bn}}{kT}\right)$$

$$A^* = \frac{4\pi e m_n^* k^2}{h^3}$$



Example 9.4

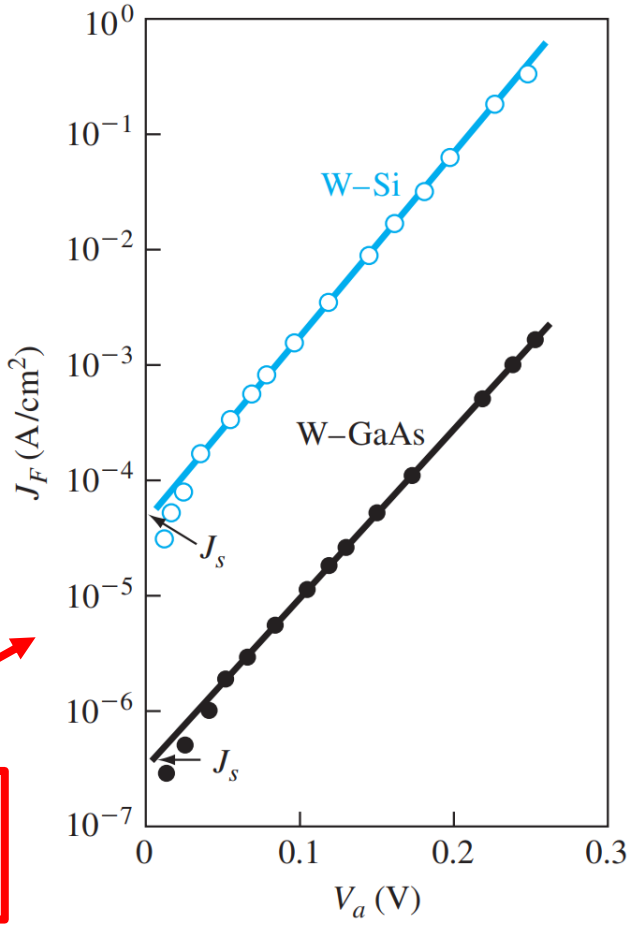
Objective: Determine the effective Richardson constant from the current–voltage characteristics.

Consider the tungsten–silicon diode curve in Figure 9.9 and assume a barrier height of $\phi_{Bn} = 0.67$ V. From the figure, $J_{sT} \approx 6 \times 10^{-5}$ A/cm^2.

$$J_{sT} = A^* T^2 \exp\left(\frac{-e\phi_{Bn}}{kT}\right)$$

$$A^* = \frac{J_{sT}}{T^2} \exp\left(\frac{+e\phi_{Bn}}{kT}\right)$$

$$A^* = \frac{6 \times 10^{-5}}{(300)^2} \exp\left(\frac{0.67}{0.0259}\right) = 114 \text{ A/K}^2\text{-cm}^2$$

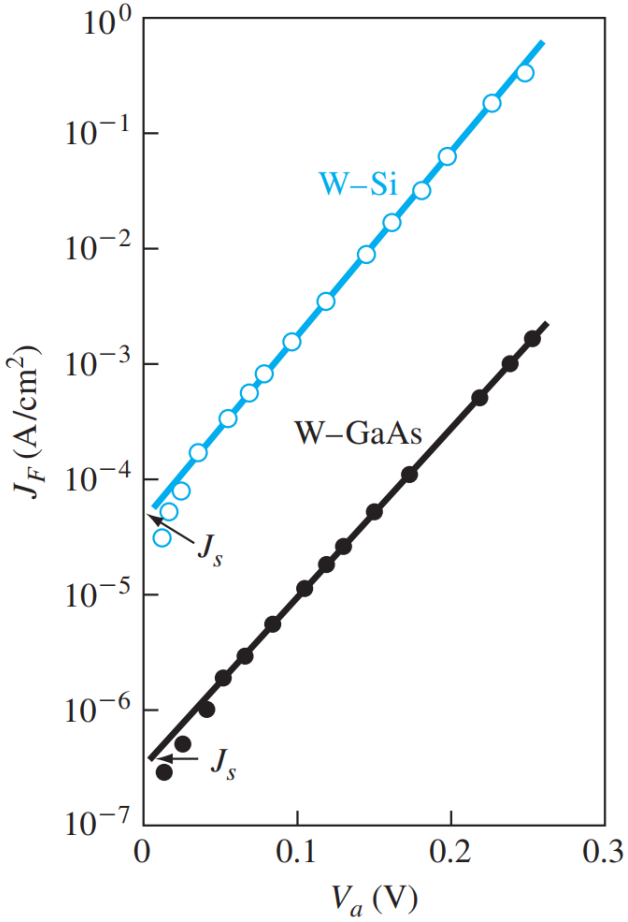


The effective mass of electron in Si is larger than GaAs, but why the forward current of Si is larger than GaAs ?

Example 9.4

The effective mass of electron in Si is larger than GaAs, but why the forward current of Si is larger than GaAs ?

	Ag	Al	Au	Cr	Ni	Pt	W
Φ_M (in vacuum)	4.3	4.25	4.8	4.5	4.5	5.3	4.6
n-Ge	0.54	0.48	0.59		0.49		0.48
p-Ge	0.5		0.3				
n-Si	0.78	0.72	0.8	0.61	0.61	0.9	0.67
p-Si	0.54	0.58	0.34	0.5	0.51		0.45
n-GaAs	0.88	0.8	0.9			0.84	0.8
p-GaAs	0.63		0.42				



Source: Vilniaus Universitetas, Semiconductor Physics Department, Lithuania

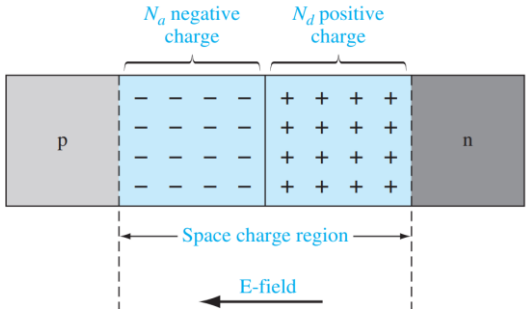
Comparison of Schottky and pn Junction

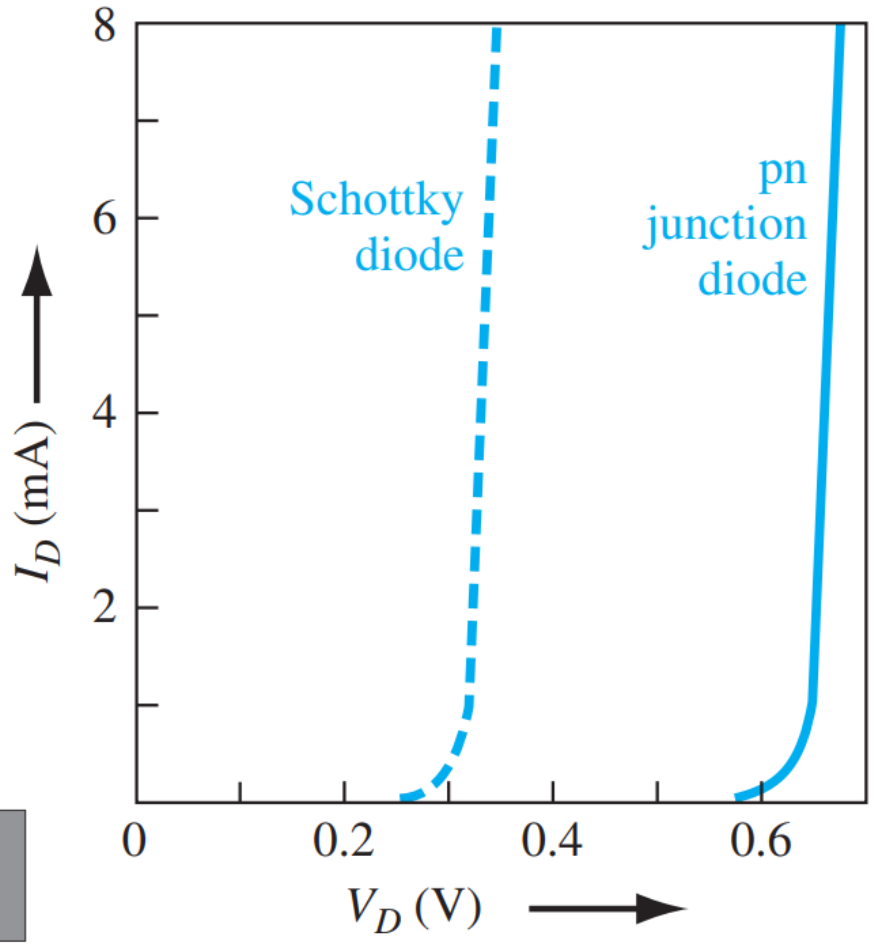
因為 $J_{sT} >> J_s$，Schottky diode 開啟的電壓比較小

$$J = J_{sT}\left[\exp\left(\frac{eV_a}{kT}\right) - 1\right]$$

Schottky diode $J_{sT} = A^* T^2 \exp\left(-\frac{e\phi_{Bn}}{kT}\right)$

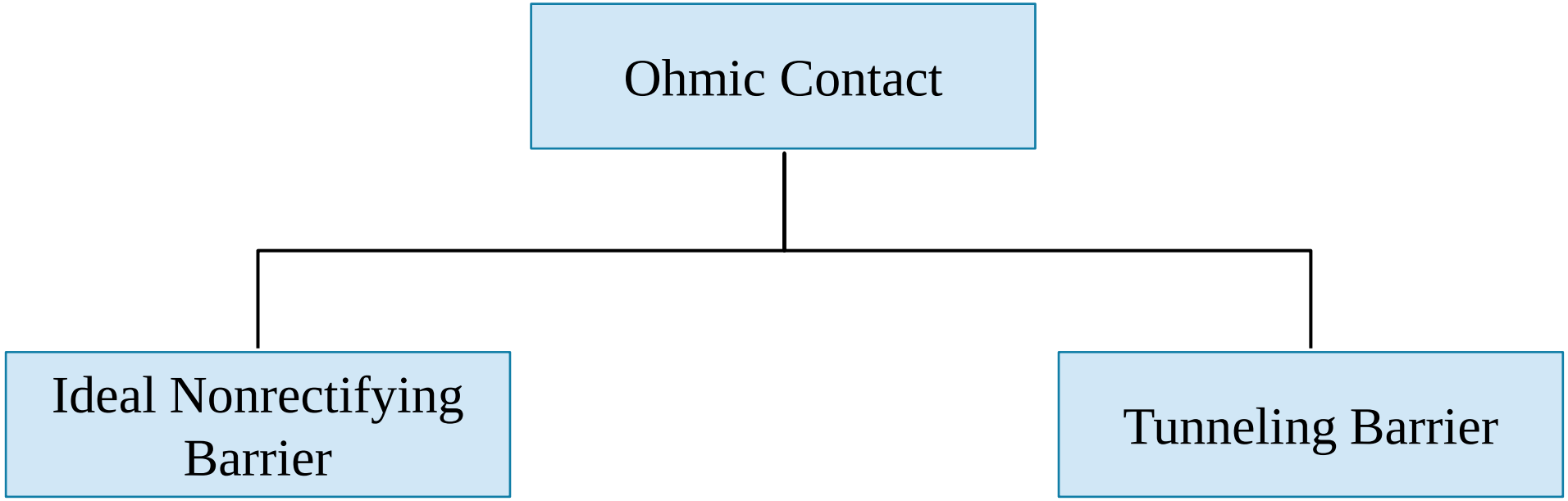
pn junction $J_s = \frac{eD_n n_{p0}}{L_n} + \frac{eD_p p_{n0}}{L_p}$





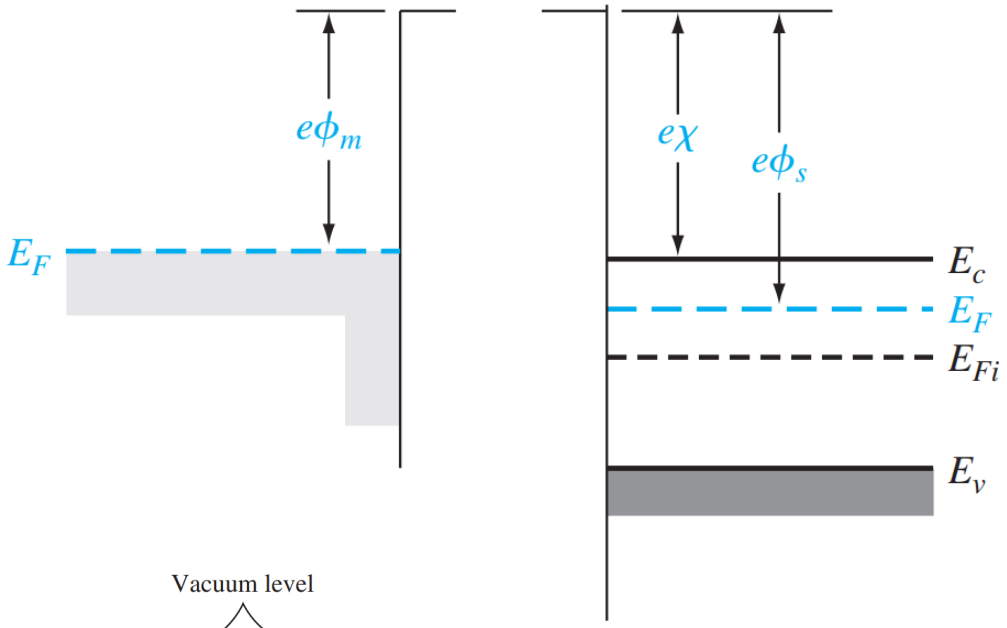
Ohmic Contact

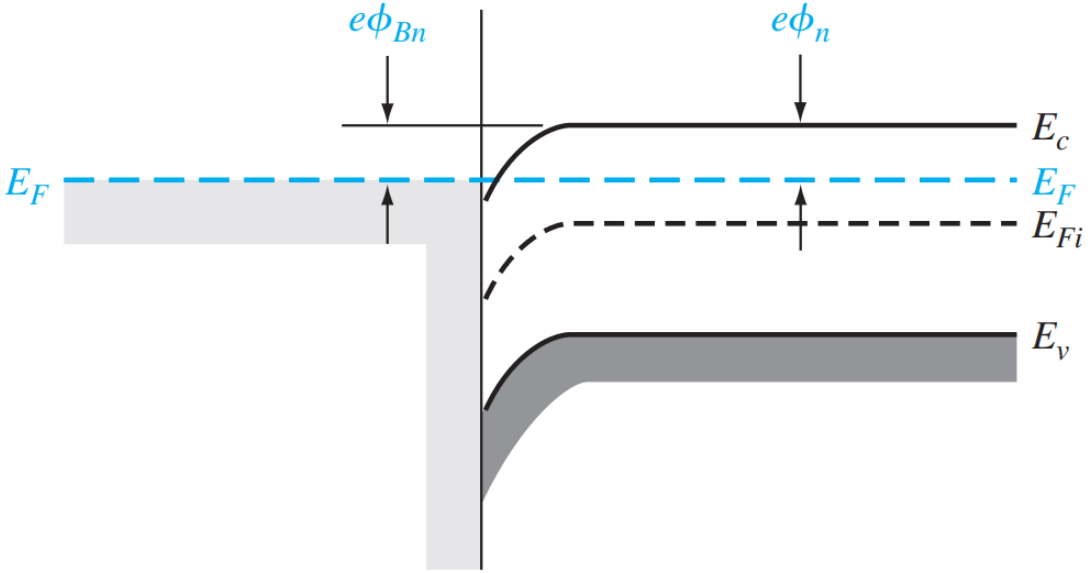
無論電位差的方向，電子都非常容易流動，電阻值低，適合拿來連接金屬導線，這類接觸就稱為歐姆接觸 (ohmic contact)

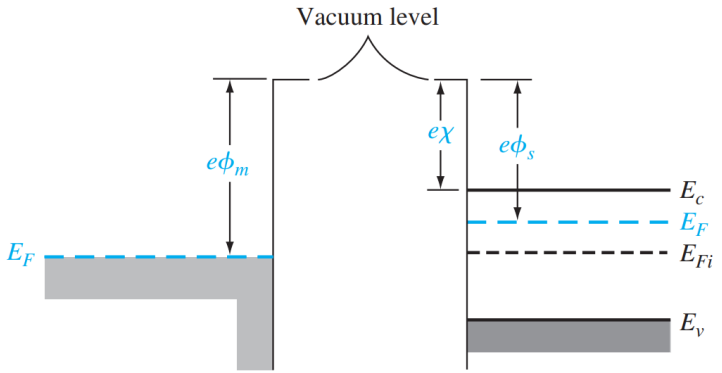


Ideal Nonrectifying Barrier (n type)

$\phi_m < \phi_s$，多數載子為電子

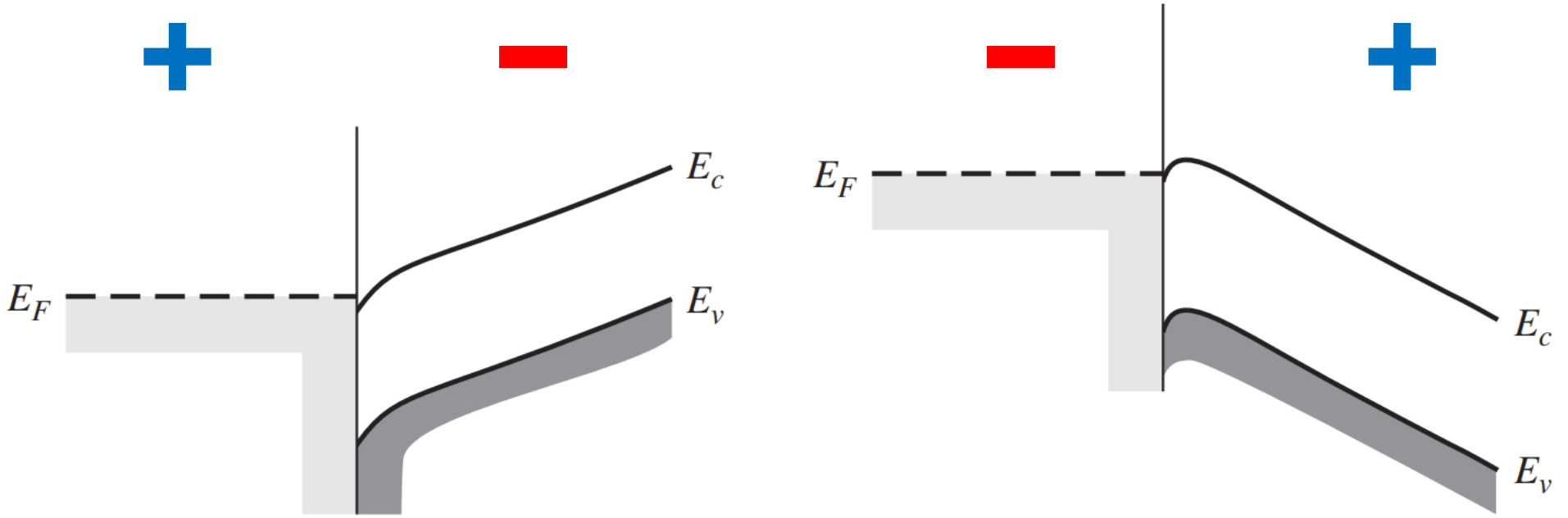






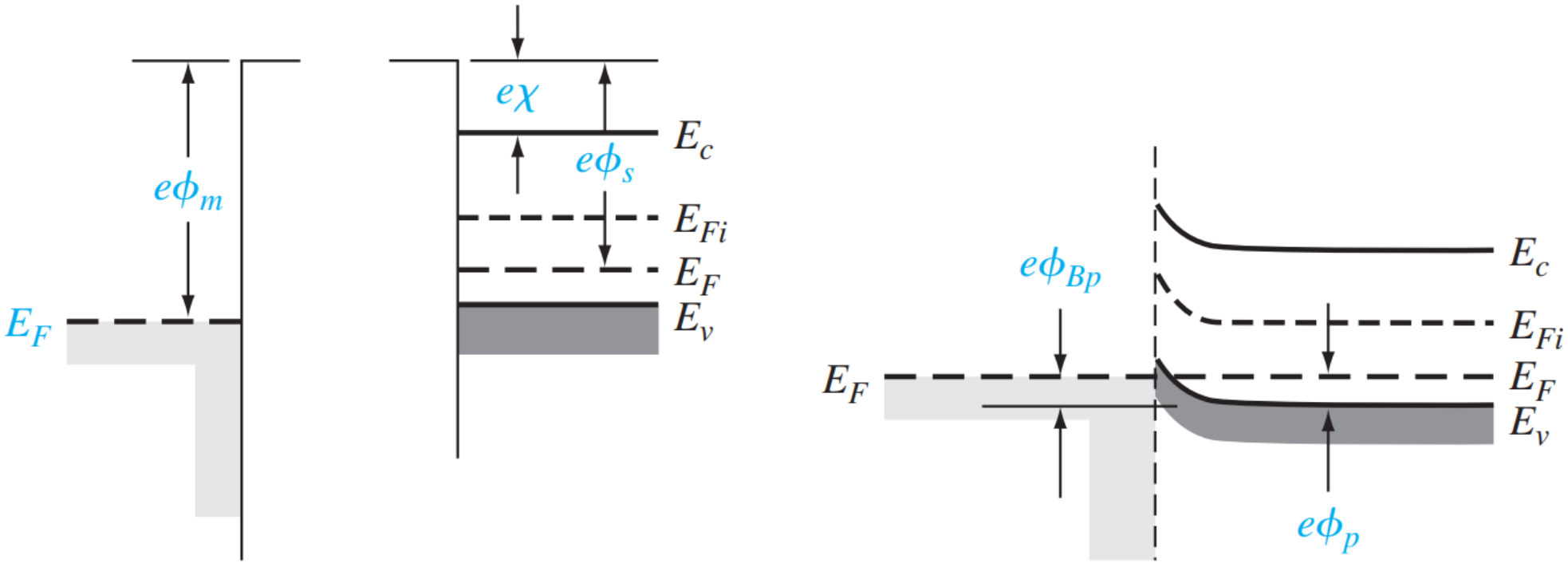
$\phi_m > \phi_s$ Schottky barrier

Ideal Nonrectifying Barrier (n type)



Ideal Nonrectifying Barrier (p type)

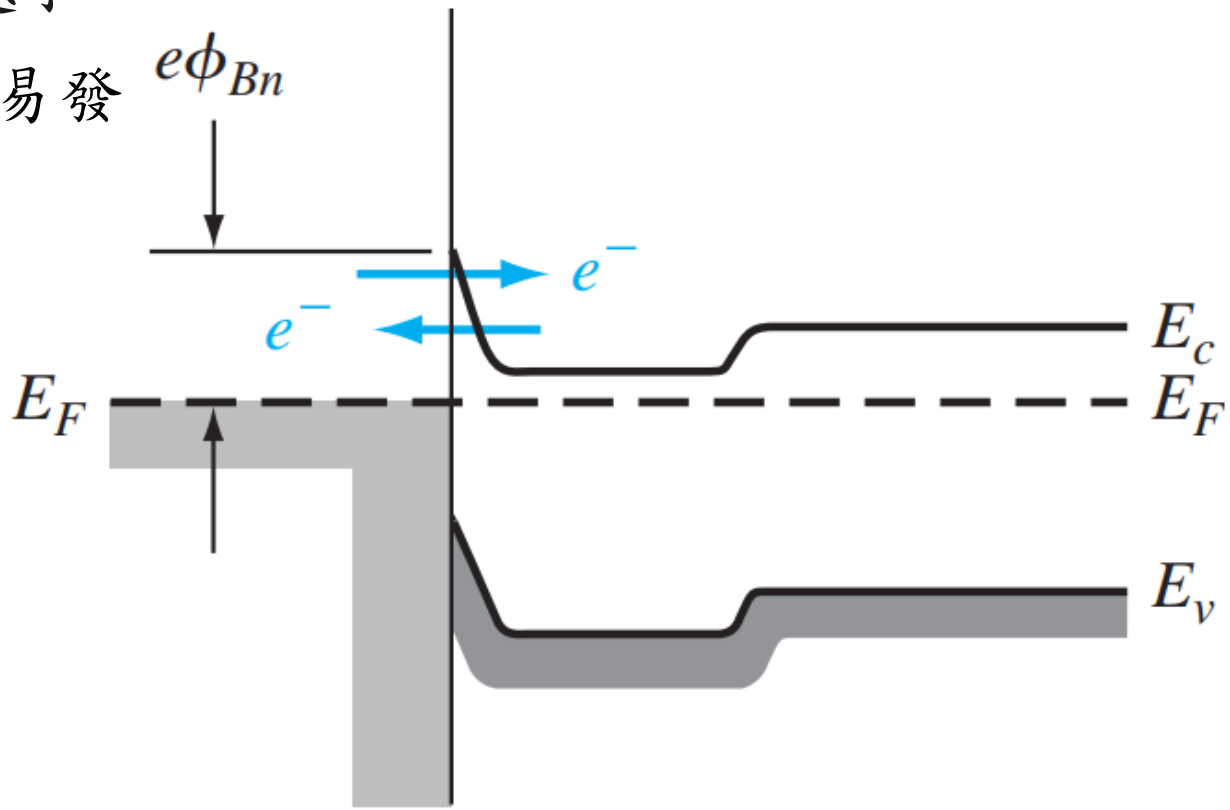
$\phi_m > \phi_s$，多數載子為電洞



Tunneling Barrier

- 金屬-半導體接觸中的空間電荷寬度與半導體摻雜的平方根成反比
- 參雜濃度越高，則空間電荷寬度越小
- Depletion region越小，表示越容易發生tunneling barrier

$$W = x_n = \left[\frac{2\epsilon_s(V_{bi} + V_R)}{eN_d}\right]^{1/2}$$



Tunneling Barrier

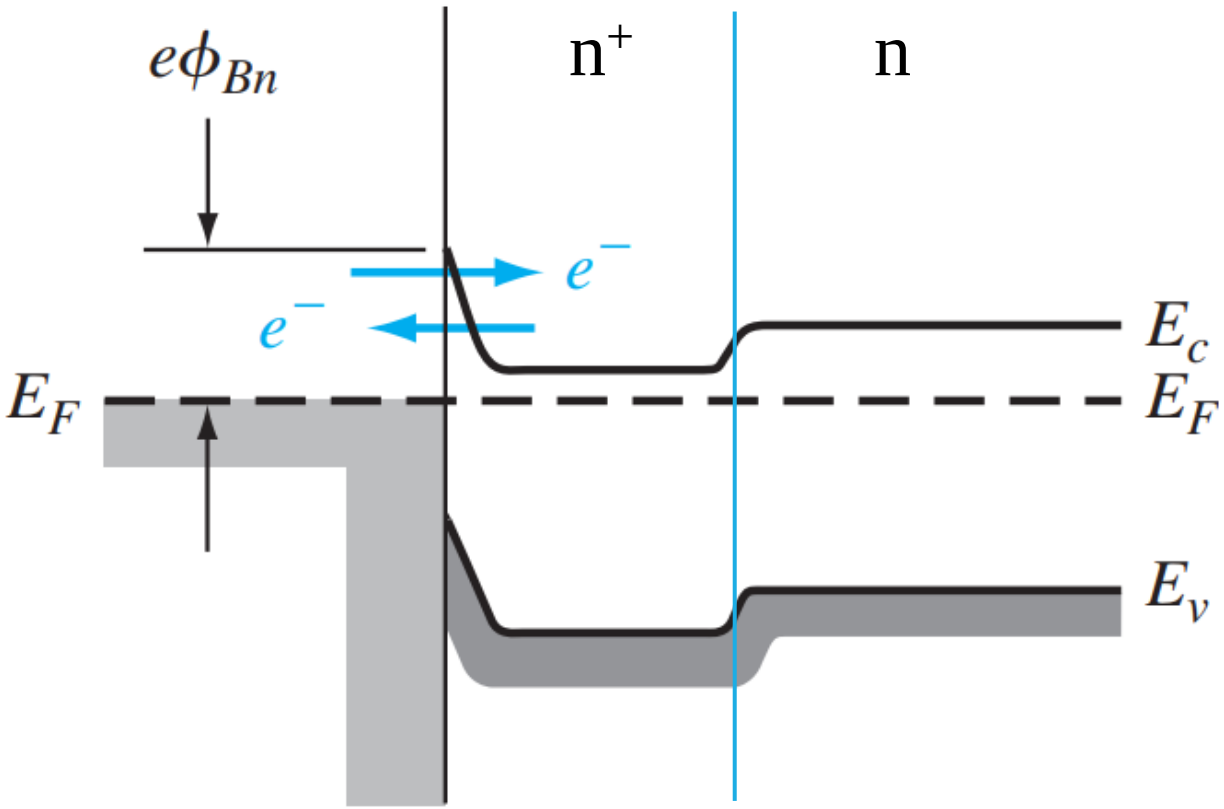
Tunneling Current：

$$J_t \propto \exp\left(\frac{-e\phi_{Bn}}{E_{oo}}\right)$$

$$E_{oo} = \frac{e\hbar}{2}\sqrt{\frac{N_d}{\epsilon_s m_n^*}}$$

摻雜愈濃愈容易穿隧

$$W = \sqrt{\frac{2\varepsilon_s\left(V_{bi}+V_R\right)}{eN_d}}$$



Example 9.7

Objective: Calculate the space charge width for a Schottky barrier on a heavily doped semiconductor.

Consider silicon at $T = 300$ K doped at $N_d = 7 \times 10^{18}$ cm^{-3}. Assume a Shottky barrier with $\phi_{Bn} = 0.67$ V. For this case, we can assume that $V_{bi} \approx \phi_{B0}$. Neglect the barrier lowering effect.

$$x_n = \left[\frac{2\epsilon_s V_{bi}}{eN_d}\right]^{1/2} = \left[\frac{2(11.7)(8.85 \times 10^{-14})(0.67)}{(1.6 \times 10^{-19})(7 \times 10^{18})}\right]^{1/2}$$

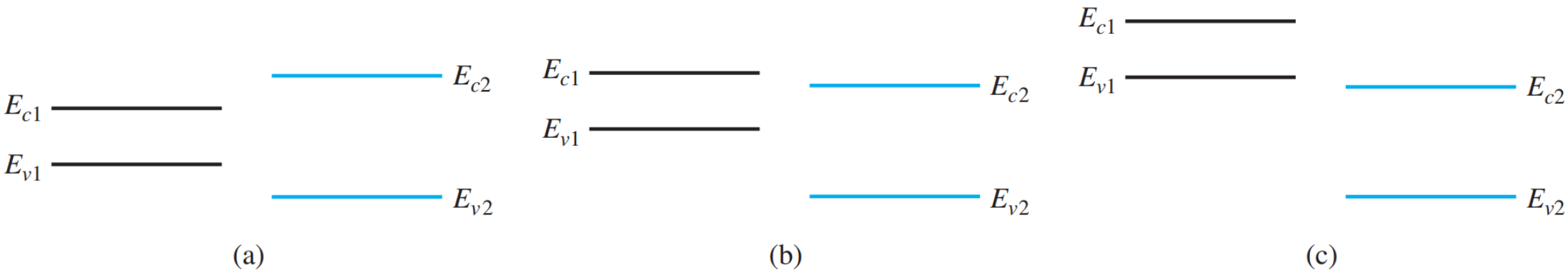
$$x_n = 1.1 \times 10^{-6} \text{ cm} = 110 \text{ Å}$$

Energy-Band Diagrams of Heterojunctions

Straddling (most cases)

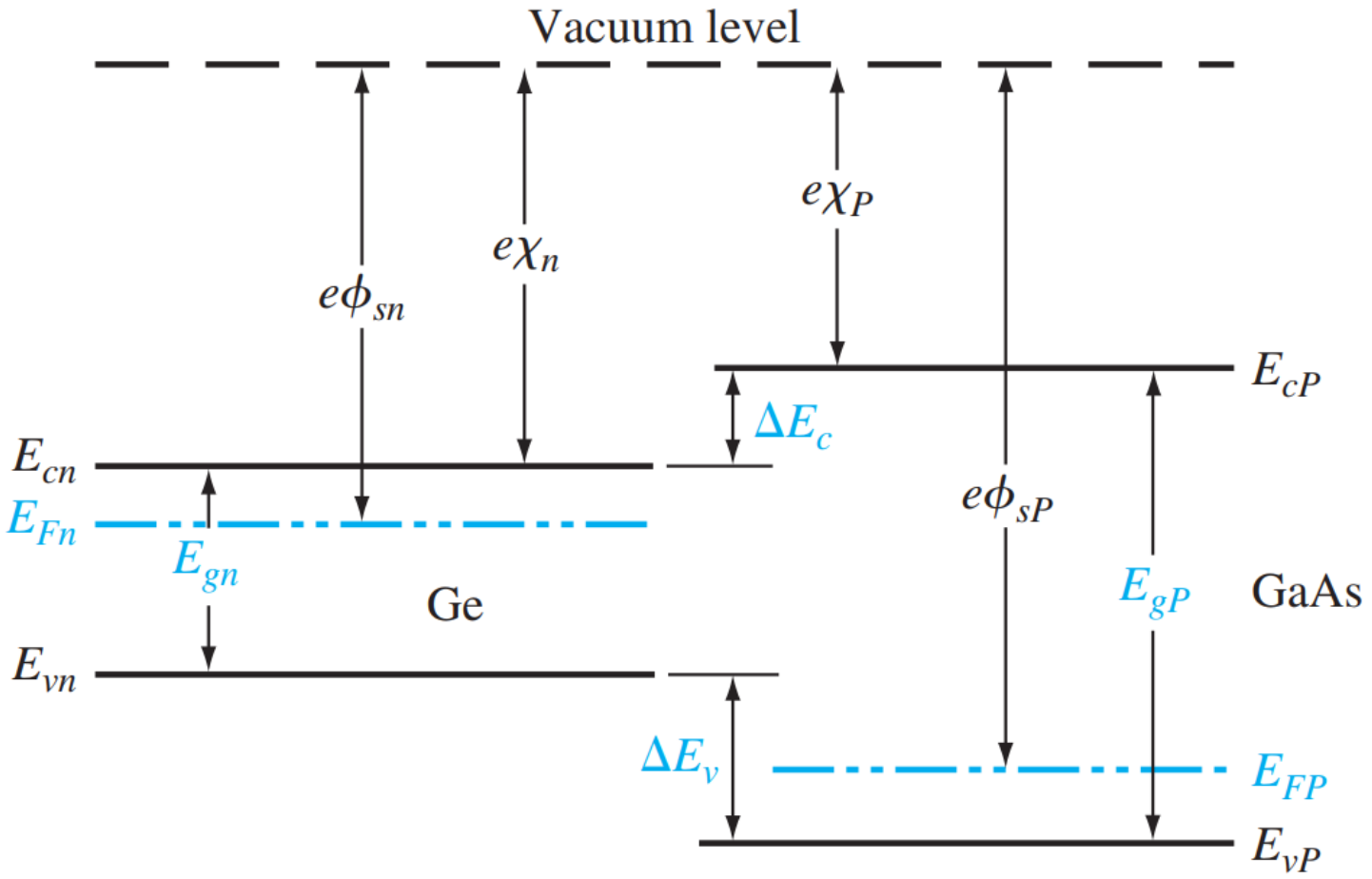
Staggered

Broken gap



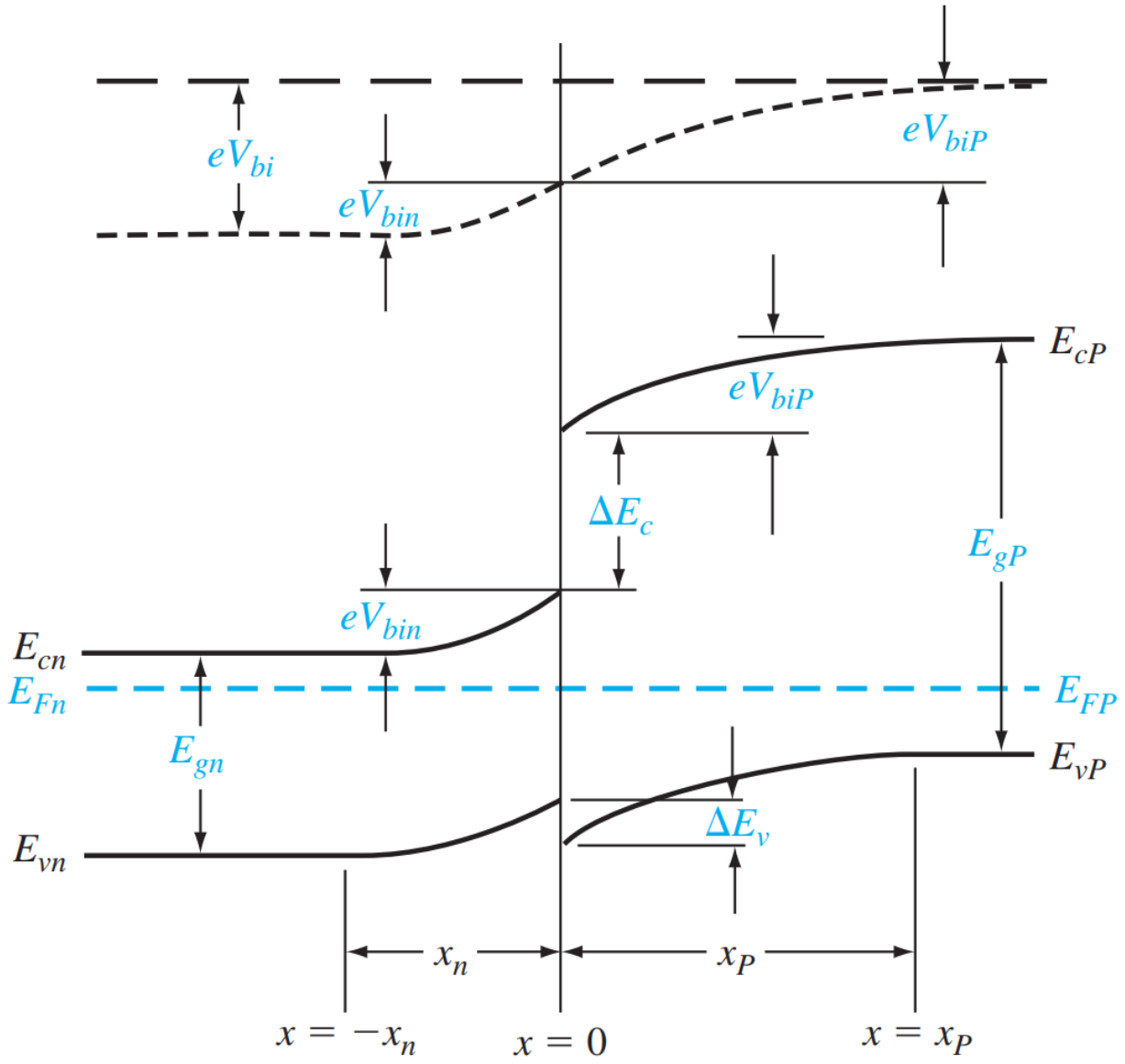
nP – Straddling (未接觸)

nP：大寫P表示能帶間隙比較大

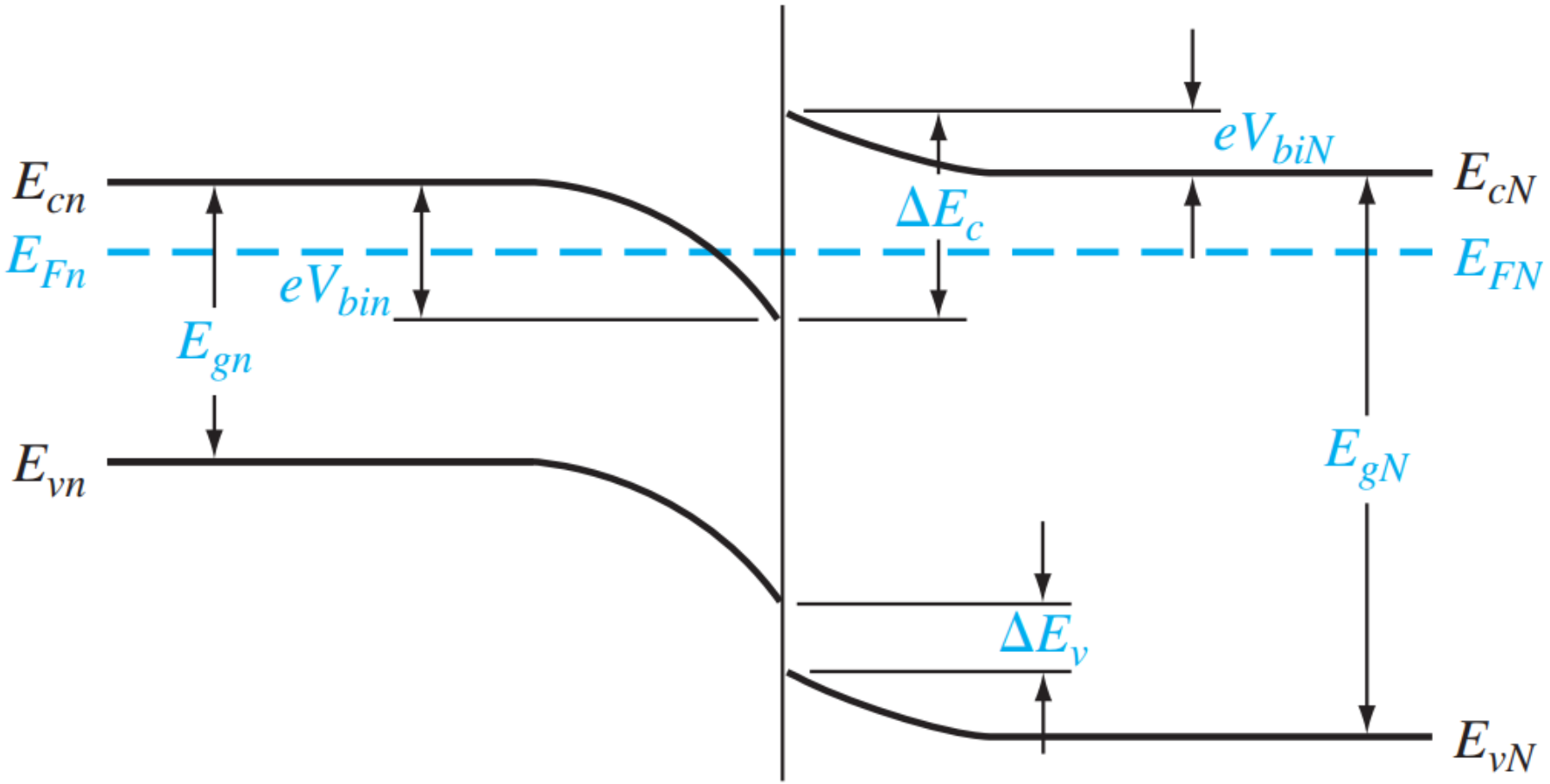


$\Delta E_C = e(\chi_n - \chi_P)$, and $\Delta E_C + \Delta E_v = E_{gP} - E_{gn} = \Delta E_g$

nP – Straddling (接觸)

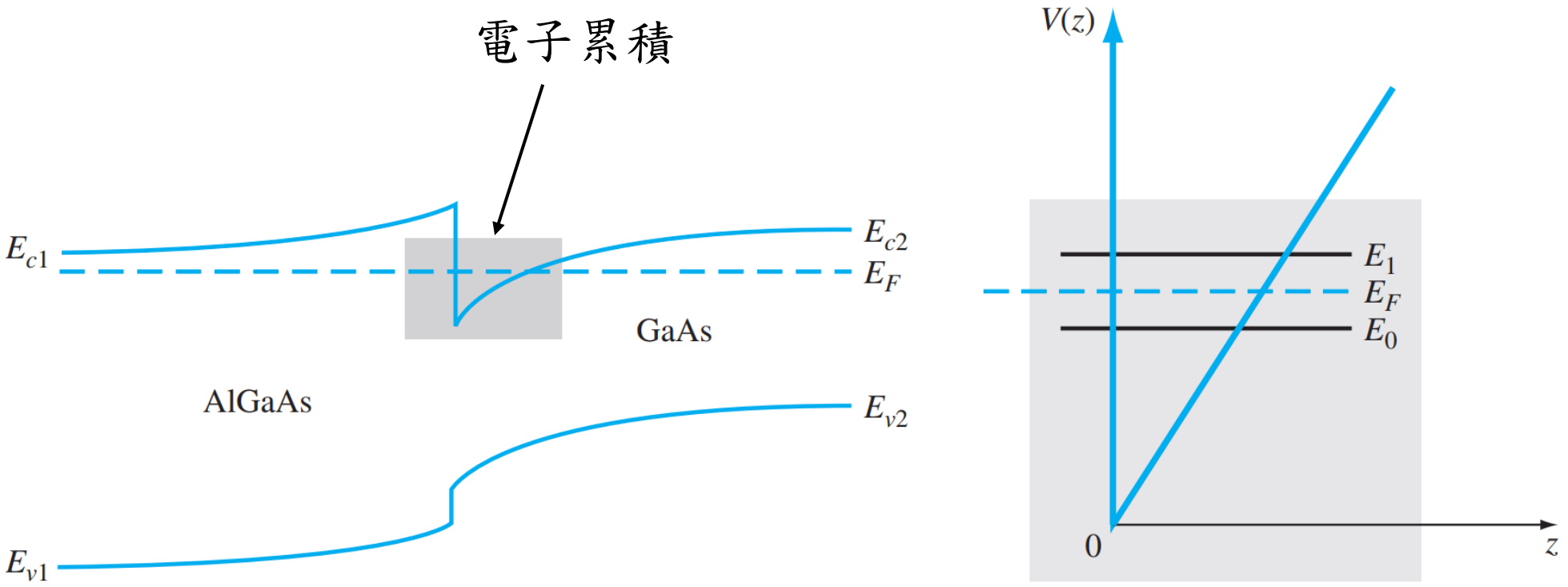


nN – Straddling (接觸)

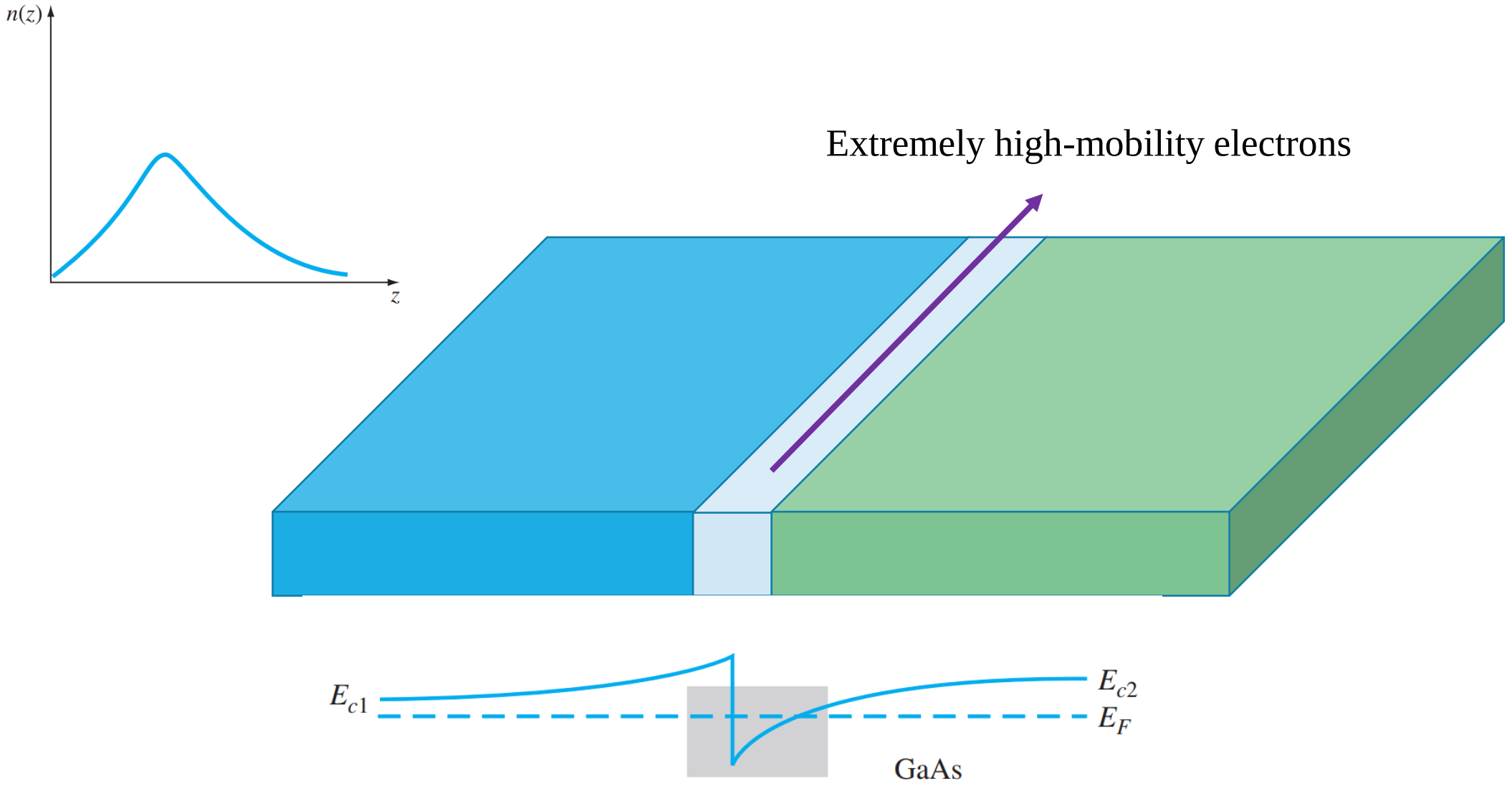


Two-Dimensional Electron Gas

2DEG：指電子因受到位能限制導致在空間中能量被量子化



Two-Dimensional Electron Gas



HEMT

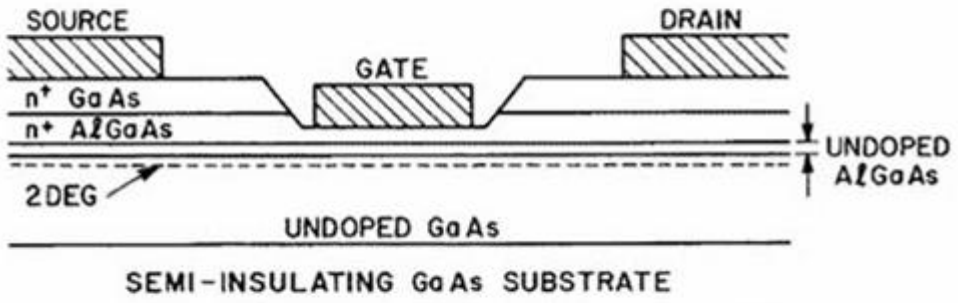


Fig. 1 Schematic of a conventional recess-gate HFET.