Tony James

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Summary

- Worked on Deep Learning and Machine Learning
  - Completed External Internship at MLBLR
    - Project - Improving the accuracy of YOLO using knowledge graphs
  - Trained Resent-50 on tiny Imagenet
  - Develepoed and Trained a CNN network for Facial Expression Recognition (FER 2013 data set)
    - used ensembling to further improve the accuracy 70.35%
    - made a tutorial on the same
- Excellent expertise on optimization for RISC/SIMD/VLIW architecture
  - ARM 9T/9E/11, Cortex A8/A9/A5/M3
  - ARM/NEON using intrinsics (reducing development time by half)
  - x86 using SSSE 3/SSE 4.1 (fixed and floating point)
  - TI TM320c64x **(c64x)**
  - Silicon Hive Architecture **(SIMD-VLIW)**
  - BCM89107 SOC with Pixel-Processor
- Audio/Speech/Video codec optimization
  - MP3, AAC/AAC+/eAAC+, WMA std/pro/loss-less, FLAC , MIDI,
  - AMR-NB, G729 AB, ILBC, WMA Voice, G719, EVS
  - HEVC
- Image-processing algorithms development and optimization and porting
  - Face Detection
  - Color conversion, Alpha-blending, Scaling
- **Float to fixed** point conversion of Audio/Speech codecs
- Overall 10+ years of experience on Optimisation

Technical Skills

- **Programming Languages**
  - C, C++, Python
  - ARM/NEON assembly for 9T/9E/11, Cortex A8/A9/A5/M3
  - x86 assembly using SSSE3/SSE4.1/AVX
  - intrincsics and assembly for BCM89107 SOC with Pixel-Processor
- **Processor Architectures**
  - ARM 9T/9E/11, Cortex A8/A9/A5,
  - x86
  - Silicon Hive
  - TI TM320c64x
  - BCM89107 SOC with Pixel-Processor
- **Tools Familiarity**

- Programming: RVDS, Visual Studio, Intel Parallel Studio, MATLAB, Code Composer Studio, Eclipse based IDEs
- Project Management: Git, IBM RTC, JIRA

Experience

Technical Architect
Continental Automotive India Bangalore, India, Dec 2017 - Present

- Optimising Traffic Sign Recognition systems on TI TDA2x/EVE platforms
- Porting and Optimising Pedestrian Detection on BCM89107 SOC with Pixel-Processor
- Porting and Optimising Single Camera Calibration on BCM89107 SOC with Pixel-Processor

Technical Leader
Aricent/Smartplay Technologies Bangalore, India, Sep 2011 - Dec 2017

- Worked as a **contract engineer** with the following firms

  Intel Mobile Communications Mar 2015 - May 2016, Oct 2016 - Dec 2017
  - HSDPA functionaliy devlopment for Sub-Component Verification
  - Optimization of EVS codec on ARM/NEON
  - Optimization of **floating point** EVS codec on x86 using SSE4.1

  NXP Semiconductorss Jun 2016 - Jul 2016
  - Developing Host APIS for NXP's Car Audio Radio board (Dirana)

  Intel(PEG/ICG) Apr 2013 - Dec 2014
  - Firmware development and optimization on multi-core VLIW-SIMD Silicon Hive architectures
  - Camera Image Processing pipeline development
  - Secure Image composition APIs development and optimization

  Samsung India Software Operations(FRG) Mar 2012 - Oct 2012
  - Optimized AAC, **HEVC** and **Face Detection** algorithm on ARM/NEON/x86

Technical Leader
Aricent/Emuzed Bangalore, India Jun 2005 - Sep 2011

- Optimized and ported several Audio/Speech codecs on ARM/NEON architecture
- Developed a method for **faster code optimization** using NEON intrinsics, this approach reduces development time by half while maintaining performance gains close to theoretical best
- **Float to fixed** point conversion of Audio/Speech codecs
- Providing customer support for CRs and Bug fixes for various Speech/Audio components

- Lead teams of small sizes(2-4)
- Sr Software Engineer Aug 2007 - May 2010
- DSP Engineer Jun 2005 - Jul 2007

Papers Published/Selected

- **An Efficient Huffman Decoding Method Using Concurrent Execution in ARM Cortex-A8** (ICCE 2011)
  - A novel method for efficient decoding of escape coded Huffman Code Words on Cortex-A8 using concurrent execution in ARM core and NEON co-processor is presented. Considerable performance improvement is obtainable using this technique.
- **Efficient Implementation of HEVC Decoder on Low Power x86 Processors** (published in **Smartplay** Internal Magazine)
  - HEVC/H.265 improves compression efficiency at the cost of extra computational complexity. But most of the mobile hand held devices still employ low power processors. This paper suggests a fast implementation of HEVC decoder for low power x86(using SSSE3 instruction set) processors. Experimental results show that HD (1920x1080p) content can be smoothly decoded (using HM 11 decoder) on Intel Atom N550 (Dual Core) processor.

Events Participated

- **Hack100-II**, A 24-hour Hackathon at Aricent, 11-12 March 2016
  - Developed a prototype of an **Intruder Alarm Device**, Our application runs on a **Raspberry-Pi2** board and uses **Open-CV** library functions, Whenever motion is detected another thread running on the **Raspberry-Pi2** sends a message to an **AWS IoT** Server, This **IoT** server alerts the concerned parties, The whole setup is controlled(like resetting alarm,switching off) via another remote server running **Node.js** as backend.
- **ICCE 2011**, IEEE International Conference on Consumer Electronics, 9-12 Jan 2011
  - Presented **An Efficient Huffman Decoding Method Using Concurrent Execution in ARM Cortex-A8**

Education

- **M-Tech** in Communication Systems, IIT Madras, 2003 - 2005
  - Project - Pre-processing and Post-Processing techniques for H.263 based video codec
- **B-Tech** in Electronics and Communication, Kerala University, 1998 - 2002

Project Profile in Detail (only Major Projects)

- **Continental Automotive India**
  1. Optimising Traffic Sign Recognition systems on TI TDA2x/EVE platforms
  2. Porting and Optimising Pedestrian Detection on BCM89107 SOC with Pixel-Processor

3. Porting and Optimising Single Camera Calibration on BCM89107 SOC with Pixel-Processor

- **Aricent | Smartplay**
  1. EVS codec optimization for ARM/Cortex-A5 (Client: Intel)
  2. Optimization of **floating point** EVS codec on x86 using SSE4.1 (Client: Intel)
  3. Camera Sub-Systems (**CSS**) firmware development for upcoming Intel's platforms (Client: Intel)
     - **CSS** Firmware APIs help applications to control the camera subsystem. **CSS** consists of an algorithmically superior Camera Image Processing pipeline implemented on a powerful Silicon Hive Processor. The proposed Silicon Hive Processor was a multi-core, SIMD-VLIW architecture designed for Image Signal Processing.
     - **CSS** firmware was developed on Silicon Hive architecture
     - Extensive testing and debugging (using **GDB**) of the Image Processing pipeline was performed to ensure resolve quality issues
  4. Secure Image composition APIs development and optimization on **Silicon Hive** (Client: Intel)
     - To develop a Secure Image composition module to be used with Wireless Display(Wi-Di) component of upcoming Intel's platforms. The composition module consists of alpha blending, bi-cubic interpolation and color space conversion algorithms.
     - Developed and ported on Silicon Hive architecture
     - Optimized to meet the real time performance requirements(60 fps)
  5. AAC Encoder optimization on Cortex-A9 (Client: Samsung)
  6. Face Detection algorithm (for Camera) optimization on Cortex-A9 (Client: Samsung)
     - The proposed technique is a variant of Adaboost with Viola-Jones. LBP is used to identify the weak classifiers based on LBP histogram. A cascade of weak classifiers is used, which achieves increased detection performance while obviously reducing computation amount. Simpler classifiers are used to reject the majority of sub-windows before more complex classifiers are used to achieve low false alarm rates.
     - The algorithm was optimized on Cortex A9
  7. **HEVC** Optimization on x86 (Client: Samsung)

- **Aricent | Emuzed**
  1. AAC-LTP tool development for AAC encoder
  2. AMR-NB Encoder/Decoder optimization on Cortex-A8
  3. G719 Encoder/Decoder optimization on Cortex-A8
  4. WMA Voice Decoder Optimization on Cortex-A8
  5. G729 AB Encoder/decoder optimization on Cortex-A8
  6. Memory (Data size and RAM usage) and performance optimization of AAC and MP3 decoders on Cortex-M3

- The challenge was to optimize Data size and RAM usage without affecting the performance, at the same time reduce performance requirement to the minimum so the customer can support the solution on a low power,low memory chip.
- Optimized Huffman tables to reduce Data size, Re-used data buffers to reduce RAM usage, Limited accurate implementation for faster performance

7. FLAC Optimization on ARM 9E
8. WMA Std/Pro decoder Optimization on ARM 9E
9. iLBC Encoder/Decoder **float to fixed point** conversion
   - The objective was to develop a high quality, performance efficient fixed point equivalent of iLBC floating point reference code. A minimum PESQ score of 4.0 and above was set to ensure the quality of the fixed point implementation.
   - The fixed point implementation achieved PESQ scores of 4.2 and above in all test cases.
   - One of Aricent's Mobile OEM customer affirmed that Aricent's Fixed Point iLBC implementation on ARM9E was one of the fastest and high quality implementation available in the market
10. G729 AB Encoder/decoder optimization on ARM 9T/9E
11. **MIDI** - Customer Support and Bug Fixes
12. GSM AMR-NB Optimization on c64x

Personal Profile

Citizenship	: India
Eligible to work in US	: **Yes, H1B petition approved in Apr 2014**
Notice Period	: 60 days