USB Charger for Mobile Devices Using Synchronous Buck Converter. EE4741 Power Electronics (Dec. 2020)

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***Abstract*— This report presents a DC-DC converter capable of maintaining a stable output voltage to be used in a USB charging system for mobile. A synchronous buck converter was chosen as numerous mobile electronics require voltage to be stepped down to 3.3 volts to charge or function. In the end, the project met all of the required specifications. The closed loop system is able to maintain a stable output voltage within 50 mV of the desired 3.3 V when the input voltage varies by ±20%. The converter also has an inductor ripple ratio of 0.98. The peak-peak voltage ripple is 0.75% of the desired output which satisfies the requirement of 5%. Finally, the overall system was found to have an efficiency of 85%.**

I. Introduction

In this report, we detail the design of a synchronous buck converter with the capability of maintaining a stable 3.3-volt output voltage with input voltage of 5 volts. The converter has a switching frequency of 2 *Mhz*. The main requirements are to maintain an average output voltage within 50 mV of the desired output voltage of 3.3 volts. The peak-peak output voltage needs to have a ripple less than 5% of 3.3 volts. The converter also needs to maintain the voltage constant when the input voltage varies by 20%. The converter's output is fed to a proportion-integral controller to regulate the output voltage. The IRF7468 and IRF 74565 MOSFETS of the buck converter are driven using the LTC4442 N-Channel MOSFET gate driver and the controller and pulse-width-modulation generator both use the LT1230 Op-Amp. The details of the general circuit can be found in section II and the LTSpice simulation results of the practical design can be found in section III.

II. Circuit Details

The duty ratio was found using the following equation.

$$D = \left(\frac{V_{out}}{V_{in}}\right)$$

The first step in designing the converter was to determine the values of the inductor L_1 and capacitor C_1. Following the requirements of the converter, we can use the equation for inductor ripple ratio to determine the average current through the inductor and then find the suitable value for the inductor.

$$\mathfrak{R}_L = \left(\frac{\Delta i_L}{I_L}\right)$$

$$L = \left(\frac{V_{in} - V_{out}}{\Delta i_L f_s} D\right)$$

We repeat a similar procedure to find the suitable value for the capacitor using the following equation.

$$C = \left(\frac{\Delta i_L}{8 f_s \Delta V_o}\right)$$

A. Small-Signal Analysis

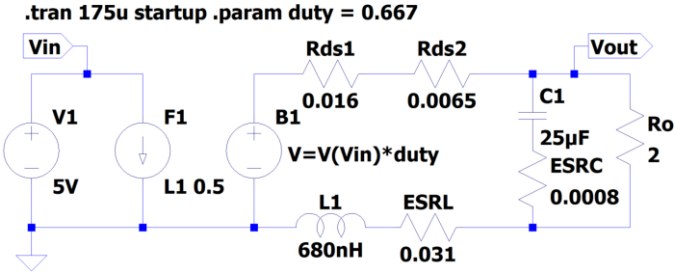

Figure 1. Small-signal average circuit model of synchronous buck converter.

The values found through calculations here provide a starting point for the design of the circuit but do not necessarily correspond to the final value of components used in the circuit. This is due to components not being ideal and each component was tuned further to meet the requirements.

In order to find the transfer function of the buck converter, we first found the small signal average model through perturbing and linearizing the estimated output around a DC operating point. The small signal average model can be found in Fig 1. The control-to-output transfer function can be found by setting the small signal input and output current to be zero, giving us the following expressions.

$$V_x = V_{in} - R_{ds1} * i_L + R_{ds2} * i_L$$
$$R_x = R_{ds1} * D - R_{ds2} * (1 - D) + ESR_L$$
$$H_d(s) = \frac{V_x R_o (1 + sESR_C)}{R_o + R_x + (ESR_c C + L + (R_o + ESR_c) C R_x) s + s^2 (R_0 + ESR_C LC)}$$

We define the sensor gain to be the output of the converter divided by the reference voltage.

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$$G_s = \frac{V_{out}}{V_{ref}}$$

Combining all of theses we can find the open loop transfer function of the converter with no feedback controller as the following.

$$G_{OL}(s) = H_d(s) * G_s * \left(\frac{1}{V_{PWM}}\right)$$

B. *Controller Design*

After obtaining the transfer function of the open loop system, we used MATLAB to generate the bode plot to find the gain and phase margin of the system found in Fig. 2.

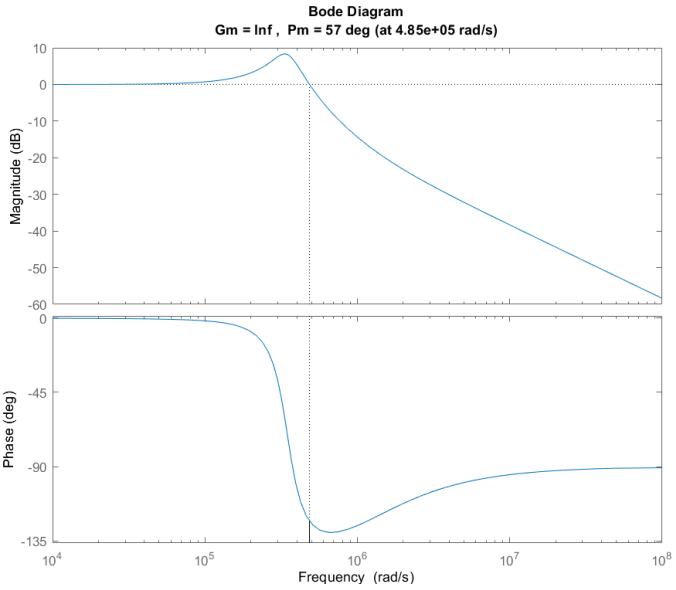

Figure 2. Bode plot of the open loop system.

From Fig 2, we can see that the open loop system is stable with a phase margin of 57°. Since the open loop system is stable without feedback, a proportional-integral (*PI*) controller was chosen primarily to reduce oscillations found when simulating the open loop converter. For the location of the zero ω_z, it was chosen to be one-tenth of the frequency of the crossover frequency to reduce minimizing the phase margin. The controller's k_{pi} factor was set to be unity as the overall system has a relatively short settling time and further gain may cause system to oscillate. The transfer function has the following form and its bode plot can be found in Fig 3.

$$K_{PI}(s) = k_{pi}\left(1 + \frac{\omega_z}{s}\right)$$

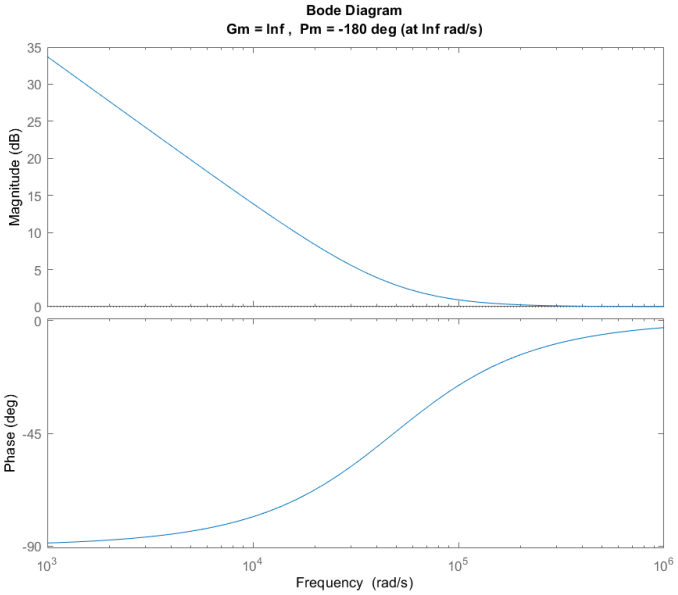

Figure 3. Bode plot of proportional-integral controller.

Using the transfer function of the *PI* controller, we can find the optimal component values to implement the controller in the circuit. We set the R_{2s} to be 100 Ω and use the following equation to find the value C_{2s} to be 0.22 μF.

$$\omega_z = \frac{1}{R_{2s}C_{2s}}$$

Since we chose the controller to have a k_{pi} factor of 1, this results in R_{1p} = R_{2s}. The fully implemented controller can be found in Fig 5.

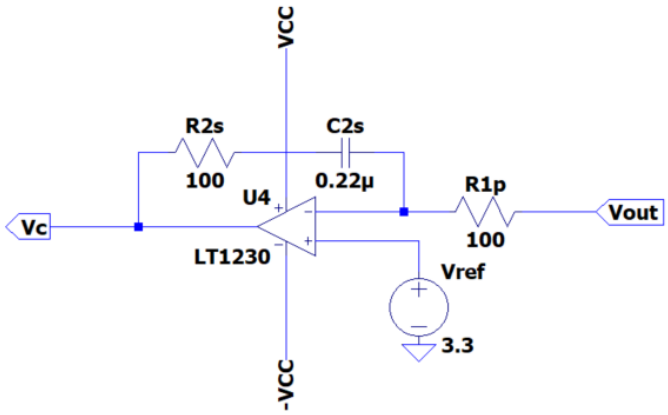

Figure 4. Schematic of *PI* controller.

C. *Pulse-Width-Modulation Generator*

To allow the entire system to respond to disturbances such as variations in input voltage or changes in load, we feed the voltage produced by the *PI* controller (V_C) to the non-verting terminal of another Op-Amp. The inverting terminal of the Op-Amp is fed a sawtooth signal creating a comparator that outputs a high or low signal depending on if the controller voltage is greater than or less than the sawtooth signal. The optimal ramp voltage of the sawtooth signal is determined by finding when the error voltage is zero and then assigning the ramp voltage

accordingly to the desired duty ratio. The duty ratio of the PWM signal can be found using

$$D_{PWM} = \frac{V_C}{V_{ramp}}$$

D. *Closed Loop System*

After obtaining the *PI* feedback controller, we can connect all of the parts together to produce the entire closed loop system found in Fig 5. The transfer function of the closed loop system can be found by multiplying the transfer function of each part in the system. The bode plot of the closed loop system can be found in Fig 6.

$$L(s) = H_d(s) * G(s) * \left(\frac{1}{V_{ramp}}\right) * K_{PI}(s)$$

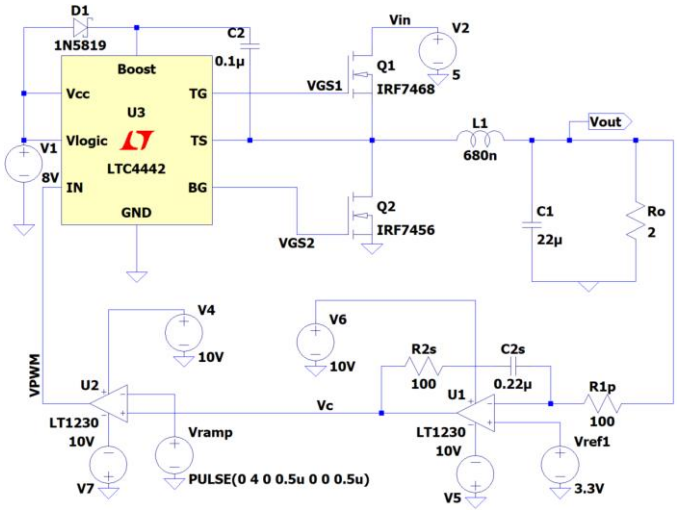

Figure 5. Schematic of complete system.

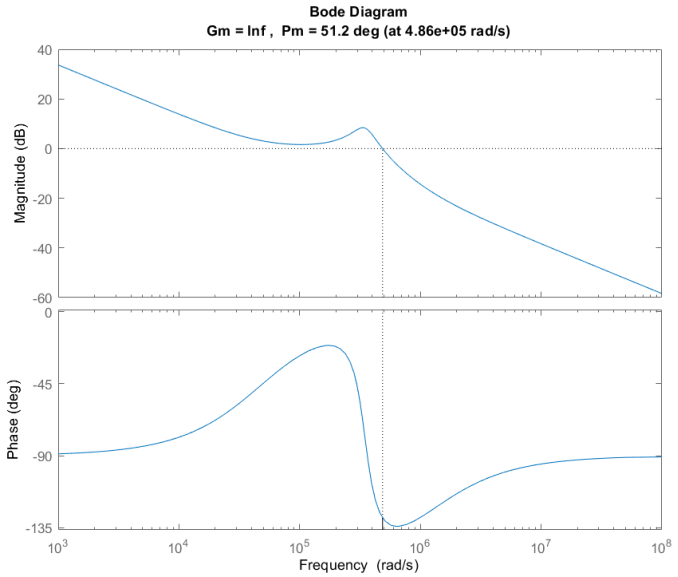

Figure 6. Bode plot of closed loop system.

Below is a list of the components used to implement the system.

Component	Part Number	Resistance (Ω)
Gate Driver	LTC4442	
Diode	1N5819	
MOS1	IRF7468	Rds1 = 0.016
MOS2	IRF7456	Rds2 = 0.0065
OP-Amp1/2	LT1230	
L1	1225AS-H-R68N	ESRL = 0.031
C1	C3225X5ROJ226M	ESRC = 0.0008
C2	GRM011E60G103KE01	
C2s	C2225C224KCRAC	
Ro	SR733ATTE2R00F	
R1p/R2s	3540100RFT	

Table 1. Bill of Materials.

III. Simulation Results

A. *Simulation Results of Converter with Real Components*

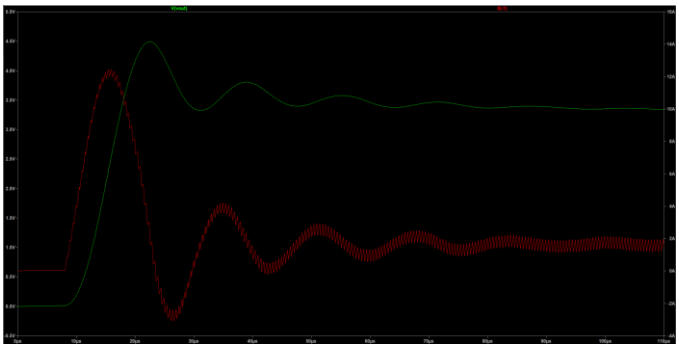

Figure 7. Startup transient of system.

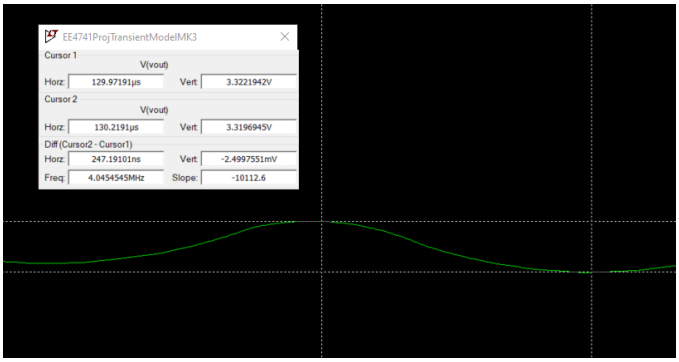

Figure 8. Simulation of output voltage ripple for 5*V* input and 100% load. The voltage ripple has a value of 2.49*mV* which is around 0.75% of the ideal output voltage and is within 50 *mV* of 3.3 *V* constraint.

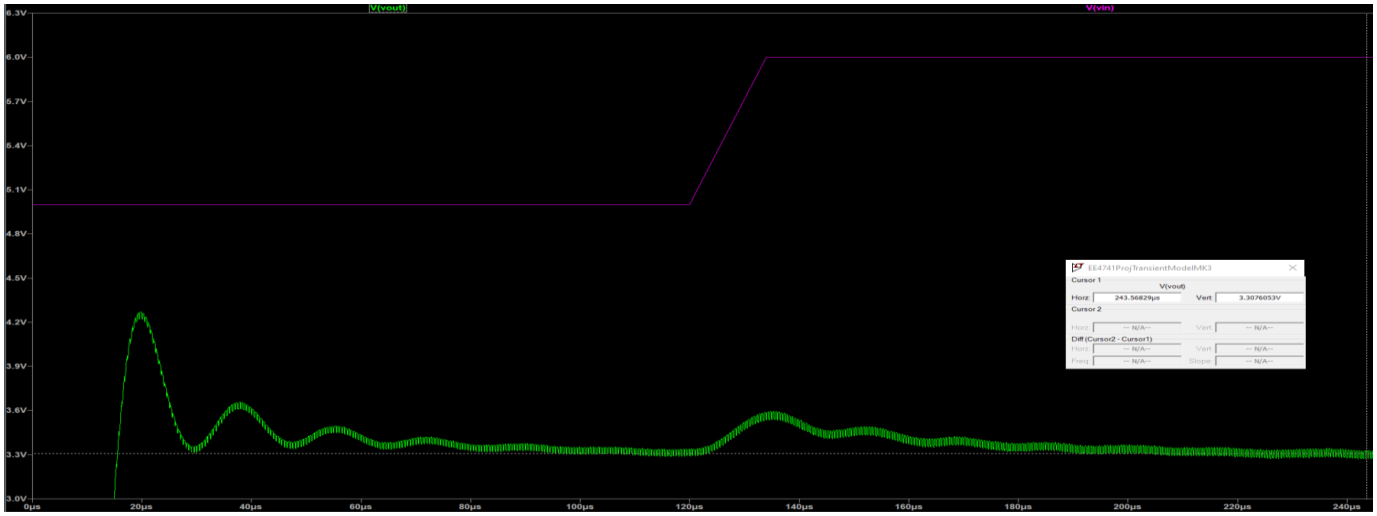

Figure 9. Simulation when input voltage varies by +20% and voltage settles at the desired output of 3.3 *volts.*

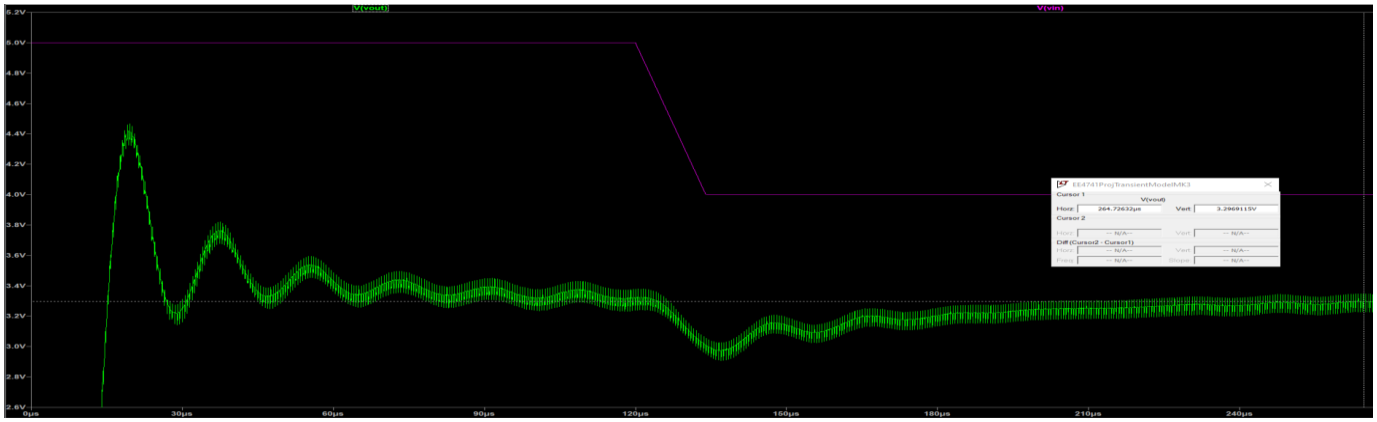

Figure 10. Simulation result for when input voltage varies by -20% and output voltage settles close to the desired output at 3.297 *volts.*

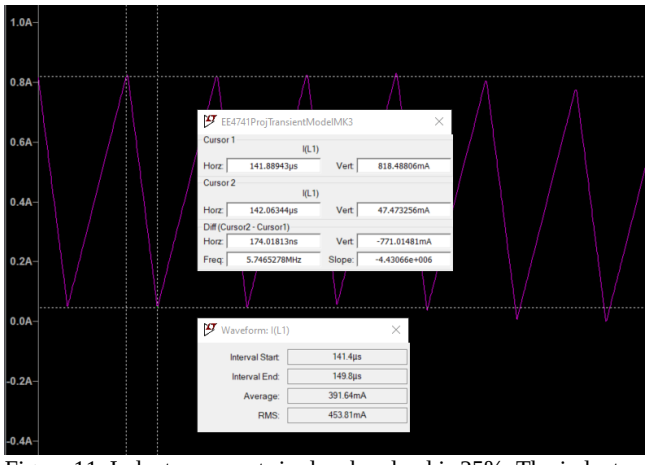

Figure 11. Inductor current ripple when load is 25%. The inductor current ripple ratio is around 0.98.

The inductor current ripple is 0.98 instead of 1 due to the components used not being ideal and there are no inductors that can be found to have the calculated ideal value so an inductor with close to the calculated value was used as a substitute.

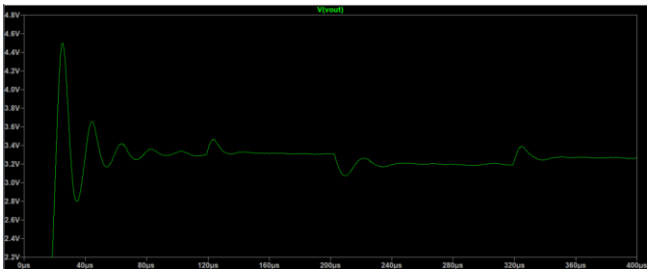

Figure 12. The transient response of system when load changes between 100% and 50%.

The output seems to be slightly below the optimal output voltage when the load switches from 50% to 100% at around 240 μs. One possible method to fix this may be to tune the k_{pi} factor so that the controller is able to detect a finer error signal in order to rectify the error.

B. Simulation Results of Averaged Model

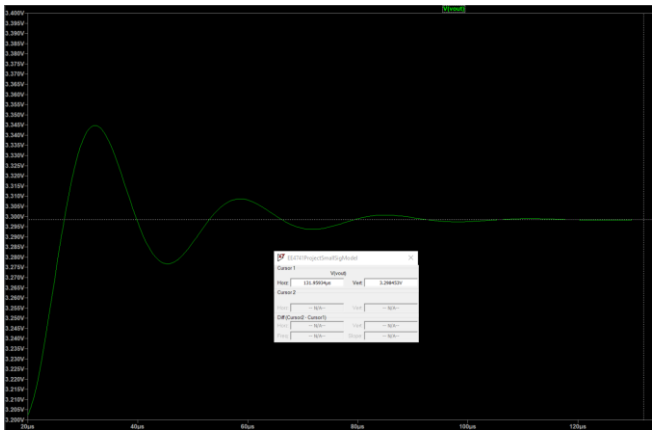

Figure 13. Simulation startup transient of averaged model with 5*V* input and 100% load.

Comparing the actual model with the averaged model, there does not seem to a large disparity between their results. Although the averaged model settles at 3.297 *V* while the actual model settles at around 3.305 *V*.

C. Circuit Losses and Efficiency

The power dissipation of certain components was found in LTSpice and their average power dissipated values can be found in Table 2.

Component	**Power Dissipated**
MOS1	370.16 mW
MOS2	347.4 mW
Op-Amp 1	96.085 mW
Op-Amp 2	178.96 mW
L1	211.87 mW
C1	437.42 mW
C2s	84.703 uW

Table 2. Average power dissipated of components.

The efficiency of the converter can be found by dividing the output power by the input power. The output power of the converter can be found by dividing the square of the output voltage by the resistance in this case which is 2 **Ω** giving us 5.445 *W*. Using LTSpice, we can find that the input power is 6.3929 *W* resulting in an overall efficiency of 85%.

IV. Conclusion

This report presents a DC-DC converter using a synchronous buck converter intended to be used for charging mobile devices. The converter has an input voltage of 5 *V* and an output of 3.*3V* A proportional-integral controller was used to remove oscillations and provide feedback to the converter. The design of the converter was validated using simulations in LTSpice.

This project provided me with a much deeper understanding of how a buck converter functions as well as the function of each component that make up the converter. I also had a chance to practice designing a controller based on the information provided by the bode plot of the open loop system. I also learned how to use an Op-Amp with a sawtooth signal to produce a PWM as well as theory behind choosing an optimal ramp voltage for the sawtooth signal.

References

[1] *Goel, Rachit et al. "A smart-USB-cable buck converter with indirect control." Presented at 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL) Stanford, CA, USA, 2017*