

Q1

(a)

$$e^{q\Phi_n/(kT)} = 10^{19-(10-(10-17))} = 10^{16}$$

$$\Phi_i = 16 \ln(10) \frac{kT}{q} = 0.9533 \text{ V}$$

$$x_d = \left[\frac{2\epsilon_{Si}}{q} \Phi_i (1/N_a + 1/N_d) \right]^{0.5} = 0.1116 \text{ } \mu m$$

$$x_p = \frac{N_d}{N_a + N_d} = 0.1105 \text{ } \mu m$$

$$x_n = \frac{N_a}{N_a + N_d} = 0.0011 \text{ } \mu m$$

$$E_{max} = \frac{-qN_ax_p}{\epsilon_{Si}} = -1.715 \times 10^5 \text{ V/cm}$$

(b) When $V_a = 1 \text{ V}$

$$C_j = \frac{A\epsilon_{Si}}{x_d} \frac{1}{\sqrt{1 + \frac{V_a}{\Phi_i}}} = 3.241 \times 10^{-12} \text{ F}$$

When $V_a = 10 \text{ V}$

$$C_j = \frac{A\epsilon_{Si}}{x_d} \frac{1}{\sqrt{1 + \frac{V_a}{\Phi_i}}} = 1.369 \times 10^{-12} \text{ F}$$

The capacitance decrease when the reverse bias increases. $C_j \propto \sqrt{V_a}$ changed little when they change.

(c)

$$\mu_p = 150 \text{ cm}^2/(\text{Vs}) \quad D_p = \frac{kT}{q} \mu_p = 3.881 \text{ cm}^2/\text{s}$$

$$\mu_n = 750 \text{ cm}^2/(\text{Vs}) \quad D_p = \frac{kT}{q} \mu_p = 19.401 \text{ cm}^2/\text{s}$$

$$L_p = 3.5 \text{ } \mu m \quad L_n = 75 \text{ } \mu m$$

$$I_p = qAn_i^2 \left(\frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a} \right) (e^{\frac{-qV_a}{kT}} - 1) = 1.3134 \text{ A}$$

Q2

(a)

$$I_D = I_S(e^{\frac{q(V_{in} - V_{out})}{kT}} - 1)$$

When $V_{in} - V_{out} \rightarrow 0$, *i.e.* $\frac{q(V_{in} - V_{out})}{kT} \rightarrow 0$, we have

$$e^{\frac{q(V_{in} - V_{out})}{kT}} \rightarrow 1 + \frac{q(V_{in} - V_{out})}{kT}$$

so $I_D \rightarrow I_S \times \frac{q(V_{in} - V_{out})}{kT}$ when $V_{in} - V_{out} \rightarrow 0$, *i.e.* their relationship is Linear.

Code:

```
Voltage Divider - DC
.model Dbreak D Is=1e-16 Rs=0 N=1 TT=0 Cjo=0pF
.DC vin -2 2 0.01
vin 1 0
d1 1 2 Dbreak
r1 2 0 1.0k
.end
```

Graph:

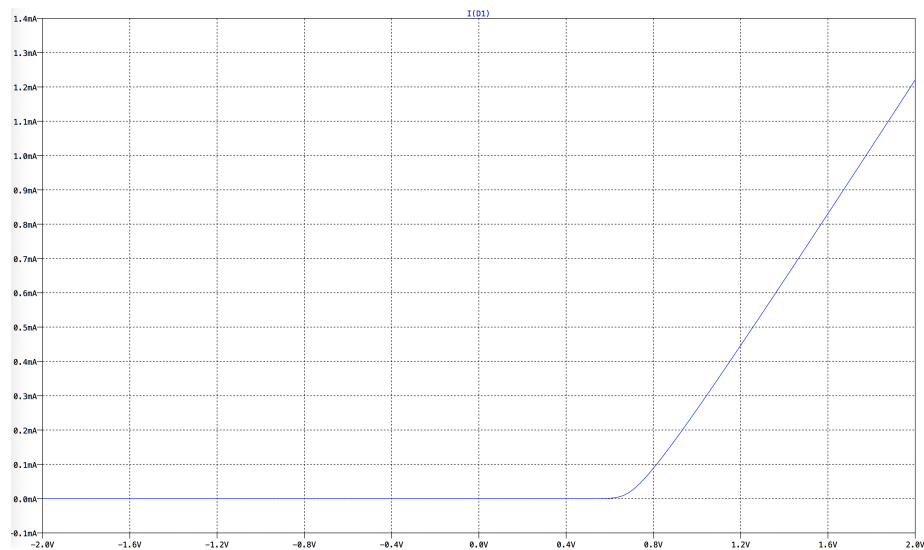


Figure 1: 2_b

- (b) According to property of diode, $V_{out} \geq 0$. And we have $V_{out} + V_D = V_{in}$. In the first half period, when V_{in} is small, V_D is much larger than V_{out} , so there is a "delay" of increase. When V_{in} is large enough, V_{in} and V_{out} behave similarly. In the second half period, $V_{in} < 0$ but $V_{out} \geq 0$, so $V_{out} = 0$.

Code:

```
Voltage Divider - Sine
.model Dbreak D Is=1e-16 Rs=0 N=1 TT=0 Cjo=0pF
vin 1 0 sin (0.0V 2.0V 60) ac 1.0 dc 0.0
d1 1 2 Dbreak
r1 2 0 1.0k
.control
tran 0.1ms 30ms
plot v(1) v(2)
.end
```

Graph:

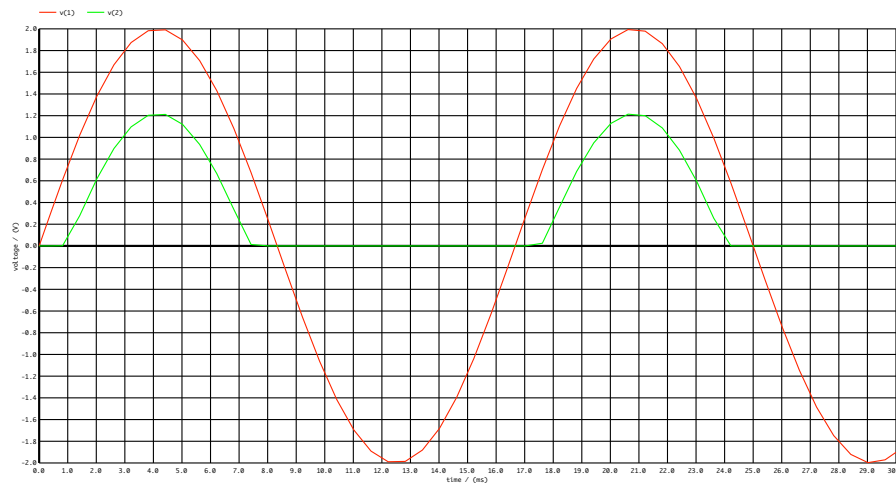


Figure 2: 2_b