To :

Data Sheet	
Product Name	**LPM026M648A**

Approval Signature

Approved by	Date		Date
			March.1, 2022

Tentative

Specifications are subject to change without notice.

Japan Display Inc.

1 CONTENTS

2 RECORD OF REVISIONS   Confidential

Date	Sheet No.	Summary
Oct. 26, 2020		Tentative
Nov.17.2020	7	Power Supply Voltage for LCD is revised
	8	Note (9) at color tone is omitted
	8	Respose time @25℃ is added
	11	Internal Pin connection is revised
	24	Dimentional outline (LCD) is revised
Sep. 17.2021	6	"(3) Ambient Temperatures vs. Allow able Forward Current" chart is updated
	8	Brightness is updated
	8	Color tone is updated
	18-23	Sequence is updated
	24	Dimentional outline (LCD) is revised
	26-29	Cosmetic spec is updated
Jan. 2022	8	Color tone is updated
	24	Dimentional outline (LCD) is revised
March 1. 2022	8	Color tone is updated

(1) Part Name   LPM026M648A

(2) Module Dimensions   50.51 (W) mm $\times$ 57.14 (H) mm $\times$ 1.78 (t) mm
(Excluding FPC and Protective Film)

(3) Active Area Dimensions   46.008 (W) mm $\times$ 46.008 (H) mm

(4) Pixel Pitch   0.0213 (W) mm $\times$ 0.0213 (H) mm   (1192ppi)

(5) Resolution   2160 $\times$ 3 (R,G,B) (W) $\times$ 2160 (H) dots

(6) Color Pixel Arrangement RGB Vertical Stripe

(7) Display Mode   Transmissive Type, Normally Black Mode, In-Plane Switching Mode

(8) Number of Colors   16,777,216 Colors

(9) Viewing Direction   Perpendicular to the display surface

(10) Backlight   Light Emitting Diode (LED), 18 LEDs (2in1) ; 3 series 6 strings

(11) Weight   TBD

(12) Power Supply Voltage   VSP = 5.7+/- 0.1V VSN=-5.7+/- 0.1V

(13) Interface I/O power supply   VDDI = 1.8V +/-0.1 V
        Note (1)   The same voltage as "H" level of a customer's interface signal
must be supplied to VDDI.

(14) IC   R63455 (Source and Power IC : Synaptics)

(15) Interface   MIPI-DSI C-Phy Video mode 1/2 DSC (4-Lane x 2-Port)
MIPI-DSI C-Phy Video mode 1/2 DSC (4-Lane x 1-Port)
MIPI-DSI C-Phy Video mode no compression (4-Lane x 2-Port)

(16) Methode of Inversion   Column Inversion

(17) Surface Treatment   HC (Hard coat)

Note (1) VDDI is the reference voltage for adjusting the I/O signal level of R63455
   VDDI voltage must be determined according to a customer's system.

50.51

13.4

A.A. 46.008

(2.25)

5.33

15

2.56"

2160 x 2160

4-C10.7352

A.A. 46.008

57.14

(5.8)

1pin

60pin
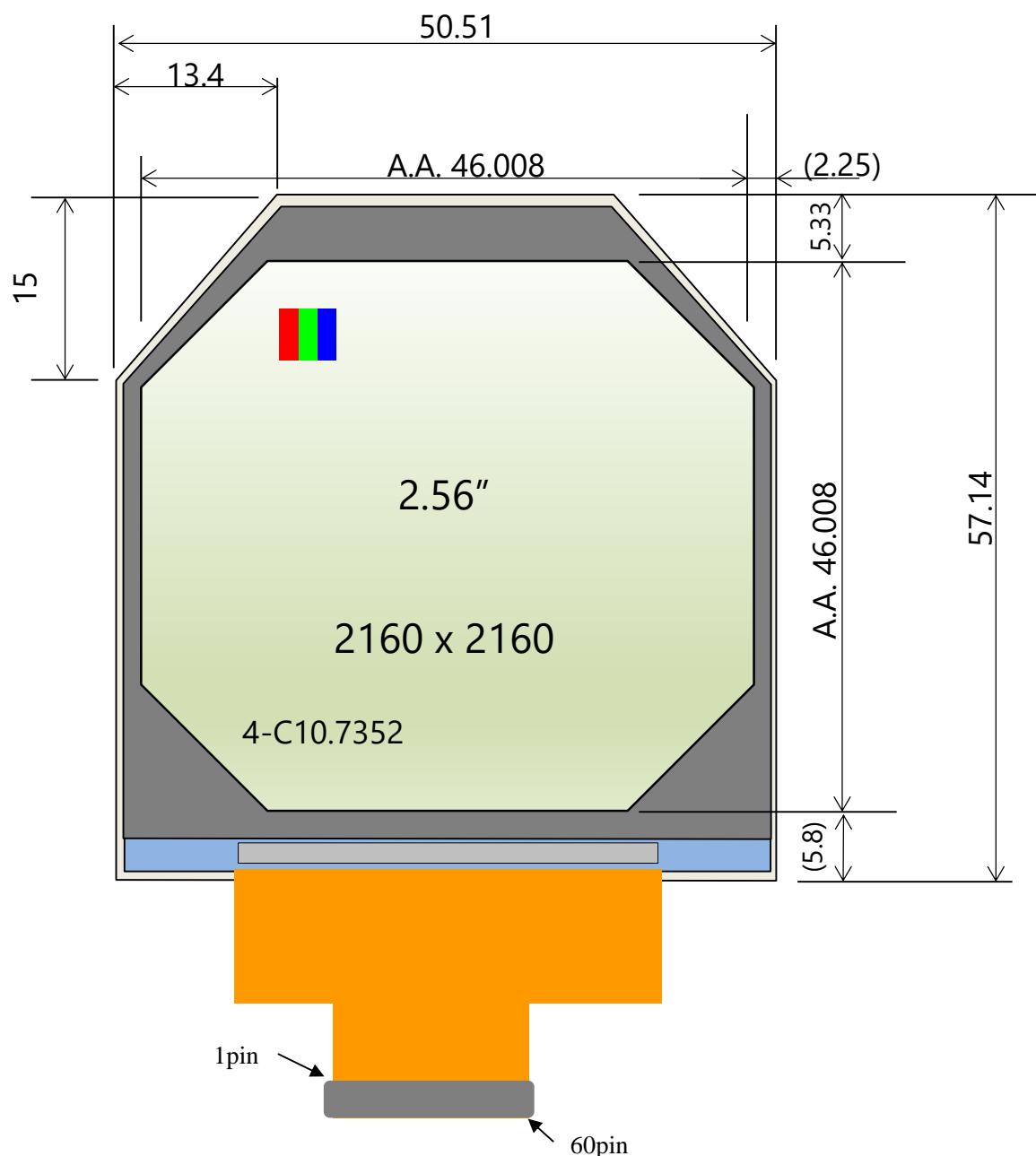
Figure not in scale

5. ABSOLUTE MAXIMUM RATINGS
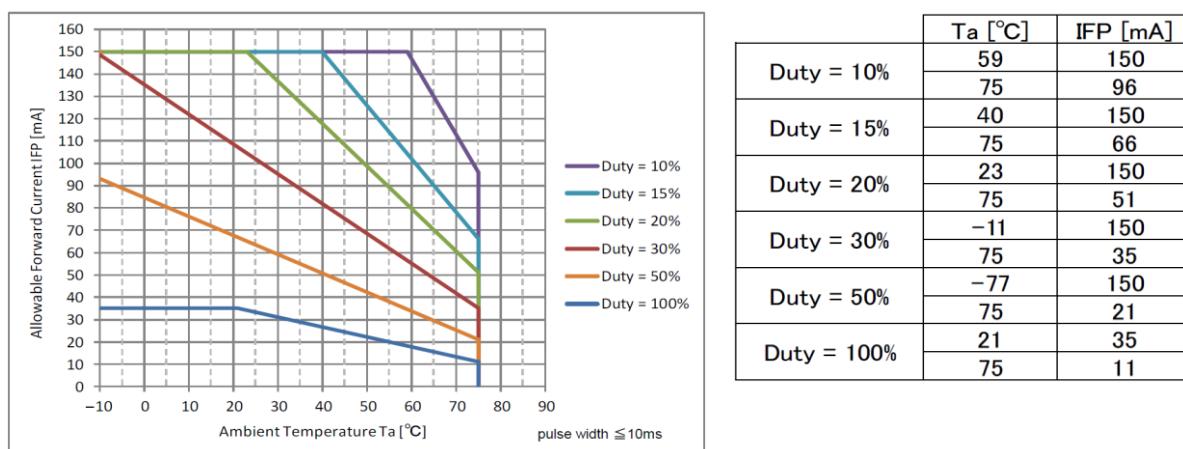
5.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS OF LCD

Ta=25°C

Item	Symbol	Min	Max	Unit	Note
Supply voltage	VSP	-0.3	6.5	V	(1)
Supply Voltage	VSN	-6.5	0.3	V	(2)
Logic Input voltage range	IOVCC	-0.3	2.3	V	(1)
MIPI line voltage range		-0.3	1.8	V	(1)
RESET voltage range		-0.3	IOVCC+0.3	V	(1)
LED Reverse Voltage	V_R	-	5	V	
LED Forward Current	I_{LED}	-	TBD	mA	per LED

Notes (1) Keep VSP, IOVCC, MIPI line and RESET Voltages no lower than GND.

(2) Keep VSN Voltages no Higher than GND.

(3) Ambient Temperatures vs. Allow able Forward Current.

	Ta [°C]	IFP [mA]
Duty = 10%	59	150
	75	96
Duty = 15%	40	150
	75	66
Duty = 20%	23	150
	75	51
Duty = 30%	−11	150
	75	35
Duty = 50%	−77	150
	75	21
Duty = 100%	21	35
	75	11
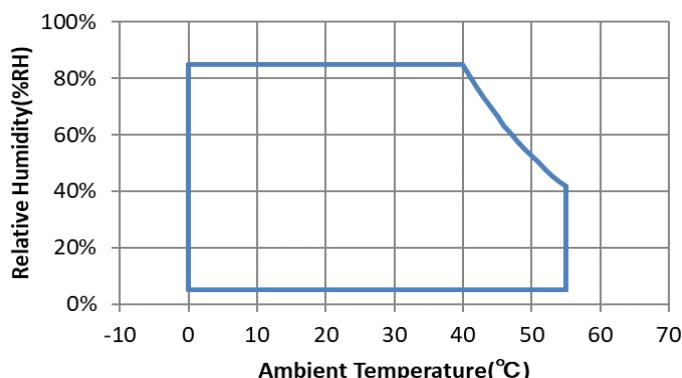
5.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS

Item	Operating		Non-Operating (Note4)		Remarks
	Min	Max	Min	Max	
Ambient Temperature	0°C	55°C (2)	-30°C	70°C (2)	Note (3)
Humidity	Note (1)		Note (1)		No condensation
Corrosive Gas	Not Acceptable		Not Acceptable		

Notes (1) Ta ≤ 40°C 85%RH max.

Ta > 40°C Absolute humidity must be lower than the humidity of 85%RH at 40°C.

(2) The temperature of LCD surface shall be equal
or less than 70℃.

(3) Background color slightly changes depending
on ambient temperature and viewing angle.
The temperature for operating in the table
above apply to operation only.
Visual qualities, such as brightness, color,
contrast ratio and response time,
to be evaluated at Ta=25°C Operating.

(4) This is not for storing condition. When storing LCM for long term, please follow the condition
mentioned in "12.5 STORAGE".

6. ELECTRICAL CHARACTERISTICS

LCD Module   Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Supply Voltage for LCD	VDDI	-	1.7	1.8	1.9	V	-
Power Supply Voltage for LCD	VSP	-	5.6	5.7	5.8	V	-
Power Supply Voltage for LCD	VSN	-	-5.8	-5.7	-5.6	V	-
Input Voltage for Logic Circuits	VIH		0.8×VDDI	-	VDDI	V	(1),(2)
	VIL		0	-	0.2×VDDI		
Output Voltage for Logic Circuits	VOH1	IOH=-0.1mA	0.8×VDDI	-	-	V	(1),(3)
	VOL1	IOL=0.1mA	-	-	0.2×VDDI		
Power Supply Current	I_VDDI	All White	-	-	TBD	mA	(4)
	I_VSP	All White	-	–	TBD	mA	(4)
	I_VSN	All White	TBD	-	-	mA	(4)
LED Forward Voltage	VLED	-	-	TBD	TBD	V	(5)
LED Forward Current	ILED	-	-	89(TBD)	-	mA	(5)(6)
LED Reverse Current	IR	-	-	-	TBD	μA	
Frame Frequency	fFLM	-	90	-	120	Hz	

Notes (1) VDDI = 1.7V to 1.9V

(2) Input : RESX

(3) Output : LEDPWM, TE

(4) VDDI=1.8V, VSP=5.7V, VSN=-5.7V, fFLM=120Hz

The current is time averaged value even for Maximum criteria.

(5) Each value is the characteristics of one LED. @If=89mA(TBD) Duty=10%

(6) The operating current of LED and the duty ratio should be determined within the maximum rating of the temperature environmental condition.

7. OPTICAL CHARACTERISTICS

Confidential

LCD (BACKLIGHT ON)

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Brightness		B	φ=0°, θ=0°	489	612	-	cd/m^2	(1),(2)
Brightness Uniformity 1		-	φ=0°, θ=0°	70	90	-	%	(2),(3),(5)
Viewing Angle		CR	φ=30°, θ=30°	TBD	-	-	-	(4),(6),(7)
			φ=30°, θ=90°	TBD	-	-		
			φ=30°, θ=45°	TBD	-	-		
Contrast Ratio		CR	φ=0°, θ=0°	-	700	-	-	(6)
Response Time		G2G	φ=0°, θ=0°, 25°C	-	-	5.5	ms	(8)
			φ=0°, θ=0°, 50°C	-	-	3.2	ms	
Color Tone (Primary Color)	Red	x	φ=0°, θ=0°	0.626	0.656	0.686	-	
		y		0.301	0.331	0.361		
	Green	x		0.261	0.291	0.321		
		y		0.629	0.659	0.689		
	Blue	x		0.117	0.147	0.177		
		y		0.020	0.050	0.080		
	White	x		0.287	0.312	0.337		
		y		0.303	0.328	0.353		
NTSC Ratio		-		-	85	-	%	-
Crosstalk				-	-	2.5	%	
Flicker				-	-	-30	db	
Gamma		-	W30~W240	1.95	2.2	2.45	%	-

All the criteria shall be applied for initial(delivered) state. (Not for whole the product life.)

Measurement Conditions
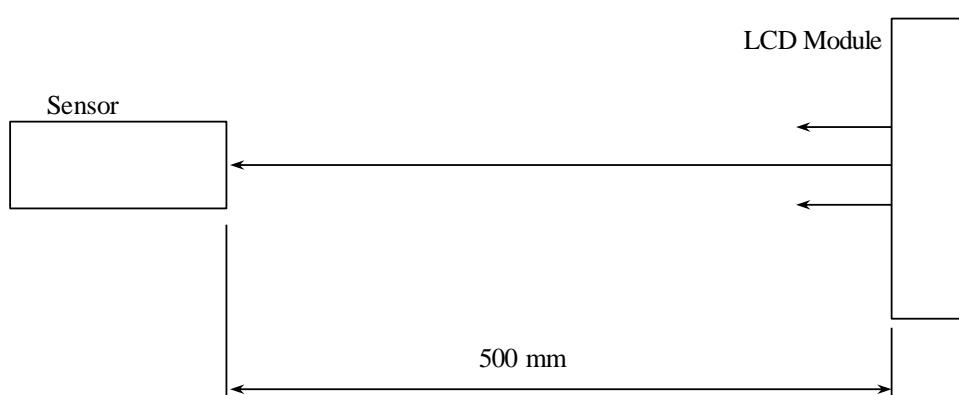
    Measurement environment : Dark room
    Ambient temperature : Ta=25°C
    Sequence : Refer to Item 9.4
    Power supply voltage : VDDI=1.8V, VSP=5.7V, VSN=-5.7V
    Backlight current : ILED=89mA (TBD) x 6 Strings Duty10%

Notes (1) Display image for measurement : All White
      (2) Measurment system;
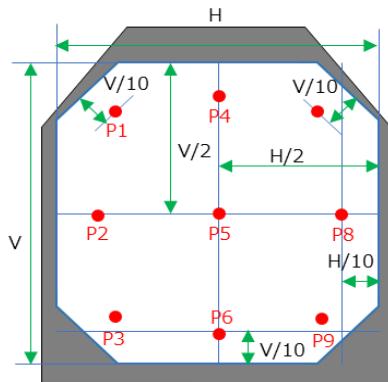
Sensor : CS-1000 or equivalent
Measurement point : Center of LCD's active area
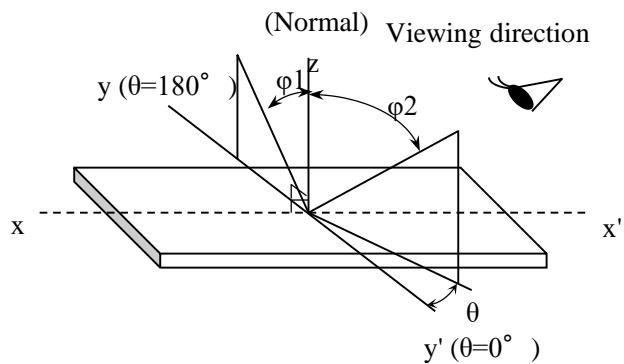
LCD Module

Sensor

500 mm

(3) Measurement point

(4) Definition of θ and φ

H

V/10   V/10

P1   P4

V/2   H/2

V   P2   P5   P8

H/10

P3   P6   P9

V/10

(Normal)   Viewing direction

y (θ=180°)   φ1   z

φ2

x   x'

θ

y' (θ=0°)

(5) Definition of brightness uniformity
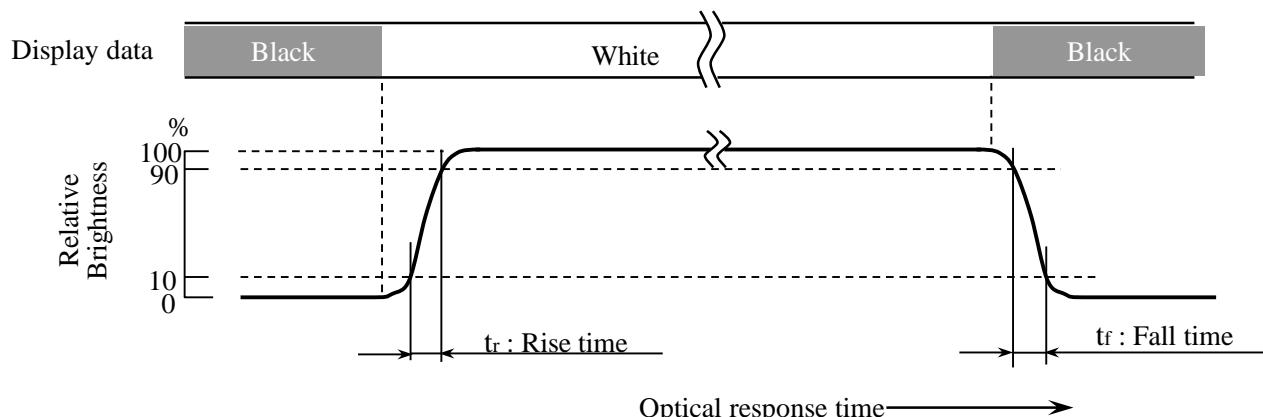
$$\text{Brightness uniformity} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100 \, (\%)$$

(6) Definition of Contrast "CR"

$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$
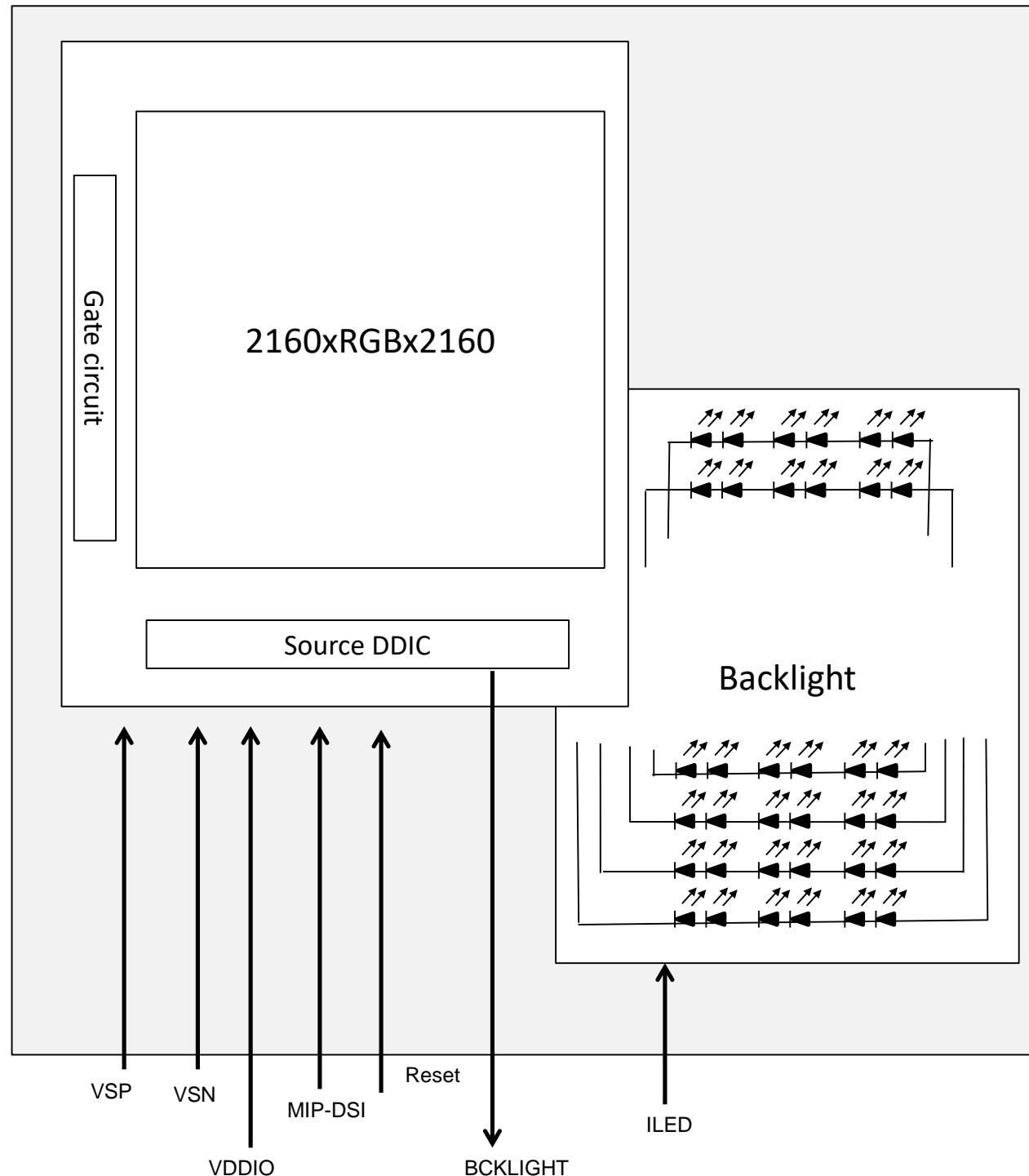
(7) Equipment   TBD

(8) Definition of Optical Response Time

Display data

| Black | White | Black |

Relative Brightness

%
100
90

10
0

t_r : Rise time

t_f : Fall time

Optical response time

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Gate circuit

2160xRGBx2160

Source DDIC

Backlight

VSP   VSN

MIP-DSI   Reset

VDDIO

BCKLIGHT

ILED
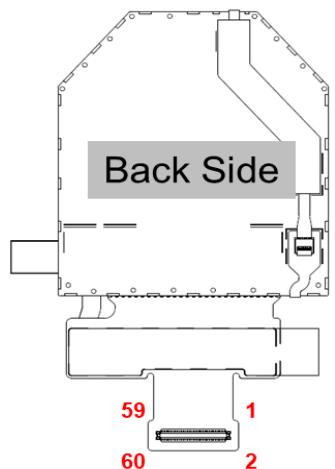
9. INTERFACE

9.1 INTERNAL PIN CONNECTION

Name	Pin No.		Pin No.	Name
GND	1		2	GND
DATA0A_B	3		4	BCKLIGHT_1
DATA0B_B	5		6	TE_2
DATA0C_B	7		8	TE_1
GND	9		10	PNSLV
DATA1A_B	11		12	GND
DATA1B_B	13		14	RESET
DATA1C_B	15		16	GND
GND	17		18	GND
DATA2A_B	19		20	GND
DATA2B_B	21		22	GND
DATA2C_B	23		24	GND
GND	25		26	VSN
VDDIO	27		28	VSN
VDDIO	29		30	GND
VDDIO	31		32	VSP
GND	33		34	VSP
DATA2C_A	35		36	GND
DATA2B_A	37		38	GND
DATA2A_A	39		40	LEDT_C1
GND	41		42	LEDT_C2
DATA1C_A	43		44	LEDB_C4
DATA1B_A	45		46	LEDB_C3
DATA1A_A	47		48	LEDB_C2
GND	49		50	LEDB_C1
DATA0C_A	51		52	NC
DATA0B_A	53		54	LEDT_A
DATA0A_A	55		56	LEDB_A
GND	57		58	LEDB_A
LEDT_A	59		60	LEDB_A

B to B connector: Panasonic AXE660124

Back Side

59   1
60   2

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MIPI C-PHY characteristics

	Item	Symbol	Unit	Condition	Min	Typ	Max	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.7~1.9V	-	-	40	
	Differential input low threshold	VIDTL	mV	IOVCC=1.7~1.9V	-40	-	-	
	Single-ended input low voltage	VILHS	mV	IOVCC=1.7~1.9V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.7~1.9V	-	-	535	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.7~1.9V	95	-	390	1
	Differential input impedance	ZID	Ω	IOVCC=1.7~1.9V		100		2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.7~1.9V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.7~1.9V	740	-	1350	
	I/O leakage current	ILEAK	μA	VIN=-50mV～1350mV	-100	-	100	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.7~1.9V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.7~1.9V	0.95	1.1	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=1.7~1.9V	110			3
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.7~1.9V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.7~1.9V	450	-	-	

Note1 VCMRX (DC) is common voltage of CPHY signal

Note2 Excluding COG resistance (contact resistance and ITO wiring resistance). VCMRX (DC) = (VDP+VDN)/2

Note3 Excluding COG resistance (contact resistance and ITO wiring resistance).

MIPI C-PHY host characteristics

|	Item	Symbol	Unit	Condition	Min	Typ	Max	Note
HS-TX	HS transmit differential voltage between strong one and strong zero	|VOD|strong	mV	IOVCC=1.7~1.9V	-	-	300	
	HS transmit differential voltage between weak one and weak zero	|VOD|weak	mV	IOVCC=1.7~1.9V	97	-	-	
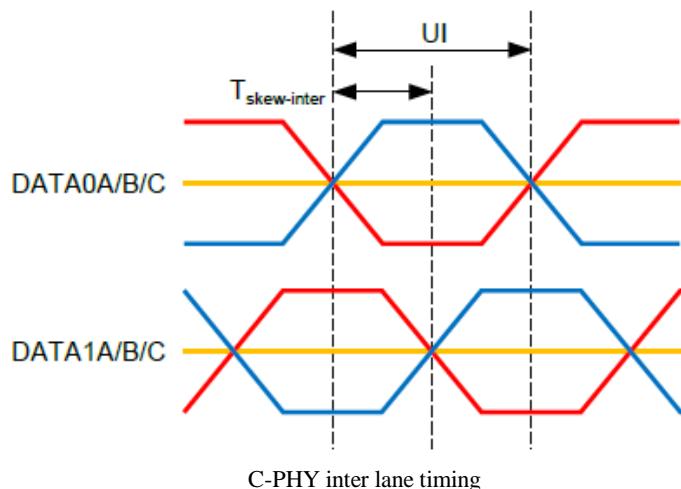
The host must be used in conformity with this HS-TX specification.

MIPI C-PHY HS-RX data specifications Confidential

Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Symbol rate	fSYMBOL	Msps	IOVCC = 1.7~1.9V	80	-	1300	1
UI instantaneous	UI	ns	IOVCC = 1.7~1.9V	0.77	-	12.5	
Data transfer rate	tDSIR	Mbps	IOVCC = 1.7~1.9V	182	-	2971	1
Inter lane skew	Tskew-inter	UI	IOVCC = 1.7~1.9V	-3.5	-	3.5	

Note1 1C-PHY data transfer rate is 2.28 times the C-PHY symbol rate

C-PHY inter lane timing
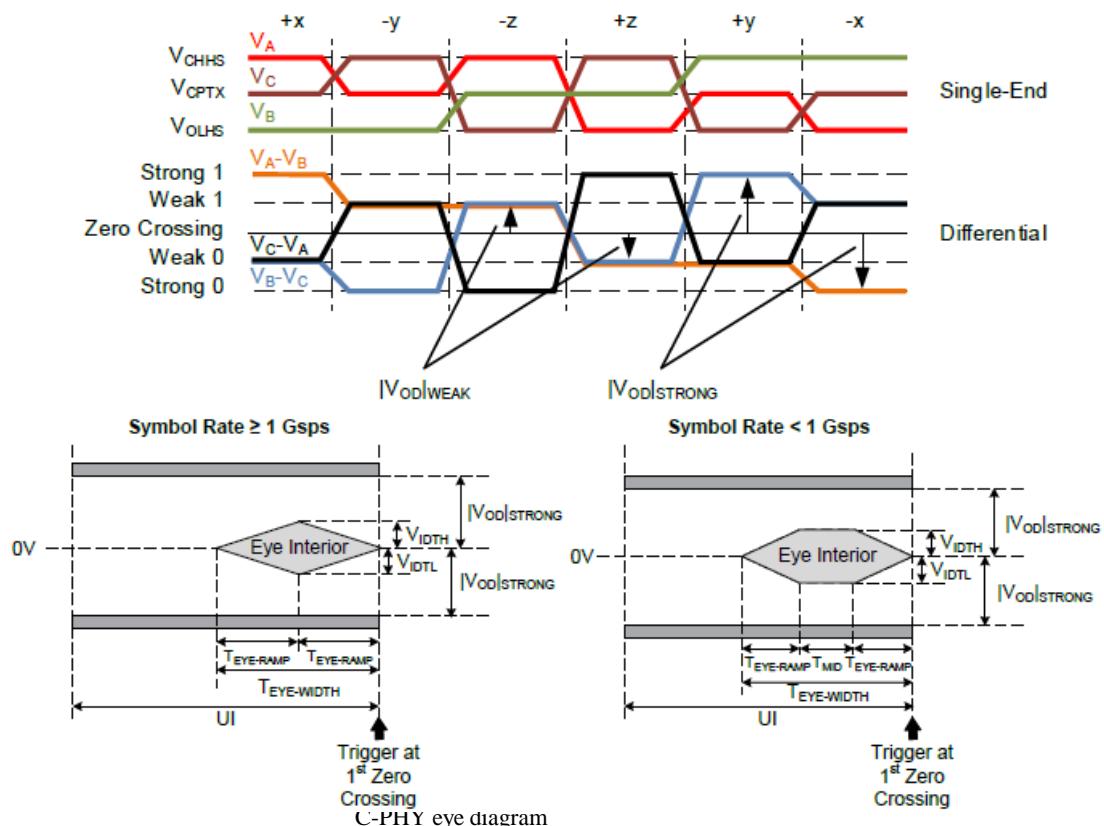
IPI C-PHY HS receiver eye diagram specifications (symbol rate≧1 Gsp

Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Eye ramp time	$T_{EYE-RAMP}$	UI	IOVCC = 1.7~1.9V	0.25	-	-	
Eye width	$T_{EYE-WIDTH}$	UI	IOVCC = 1.7~1.9V	0.5	-	-	

The Eye diagram specifications are defined at the PAD of R63455.

Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Eye ramp time	$T_{EYE-RAMP}$	ps	IOVCC = 1.7~1.9V	250	-	-	
Eye_horizontal-mid section	T_{MID}	ps	IOVCC = 1.7~1.9V	UI-1000	-	-	
Eye width	$T_{EYE-WIDTH}$	ps	IOVCC = 1.7~1.9V	T_{MID} + 500	-	-	

The Eye diagram specifications are defined at the PAD of R63455.

C-PHY eye diagram

MIPI C-PHY LP-RX/TX clock and data specifications   Confidential
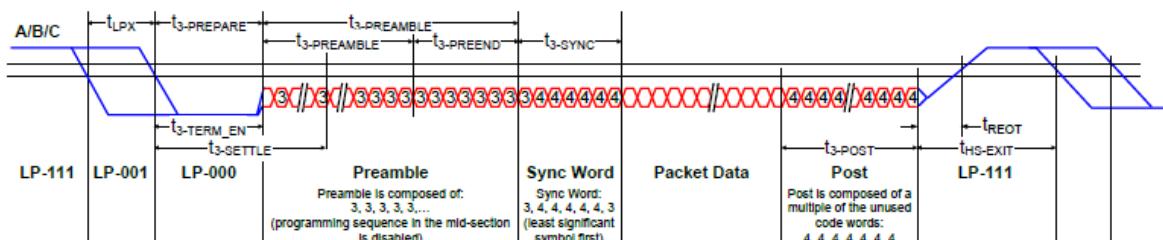
Item	Symbol	Unit	Condition	Min	Typ	Max	Note
Time to drive LP-000 to prepare for high speed transmission	$T_{3\text{-PREPARE}}$	ns	IOVCC = 1.7~1.9V	38	-	95	
Time interval during high speed receiver can receive high speed data starting at the beginning of $t_{3\text{-PREPARE}}$	$T_{3\text{-SETTLE}}$	ns	IOVCC = 1.7~1.9V	95	-	300	
Time from driving LP-000 to sending sync word	$T_{3\text{-PREPARE}} + T_{3\text{PREAMBLE}}$	-	IOVCC = 1.7~1.9V	300ns	-	-	1
Time to drive LP-111 after a HS burst	$T_{\text{HS-EXIT}}$	ns	IOVCC = 1.7~1.9V	100	-	-	
Time to drive LP-000 after a turnaround request	$T_{\text{TA-GO}}$	-	IOVCC = 1.7~1.9V		$4*T_{\text{LPTX}}$		
Time that the new transmitter waits after the LP-100 state before transmitting the bridge state (LP-000) during a link turnaround	$T_{\text{TA-SURE}}$	-	IOVCC = 1.7~1.9V	$1*T_{\text{LPTX}}$	-	$2*T_{\text{LPTX}}$	
Time that the new transmitter drives the bridge state (LP-000) after accepting control during a link turnaround	$T_{\text{TA-GET}}$	-	IOVCC = 1.7~1.9V		$5*T_{\text{LPTX}}$		
Length of any low-power state period	TLPX	ns	IOVCC = 1.7~1.9V	50	-	-	
Ratio of $T_{\text{LPX(MASTER)}}/T_{\text{LPX(SLAVE)}}$ between the master and slave sides	Ratio T_{LPX}	-	IOVCC = 1.7~1.9V	2/3	-	3/2	
Time that the transmitter continues sending post words (4444444) after the last associated data lane has transitioned to LP mode	$T_{3\text{-POST}}$	-	IOVCC = 1.7~1.9V	224	-	-	2
Length of the low-power transmitter period	TLPTX	ns	IOVCC = 1.7~1.9V	-	(8/fosc)	-	

Note1 The minimum value of $T_{3\text{-PREPARE}}$ is 38 ns and the minimum value of $T_{3\text{-PREAMBLE}}$ is 14 UI, so the minimum value of $T_{3\text{-PREPARE}} + T_{3\text{-PREAMBLE}}$ is

calculated as 38 ns + 14 UI. However, there is a relation where $T_{3\text{-PREPARE}} + T_{3\text{-PREAMBLE}} > T_{3\text{-SETTLE}}$. As a result, the minimum value,

$T_{3\text{-PREPARE}}+T_{3\text{-PREAMBLE}}$, is the same as the $T_{3\text{-SETTLE}}$ minimum value.

Note2 The minimum value of $T_{3\text{-POST}}$ is defined as 7 UI in the CPHY specification. However, R63455 requires a $T_{3\text{-POST}}$ period at 224 UI. The

CPHY specification states that the value of $T_{3\text{-POST}}$ should be adjustable at the transmitter from 7 UI to 224 UI in increments of 7 UI.
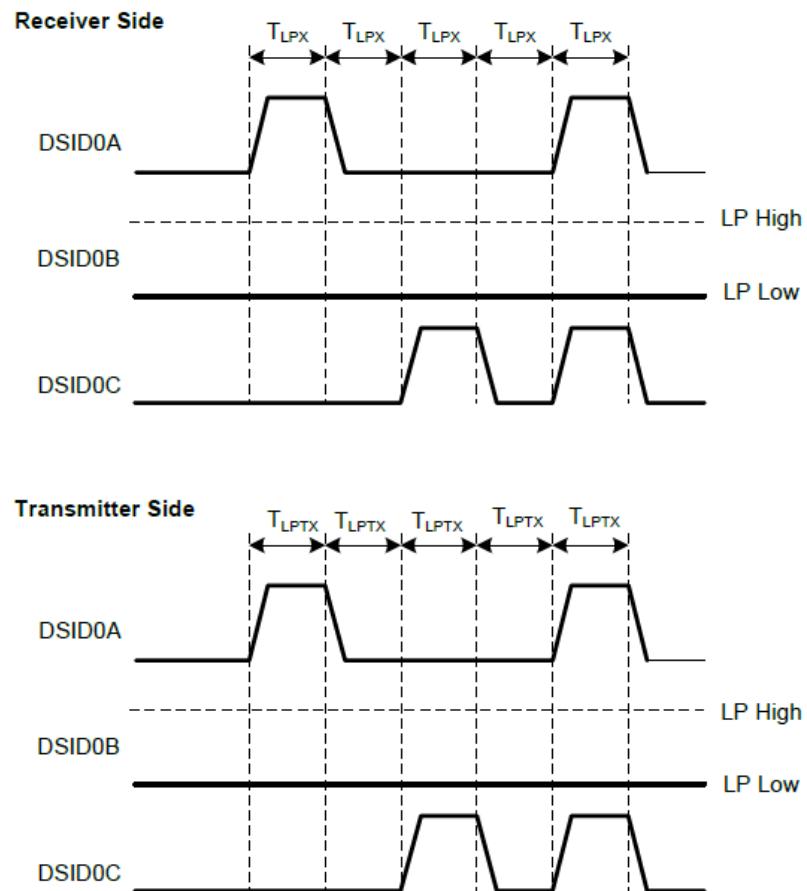
C-PHY LP mode

C-PHY HS data transmission in bursts

Note MIPI Alliance Standard for C-PHY, Version 1.1 7-October-2015

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Receiver Side

T_{LPX} T_{LPX} T_{LPX} T_{LPX} T_{LPX}

DSID0A

LP High

DSID0B

LP Low

DSID0C

Transmitter Side

T_{LPTX} T_{LPTX} T_{LPTX} T_{LPTX} T_{LPTX}

DSID0A

LP High

DSID0B

LP Low

DSID0C

C-PH LP mode

MIPI C-phy VideoMode bypass w FIFO 1port 1/2 DSC

Item		Specification	unit	Note
PHY	D/CPHY	CPHY	-	
	Lane/Trio	3trio	-	
Comp.	VesaDSC	1/2comp	-	
	Slice width	544	pxl	Horizontal 4slice
	Slice height	divisor of V.resolution	line	typically 8 or 16
Resol.	H resolution	2160	pxl	
	H res + Hdmy	2176	pxl	
	V resolution	2160	pxl	
V	Frame rate	120	Hz	
	V total	2392	line	
	V back porch	20	line	
	V front porch	212	line	
H	1line time	3.48	us	
	H active	1080	pxl	per port
	H active + Hdmy	1088	pxl	per port
	H back porch	min. 20	wordclock	
	H front porch	min. 20	wordclock	
	MIPI rate	1300	Msps	

MIPI rate including transfer overhead.

fWordClock = (1/7) * fDSICLK. fWordClock is the frequency of WordClock.
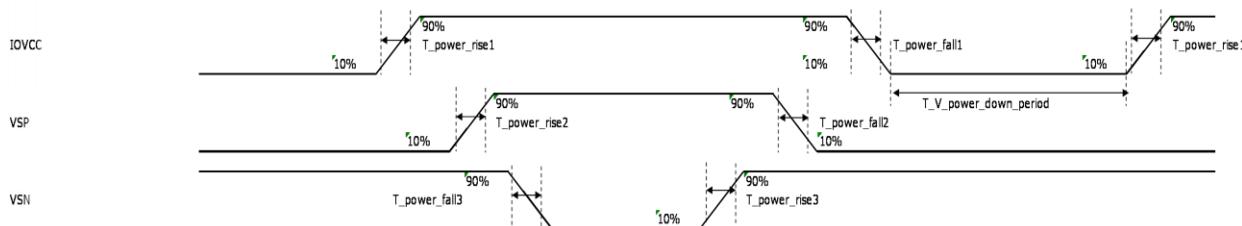
1. Supply Power Voltage
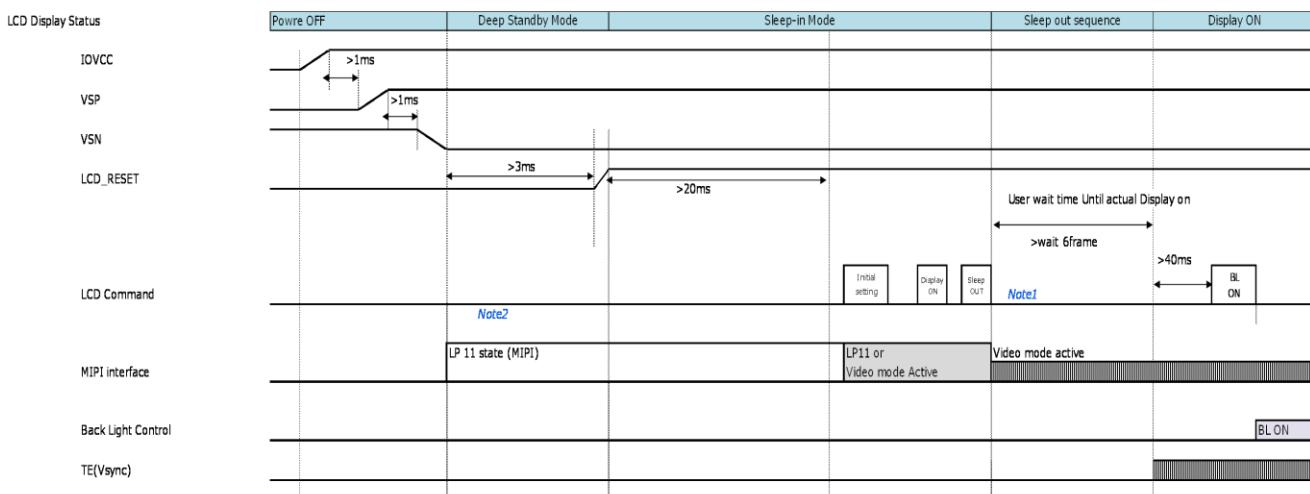
	Min	Typ	Max	Description
VSP	5.7	5.8	5.9	Analog power supply for LCD.
VSN	-5.9	-5.8	-5.7	Analog power supply for LCD.
IOVCC	1.7	1.8	1.9	Digital power supply for LCD

2. Supply Power Slew rate
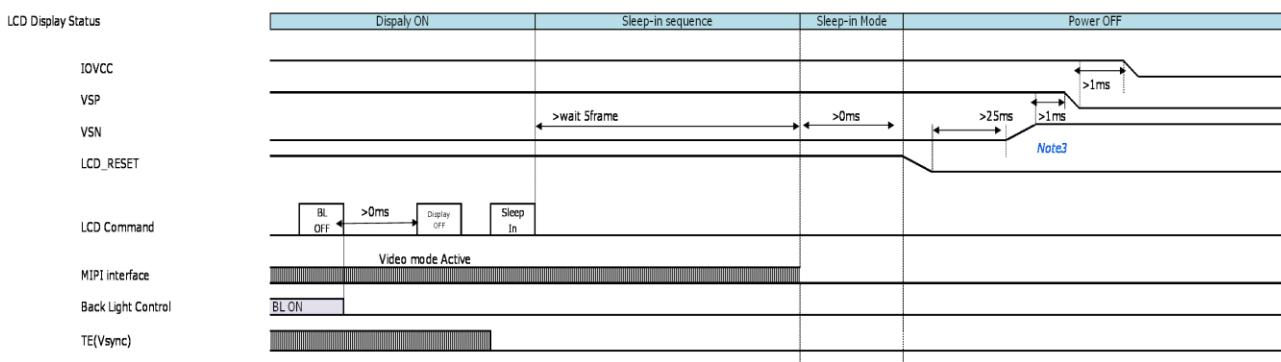
	Min	Typ	Max	Description
T_power_rise1	0.2ms	-	5ms	IOVCC from 10% to 90% target voltage
T_power_fall1	0.2ms	-	5ms	IOVCC from 90% to 10% target voltage
T_power_rise2	0.2ms	-	5ms	VSP from 10% to 90% target voltage
T_power_fall2	0.2ms	-	5ms	VSP from 90% to 10% target voltage
T_power_rise3	0.2ms	-	5ms	VSN from 10% to 90% target voltage
T_power_fall3	0.2ms	-	5ms	VSN from 90% to 10% target voltage
T_V_power_down_period	10ms	-	-	IOVCC < 100mV

3. Power On sequence

4. Power Off sequence

Note 1: After Sleep-out command, Driver IC will reload MTP regssiters and do internal power on action.
Therefore, any inital setting by MIPI should be set
after Sleep-outcommand with minimum delay time 6frame.
Note 2: When use MIPI I/F, MIPI lanes must go to LP11 state during power-on and RESET sequnece.
Note 3: After Sleep In sequence is completed, turn off power supply (at least VSN,VSP) to avoid flicker and sticking image issue.
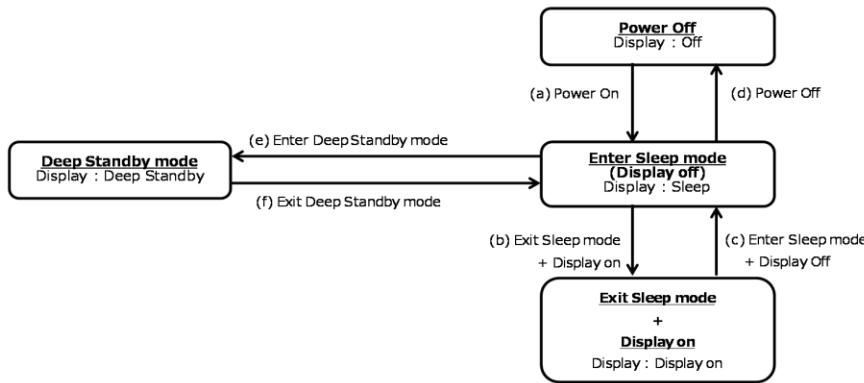
State transition diagram

(a) Power On Sequence

Step	Action/Command	DSI Data Type (DDIC)	Address	Data	Note
1	RESET="L"				
2	IOVCC On				
3	Wait 1ms (min.)				Over 1ms from IOVCC=90% (depends on External Power Supply Circuit)
4	VSP On				
5	Wait 1ms (min.)				Over 0us from VSP=10%/50% to VSN=10%/50% (depends on External Power Supply Circuit)
6	VSN On				
7	Wait 3ms (min.)				Over 3ms from IOVCC=90% (depends on External Power Supply Circuit)
8	RESET="H"				
9	Wait 20ms (min.)				Wait Min. 20ms

Initial setting & exit sleep mode sequence for MIPI C-phy VideoMode with RAM 1port DSC(1:2)

(b) Exit Sleep mode + Display On Sequence (Initial setting & Exit Sleep mode & Display On)

Step	Action/Command	DSI Data Type (DDIC)	Address	Data	Note
1	Manufacture Command access protect	MCS	0x29	0xB0	0x04	Manufacture Command access protect off
2	Sequence control	MCS	0x29	0xD6	0x00	
3	DSI Control	MCS	0x29	0xB6	0x20	
					0x6B	
					0x80	1port
					0x06	
					0x33	
					0x8A	
					0x00	
					0x1A	
					0x7A	
4	Display Mode	MCS	0x29	0xB7	0x54	FIFO
					0x00	
					0x00	
					0x00	
5	Generic Outpin setting	MCS	0x29	0xB9	0x00	Generic pin start setting
					0x46	
					0x01	Generic pin pulse width setting
					0x9A	
6	Display setting1	MCS	0x29	0xC0	0x42	
					0x86	
					0xF4	
					0x01	
					0x08	
					0x70	
					0x04	
					0x2E	
7	Display setting2	MCS	0x29	0xF1	0x1E	
8	Display setting3	MCS	0x29	0xC6	0x70	
					0x08	
					0x40	
					0x04	
					0x32	
					0x6F	
					0x08	
					0x88	
					0x00	
					0x00	
					0x00	
					0x00	
					0x00	
					0x00	
					0x00	
					0x10	

No	Item	Type				Notes
9	Display setting3	MCS	0x29	0xCD	0x00	
10	Display setting4	MCS	0x29	0xCF	0x8A	
					0x00	
					0x80	
					0x46	
					0x61	
					0x00	
					0x8A	
11	Display setting5	MCS	0x29	0xEC	0x02	
					0xB2	
					0x00	
					0x00	
					0x00	
12	PPS setting	MCS	0x29	0xE6	1st_para PPS0_A[7:0] 2nd_para PPS1_A[7:0] | | | | 93rd_para PPS92_A[7:0] 94th_para PPS93_A[7:0]	(*) Please set the PPS setting
13	get_compression_mode	DCS	0x39	0x03	0x01	Compression mode = enable
14	set_tear_scanline	DCS	0x39	0x44	0x00	
					0x00	
15	set_tear_on	DCS	0x15	0x35	0x00	
16	set_address_mode	DCS	0x15	0x36	0x00	
17	set_pixel_format	DCS	0x15	0x3A	0x77	
18	Video stream Packect Start					
19	Wait 0 frames (min.)					
20	set_display_on	DCS	0x05	0x29	-	
21	exit_sleep_mode	DCS	0x05	0x11	-	
22	Wait 6frame (min.)					Do NOT input any command during ON sequence.
23	Sequence control	MCS	0x29	0xD6	0x80	
24	Manufacture Command access protect	MCS	0x29	0xB0	0x03	Manufacture Command access protect on

(c) Display off & Enter Sleep mode Sequence

Step	Action/Command	DSI Data Type (DDIC)		Address	Data	Note
1	set_display_off	DCS	0x05	0x28	-	
2	set_tear_off	DCS	0x05	0x34	-	
3	enter_sleep_mode	DCS	0x05	0x10	-	
4	Wait 5frame (min.)					

(d) Power Off Sequence

Step	Action/Command	DSI Data Type (DDIC)		Address	Data	Note
1	RESET="L"					
2	Wait 25ms(min.)					Wait Min. 25ms
3	VSN Off					
4	Wait 1ms					
5	VSP Off					
6	Wait 10ms					
7	IOVCC Off					

(e) Enter Deep Standby mode Sequence
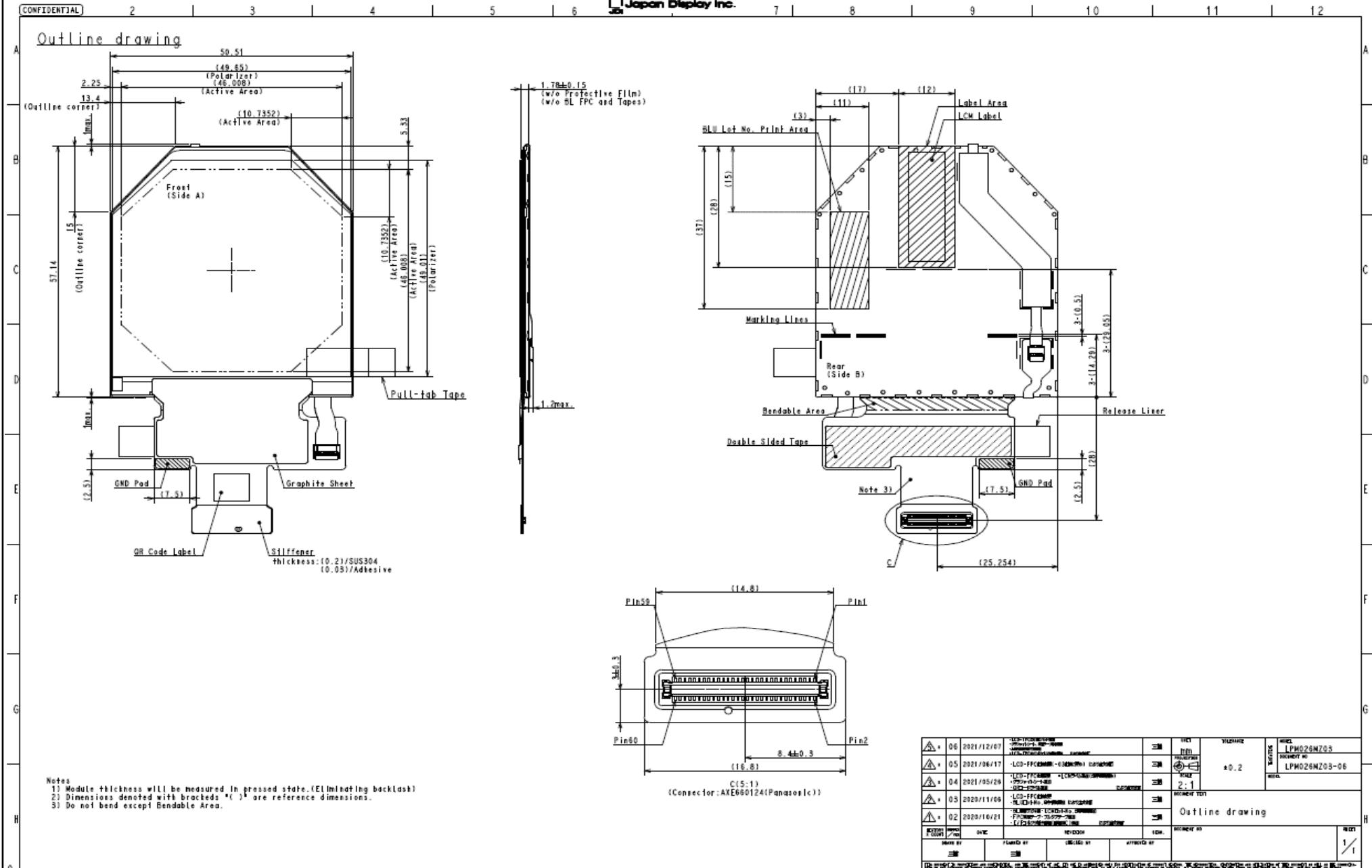
Step	Action/Command	DSI Data Type (DDIC)		Address	Data	Note
1	RESET="L"					
2	Wait 25ms(min.)					Wait Min. 25ms

(f) Exit Deep Standby mode Sequence

Step	Action/Command	DSI Data Type (DDIC)		Address	Data	Note
1	RESET="H"					
2	Wait 20ms (min.)					

Outline drawing

Notes
1) Module thickness will be measured in pressed state.(Eliminating backlash)
2) Dimensions denoted with brackets "( )" are reference dimensions.
3) Do not bend except Bendable Area.

10. VISUAL INSPECTION

10.1 INSPECTION CONDITION

(1) Standard
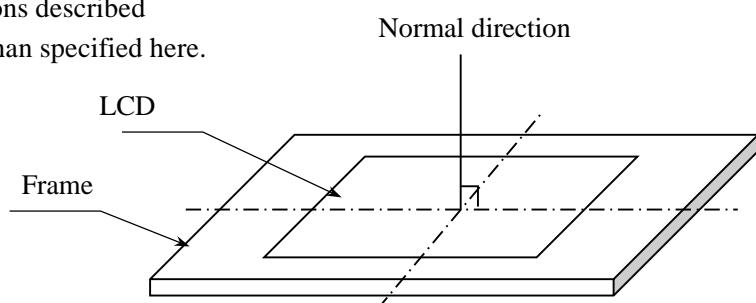
The standards are the quality level used to judge whether or not products lots pass during acceptance inspection of products delivered to your company.

The standards are shown below.

*Inspection method: Compliant with ANSI/ASQC Z1.4-1993,
ordinary inspection level II, inspection by one time sampling.

(2)	Ambient illumination 1	: 50[lx] for B/L ON item
(3)	Ambient illumination 2	: 1000 - 1500 [lx] for B/L OFF item
(4)	Distance between inspector's eyes and LCD Module	: Approximately 30 [cm]
(5)	Viewing angle	: φ=0° (Normal direction)
(6)	Ambient Temperature	: 25°C

Refer to the Measurement Conditions described
in Item 6 for the conditions other than specified here.
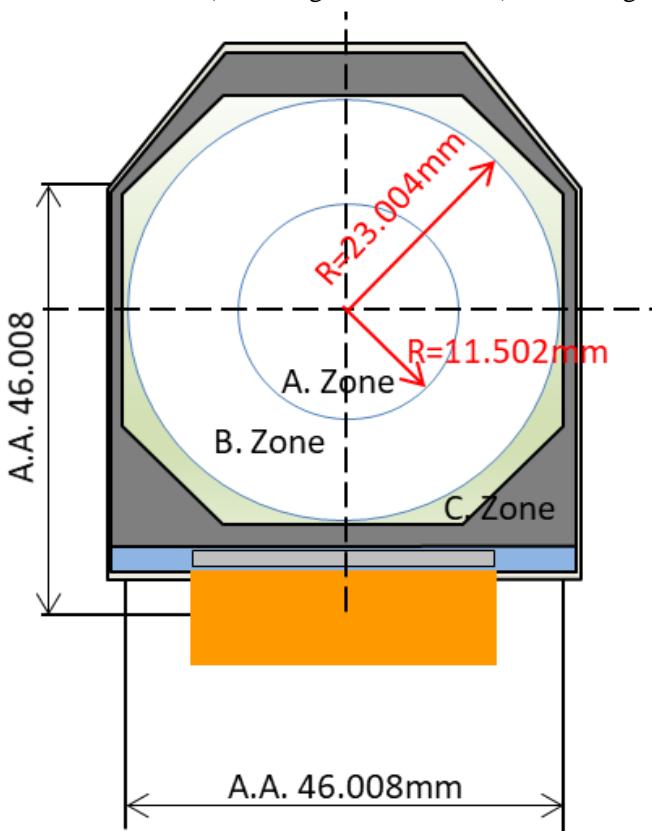
10.2 DEFINITION OF ZONE

A zone: Center of active area , which consist of two R=11.502mm circles

B zone: The area, which consist of two R=23.004mm circules, excluding A zone

C zone: The active area excluding A zone and B zone (C zone is out of inspection area.)

D zone: Whole LCD modue (including FPC and frame), excluding active area

11.3 COSMETIC SPECIFICATION

11.3.1 Screen Defects Specification for LCD Module
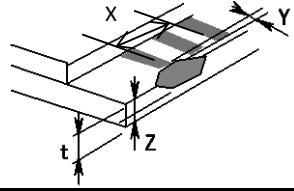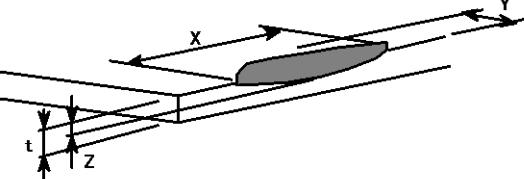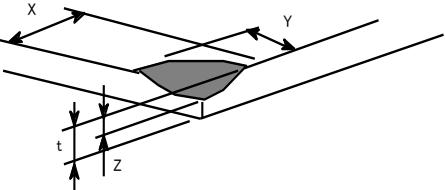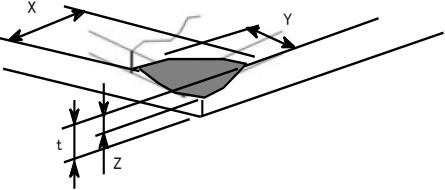
No.	Item		Maximum Acceptable Number	Unit	Applied zone	LCD module	Back light	Note
1	Bright Defect (Bright Dot, Bright Foreign Particles, Stain, Scratch, Air Bubble)		Ignored	PC	C	On		(1), (2)
	Brightness is equl to or brighter than (W60,R85,G65,B140)	L >=1 pixel (R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be greater than or equal to .021mm	0	PC	A, B			
	Brightness is dakar than (W60,R85,G65,B140)	L < 1 pixel (R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be less than .021mm	Ignored	PC	A, B			
	Brightness is equl to or brighter than (W60,R85,G65,B140)	L < 1 pixel (R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be less than .021mm	0	PC	A			
	Brightness is equl to or brighter than (W60,R85,G65,B140)	L < 1 pixel (R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be less than .021mm	3 (DS>=5mm) 0 (DS<5mm)	PC	B			
2	Dark Dots (including particl		Ignored	PC	C	On		(1), (2)
	Darkar than W170	L < 1 pixel (R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be less than .021mm	ignored	PC	A, B			
	Darkar than W195	L >=1 pixel (R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be greater than or equal to .021mm	1	PC	A			
	Darkar than W195	L >=1 pixel (R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be greater than or equal to .021mm	2 (DS>=5mm) 0 (DS<5mm)	PC	B			
	Darkar than W215	L >= 2x(R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be greater than or equal to .042mm OR 2 adjacent black dots	0	PC	A			
	Darkar than W215	L >= 2x(R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be greater than or equal to .042mm OR 2 adjacent black dots	2 (DS>=5mm) 0 (DS<5mm)	PC	B			
	Darkar than W220	L >= 3x(R + G + B) (L+W)/2 = (Length of Defect and width of defect)/2 should be greater than or equal to .063mm OR 3 adjacent black dots	Ignored	PC	A, B			

11.3.1 Screen Defects Specification for LCD Module

No.	Item			Maximum Acceptable Number	Unit	Applied zone	LCD module Back light	Note
3	Line Defect			0	PC	A, B	On	(2)
4	Uneven Brightness (Linear)			Serious one is not allowed	-	A, B	On	(2), (4)
5	Uneven Brightness (Circular)							
6	Foreign particles, stain, Scratch of Polarizer (Limer)[mm] W:Width, L:Length	W≤0.05	L≤5	Ignored	PC	A, B	Off	(3), (4), (5)
			5<L	0				
		0.05<W	-	0				
			-	-	-			
7	Foreign particles, stain, Scratch of Polarizer (Circular)[mm] D:Average diameter	D≤0.25		Ignored		A, B	Off	(3), (4), (5)
		0.25<D		0				
		-		-				
		-		-				
8	Air Bubble [mm] D:Average diameter	D≤0.25		Ignored	PC	A, B	Off	(3), (4), (5)
		0.25<D		0				
		-		-				
9	Scratch of FPC			Serious one is not allowed	-	C,D	Off	(5)

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Item	Criterion for Defects		Note
Glass Chipping [Pad Area]		Size (mm) $X \leqq 3.0$ $Y \leqq 0.5$ $Z \leqq t$	
Glass Chipping [Except Pad Area]		Size (mm) $X \leqq 3.0$ $Y \leqq 1.0$ $Z \leqq t$	
Glass Chipping [Corner PAD Area]		Size (mm) $X(or\ Y) \leqq 2.5$ $Y(or\ X) \leqq 2.5$ $Z \leqq t$	
Glass Chipping [Corner No Pad Area]		Size (mm) $X(or\ Y) \leqq 1.0$ $Y(or\ X) \leqq 2.0$ $Z \leqq t$	
Progressive crack is NG			

Notes   (1)   The defect is counted when brightness and size meet the criteria together.

(2)   Defect is judged with the Lupe (10x) (or other equvalent method) and it is disregarded,
if it can not be recoginized through the Lupe.
If there is any judgement difference or dispute, it can be discussed for special case.
and can not be lot judgement.
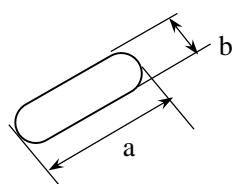
(3)   Something which can be easily wiped off is disregarded as a defect.

(4)   In case a problem arises, both parties should discuss needed items such as limit samples.
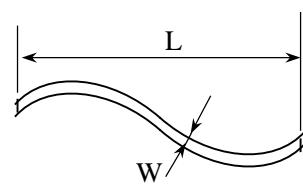
(5)   Definitions for D, W and L are as follows.

<table>
<tr><td align="center">Definition of D</td><td align="center">Definition of W and L</td></tr>
</table>

$$D = \frac{a + b}{2}(mm)$$

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No.	Test Items	Test Conditions	Note
1	High temperature, operating	55°C, 240 h	(1), (2), (3)
2	Low temperature, operating	5°C, 240 h	(1), (2), (3)
3	High temperature, Storage Non-operation	70°C, 240 h	(3)
4	Low temperature, Storage Non-operation	-30℃, 240 h	(3)
5	High temperature & high humidity, Operating	55°C, 90%RH, 240 h	(1), (2), (3)
6	Thermal shock, Non-operation	-30℃ (30min) / +70℃ (30min), 50 cycles	(3)
7	ESD (HBM) x 5 each	1kV 150pF, 1.5KOhm	
8	ESD Contact discharge x 5 each	Center+4 cornner,+/-4kV 150pF,330Ohm	
9	Image sticking	Checkerboard pattern (G255/G0) for 60 mins, no residual image in G128	
10	FPC bending	200g/±90° 10 cycles	
11	FPC peel strength	4.9N/cm/+90° 10 once	
12	Box vibration and drop	Random vibration frequency:5-500Hz, PSD:0.04-0.000006G^2/Hz Time: X(18min), Y(18min), Z(101min) Condition on the stage: Fixed	(4)
13	Drop test	60cm height, 1corner, 3edges, 6surfaces 1time each	(4)

Notes

(1) Operation conditions : VDDI=1.8V, VSP=5.7V, VSN=-5.7V, fFLM=120Hz.

(2) No loss of function during the test.

(3) All the measurement shall be done @25℃

(4) One set includes 4 inner boxes and each inner box has 10 trays which contain 3 pieces of LCD modules each and an empty tray as the cover.