

» ADDER CIRCUIT:-

Adder circuit is a combinational digital circuit that is used for adding two binary numbers. Adder circuits are of two types.

- Half adder
- Full adder

⇒ HALF ADDER:-

• Half adder is a combinational arithmetic circuit that adds two binary numbers and produces a sum bit (S) and carry bit (C) as the output.

If A and B are the input bits, then sumbit(S) is the X-OR of A and B and carry bit (C) will be the And of A and B.

From this, it is clear that the half adder can be easily constructed by using one

XOR gate and one And gate.

- Half adder is simplest of all adder circuit but it has a major disadvantage. Half adder can add only two input bits A and B and has nothing to do with the carry if there is any in the input. That's why it is called half adder circuit.

LOGIC EXPRESSIONS :-

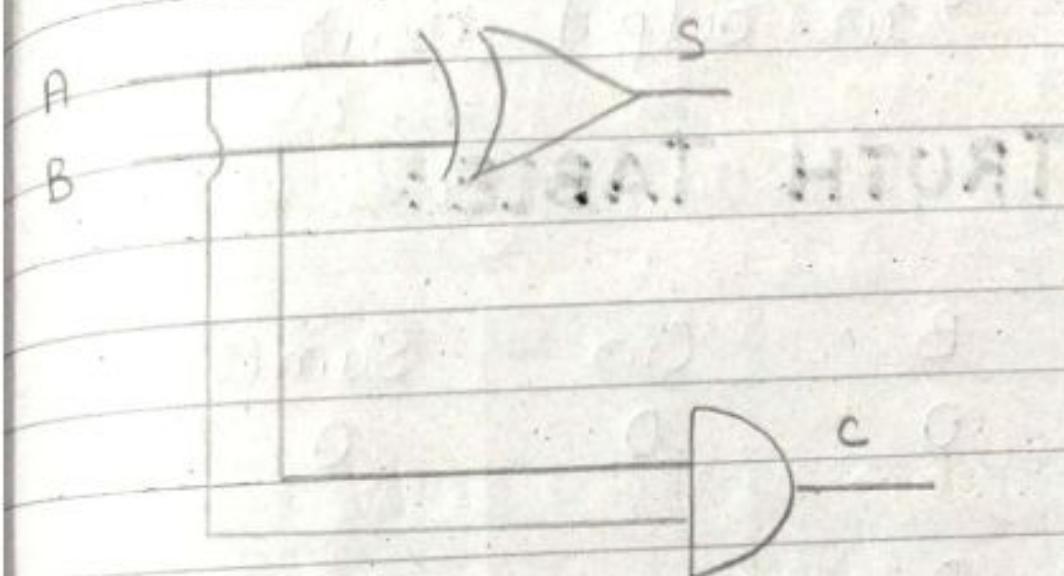
$$\text{Sum} = \Sigma = A \oplus B$$

$$\text{Carry}, C = A \cdot B$$

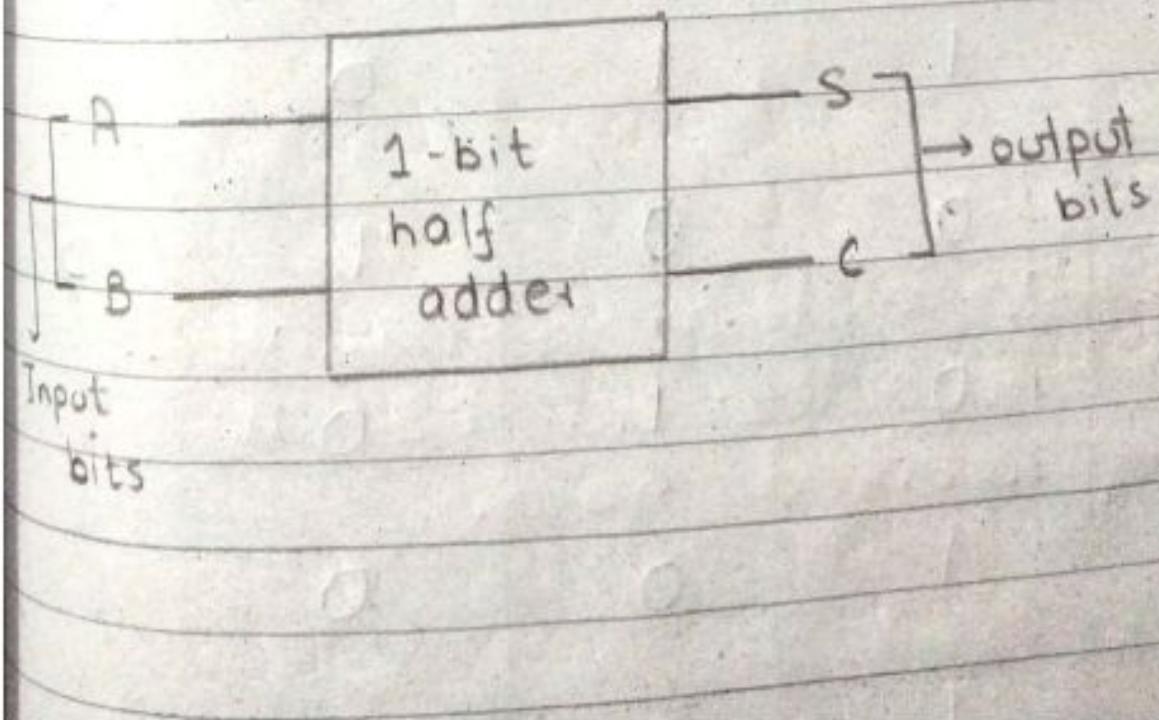
TRUTH TABLE:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

REALIZATION / LOGIC DIAGRAM:-



SCHEMATIC:-



=> Full ADDER:-

A full adder accepts two input bits and an input carry and generates a sum output and an output carry.

TRUTH TABLE:

A	B	Cin	Sum(3)	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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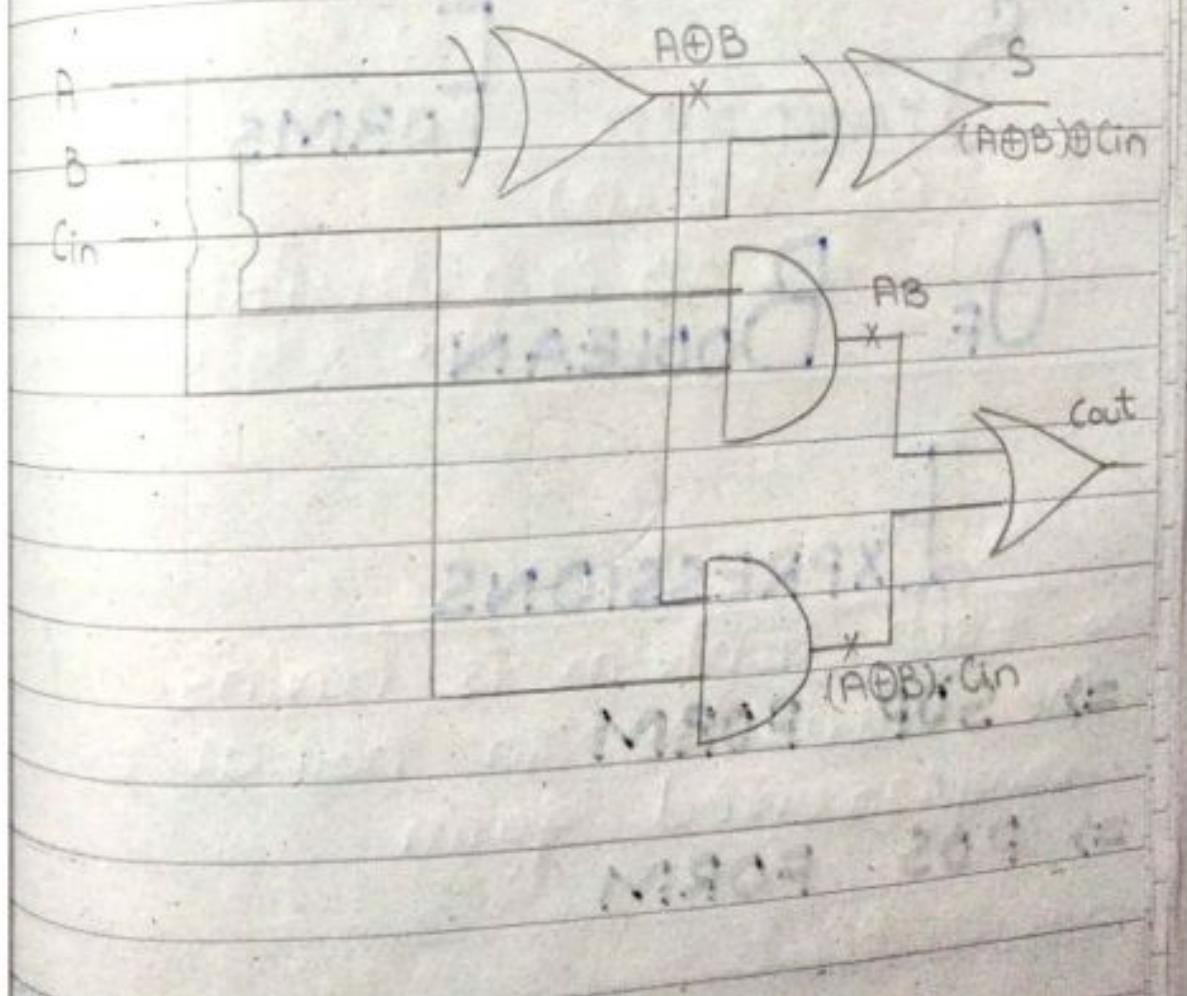
LOGIC EXPRESSIONS:-

$$\text{Sum} = S = (A \oplus B) \oplus \text{Cin}$$

$$\text{Cout} = A \cdot B + (A \oplus B) \cdot \text{Cin}$$

LOGIC DIAGRAM /

REALIZATION:-

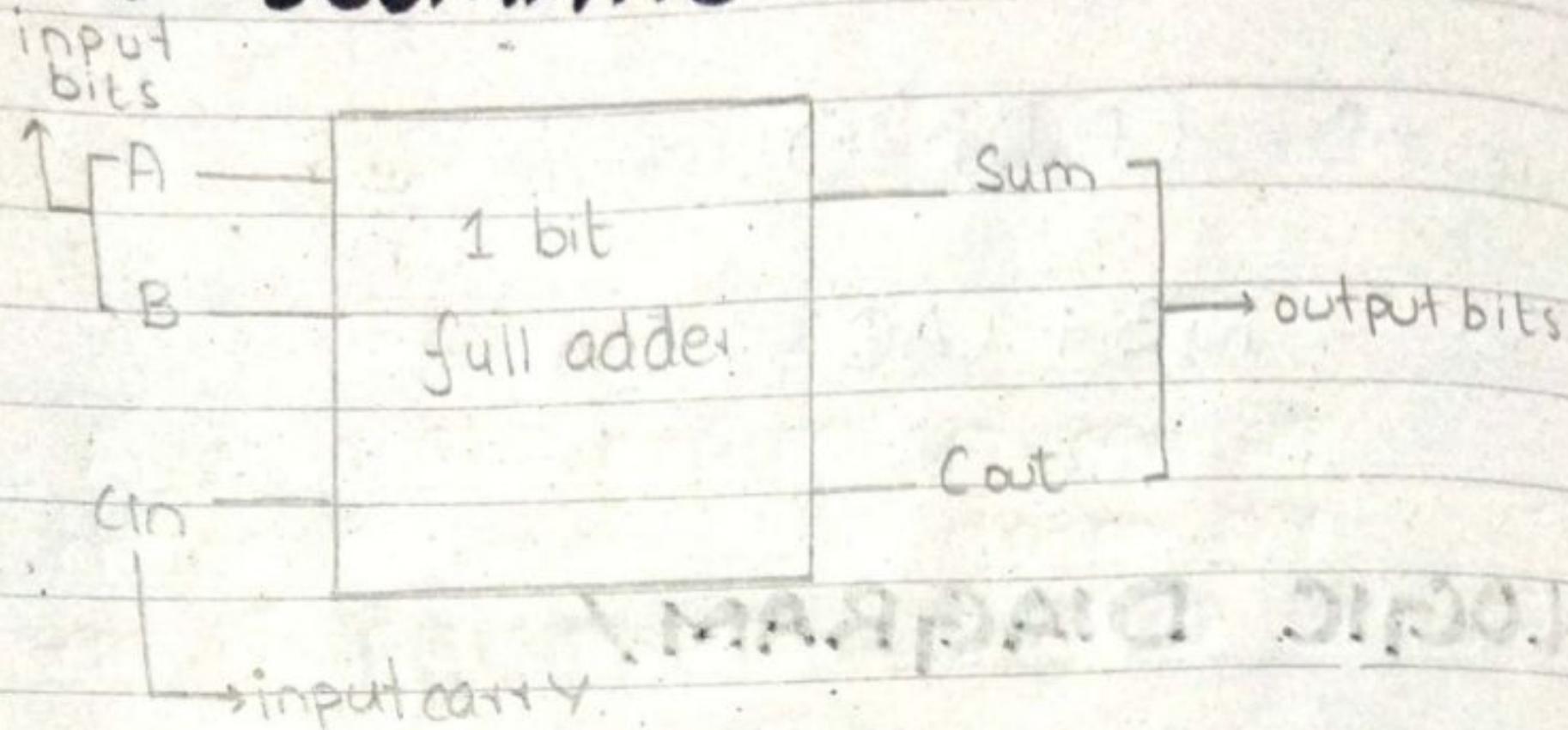


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⇒ SCHEMATIC :-



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⇒ DECODER:-

⇒ A decoder is a digital circuit that detects the presence of a specific combination of bits on its input and indicates the presence of that code by a specified output level.

⇒ A decoder has n input lines to handle n bits and from one to 2^n output lines to indicate the presence of one or more n -bit combinations.

⇒ It take n input and give 2^n output.

⇒ accept n -input line and give 2^n output lines.

TWO BIT INPUT DECODER

A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
1	0	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

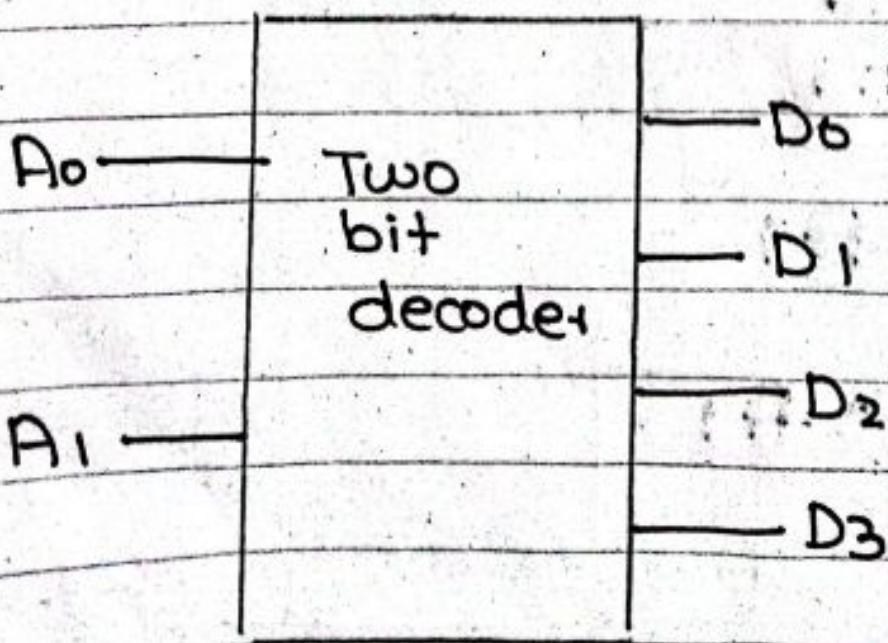
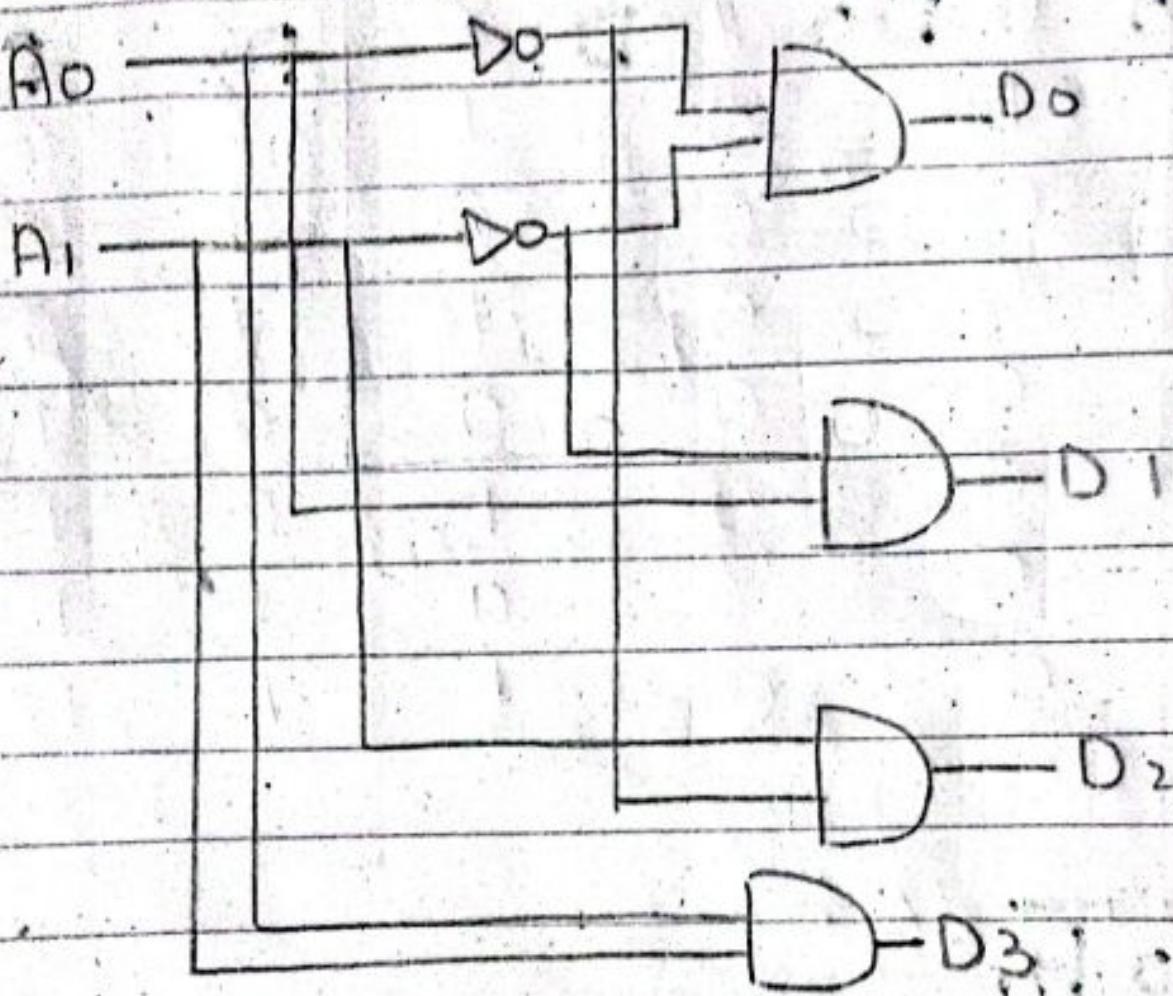
$$D_0 = \frac{A_0}{A_0 - A_1}$$

$$D_1 = \text{AoA}_1$$

$$D_2 = \overline{A_0 A_1}$$

$$D_3 = A_0 \cdot A_1$$

LOGIC DIAGRAM:-



3 bit to 8 bit decoder

A_2	A_1	A_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0

$$D_0 = \overline{A_0} \overline{A_1} \overline{A_2}$$

$$D_1 = A_0 \overline{A_1} \overline{A_2}$$

$$D_2 = \overline{A_0} A_1 \overline{A_2}$$

$$D_3 = A_0 A_1 \overline{A_2}$$

$$D_4 = \overline{A_0} \overline{A_1} A_2$$

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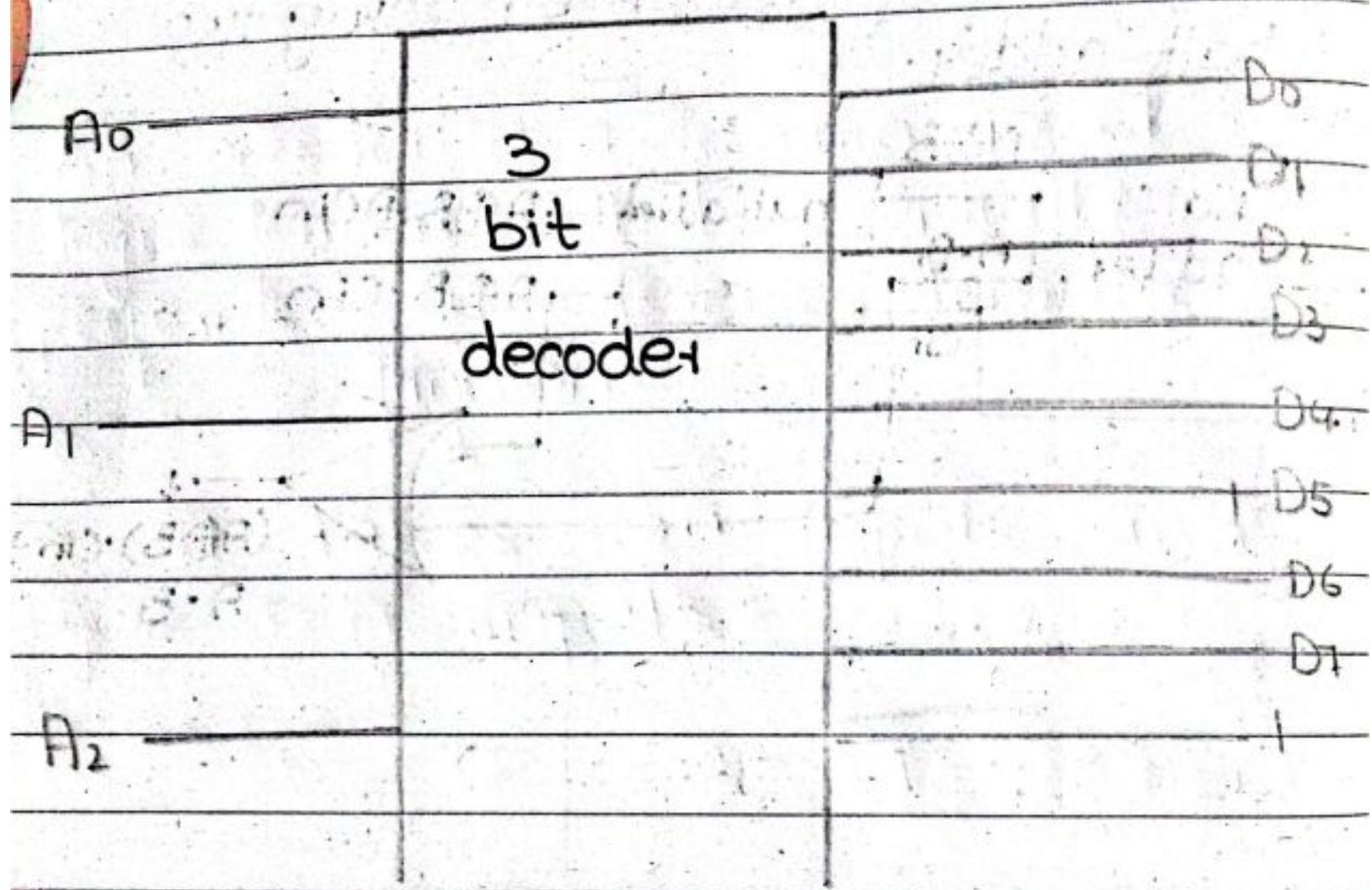
D ₃	D ₄	D ₅	D ₆	D ₇	D ₈
0	0	0	0	0	
0	0	0	0	0	
0	0	0	0	0	
1	0	0	0	0	
0	1	0	0	0	
0	0	1	0	0	
0	0	0	1	0	
0	0	0	0	1	

$$D_5 = A_0 \bar{A}_1 A_2$$

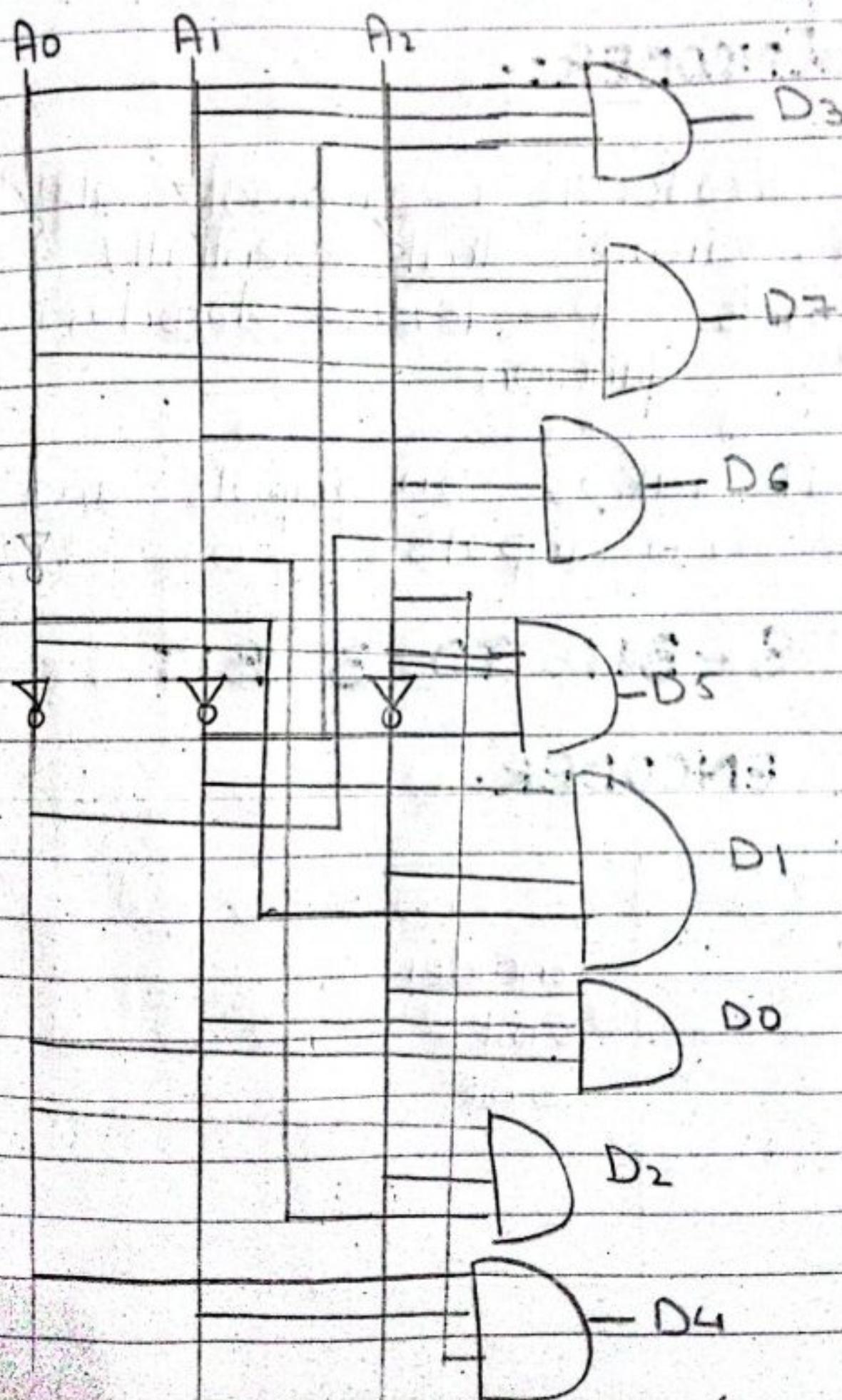
$$D_6 = \bar{A}_0 A_1 A_2$$

$$D_7 = A_0 A_1 A_2$$

SCHEMATIC DIAGRAM



LOGIC DIAGRAM:-



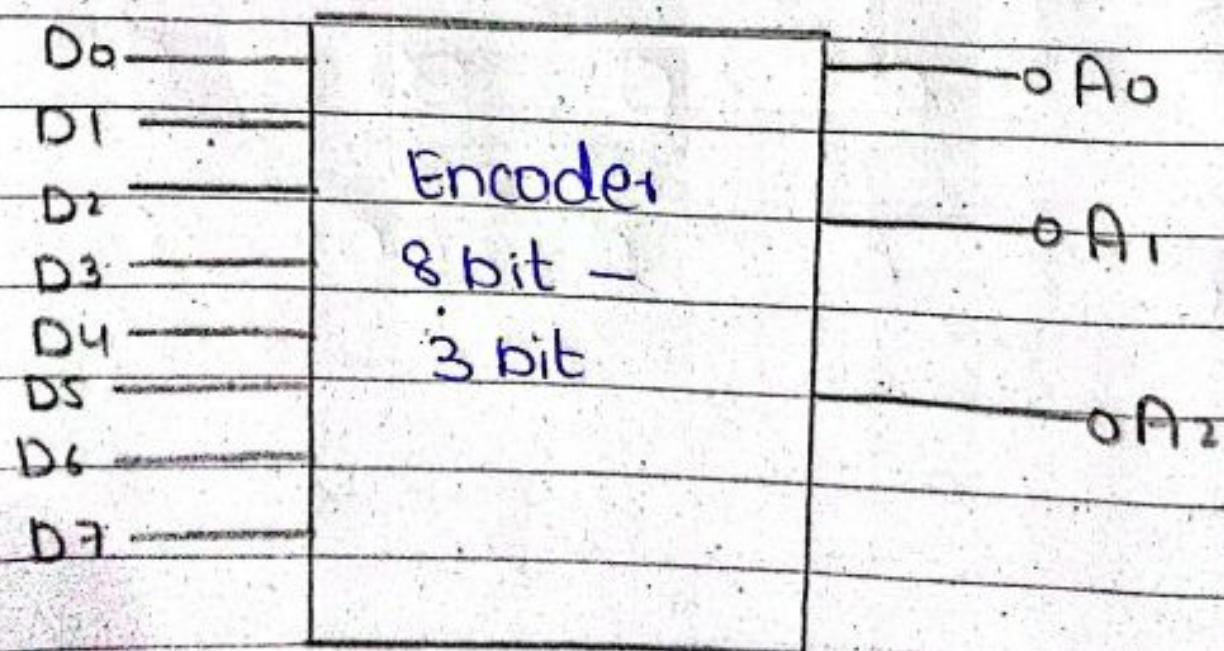
⇒ ENCODER:-

An encoder is a combinational logic circuit that essentially performs a reverse decoder function.

⇒ It takes 2^n inputs and give n inputs.

8-BIT TO 3 BIT

ENCODER.



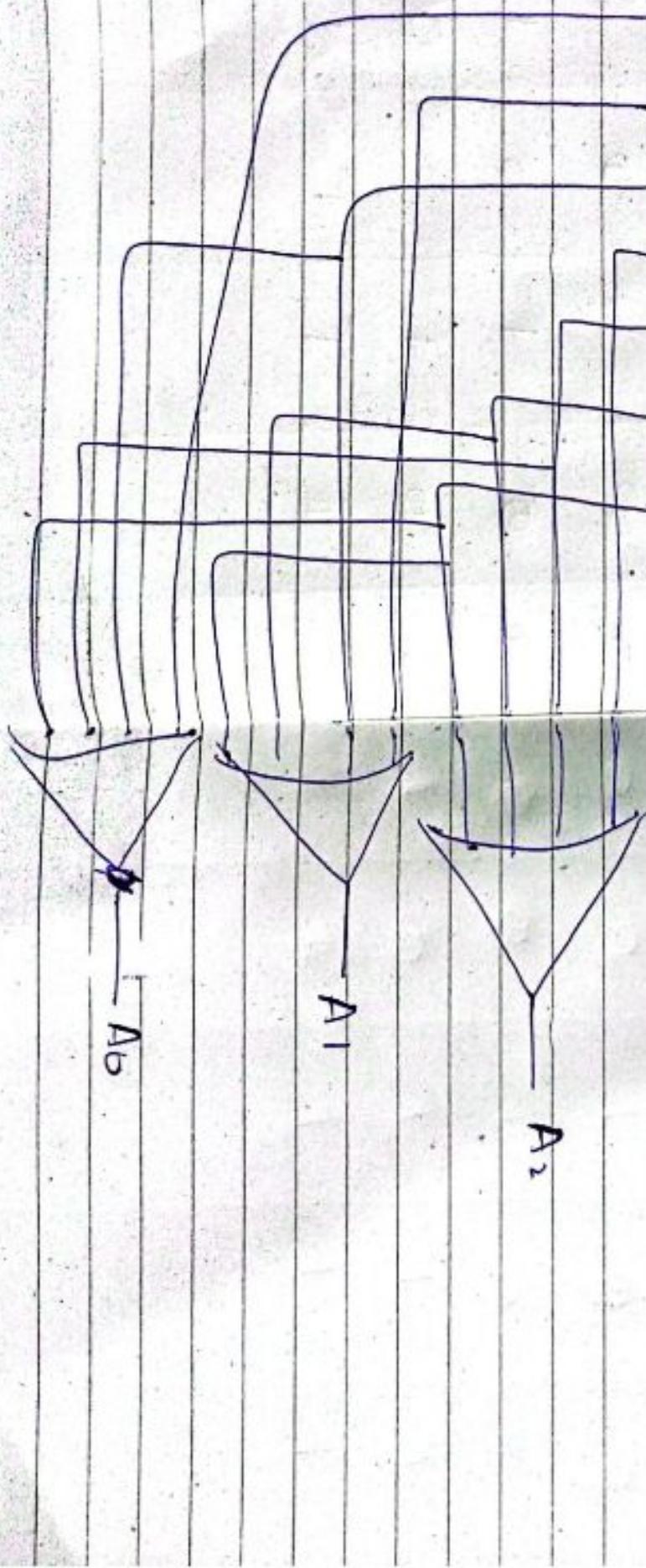
LOGIC DIAGRAM:-

$$A_2 = D_4 + D_5 + D_6 + D_7$$

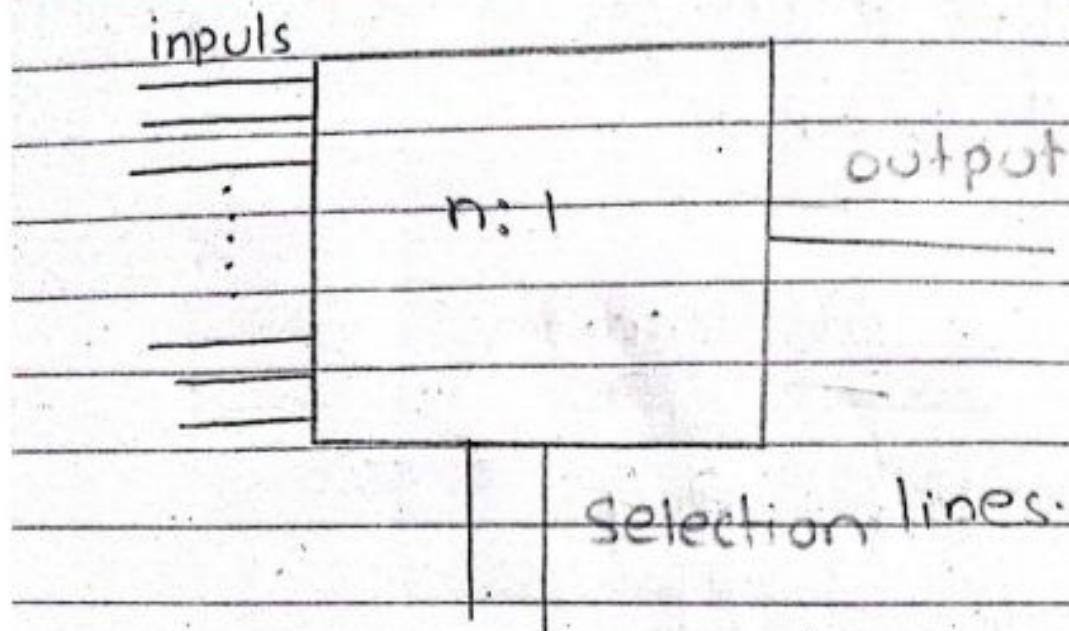
$$A_1 = D_2 + D_3 + D_6 + D_7$$

$$A_0 = D_1 + D_3 + D_5 + D_7$$

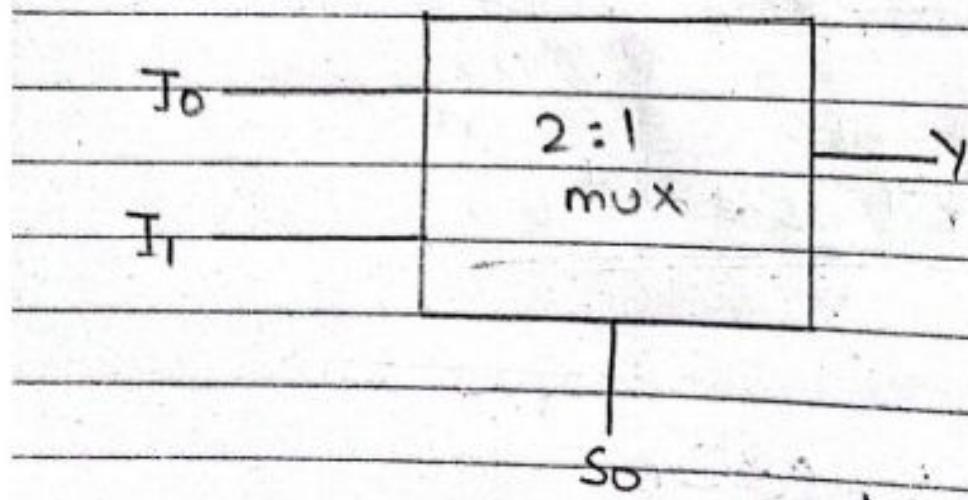
D₀ D₁ D₂ D₃ D₄ D₅ D₆ D₇



MULTIPLEXER :-



2:1 MUX:



$2 = 2^{\textcircled{1}} \rightarrow 1$ selection line

$4 = 2^{\textcircled{2}} \rightarrow 2$ selection line.

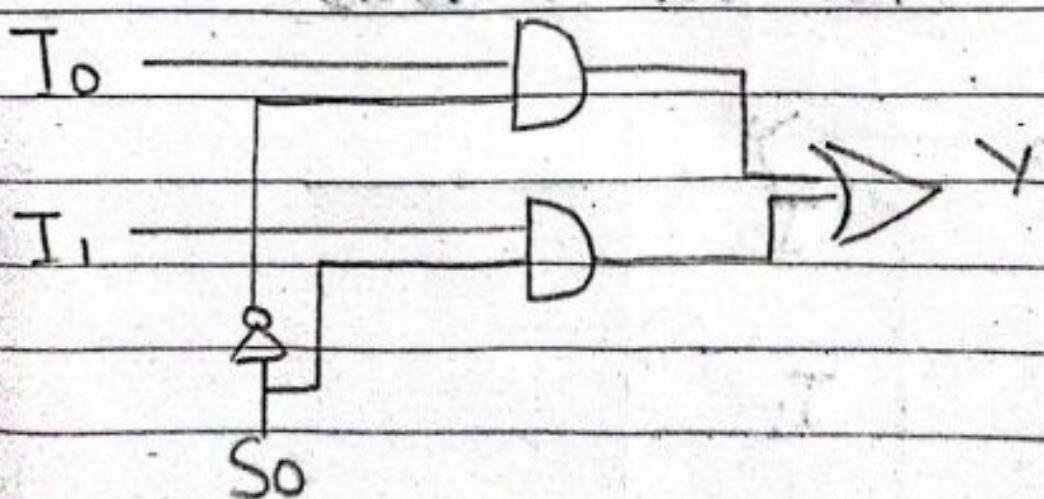
TRUTH TABLE:-

S_0	Y
0	T_0
1	T_1

logic expression

$$Y = \overline{S_0} T_0 + \overline{S_0} T_1$$

CIRCUIT DIAGRAM:-

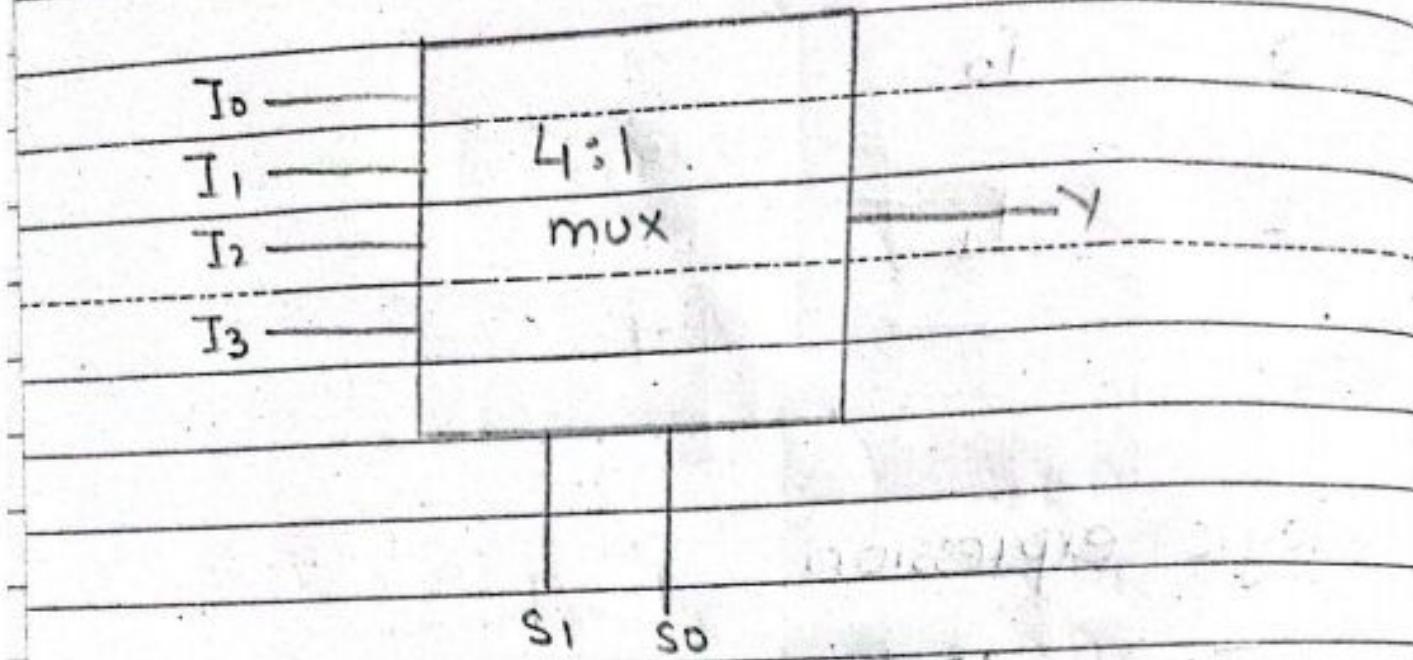


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4:1 MUX



inputs = 4 transmission lines

$\therefore 2^2 = 4$ lines required

TRUTH TABLE:-

S_1	S_0	Y	
0	0	I_0	
0	1	I_1	
1	0	I_2	
1	1	I_3	

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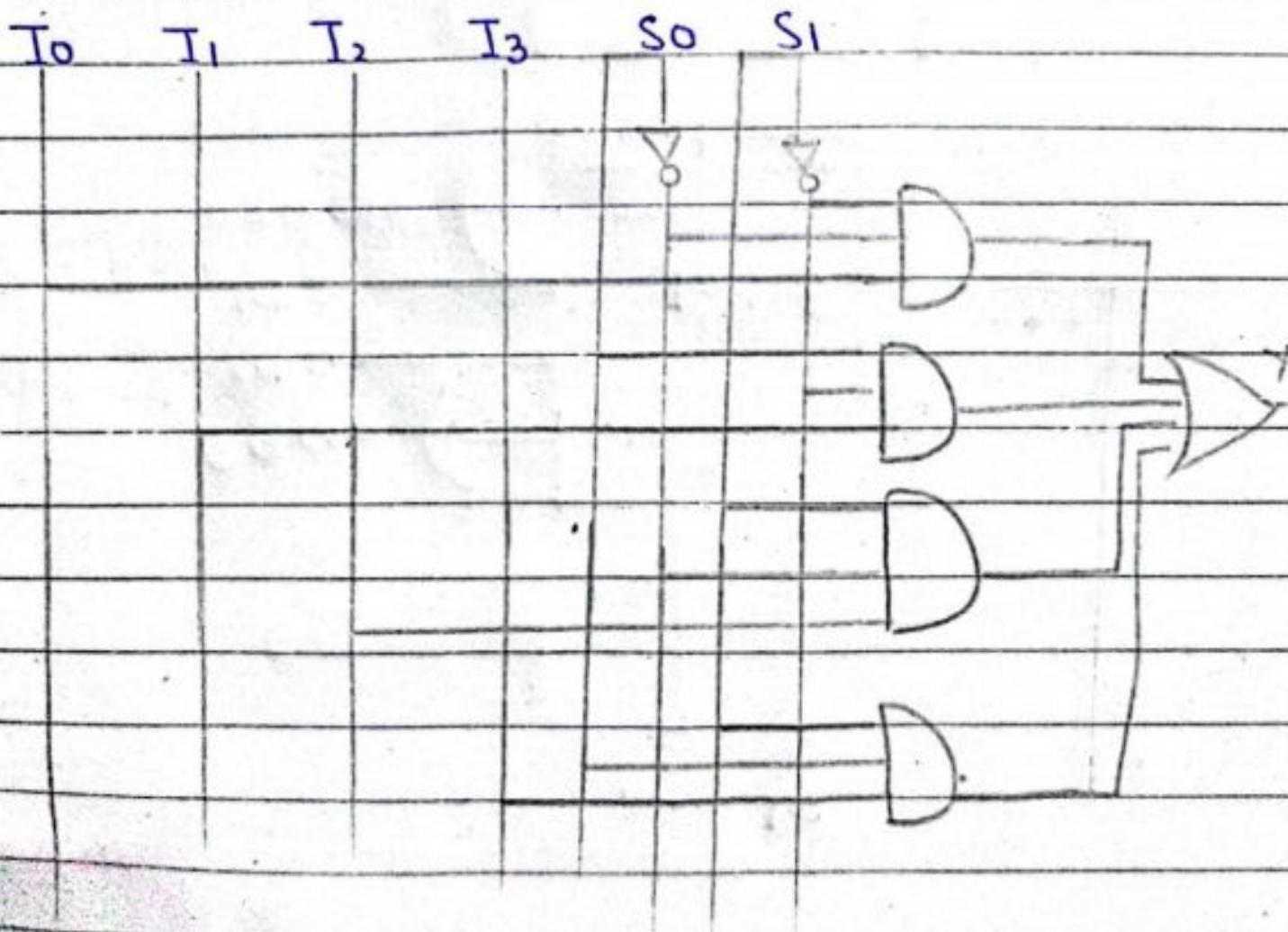
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LOGIC EXPRESSION:-

$$Y = \bar{S_0} \bar{S_1} I_0 + S_0 \bar{S_1} I_1 + \bar{S_0} S_1 I_2 + S_0 S_1 I_3$$

LOGIC DIAGRAM:-

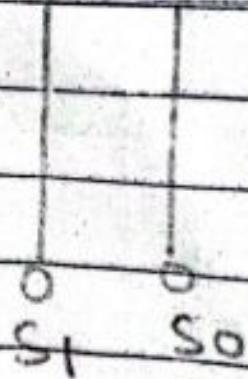
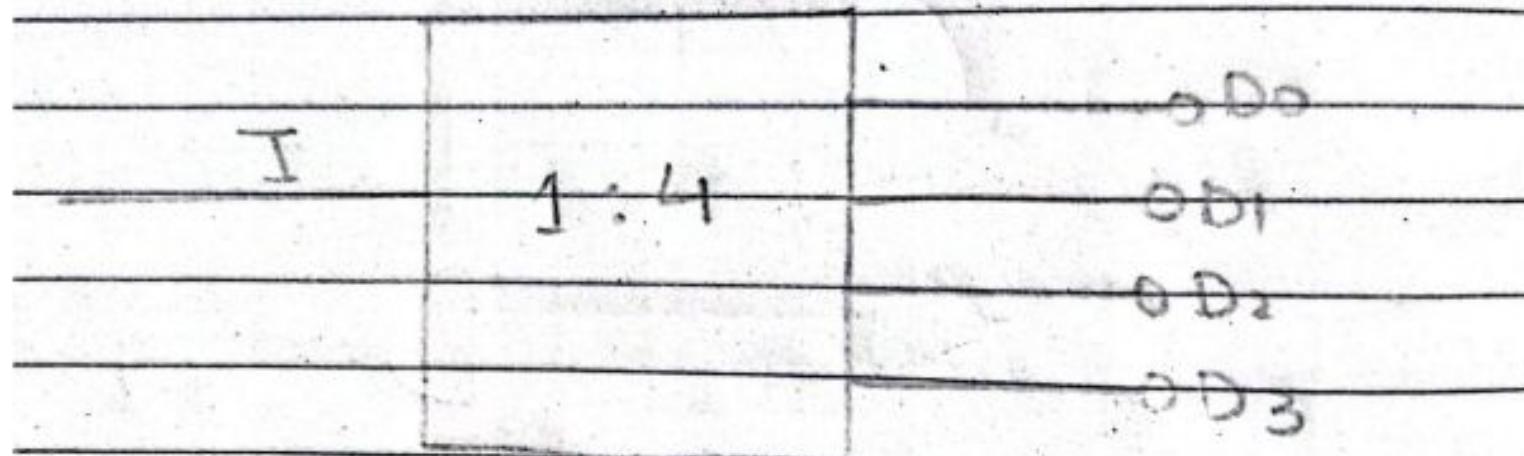
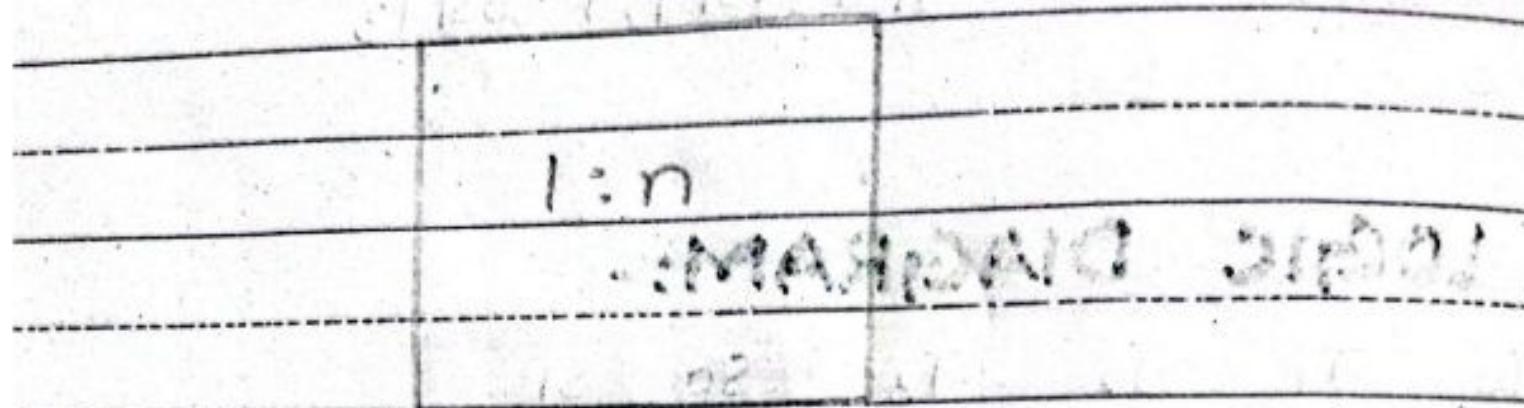


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D MUX:



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TRUTH TABLE :-

Input	S ₁	S ₀	D ₀	D ₁	D ₂	D ₃
I	0	0	1	0	0	0
I	0	1	0	1	0	0
I	1	0	0	0	1	0
I	1	1	0	0	0	1

LOGIC EXPRESSIONS

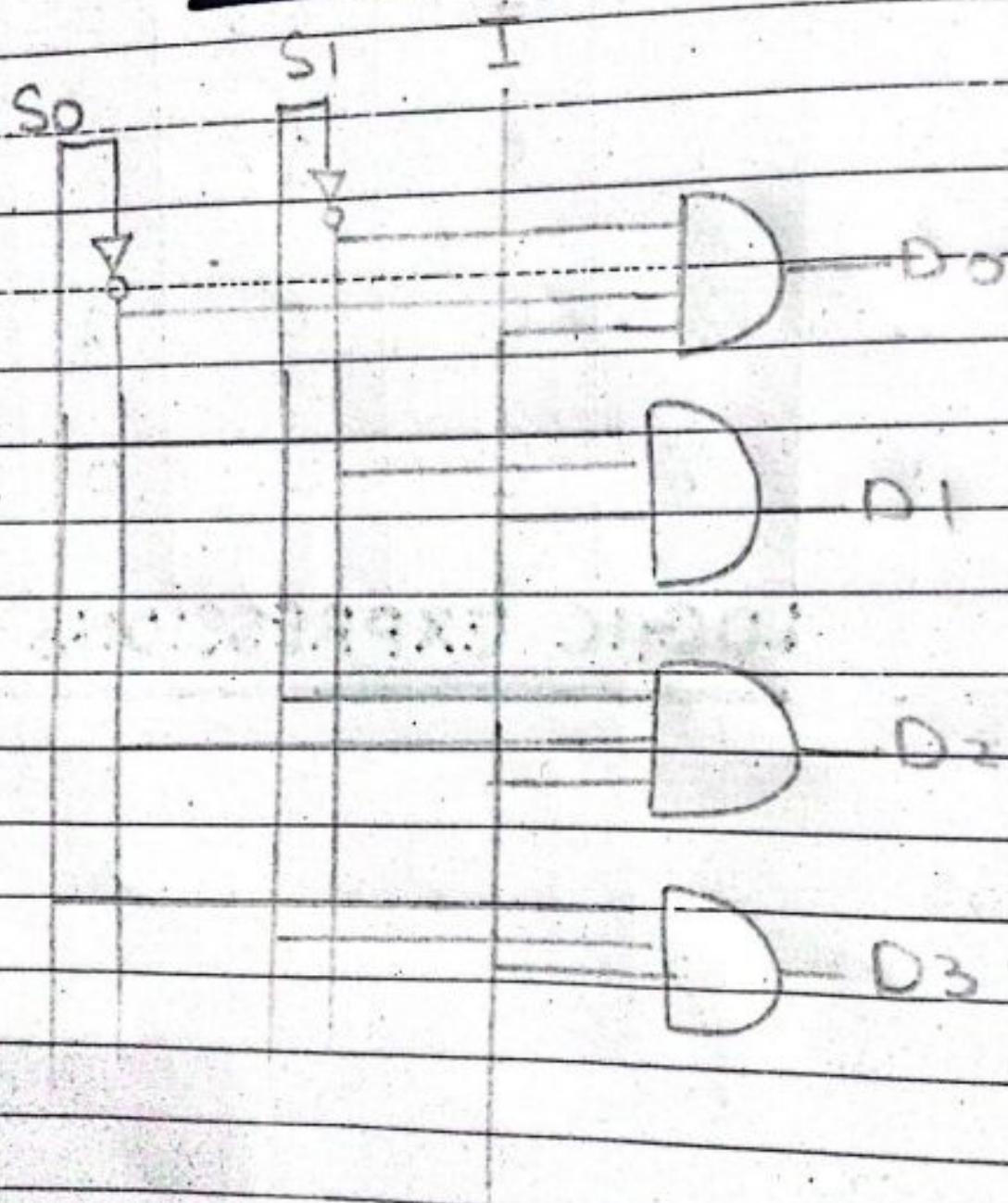
$$D_0 = \overline{S_0} \overline{S_1} I$$

$$D_1 = \overline{S_0} S_1 I$$

$$D_2 = S_0 \overline{S_1} I$$

$$D_3 = S_0 S_1 I$$

LOGIC DIAGRAM:

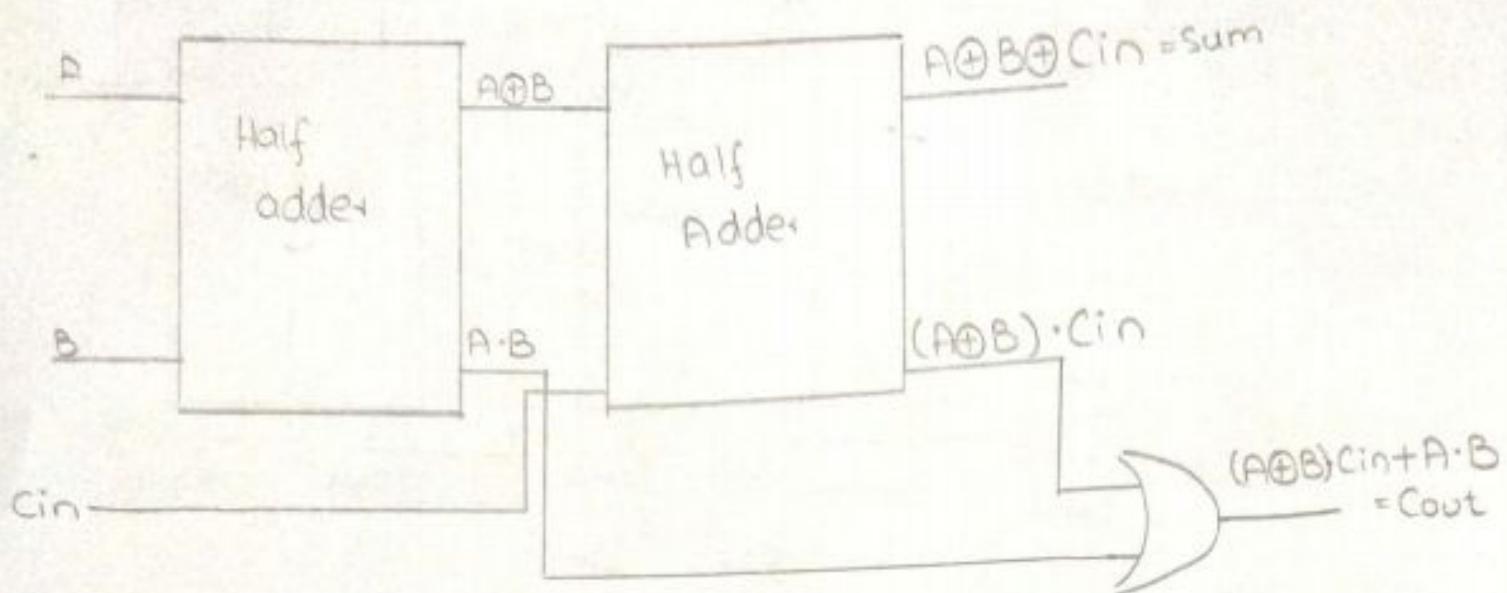


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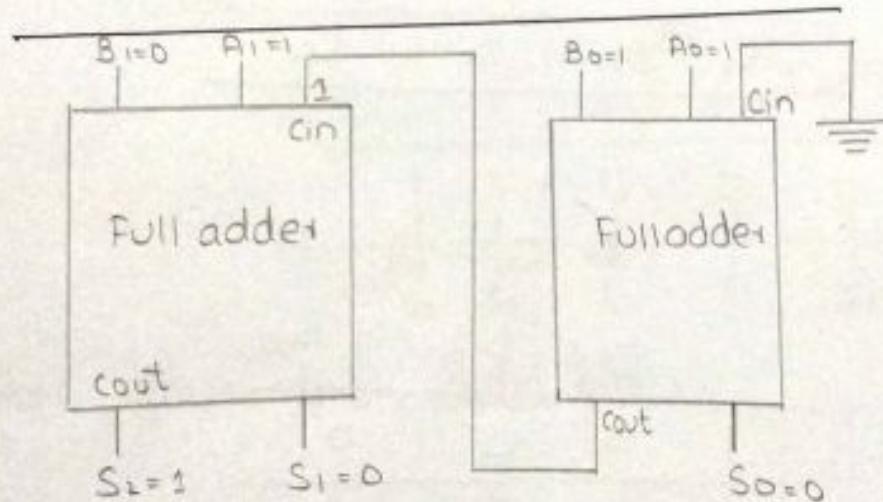
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⇒ constructing full adder by two half adders



⇒ Two bit parallel Adder:



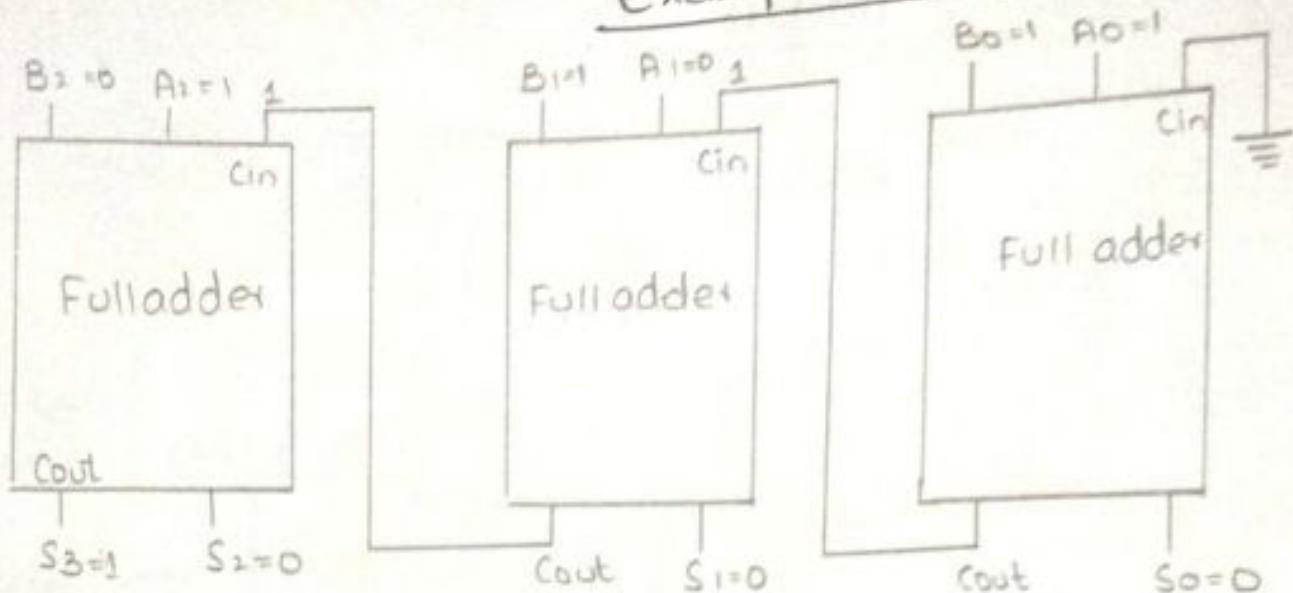
$$\begin{array}{r} A_1 \quad A_0 \\ + \quad B_1 \quad B_0 \\ \hline S_2 \quad S_1 \quad S_0 \end{array}$$

⇒ For two bit addition

$$\begin{array}{r} A_1 \leftarrow | \rightarrow A_0 \\ + B_1 \leftarrow 0 | \rightarrow B_0 \\ \hline 1 \quad 0 \quad 0 \end{array}$$

⇒ Three bit parallel adder

Example 6-2



$\frac{C_1}{A_2} \quad \frac{C_0}{A_1} \quad A_0$

$$\begin{array}{r} + \\ B_2 \quad B_1 \quad B_0 \\ \hline S_3 \quad S_2 \quad S_1 \quad S_0 \end{array}$$

| |

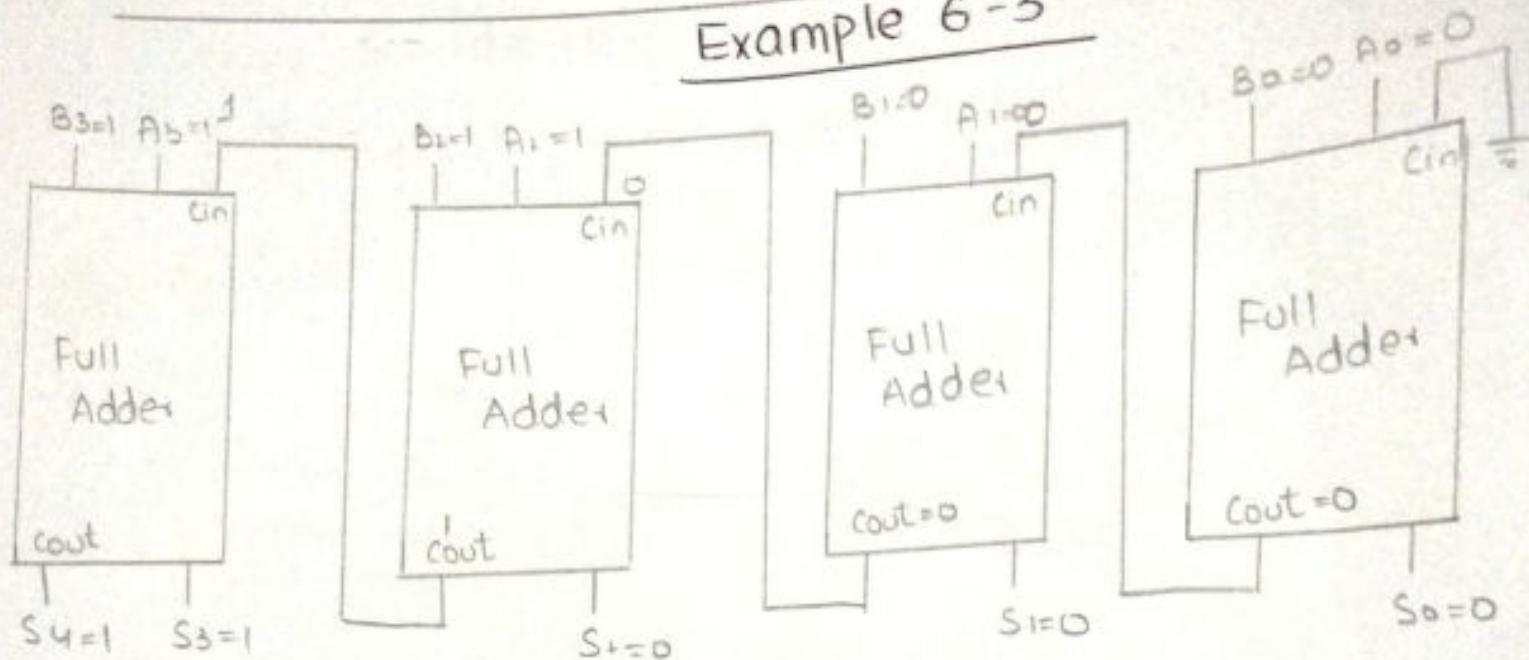
$| \rightarrow A_2 \quad 0 \rightarrow A_1 \quad | \rightarrow A_0$

$$\begin{array}{r} + \\ 0 \rightarrow B_2 \quad 0 \rightarrow B_1 \quad 0 \rightarrow B_0 \\ \hline \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \\ S_3 \quad S_2 \quad S_1 \quad S_0 \end{array}$$

⇒ for three bit addition

Four bit parallel adder

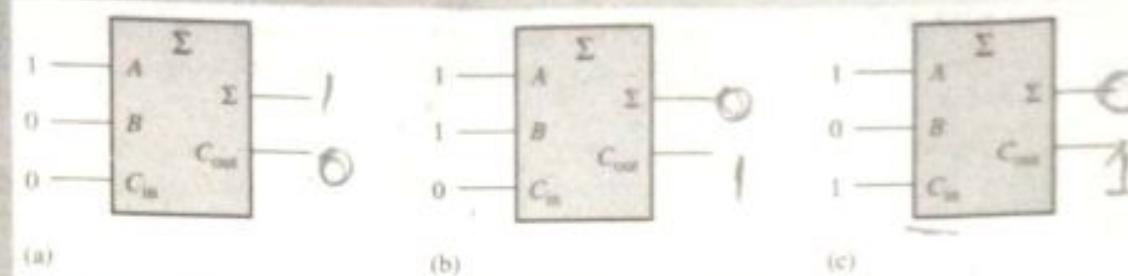
Example 6-3



$$\begin{array}{r}
 & A_3 & A_2 & A_1 & A_0 \\
 & | & | & | & | \\
 + & B_3 & B_2 & B_1 & B_0 \\
 \hline
 & S_4 & S_3 & S_2 & S_1 & S_0
 \end{array}$$

=> For four bit addition

For each of the three full-adders in Figure 6–6, determine the outputs for the inputs shown.



Solution (a) The input bits are $A = 1$, $B = 0$, and $C_{in} = 0$.

$$\begin{array}{r} 1 \\ + 0 \\ + 0 \\ \hline 1 \end{array} \text{ with no carry}$$

Therefore, $\Sigma = 1$ and $C_{out} = 0$.

(b) The input bits are $A = 1$, $B = 1$, and $C_{in} = 0$.

$$\begin{array}{r} 1 \\ + 1 \\ + 0 \\ \hline 0 \end{array} \text{ with a carry of 1}$$

Therefore, $\Sigma = 0$ and $C_{out} = 1$.

(c) The input bits are $A = 1$, $B = 0$, and $C_{in} = 1$.

$$\begin{array}{r} 1 \\ + 0 \\ + 1 \\ \hline 0 \end{array} \text{ with a carry of 1}$$

Therefore, $\Sigma = 0$ and $C_{out} = 1$.

Related Problem* What are the full-adder outputs for $A = 1$, $B = 1$, and $C_{in} = 1$?

*Answers are at the end of the chapter. $\Sigma = 1$ $C = 1$

at the end of the

1. Determine the sum (Σ) and the output carry (C_{out}) of a half-adder for each set of input bits:

$$\begin{array}{cccc} (a) 01 & (b) 00 & (c) 10 & (d) 11 \end{array}$$

$$\begin{array}{cccc} \Sigma = 0 & \Sigma = 0 & \Sigma = 0 & \Sigma = 0 \\ C = 0 & C = 0 & C = 0 & C = 1 \end{array}$$

2. A full-adder has $C_{in} = 1$. What are the sum (Σ) and the output carry (C_{out}) when $A = 1$ and $B = 1$?

$$\begin{array}{l} \Sigma = 1 \\ C_{out} = 1 \end{array}$$

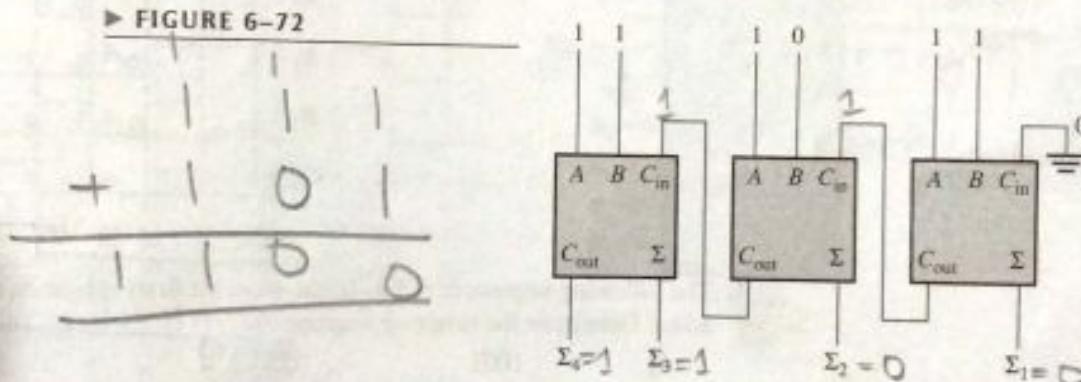
Section 6-1 Basic Adders

1. For the full-adder of Figure 6-4, determine the logic state (1 or 0) at each gate output for the following inputs:
- $A = 1, B = 1, C_{in} = 1 \Rightarrow S = 1 = C = 1$
 - $A = 0, B = 1, C_{in} = 1 \Rightarrow S = 0 = C = 1$
 - $A = 0, B = 1, C_{in} = 0 \Rightarrow S = 1 = C = 0$
2. What are the full-adder inputs that will produce each of the following outputs?
- $\Sigma = 0, C_{out} = 0 \rightarrow A = 0, B = 0, C_{in} = 0$
 - $\Sigma = 1, C_{out} = 0 \rightarrow A = 0, B = 1, C_{in} = 0$
 - $\Sigma = 1, C_{out} = 1 \rightarrow A = 1, B = 1, C_{in} = 0$
 - $\Sigma = 0, C_{out} = 1 \rightarrow A = 1, B = 1, C_{in} = 1$
3. Determine the outputs of a full-adder for each of the following inputs:
- $A = 1, B = 0, C_{in} = 0 \Rightarrow S = 1, C = 0$
 - $A = 0, B = 0, C_{in} = 1 \Rightarrow S = 1, C = 0$
 - $A = 0, B = 1, C_{in} = 1 \Rightarrow S = 0, C = 1$
 - $A = 1, B = 1, C_{in} = 1 \Rightarrow S = 1, C = 1$

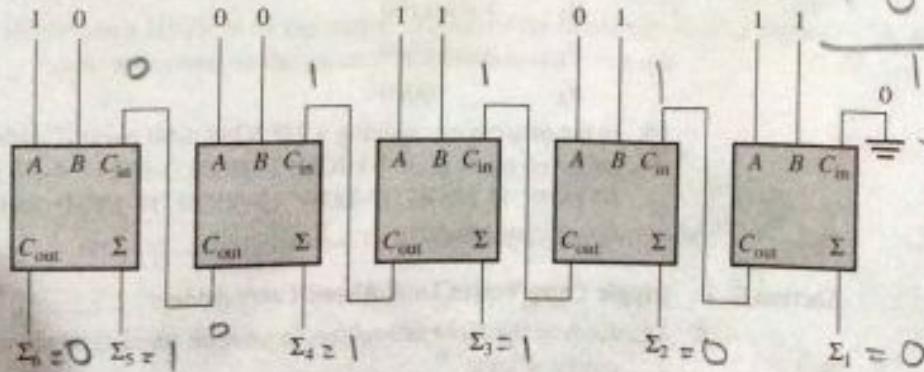
Section 6-2 Parallel Binary Adders

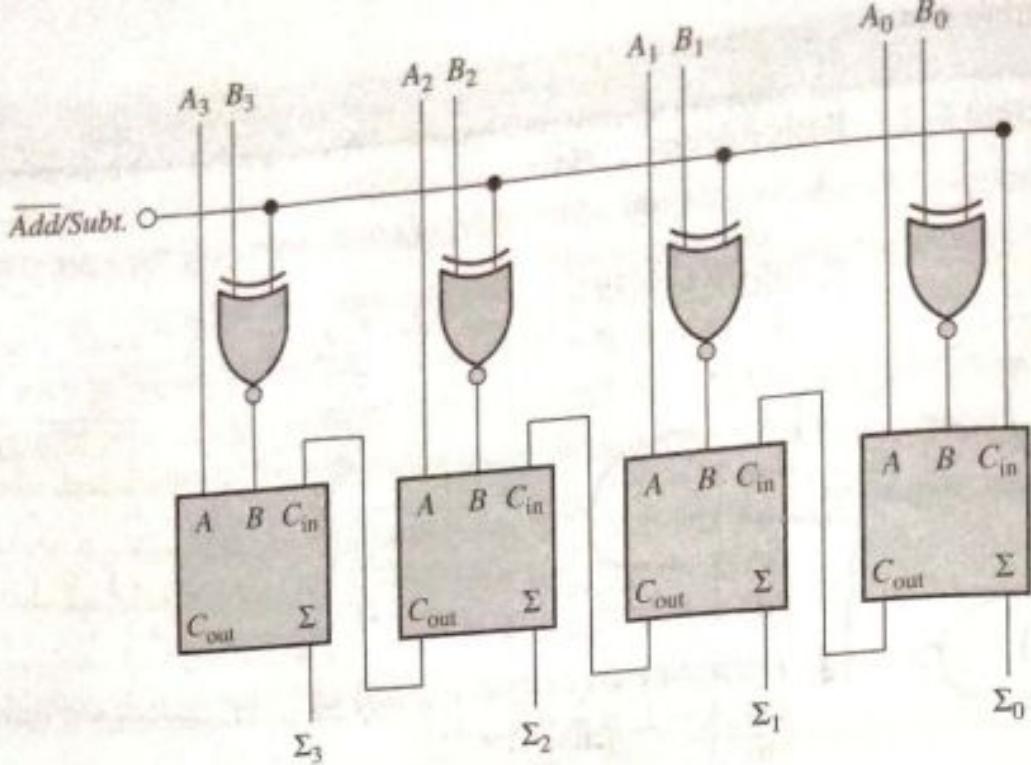
4. For the parallel adder in Figure 6-72, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers.

► FIGURE 6-72



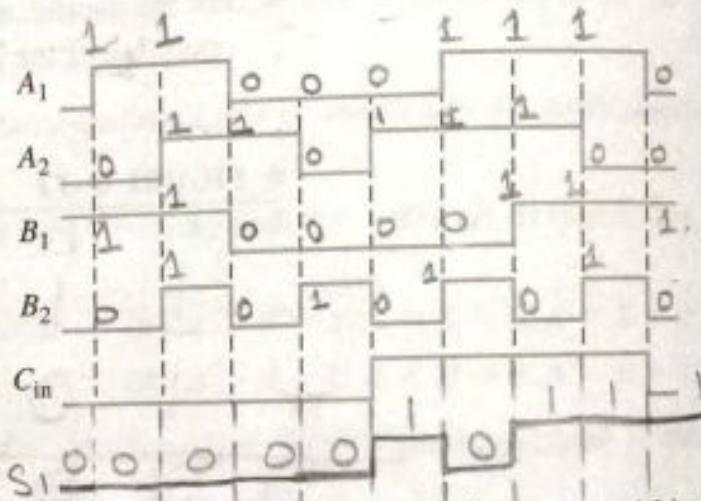
5. Repeat Problem 4 for the circuit and input conditions in Figure 6-73.





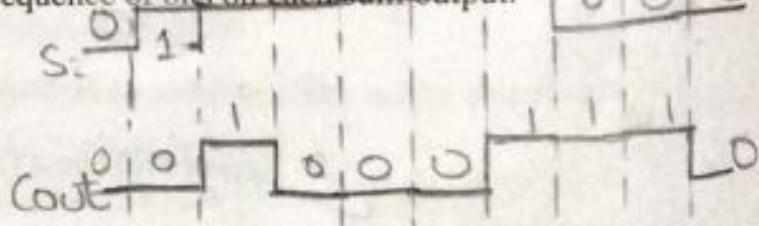
8. The input waveforms in Figure 6-75 are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.

► FIGURE 6-75



9. The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder. Determine the resulting sequence of bits on each sum output.

A_1	1001
A_2	1110
A_3	0000
A_4	1011
B_1	1111
B_2	1100
B_3	1010
B_4	0010



10. In the process of checking a 74LS283 4-bit parallel adder, the following logic levels are observed on its pins: 1-HIGH, 2-HIGH, 3-HIGH, 4-HIGH, 5-LOW, 6-LOW, 7-LOW, 9-HIGH, 10-LOW, 11-HIGH, 12-LOW, 13-HIGH, 14-HIGH, and 15-HIGH. Determine if the IC is functioning properly.

LE 6-3

Use the 4-bit parallel adder truth table (Table 6-3) to find the sum and output carry for the addition of the following two 4-bit numbers if the input carry (C_{n-1}) is 0:

$$A_4 A_3 A_2 A_1 = 1100 \quad \text{and} \quad B_4 B_3 B_2 B_1 = 1100$$

Solution For $n = 1$: $A_1 = 0$, $B_1 = 0$, and $C_{n-1} = 0$. From the 1st row of the table,

$$\Sigma_1 = 0 \quad \text{and} \quad C_1 = 0$$

For $n = 2$: $A_2 = 0$, $B_2 = 0$, and $C_{n-1} = 0$. From the 1st row of the table,

$$\Sigma_2 = 0 \quad \text{and} \quad C_2 = 0$$

For $n = 3$: $A_3 = 1$, $B_3 = 1$, and $C_{n-1} = 0$. From the 4th row of the table,

$$\Sigma_3 = 0 \quad \text{and} \quad C_3 = 1$$

For $n = 4$: $A_4 = 1$, $B_4 = 1$, and $C_{n-1} = 1$. From the last row of the table,

$$\Sigma_4 = 1 \quad \text{and} \quad C_4 = 1$$

C_4 becomes the output carry; the sum of 1100 and 1100 is 11000.

Related Problem

Use the truth table (Table 6-3) to find the result of adding the binary numbers 1011 and 1010.

$$\begin{array}{r} A_3 \leftarrow 1 \ 0 \ | \ 1 \rightarrow A_0 \\ + B_3 \leftarrow 1 \ 0 \ | \ 0 \rightarrow B_0 \\ \hline \end{array}$$

$$\begin{array}{r} B_3 \leftarrow 1 \ 0 \ | \ 0 \rightarrow B_0 \\ + B_3 \leftarrow 1 \ 0 \ | \ 0 \rightarrow B_0 \\ \hline \end{array}$$

$$\begin{array}{r} 1 \ 0 \ | \ 1 \ 0 \ | \ 1 \ 1 \rightarrow S_0 \\ + 1 \ 0 \ | \ 0 \ | \ 0 \rightarrow S_0 \\ \hline S_4 \ S_3 \ S_2 \ S_1 \ S_0 \end{array}$$

74LS283 4-BIT PARALLEL ADDER

An example of a 4-bit parallel adder that is available in IC form is the 74LS283. For the

ripple carry adder. The look-ahead carry operation is internal to each MSI adder and the ripple carry feature comes into play when there is a carry out of one of the adders to the next one.

SECTION 6-3 CHECKUP

1. The input bits to a full-adder are $A = 1$ and $B = 0$. Determine C_g and C_p .
2. Determine the output carry of a full-adder when $C_{in} = 1$, $C_g = 0$, and $C_p = 1$.

$$C_g = A \cdot B \\ = 1 \cdot 0 \\ C_g = 0$$

$$C_p = A + B \\ C_p = 1 + 0 \\ C_p = 1$$

6-4 COMPARATORS

The basic function of a comparator is to compare the magnitudes of two binary quantities to determine the relationship of those quantities. In its simplest form, a comparator circuit determines whether two numbers are equal.

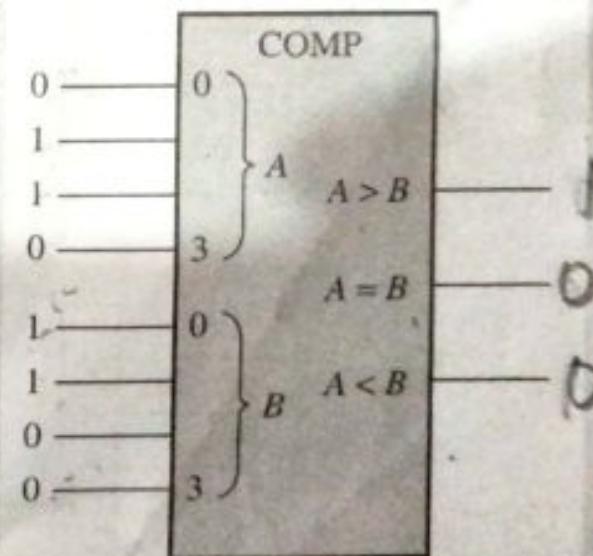
$$Cout = Cg + Cp Cin = Cout \cdot 0 + 1 \cdot 1$$

$$\boxed{Cout = 1}$$

EXAMPLE 6-6

Determine the $A = B$, $A > B$, and $A < B$ outputs for the input numbers shown on the comparator in Figure 6-23.

► FIGURE 6-23



- FUNCTIONS OF COMBINATIONAL LOGIC

Solution The number on the A inputs is 0110 and the number on the B inputs is 0011. The **$A > B$ output is HIGH and the other outputs are LOW.**

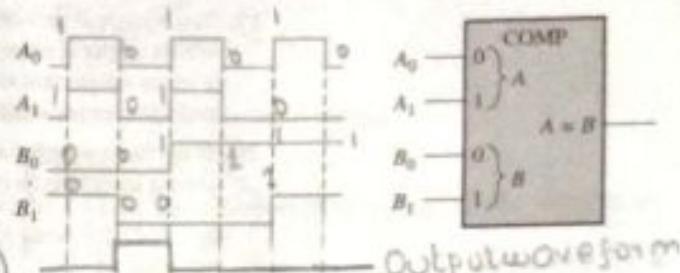
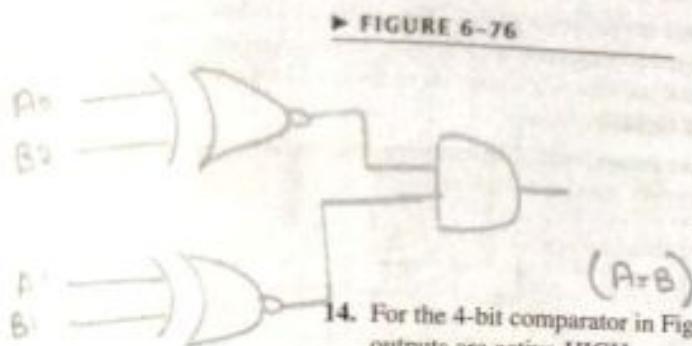
Related Problem What are the comparator outputs when $A_3A_2A_1A_0 = \underline{1001}$ and $B_3B_2B_1B_0 = \underline{1010}$?

$B > A = \text{out}_P$

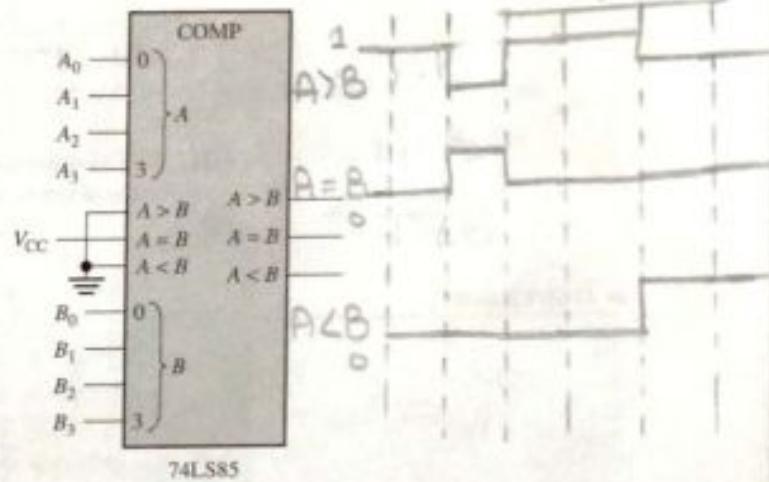
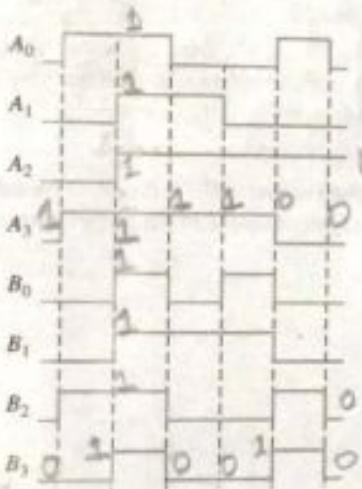
E 74LS85 4-BIT MAGNITUDE COMPARATOR

Section 6-4 Comparators

13. The waveforms in Figure 6-76 are applied to the comparator as shown. Determine the output ($A = B$) waveform.



14. For the 4-bit comparator in Figure 6-77, plot each output waveform for the inputs shown. The outputs are active-HIGH.

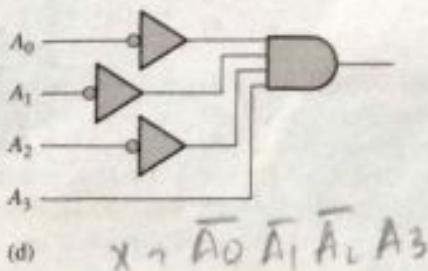
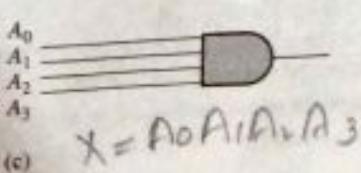
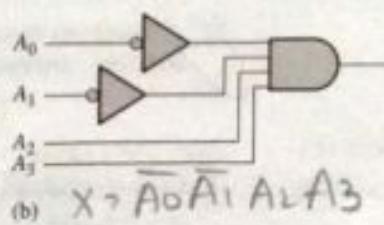
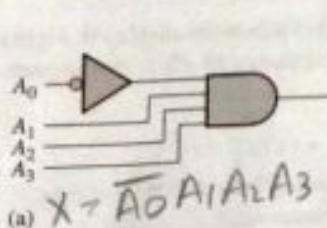


15. For each set of binary numbers, determine the output states for the comparator of Figure 6-22:

$$(A > B) \leftarrow \begin{array}{lll} (a) A_3 A_2 A_1 A_0 = 1100 & (b) A_3 A_2 A_1 A_0 = 1000 & (c) A_3 A_2 A_1 A_0 = 0100 \\ B_3 B_2 B_1 B_0 = 1001 & B_3 B_2 B_1 B_0 = 1011 & B_3 B_2 B_1 B_0 = 0100 \end{array}$$

Section 6-5 Decoders

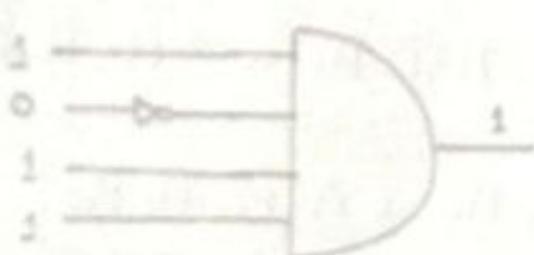
16. When a HIGH is on the output of each of the decoding gates in Figure 6-78, what is the binary code appearing on the inputs? The MSB is A_3 .



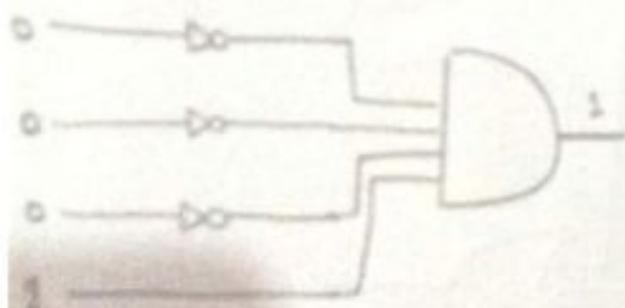
Q-17

Show the decoding logic if an active high output is required. Q-18

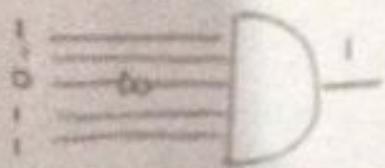
(a) $\overline{A_3} \overline{A_2} \overline{A_1} \overline{A_0}$



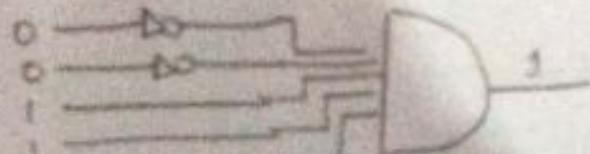
(b) $\overline{A_3} \overline{A_2} \overline{A_1} \overline{A_0}$



(c) $\overline{A_3} \overline{A_2} \overline{A_1} \overline{A_0}$

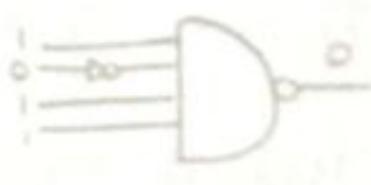


(d) $\overline{A_3} \overline{A_2} \overline{A_1} \overline{A_0}$



active low output

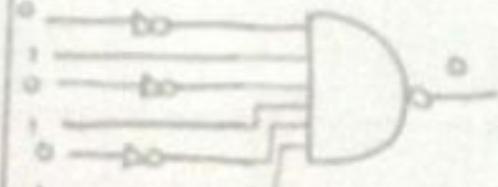
(a) $1 \ 1 \ 0 \ 1$



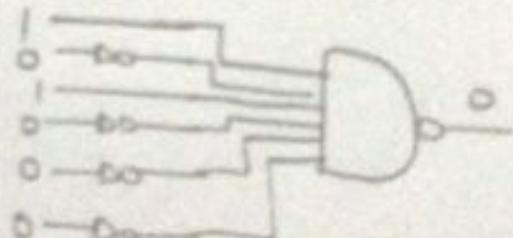
(b) $1 \ 0 \ 0 \ 0$



(e) $1 \ 0 \ 1 \ 0 \ 1 \ 0$



(g) $0 \ 0 \ 0 \ 1 \ 0 \ 1$

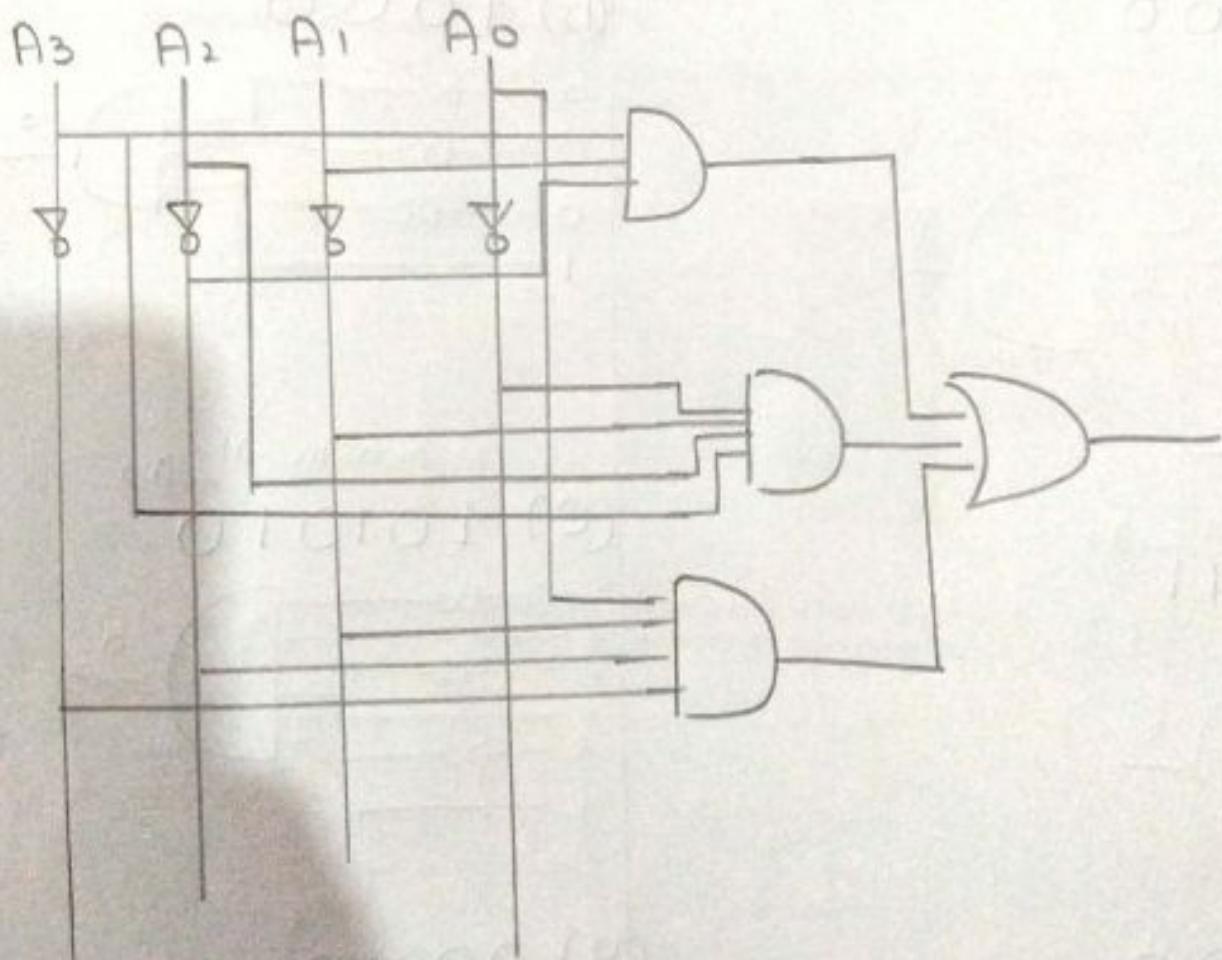


Q.19

$$X = A_3 \bar{A}_2 A_1 \bar{A}_0 + A_3 A_2 \bar{A}_1 \bar{A}_0 + \bar{A}_3 \bar{A}_2 \bar{A}_1 A_0 \\ + A_3 \bar{A}_2 A_1 A_0$$

$$X = A_3 \bar{A}_2 A_1 (\bar{A}_0 + A_0) + A_3 A_2 \bar{A}_1 \bar{A}_0 + \bar{A}_3 \bar{A}_2 \bar{A}_1 A_0$$

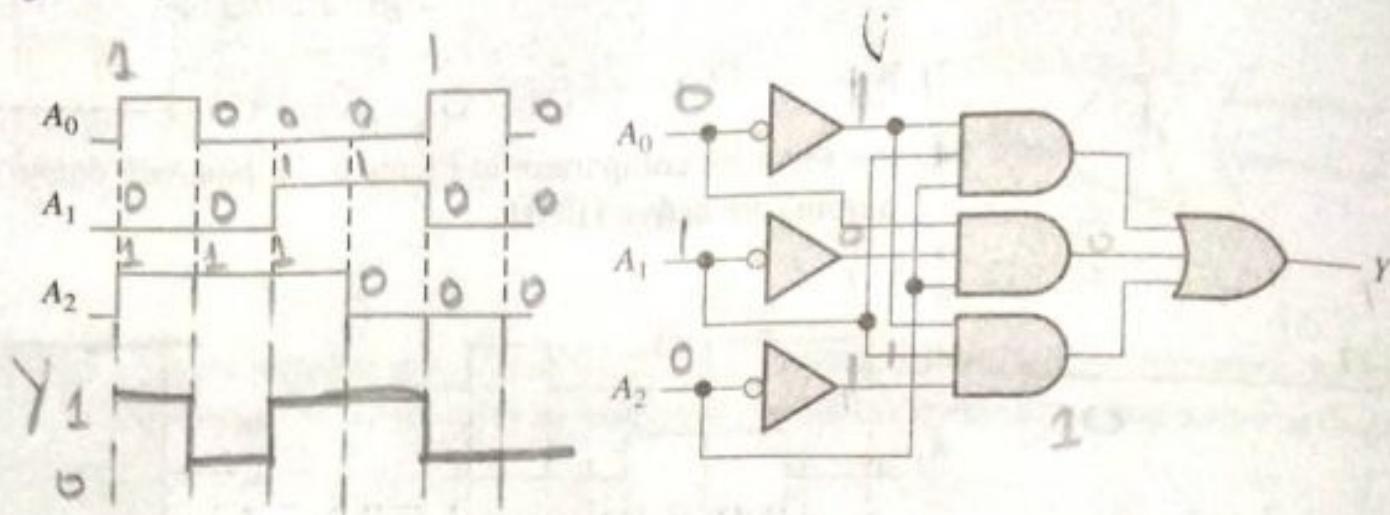
$$X = A_3 \bar{A}_2 A_1 + A_3 A_2 \bar{A}_1 \bar{A}_0 + \bar{A}_3 \bar{A}_2 \bar{A}_1 A_0$$



code, the output must be LOW.

20. If the input waveforms are applied to the decoding logic as indicated in Figure 6-79, sketch the output waveform in proper relation to the inputs.

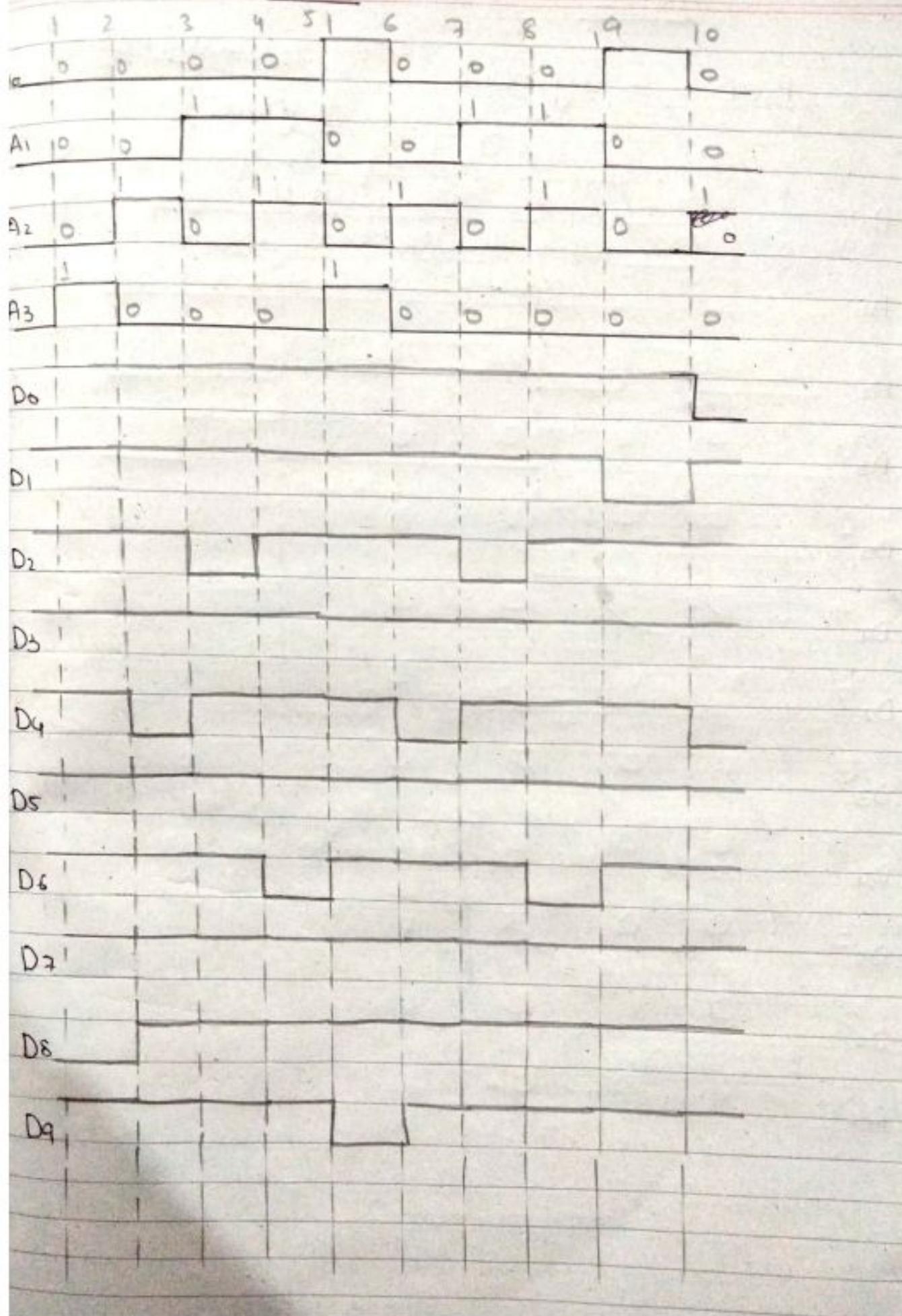
► FIGURE 6-79



21. BCD numbers are applied sequentially to the BCD-to-decimal decoder in Figure 6-80. Draw a

\Rightarrow BCD - Decimal
decoder Q-21

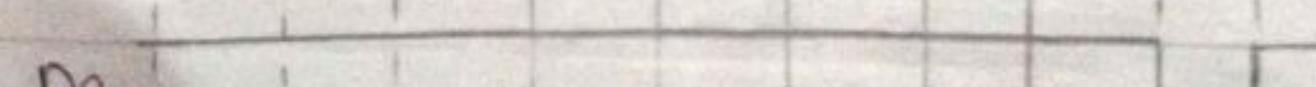
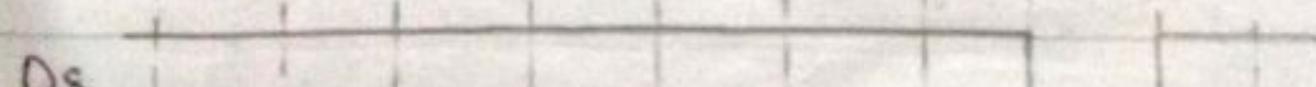
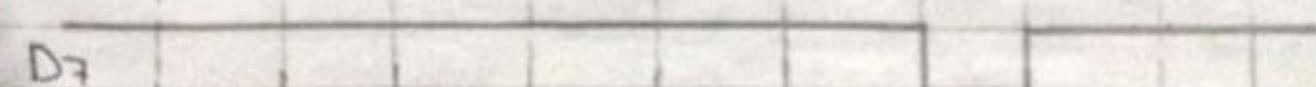
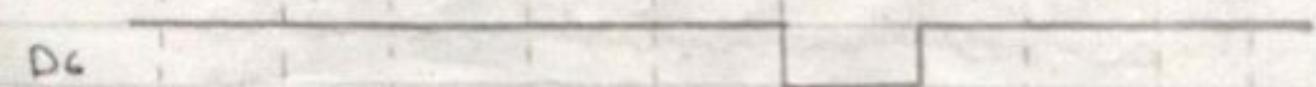
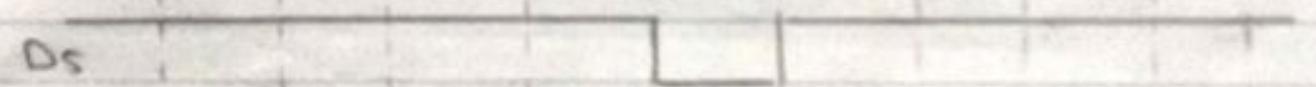
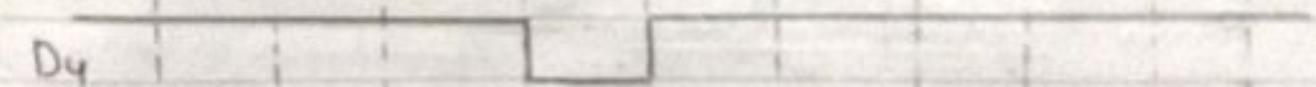
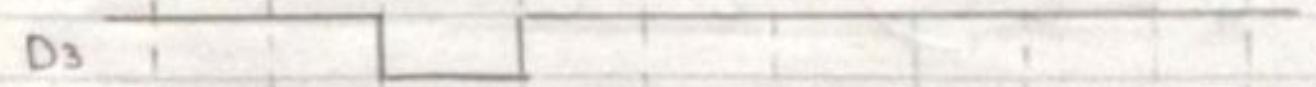
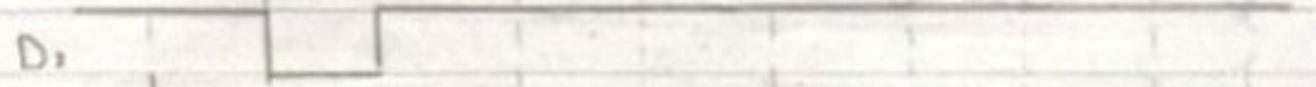
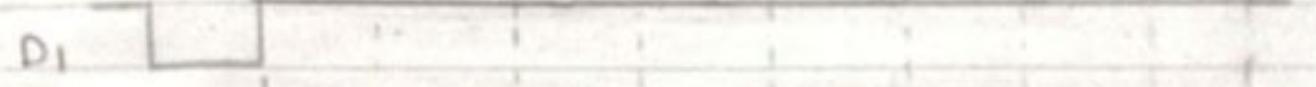
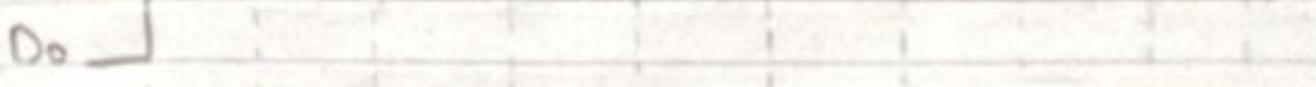
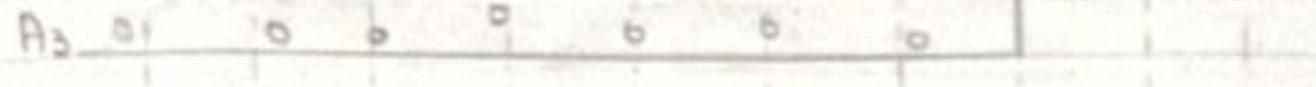
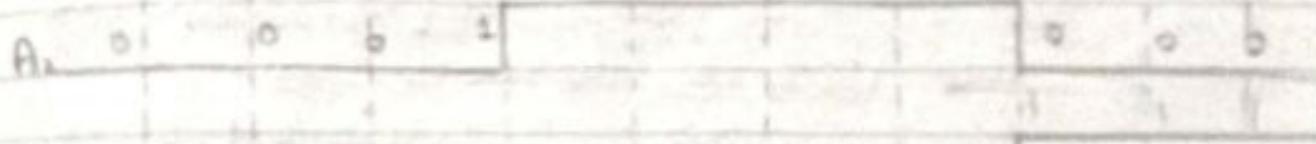
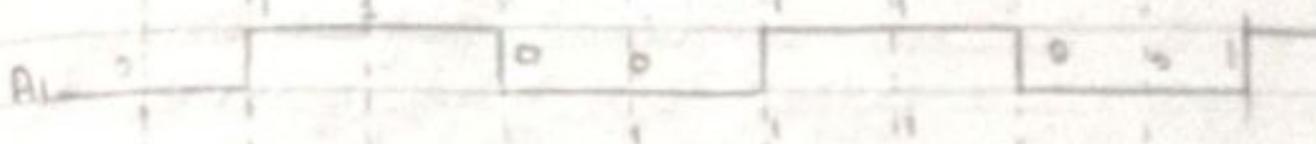
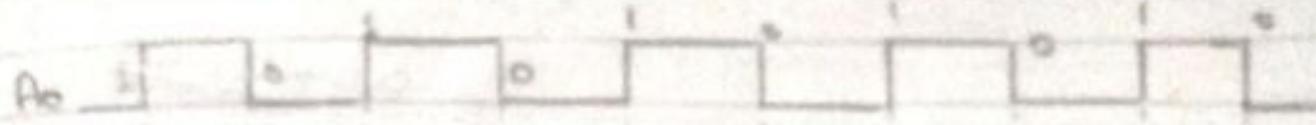
8 4 2 1
A₃ A₂ A₁ A₀



BCD - Decimal

8 4 2 1

Example 6-10



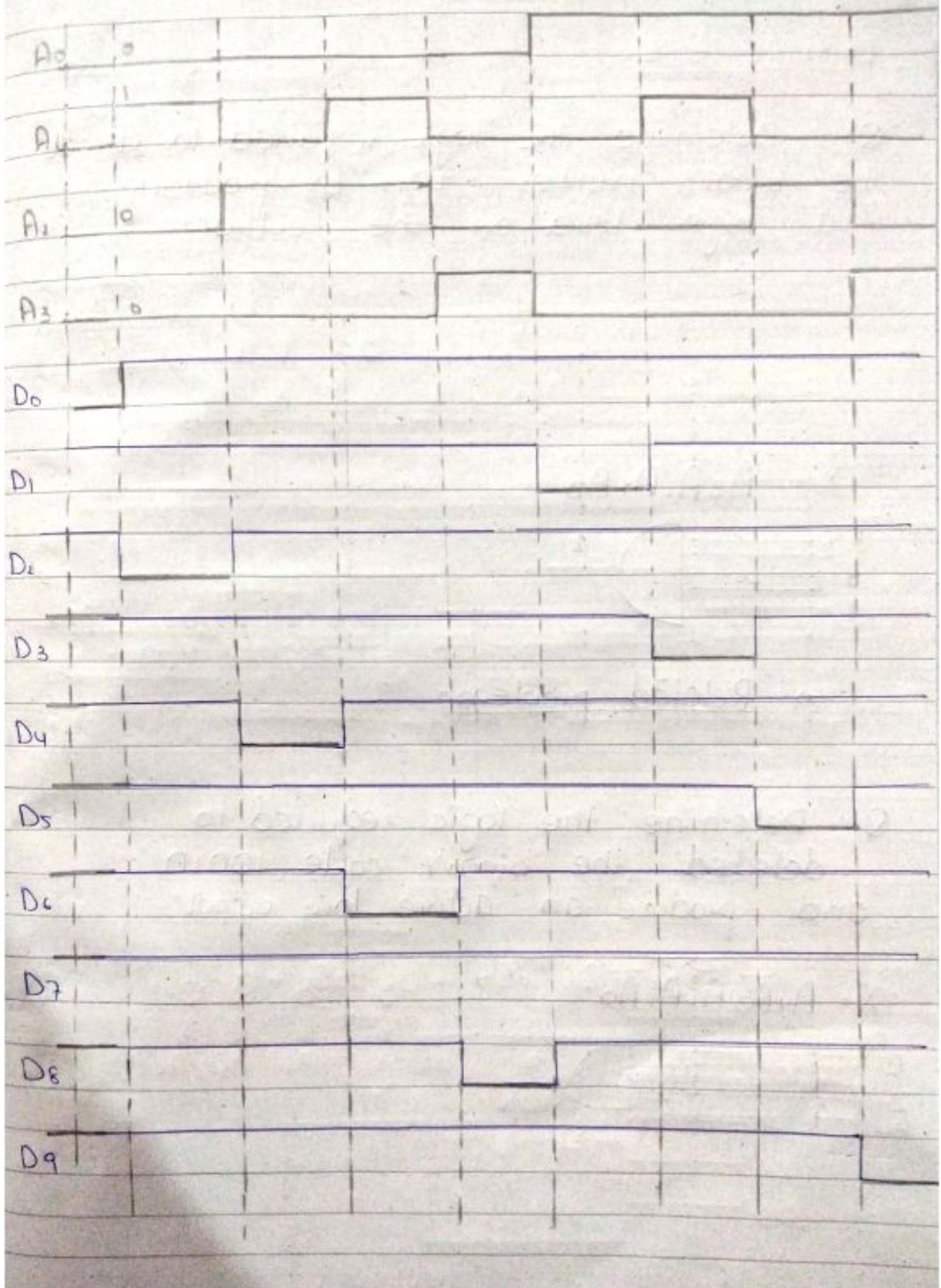
6-10 Related problem-

 $\Rightarrow \text{BCD} \rightarrow \text{Decimal}$

\Rightarrow Q. construct a timing diagram showing input and output waveforms for the case where the BCD inputs sequence through the decimal numbers as follows: 0, 2, 4, 6, 8, 1, 3, 5, 9

Decimal	A ₃	A ₂	A ₁	A ₀	
0	0	0	0	0	
2	0	0	1	0	
4	0	1	0	0	
6	0	1	1	0	
8	1	0	0	0	
1	0	0	0	1	
3	0	0	1	1	
5	0	1	0	1	
9	1	0	0	1	

Timing diagram



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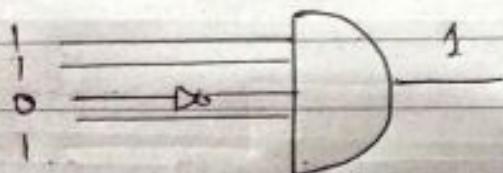
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Example 6-8

Q. Determine the logic required to decode the binary number 1011 by producing a - high level on the output.

1 0 1 1
A₃ A₂ A₁ A₀

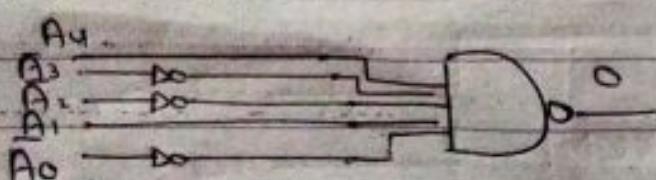
$$X = A_3 \bar{A}_2 A_1 A_0$$



=> Related problem:

Q. Determine the logic required to detect the binary code 10010 and produce an active low output.

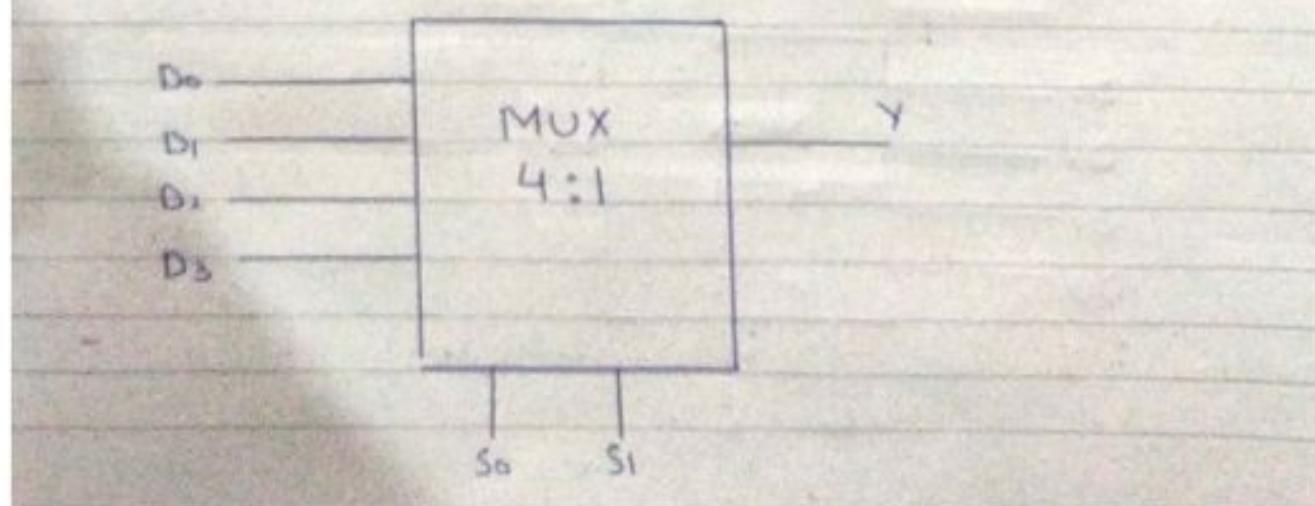
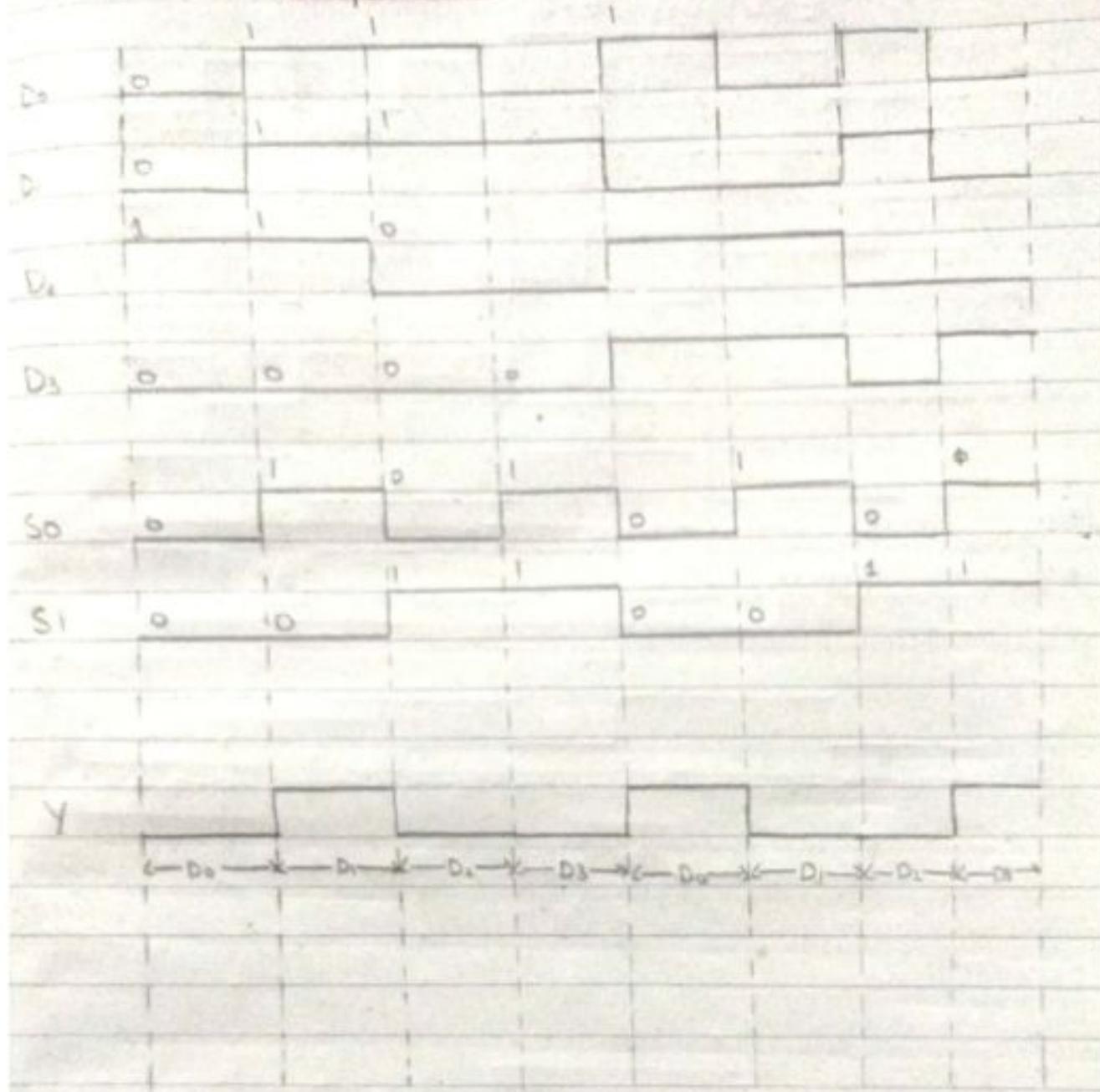
$$X = A_4 \bar{A}_3 \bar{A}_2 A_1 \bar{A}_0$$



1 0 0 1 0
↓ ↓ ↓ ↓ ↓
A₄ A₃ A₂ A₁ A₀

(MUX)

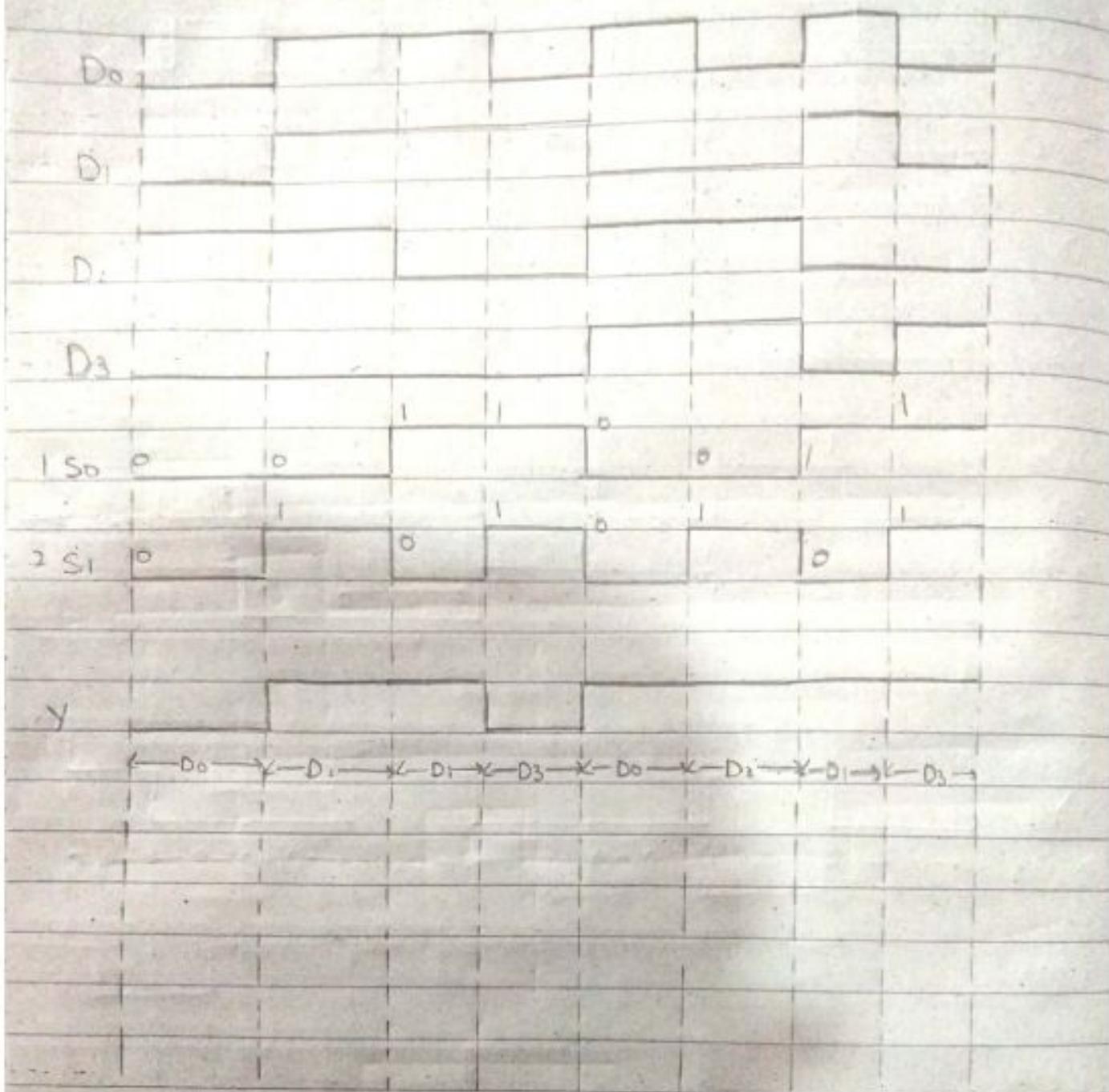
Example 6-14



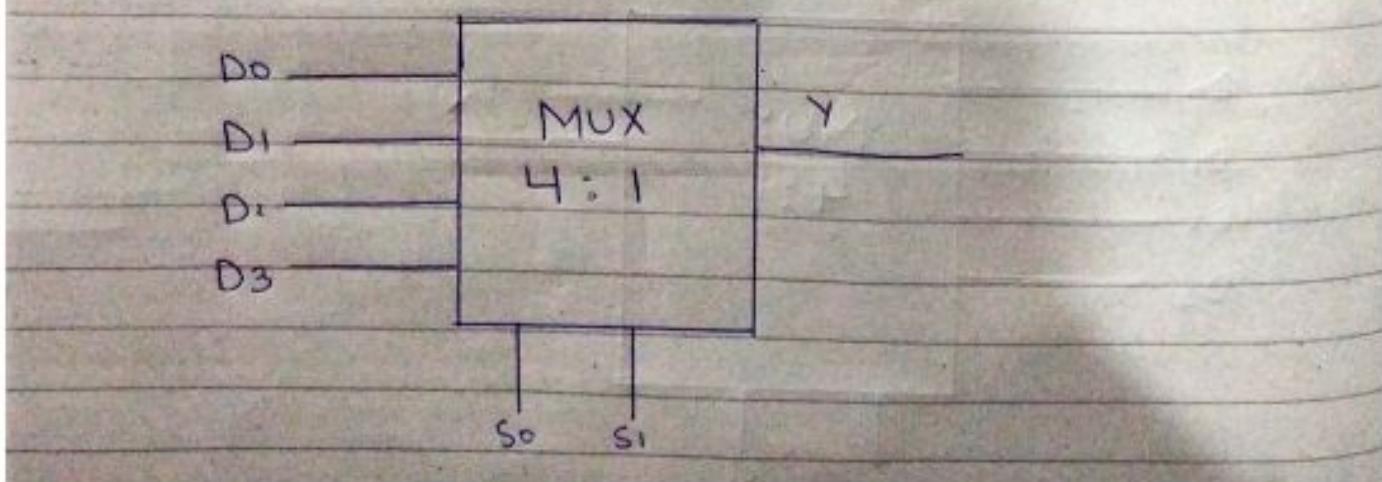
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Related problem 6.14



$$Y = D_0 \bar{S}_0 \bar{S}_1 + D_1 \bar{S}_0 S_1 + D_2 S_0 \bar{S}_1 + D_3 S_0 S_1$$

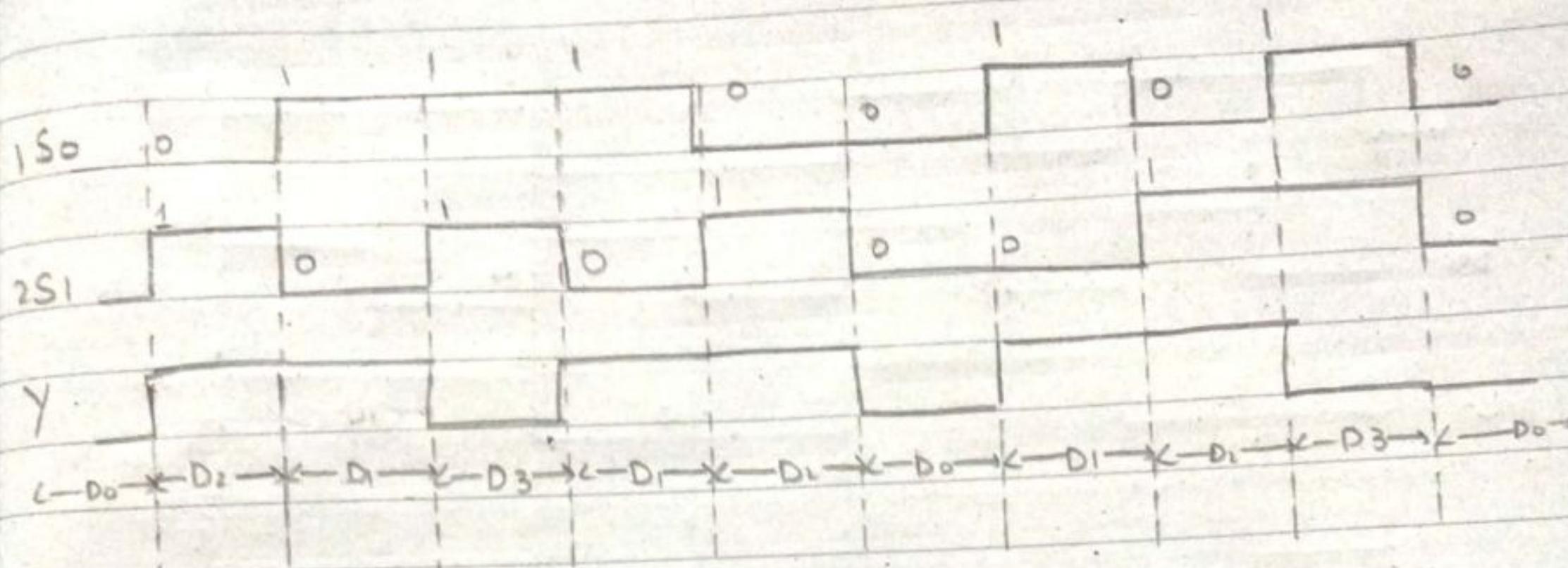


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Q.29

$$D_0 = 0, D_1 = 1, \\ D_2 = 1, D_3 = 0$$



(a) 110100000000 (b) 0011001100 (c) 111100000000

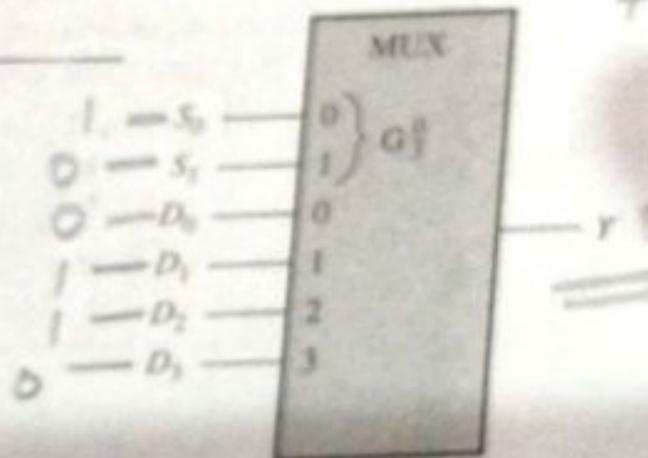
Section 6-8 Multiplexers (Data Selectors)

28. For the multiplexer in Figure 6-82, determine the output for the following input states:

$$D_0 = 0, D_1 = 1, D_2 = 1, D_3 = 0, S_0 = 1, S_1 = 0.$$

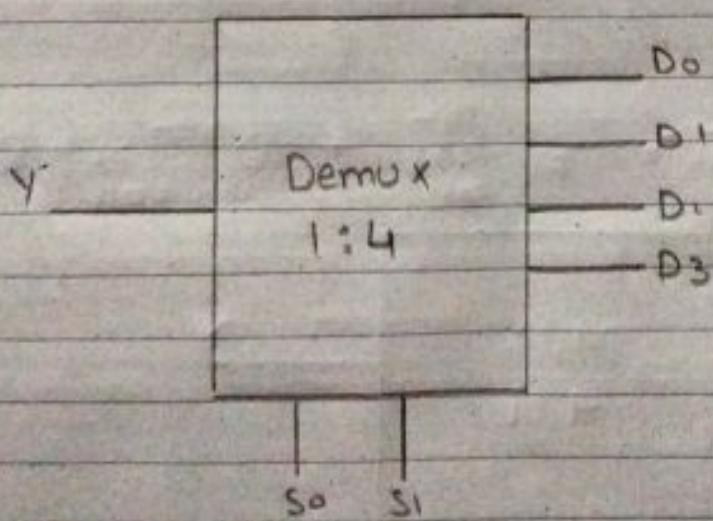
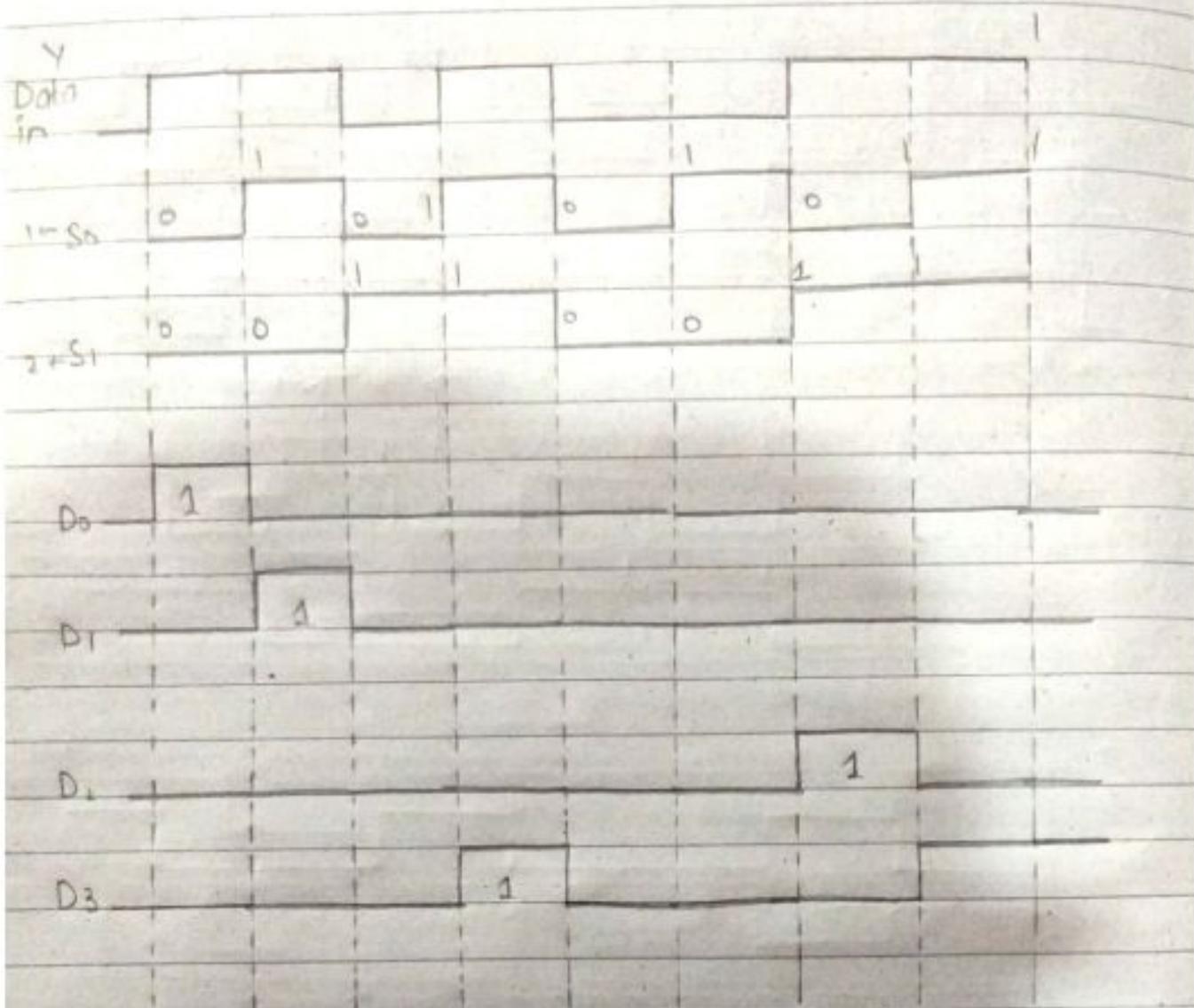
$$\begin{aligned} Y &= D_0 \bar{S}_0 \bar{S}_1 + D_1 \bar{S}_1 S_0 \\ &\quad + D_2 \bar{S}_0 S_1 \rightarrow 0 \\ &\quad + D_3 S_0 S_1 \rightarrow 0 \\ r &\equiv 1 \end{aligned}$$

► FIGURE 6-82



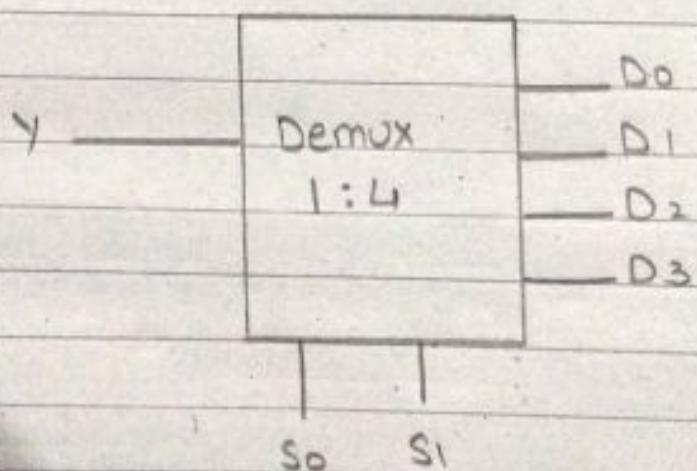
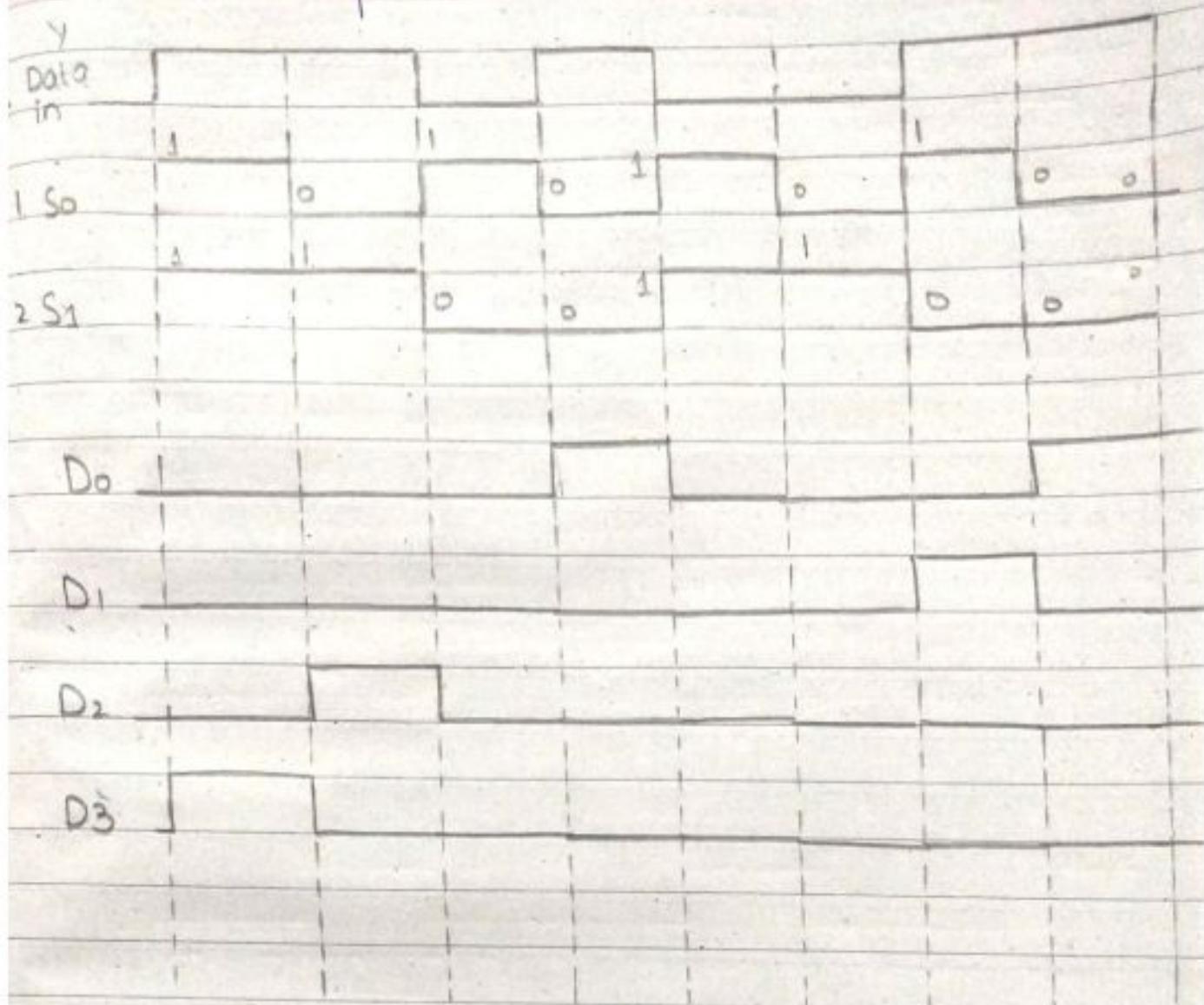
(DEMUX) 1-4

Example 6-18



1 - 4

Related problem 6-18



Q. 30

5-84

