LDST.

Q.4 (a) A keypad attached with input terminal of a machine has 4 keys Up (U), Down (D), Right (R) & Left(L) on it. Pressing Up, Down, Right or Left generates a 2-bit binary code (X Y) of 00, 01, 10 & 11 respectively. If Up has the least priority and it gradually increases in the same order as keys' names are mentioned in the questions then design a *low priority encoder* with an active low enable pin for this keypad. Include additional logic needed to detect the condition when none of the keys has been pressed. Give reduced logic expressions for all the outputs and draw a neat logic circuit diagram. **[5]**

Q.4 (b) Using *4x1 MUX* as a building block, design a logic circuit that accepts four 3-bit inputs $A = A_2A_1A_0$, $B = B_2B_1B_0$, $C = C_2C_1C_0$ & $D=D_2D_1D_0$ along with 2 selection inputs S_1S_0 such that its 3-bit output $Z_2Z_1Z_0$ is as per following table. Clearly state all your assumptions. **[5]**

S_1S_0	00	01	10	11
$Z_2Z_1Z_0$	A	B	C	D

Q.5 (a) Use K-Map method to find reduced *SOP* expression for given logic function. **[5]**

F (a, b, c, d, e) = Σ (only those minterms, which are not an integral power of 2)

Q.5 (b) Design a *sequential circuit* for the given state transition diagram (*See Figure 1*) using D-FF. Draw present & next state table and use excitation table of D-Flip Flop to find logic expressions for D_1 & D_0. Also draw a neat logic circuit diagram. **[5]**

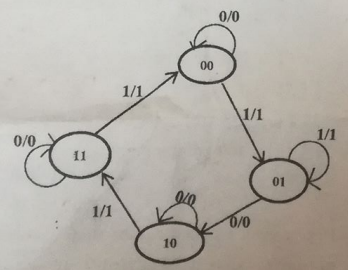

Figure 1

Q.6 (a) Design a *MOD-9 asynchronous up counter* using T FF as the building block. Also draw clock diagram for first ten clock cycles, clearly indicating the RESET condition. State assumptions for your design. **[5]**

Q.6 (b) Draw a properly labeled block diagram of a 4-bit *Serial In parallel out Shift register*. Also draw a neat clock cycle diagram to show that how the data word **1011)$_2$** can be serially stored in this register which initially contains **0000**. Show states of all FFs at each clock pulse. **[5]**

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NED UNIVERSITY OF ENGINEERING & TECHNOLOGY
SECOND YEAR FALL SEMESTER (ELECTRICAL ENGINEERING)
EXAMINATION 2016
BATCH 2014-15 & PREVIOUS BATCHES

Time: 3 Hours

Dated: 29-11-2016
Max. Marks: 60

LOGIC DESIGN & SWITCHING THEORY- CS-205

Instructions: 1. Attempt **ALL** questions
2. **CALCULATORS** are not allowed.
3. All parts of a question should be attempted at one place.
5. Make reasonable assumptions where necessary.

Q.1 (a) Briefly answer the given questions. **[5]**

(i) Discuss the role of CLEAR pin on a Flip Flop IC. Why is it considered as an asynchronous direct input line?

(ii) Why *Carry Look Ahead Adder* is preferred over a *Ripple Carry Adder*?

(iii) Give one meaningful difference between *Latch* and *Flip Flop.*

(iv) What is meant by a *self-complementing code*? Use number $4)_{10}$ to verify that XS-3 code is a self-complementing code.

(v) For a data word of 6 bits ($A_5, A_4, A_3, A_2, A_1, A_0$) give logic expressions for even Parity bit (P_{even}) & check bit (P_{check}).

Q.1 (b) Perform the operations as indicated. **[5]**

(i)	$\overline{x\bar{y} + xyz + x\,(y + x\bar{y})} = 0$	→	(?)	Dual Expression
(ii)	$625)_{10}$	=	(?)	Gray code
(iii)	$0\,1\,0\,1\,1\,1\,0)_{Gray}$	=	(?)	Straight Binary Code
(iv)	$0110\ 0101\ 0000\ 1001\ 0000)_{BCD}$	=	(?)	10's complement
(v)	If $A \oplus B = C$ then $A \oplus B \oplus C$	=	(?)	

Q.2 (a) Ali, Hadi & Wali are prosecution witnesses at Jaree's trial. To corroborate their testimony, each witness is given a lie-detector test. The jury is willing to convict Jaree, if Ali & Hadi both passes the lie-detector test. The jury is also willing to convict if either Ali or Hadi (or both) fail the test, but Wali passes it. Find a canonical **POS** expression for the terms under which Jaree will **NOT** be convicted. Use this *canonical* expression to find an all- **NAND** solution of the situation. **[5]**

Q.2 (b) Use *Boolean algebra / De Morgan's identities* to show that: **[5]**

(i) $a\bar{c} + a\bar{b}c + abcd + abd\bar{d} = a$

(ii) $\overline{(\bar{x} + y)(\bar{y} + z)} + \bar{x} + z = 1$

Q.3 (a) Perform the arithmetic as indicated. **[5]**

(a) $688)_{10} + 287)_{10}$ (Use XS-3 arithmetic principles)

(b) $984)_{10} - 36)_{10}$ (Use 10's complement BCD arithmetic principles)

Q.3 (b) Use 4-bit parallel adders as a building block to design an 8-bit 2's complement adder/subtractor logic. Clearly label all the input/output connections & briefly explain its working. **[5]**
