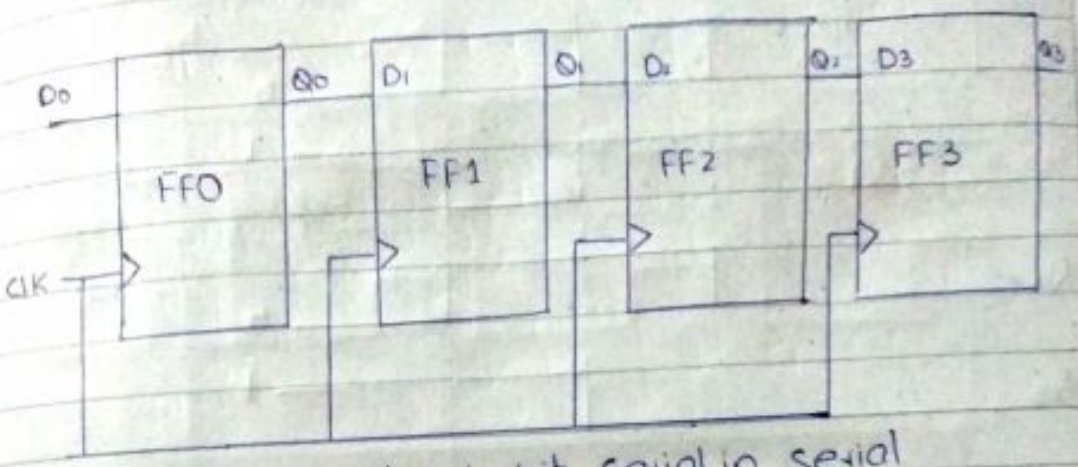
→ n bits to load

→ n-1 bits to read.

SERIAL IN SERIAL OUT

REGISTERS:-



↳ 4 bit serial in serial out register.

Example : 9.1

Data input	CLK	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0	0
1	1	1	0	0	0	0
1	2	1	1	0	0	0
0	3	0	1	1	0	0
1	4	1	0	1	1	0
0	5	0	1	0	1	1

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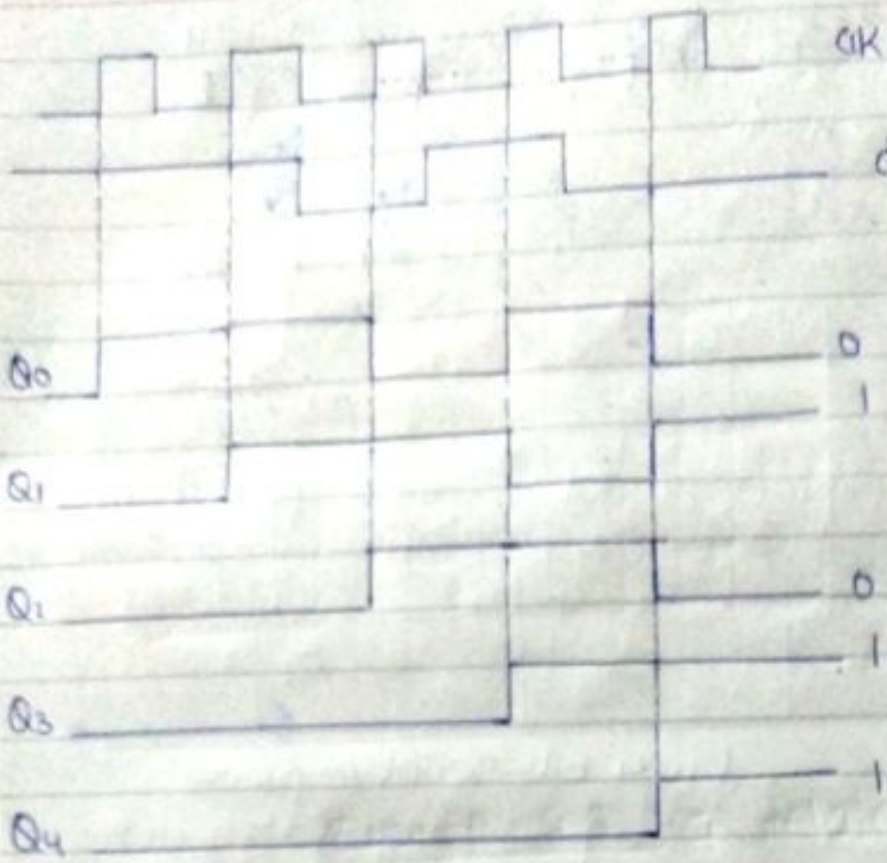
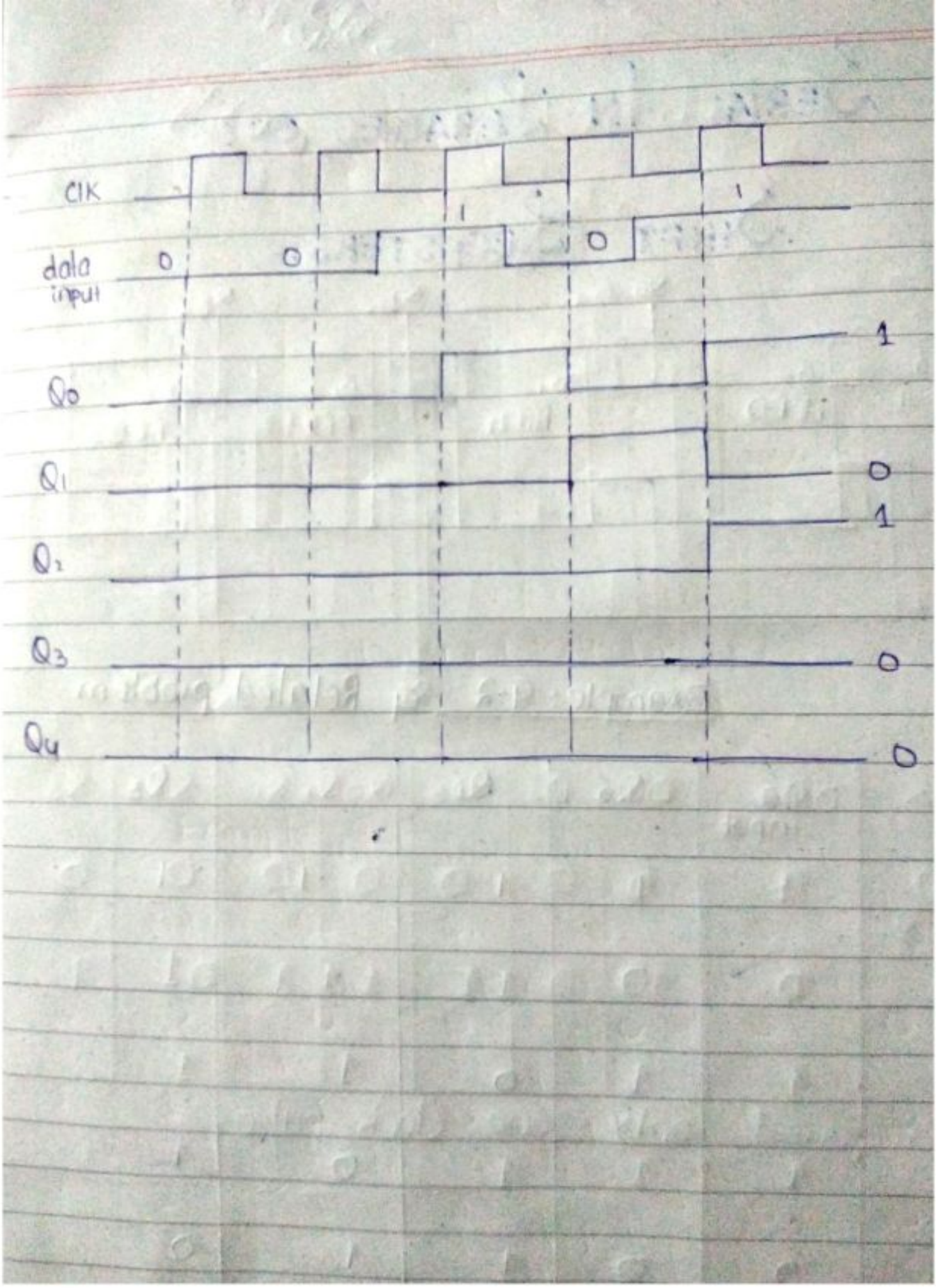


Related problem

CLK.	Data input	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0	0
1	0	0	0	0	0	0
2	0	0	0	0	0	0
3	1	1	0	0	0	0
4	0	0	1	0	0	0
5	1	1	0	1	0	0

Scanned with CamScanner



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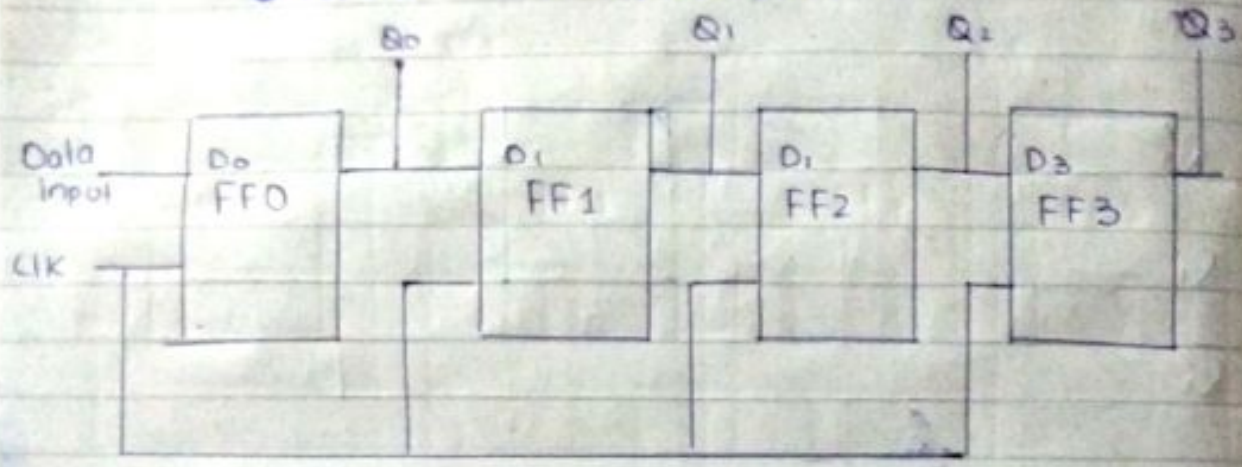
n bits to load

0 bits to read

Serial In Parallel Out Shift Registers:-



Example: 9.2 & Related problem

CLK	Data input	Q_0	Q_1	Q_2	Q_3
0	1	1	1	1	1
1	0	0	1	1	1
2	1	1	0	1	1
3	1	1	1	0	1
4	0	0	1	1	0
5	0	0	0	1	1
6	0	0	0	0	1
7	0	0	0	0	0

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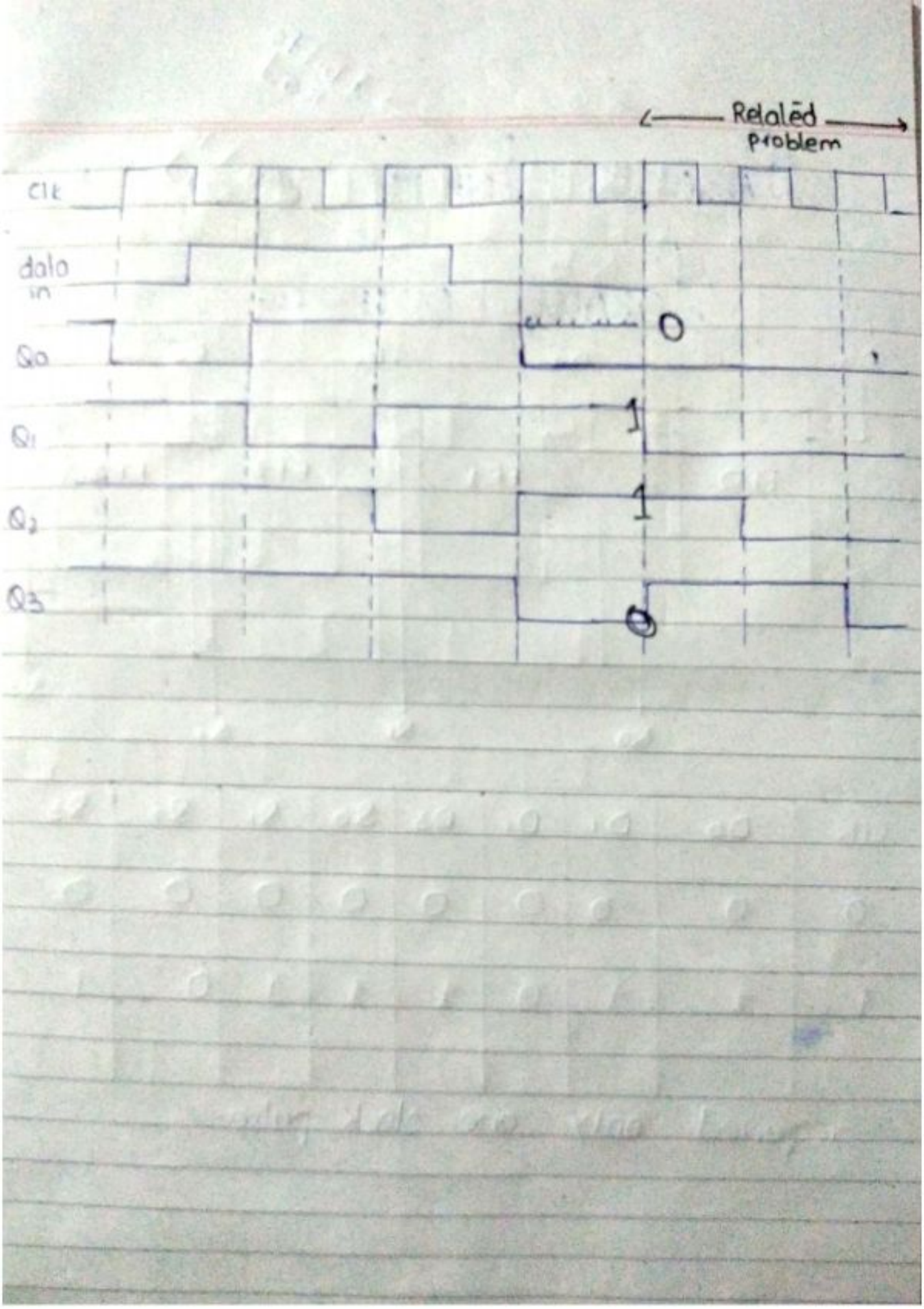

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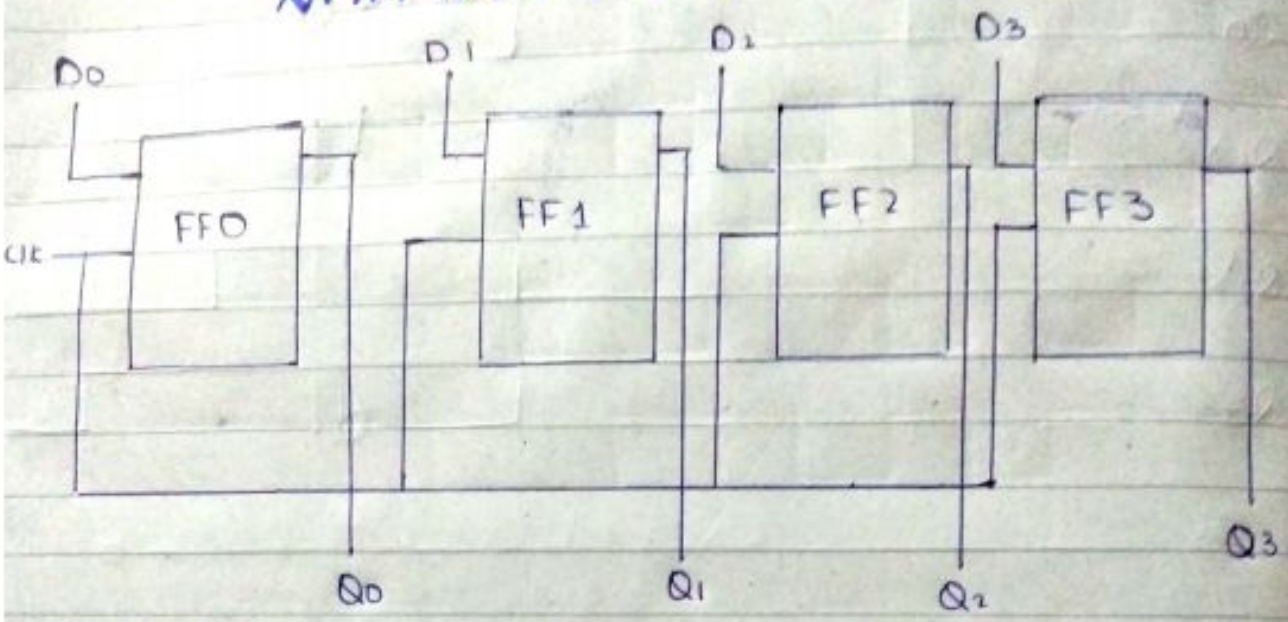
PARALLEL INPUT

1 bit to load

0 bit to read.

PARALLEL OUTPUT:-



CIK	D0	D1	D2	D3	Q0	Q1	Q2	Q3
0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1

required only one clock pulse.

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Section : 9.2

Q.4

CLK	data in	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0
1	1	1	0	0	0
2	0	0	1	0	0
3	1	1	0	1	0

=> After three clock pulses

$Q_3Q_2Q_1Q_0 = 0101$

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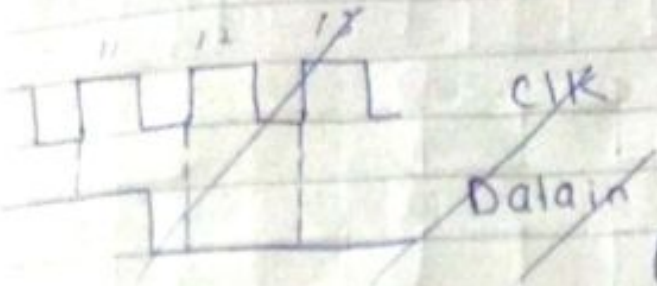

Q.5

⇒ Truth table

CLK	Data In	Q_0	Q_1	Q_2	Q_3
0	1	1	1	1	1
1	1	1	1	1	1
2	0	0	1	1	1
3	0	0	0	1	1
4	1	1	0	0	1
5	1	1	1	0	0
6	0	0	1	1	0
7	1	1	0	1	1
8	0	0	1	0	1
9	1	1	0	1	0
10	1	1	1	0	1
11	1	1	1	1	0
12	0	0	1	1	1
13	0	0	0	1	1

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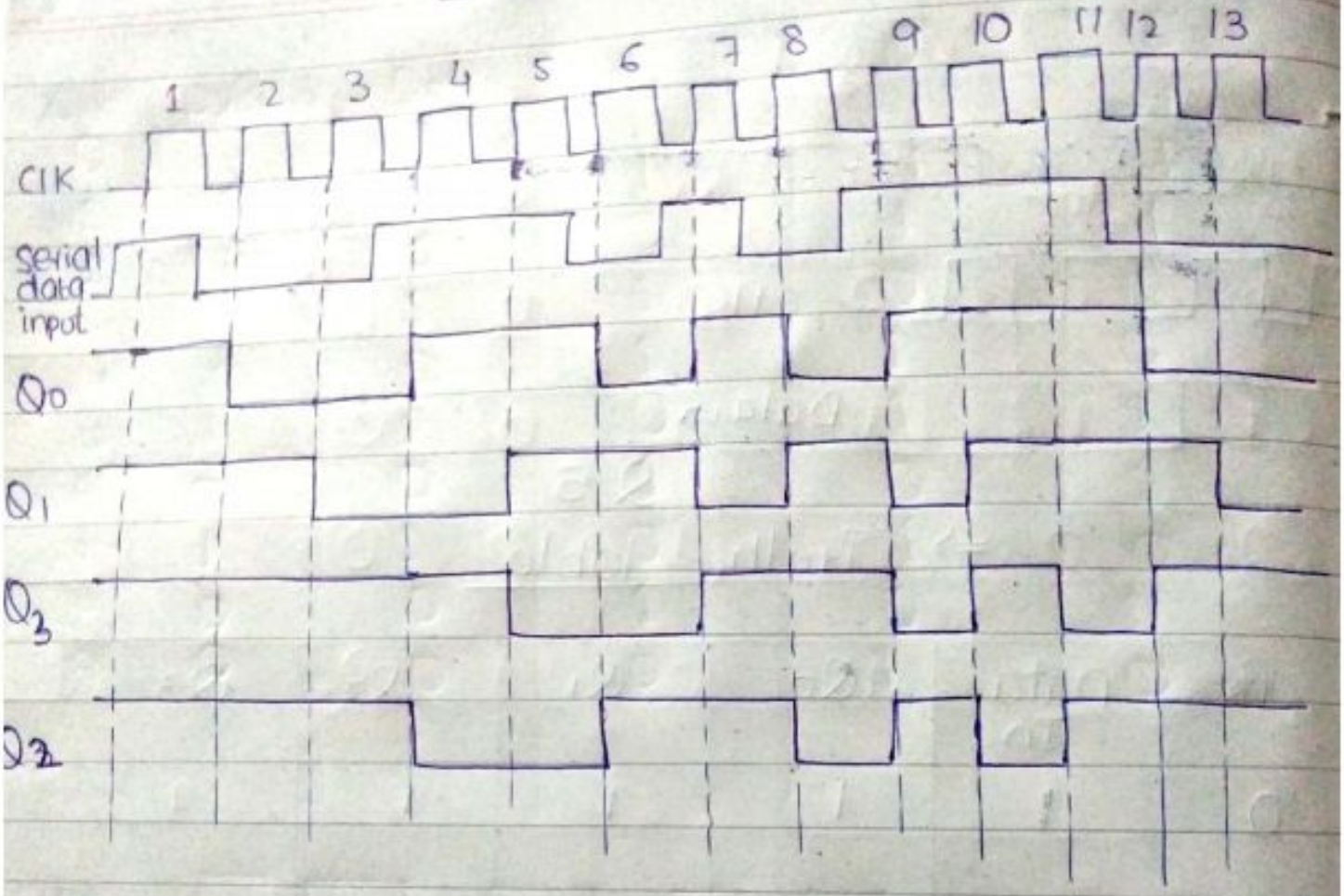
Q.5



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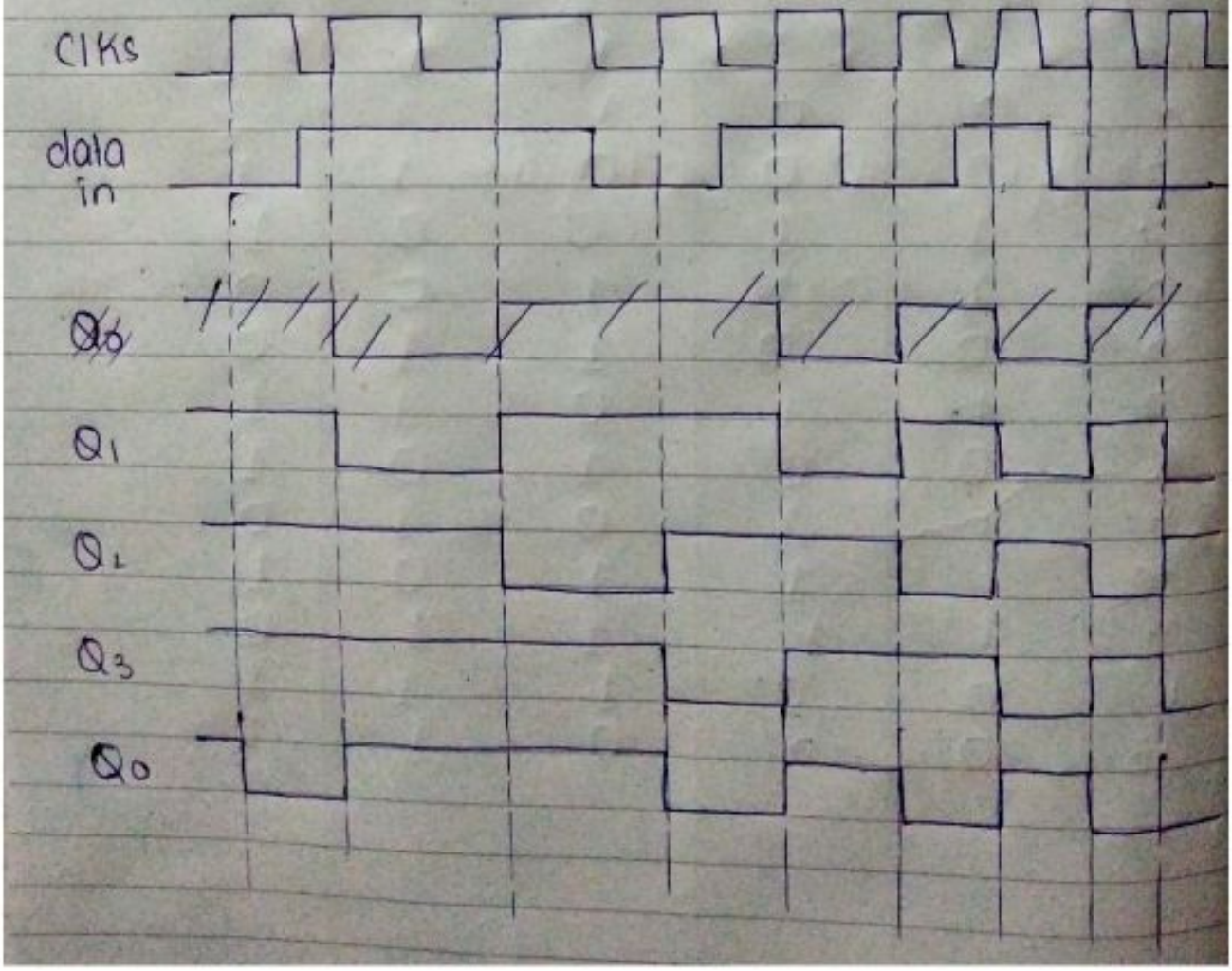
Q.6

CLK	Data in	Q_0	Q_1	Q_2	Q_3
0	1	1	1	1	1
1	0	0	1	1	1
2	1	1	0	1	1
3	1	1	1	0	1
4	0	0	1	1	0
5	1	1	0	1	1
6	0	0	1	0	1
7	1	1	0	1	0
8	0	0	1	0	1
9	0	0	0	1	0



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Q.9

Clk	data	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}
0	'8'	-	-	0	0	0	0	0	0	0	0	0	0
1	-	-	0	0	0	0	0	0	0	0	0	0	0
2	-	-	1	1	0	0	0	0	0	0	0	0	0
3	0	0	0	1	1	0	0	0	0	0	0	0	0
4	0	0	0	0	1	1	0	0	0	0	0	0	0
5	1	1	0	0	0	1	1	0	0	0	0	0	0
6	1	1	1	0	0	0	1	1	0	0	0	0	0
7	0	0	1	1	0	0	0	1	1	0	0	0	0
8	1	1	0	1	1	0	0	0	1	1	0	0	0
9	1	1	1	0	1	1	0	0	0	1	1	0	0
10	0	0	1	1	0	1	1	0	0	0	1	1	0
11	0	0	0	1	1	0	1	1	0	0	0	1	1
12	1	1	0	0	1	1	0	1	1	0	0	0	1
13	1	1	1	0	0	1	1	0	1	1	0	0	0
14	0	0	1	1	0	0	1	1	0	1	1	0	0
15	0	0	0	1	1	0	0	1	1	0	1	1	0
16	9	1	0	0	1	1	0	0	1	1	0	1	1
17	-	1	1	0	0	1	1	0	0	1	1	0	1
18	-	1	1	1	0	0	1	1	0	0	1	1	0
19	0	0	1	1	1	0	0	1	1	0	0	1	1
20	0	0	0	1	1	1	0	0	1	1	0	0	1

→ Required output

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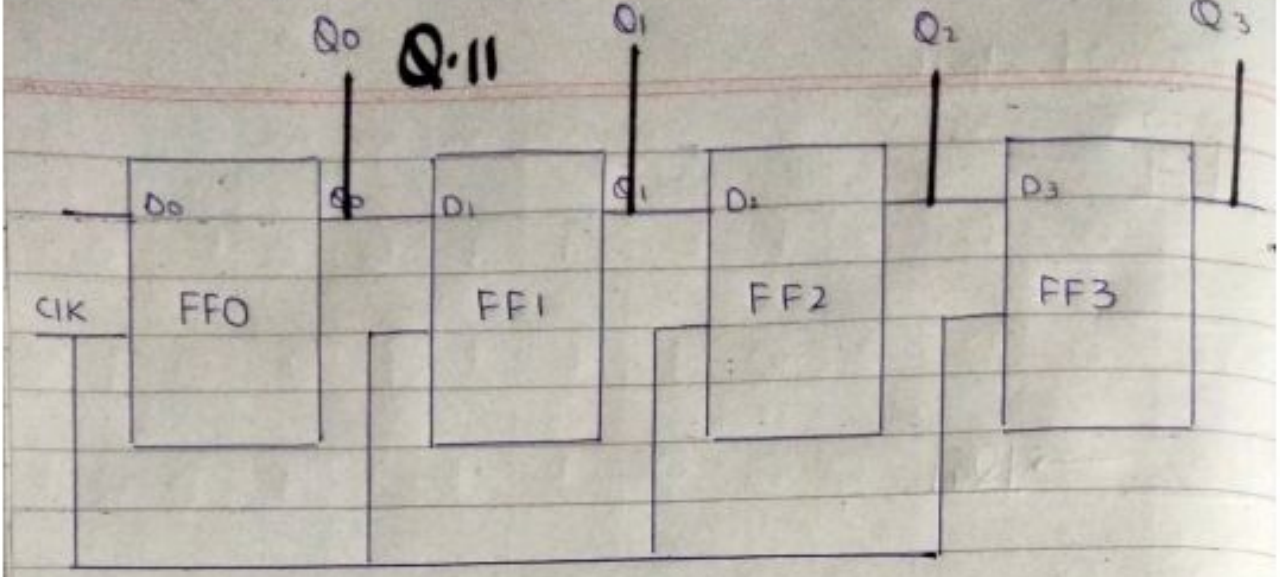
Scanned with CamScanner

Q.11



CLK	data input	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
1	0	0	0	0	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0	0	0	0
3	0	0	1	0	0	0	0	0	0	0	0
4	1	1	0	1	0	0	0	0	0	0	0
5	0	0	1	0	1	0	0	0	0	0	0
6	0	0	0	1	0	1	0	0	0	0	0
7	1	1	0	0	1	0	1	0	0	0	0
8	1	1	1	0	0	1	0	1	0	0	0
9	1	1	1	1	0	0	1	0	1	0	0
10	0	0	1	1	1	0	0	1	0	1	0
11	0	0	0	1	1	1	0	0	1	0	1
12	1	1	0	0	1	1	1	0	0	1	0
13	0	0	1	0	0	1	1	1	0	0	1
14	0	0	0	1	0	0	1	1	1	0	0
15	1	1	0	0	1	0	0	1	1	1	0
16	0	1	1	0	0	1	0	0	1	1	1
17	0	0	1	1	0	0	1	0	0	1	1
18	1	1	0	1	1	0	0	1	0	0	1
19	1	1	1	0	1	1	0	0	1	0	0
20	0	0	1	1	0	1	1	0	0	1	0

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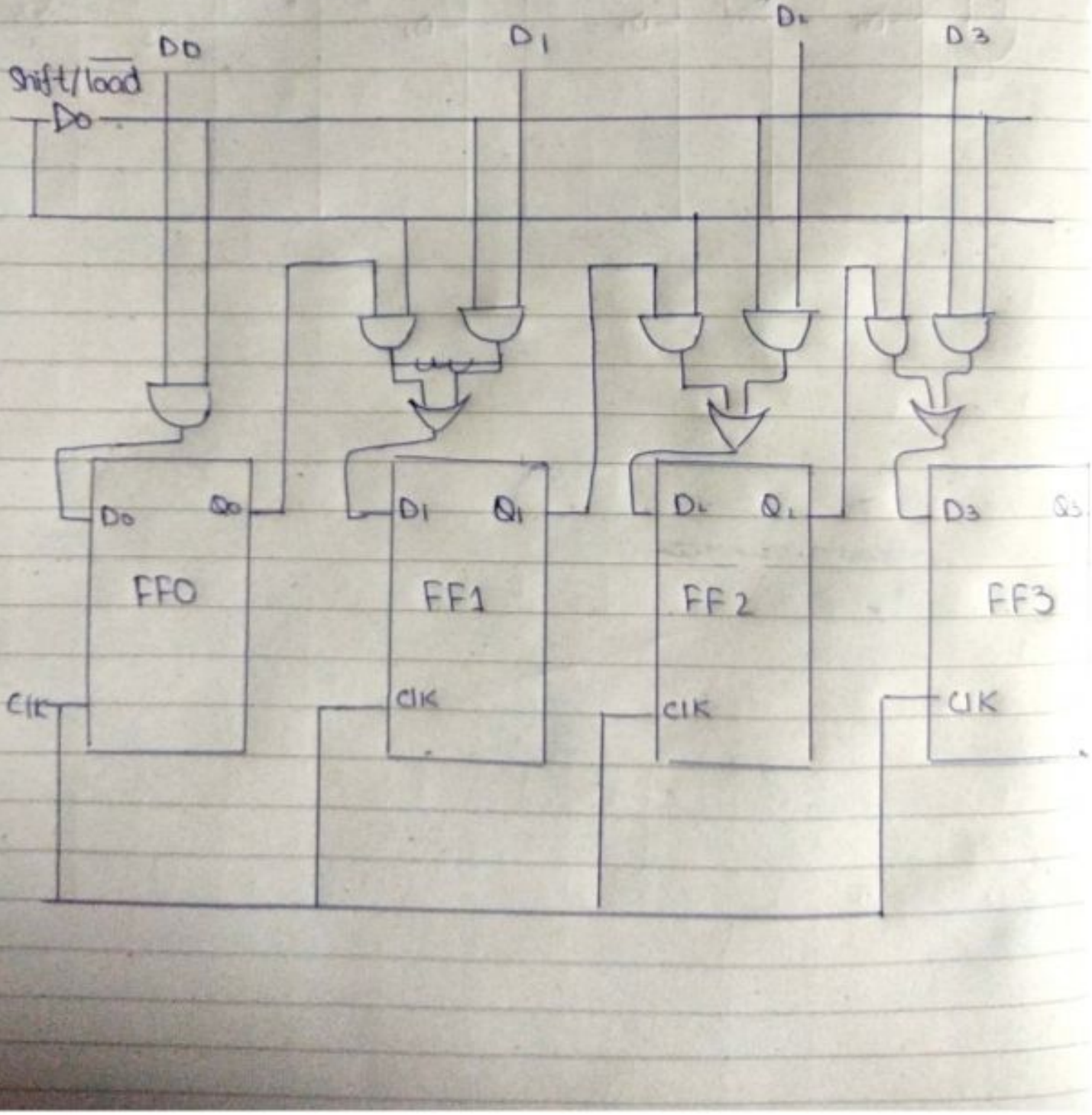
Parallel In Serial Out

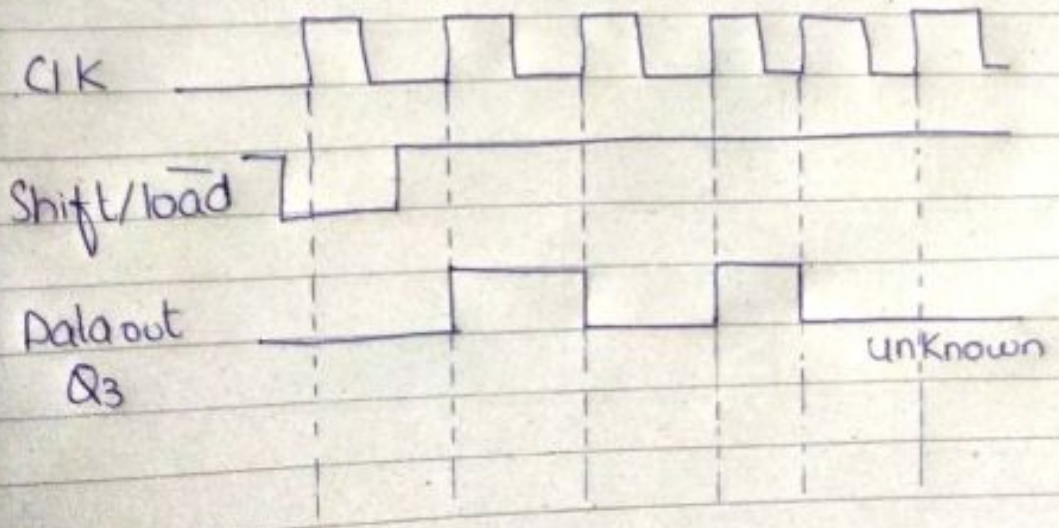


Scanned with CamScanner

Example : 9-3

$D_0 = 1$ $D_1 = 0$ $D_2 = 1$ $D_3 = 0$

CIK	Shift/$\overline{load}$	Q_0	Q_1	Q_2	Q_3
1	0	1	0	1	0
2	1	0	1	0	1
3	1	0	0	1	0
4	1	0	0	0	1
5	1	0	0	0	0
6	1	0	0	0	0



Scanned with CamScanner