Two Factor Analysis

Simple Processor Pipeline Simulator

Version 1.0 Final
Prepared by Dylan and Travis
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1. Introduction

1.1 Purpose

The purpose of this paper is to run a two-factor experimental design on our Simple Processor Pipeline Simulator. We will measure the impact of the pipeline width and the workload trace. The overall mean runtime, impact of each level, allocation of variation to W, T, and their interaction and experimental errors will be all measured. Six replications will be measured to estimate the impact of each level and allocation of variation.

1.2 Simulator

1.2.1 Simulation Information

5-stage pipeline: Instruction Fetch (IF), Instruction Decode and Read Operands (ID), Instruction Issue and Execute (EX), Memory access (MEM), and writeback results/retire (WB). Process has a W-wide superscalar. Instructions proceed to the next stage as long as they have no dependencies. Processor has 1 integer ALUY unit, 1 floating point unit, 1 branch execution unit, 1 read port from L1 data cache, and 1 write port into L1 data cache.

1.2.2 Installation

1. Download proj2.tar.gz

2. Unzip the tar.gz:

```
tar xvzf proj2.tar.gz
```

3. Make the executable file:

```
make proj2
```

1.2.3 Run

Run the program using the command below, with the parameters.

```
./proj2 trace_file_name start_inst inst_count W
```

Parameters	Description
trace_file_name	Name of the trace file
start_inst	Instruction number to start the simulation
inst_count	Number of instructions to simulate
W	Pipeline width

1.3 Factors

1.3.1 Pipeline width (A)

Pipeline width determines how many instructions in parallel can go to IF, ID, EX, MEM, and WB in any given cycle (as long as their dependencies are satisfied).

#	Width
1	1
2	2
3	3
4	4

1.3.2 Workload trace (B)

Workload trace are based on three sample traces from https://www.microarch.org/cvp1/

#	Width
1	Integer Trace
2	Floating Point Trace
3	Server Trace

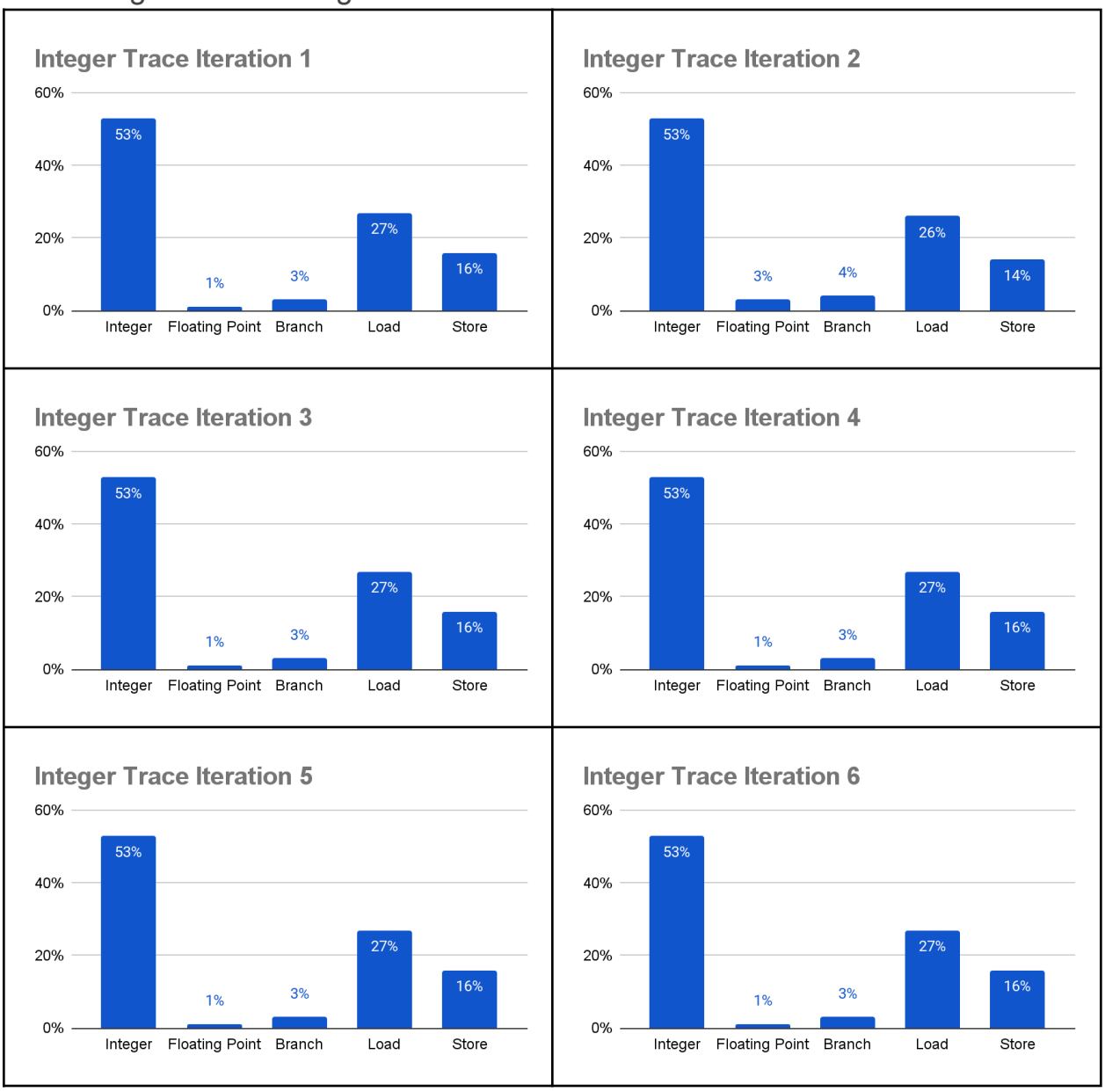
1.4 Iterations

Iteration	start_inst	inst_count
1	1	1,000,000
2	5,000,000	1,000,000
3	10,000,000	1,000,000
4	15,000,000	1,000,000
5	20,000,000	1,000,000
6	25,000,000	1,000,000

2. Trace Inputs

2.1 Integer Trace

2.1.1 Integer Trace Histogram

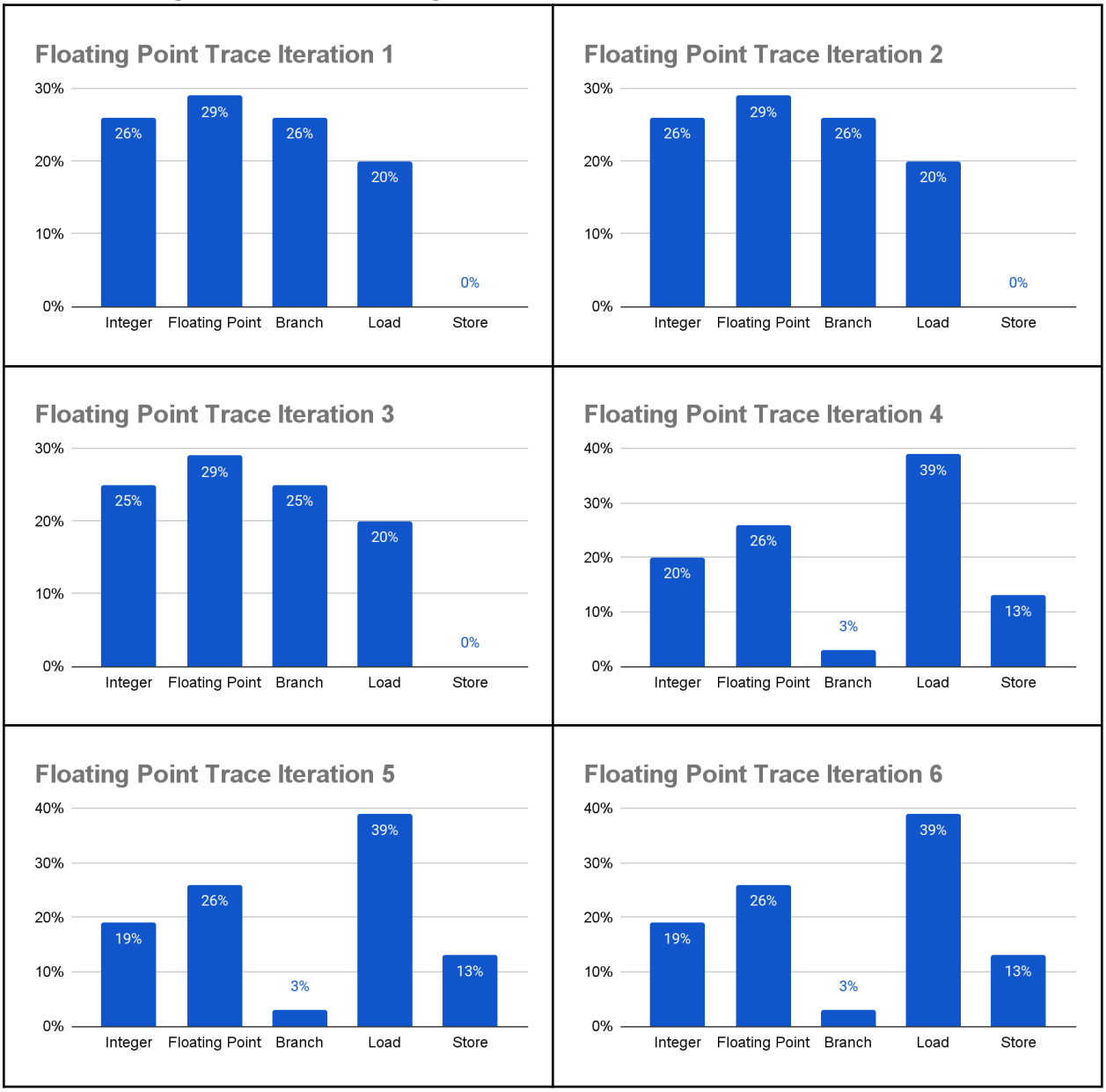


2.1.2 Integer Trace Execution Time

Iteration	Width = 1	Width = 2	Width = 3	Width = 4
1	1205686	937642	827661	796787
2	1222309	959108	857964	829287
3	1205688	937644	827663	796789
4	1205689	937647	827666	796790
5	1205688	937641	827660	796786
6	1205691	937635	827648	796769
Average	1208458.5	941219.5	832710.33	802201.33

2.2 Floating Point Trace

2.2.1 Floating Point Trace Histogram

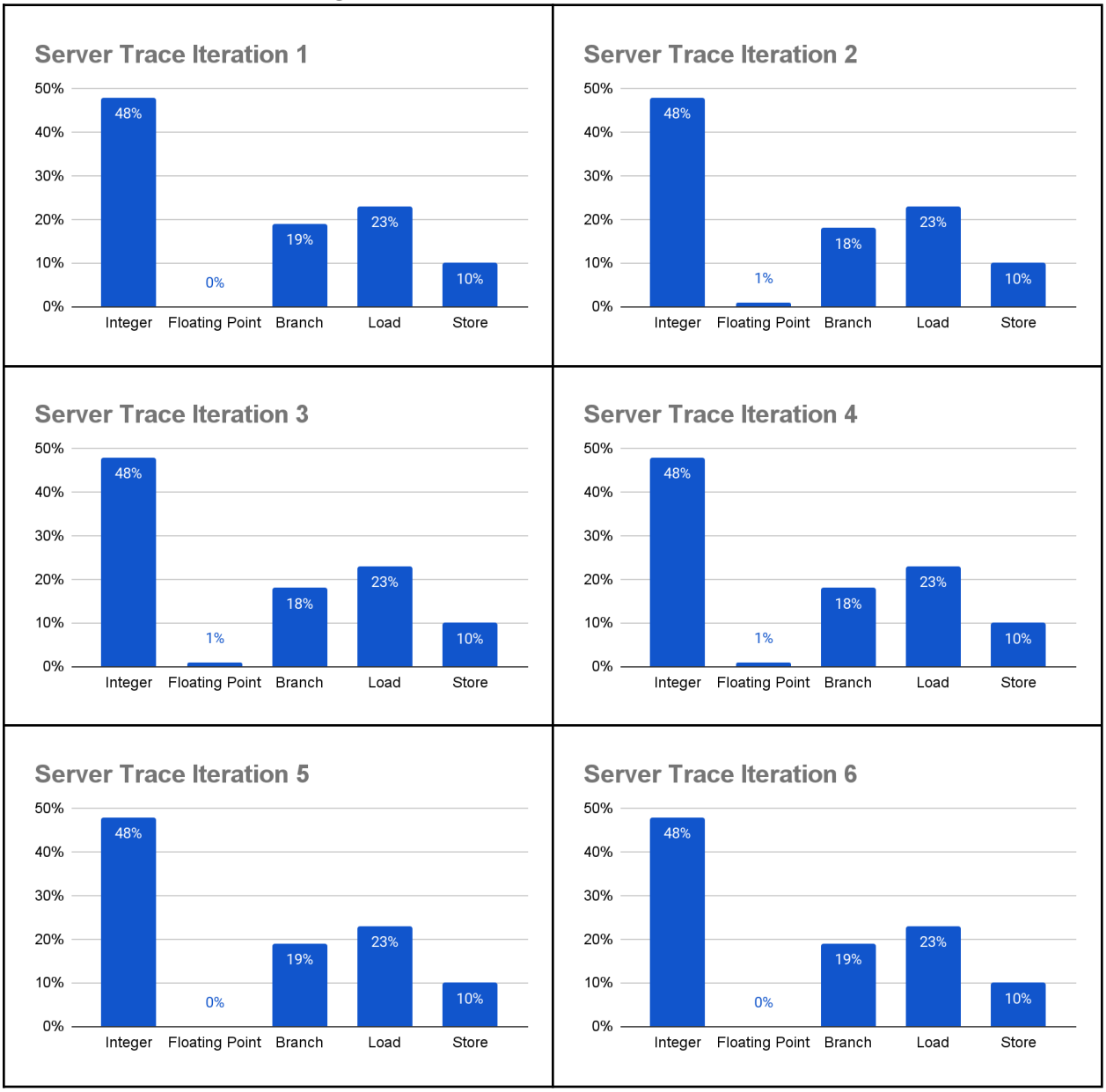


2.2.2 Floating Point Trace Execution Time

Iteration	Width = 1	Width = 2	Width = 3	Width = 4
1	1666382	1317872	1317872	1317872
2	1665528	1316938	1316936	1316936
3	1660202	1311129	1311129	1311129
4	1066211	808243	743867	583377
5	1065799	807809	743404	582719
6	1065577	807575	743155	582359
Average	1364949.833	1061594.333	1029393.833	949065.333

2.3 Server Trace

2.3.1 Server Trace Histogram



2.3.2 Server Trace Execution Time

Iteration	Width = 1	Width = 2	Width = 3	Width = 4
1	1476020	1177930	1132101	1118987
2	1457171	1157162	1111247	1099020
3	1467840	1168770	1122941	1110018
4	1463484	1163008	1117006	1104028
5	1479488	1182871	1136939	1123879
6	1478127	1180310	1134042	1120728
Average	1470355	1171675.167	1125712.667	1112776.667

3. Two-factor Experiment Design

3.1 Experiment Description

We will analyze the impact of width size and the different trace input. It will be measured with cycle count. Factor A is width and factor B is the workload trace..

3.2 Means and Effect

3.3.1 Mean Cycle Times and Effects

	Width = 1	Width = 2	Width = 3	Width = 4	Row Mean	Row Effect
Int Trace	1208458.5	941219.5	832710.33	802201.33	946147.4167	-143028.625
FP Trace	1364949.83	1061594.33	1029393.83	949065.33	1101250.833	12074.792
Server Trace	1470355	1171675.17	1125712.67	1112776.67	1220129.875	130953.833
Column Mean	1347921.111	1058163	995938.9444	954681.1111	1089176.042	
Column Effect	258745.069	-31013.0417	-93237.097	-134494.931		0

The average width on average trace has 1,089,176.042 cycles.
Impact of width 1: 258,745.069, Impact of width 2: -31,013.0417,
Impact of width 3: -93,237.097, Impact of width 4: -134,494.931
Integer trace has 143,028.625 lower cycle count than average workload.
Floating point trace has 12,074.792 higher cycle count than average workload
Server trace has 130,953.833 higher cycle count than average workload.

3.3.2 Computation of Effects

	Width = 1	Width = 2	Width = 3	Width = 4	yj	Row Effect
Int Trace	3566.0139	26085.125	-20199.986	-9451.153	946147.417	-143028.625
FP Trace	4953.931	-8643.458	21380.097	-17690.569	1101250.833	12074.792
Server Trace	-8519.944	-17441.667	-1180.111	27141.722	1220129.875	130953.833
yi	1347921.111	1058163	995938.944	954681.111		
Column Effect	258745.069	-31013.0417	-93237.097	-134494.931		0

3.3 Errors

3.3.1 Integer Trace Errors

Iteration	w=1	w=2	w=3	w=4
1	1,430.917	625.917	-5,049.333	-5,414.333
2	-7,169.083	-3,131.083	25,253.667	27,085.667
3	1,430.917	625.917	-5,047.333	-5,412.333
4	1,429.917	626.917	-5,044.333	-5,411.333
5	1,433.167	625.167	-5,050.333	-5,415.333
6	1,444.167	627.167	-5,062.333	-5,432.333

SSE = 1,719,097,179.333

3.3.2 Floating Point Trace Errors

Iteration	w=1	w=2	w=3	w=4
1	-2,316.500	-47,471.000	288,478.167	368,806.667
2	-2,255.500	-47,490.000	287,542.167	367,870.667
3	-1,894.250	-47,611.750	281,735.167	362,063.667
4	2,087.500	47,475.000	-285,526.833	-365,688.333
5	2,167.250	47,532.750	-285,989.833	-366,346.333
6	2,211.500	47,565.000	-286,238.833	-366,706.333

SSE = 1,308,951,021,752.420

3.3.3 Server Trace Errors

Iteration	w=1	w=2	w=3	w=4
1	-464.625	125.208	6,388.333	6,210.333
2	795.875	-533.292	-14,465.667	-13,756.667
3	222.625	-167.542	-2,771.667	-2,758.667
4	1,377.375	-418.792	-8,706.667	-8,748.667
5	-1,531.375	531.458	11,226.333	11,102.333
6	-399.875	462.958	8,329.333	7,951.333

SSE = 1,033,713,223.438

3.3.4 Mean Cycle Times Errors

	Width = 1	**Width = 2**	**Width = 3**	**Width = 4**
Integer Trace	3566.014	26085.125	-20199.986	-9451.153
FP Trace	4953.931	-8643.458	21380.098	-17690.570
Server Trace	-8519.944	-17441.667	-1180.111	27141.722

3.4 Sum of All Squares

SSA	3 * Sum of all squared column effects	1,704,471,522,458.37
SSB	4 * Sum of all squared row effects	906,045,471,069.08
SSAB	The sum of the squared interaction between A and B	19,048,178,822
SSE	Sum of all squared errors	3,174,696,470
SST	SSA+SSB+SSAB+SSE	2,632,739,868,819.69

3.5 Analysis of Variation

SSA/SST	284,078,587,076/2,632,739,868,819.69	0.6474135719	64.7%
SSB/SST	151,007,578,512/2,632,739,868,819.69	0.3441454592	34.4%
SSAB/SST	19,048,178,822/2,632,739,868,819.69	0.00723511618	0.7%
SSE/SST	3,174,696,470/2,632,739,868,819.69	0.001205852697	0.1%

64.7% of variation explained by width size.
34.4% of variation explained by workload trace.
0.7% of variation explained by interaction of width size and workload trace.
0.1% of variation explained by experimental error.