University of Oulu
521404A Digital Techniques 2
Project Report: I^2C Controlled FIR Filter

Tiia Leinonen
2551463

Table of Contents

Revision History

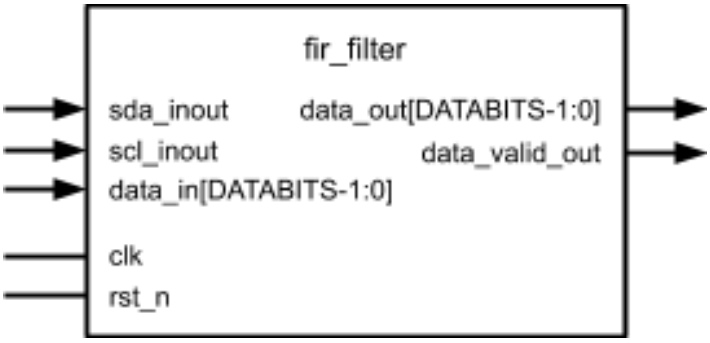
Version	Date	Author	Comment
1.0	16.12.2019	Tiia Leinonen	Start of the report, section 4 done
1.1	17.12.2019	Tiia Leinonen	Rest of the sections started
1.2	18.12.2019	Tiia Leinonen	Finished report

1. Introduction

The purpose of this project is to design and program a FIR (finite impulse response) filter, but in practice only the I2C slave and the FIR filter logic are designed.
The FIR filter unit should work as following: read signal data samples from an interface at a fixed sample rate, then filter the data using constant coefficients, and finally write the filtered data samples into another interface.

2. Design Requirements

The overall functionality is defined here. Details can be found in the project specification [1].



The circuit is synchronous to clock input signal clk, and all flip-flops are clocked to the rising edge of it. The asynchronous active-low reset signal, rst_n, which is synchronized to clock, is used to reset all the flip-flops.

First, after a reset or interruption, in idle state the FIR filter unit is inactive, but I2C slave interface logic, of which I2C buses sda_inout and scl_inout are part of, is active and waits for data to be written to the slave's address. If the detected data frame is valid, i.e. one header byte containing the right address and a write access bit + 14 bytes representing the (in my case) 7 filter coefficients, the circuit becomes active. The received bytes are stored in a shift register.

In active state the FIR filter unit becomes active and executes the following sequence until an invalid I2C access (a short frame or read access bit) is detected: read data sample from input data_in and write it into a register bank; compute FIR algorithm with data from the register bank and filter coefficient register; and finally write the filtered data to output data_out. If invalid I2C access is detected, the circuit returns to idle state. If data is valid, the validity indicator output data_valid_out is 1.

3. Design Methods and Tools

3.1. Design Flow and Tools

I followed the weekly task list [2] through the project. The usual order of things was to first read the instructions and specification sheets, next write the RTL code for the module, and finally perform the verification, synthesis and simulation with the tools provided. At the end of the course I also had to design some parts myself, and I drew ASM charts to help with the task.

Tools used: QuestaSim for simulation; Questa AutoCheck for finding common errors, such as latches; Design Compiler for running synthesis; and Formality for logic equivalence checking.

3.2. RTL Architecture Specification Methods

The RTL architecture was specified in the specification sheets provided [3], which contained usually the names and specs of input and output signals, block diagrams, and verification plans for each module. The block diagrams clearly showed the hierarchical structure of the design. The top-module, fir_filter, contains submodules for i2c_slave, control_unit, filter_unit and reset_sync.

i2c_slave contains submodules i2c_sync, i2c_detector, i2c_fsm, i2c_ctr3 and i2c_srg, which are used in controlling and maintaining the shift register and bit counter; filter_unit contains submodules filter_unit_control, cregs, dregs, muladd, acc, sat and oreg, which are modules for datapath and control; and control_unit controls the start and stop of filter unit and generates ACK signal for i2c_slave.

3.3. RTL Coding Principles

The basic block of the design is called a module. It defines the name of the design, the types and names of its inputs and outputs, parameters, and its functionality or hierarchical structure. When instantiating a module, ports in the module to be instantiated must be connected to variables or ports of the instantiating module.

Modules can contain one to many concurrent processes, which are blocks of sequential statements, that are executed continuously. In SystemVerilog, *always* is this kind of procedure, but *always_comb* for combinational logic and *always_ff* for sequential logic should be used instead, as the synthesis tool can better issue a warning if the design contains errors.

Things to remember when coding combinational processes: processes must be sensitive to all of their inputs, processes must always assign a value to all of their outputs, internal

variables must be given a value before they are read, they must not contain a feedback loop and variables must be assigned using blocking assignment operator (=).

Things to remember when coding sequential processes: variables that model edge-sensitive storage devices should be assigned using nonblocking assignment operator (<=), but blocking assignment operator can be used with temporal variables too; and processes must contain an event list containing edge events representing the clock and possible asynchronous control variables.

Additionally, a variable cannot be driven from two processes at the same time, and initial assignments of variables should be avoided.

Finite state machines should be coded as two processes: one always_comb representing the logic defining the changes of states and one always_ff representing the state register. Assigning default values to outputs in the beginning of the always_comb procedure is useful and helps prevent latches from occurring. Using enumeration type for state codes can also make debugging easier.

Three-state output, simply put means that accepted output values can be ‘1 (logical one), ‘0 (logical zero) or ‘z (high impedance), instead of only ‘1 and ‘0. The third option ‘z is used to effectively remove the influence of the device from the circuit, e.g. prevent one device dominating the circuit and ‘making room’ for other devices [4]. The ‘z value is used in I2C buses such as sda_inout and scl_inout instead of ‘1.

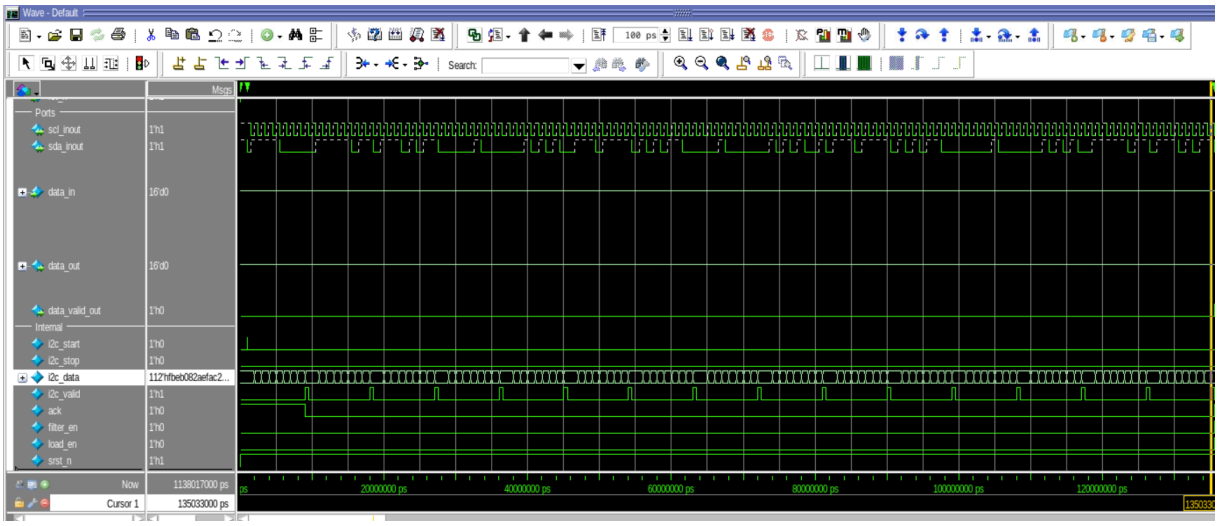
4. RTL Verification Results

4.1. Functional Verification Results

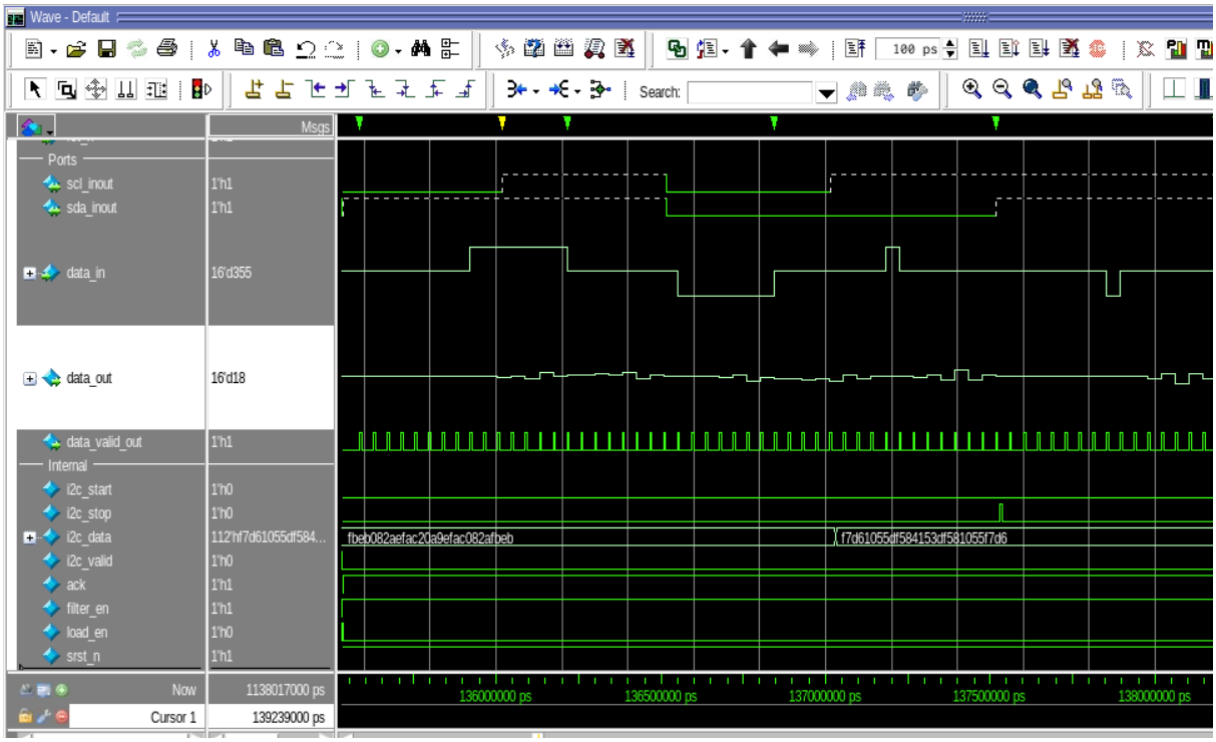
Test Name	Result	Comment
T1	PASS	Reset works as it should
T2	PASS	I2c_valid occurs 15 times (1 address byte + 2*NTAPS = 14 bytes of data) and data is correct (K8,K4,K2,K,K2,K4,K8)
T3	PASS	NTAPS zero and NTAPS value L observed in data_in (ACK fail occurs here because in control_unit.sv I set the ack_out to 1 in my STOP state already, because it created the correct waves shown in the example, control_unit_waves, but it probably should be 0 here)
T4	PASS	NTAPS zeros and NTAPS value -L observed in data_in
T5	PASS	Impulse of NTAPS zeros followed with value L and another impulse of NTAPS zeros observed in data_in
T6	PASS	Impulse of NTAPS zeros followed with value -L and another impulse of NTAPS zeros observed in data_in
T7	PASS	A sine waveform observed

Supplementary information:

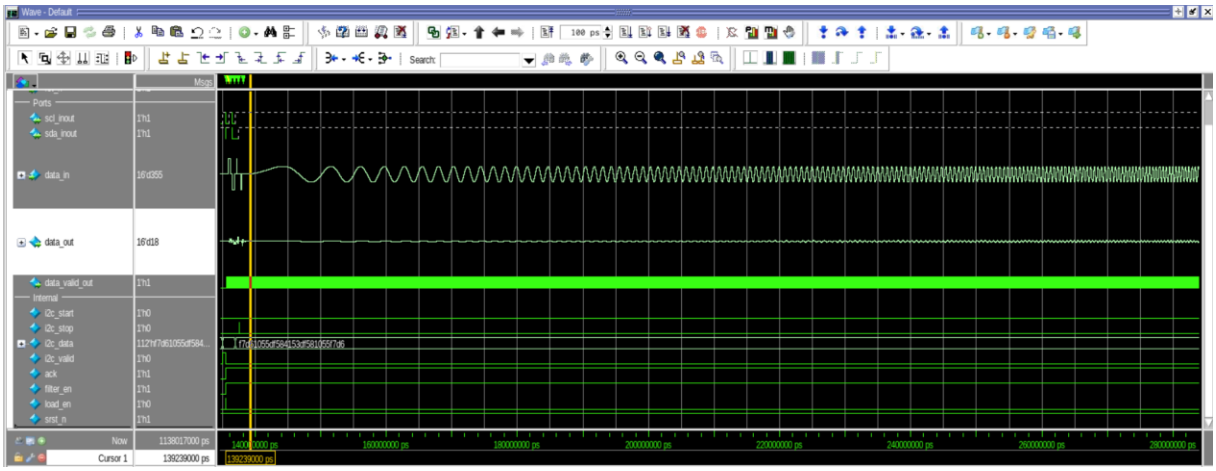
T2 waves



T3-T6 waves



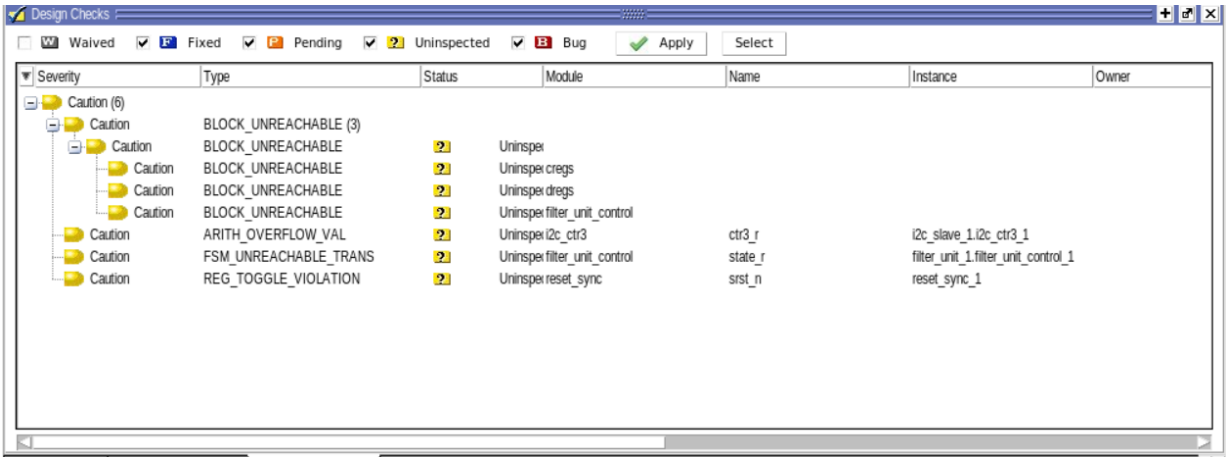
T7 waves



4.2. Static Verification Results

Issue Type	Module	Explanation / Comment
BLOCK_UNREACHABLE	cregs	I check that the faddr_in < NTAPS, the else condition is never reached
BLOCK_UNREACHABLE	dregs	I check that the faddr_in < NTAPS, the else condition is never reached
BLOCK_UNREACHABLE	filter_unit_control	Else condition, next_state = STOPPED, is never reached here, but it's here just in case anyways
ARITH_OVERFLOW_VAL	i2c_ctr3	Warning about overflow, but it's not going to happen because I reset the counter in i2c_fsm when needed
FSM_UNREACHABLE_TRANS	filter_unti_control	The state STOPPED is unreachable, as I mentioned above
REG_TOGGLE_VIOLATION	Reset_sync	The flip flop is "stuck" at a value, but it just can't be changed by anything else than the reset signal

Supplementary information:



5. Synthesis Results

5.1. Area Results

Property	**Value**	**Unit**
Total Cell Area	4350.430103	N/A
NAND2 equivalent gate area[1]	5451.66679573	gates
Number of cells	1753	
Number of sequential cells (total /expected)	417 / 0	

5.2. Timing Results

Property	Value	Unit
Critical Path = reg2reg path		
Max delay (critical path length)	5.30	ns
Critical path slack	0.66	ns
Critical path start point	filter_unit_1/filter_unit_control_1/state_r_reg[2]	
Critical path end point	filter_unit_1/acc_1/acc_r_reg[37]	
Explain through which design modules the critical path goes	filter_unit only	
Number of logic gates on critical path	55	

5.3. Synthesis Results Checks

Check	Result
Latches synthesized from combinational parts?	0
Timing loops reported?	0

[1] Divide Total cell area by area of the NAND2_X1 gate (0.798 in this component library).

Warnings about variable initializations generated?	0
Three-state buffer synthesised (give component name)	i2c_slave_1/sda_inout_tri/Z (TBUF_X1)
Other warnings or errors?	0

6. Gate-Level Verification

6.1. Formal Logic Equivalence Check results

```
****************************** Verification Results ******************************
Verification SUCCEEDED
   ATTENTION: synopsys_auto_setup mode was enabled.
              See Synopsys Auto Setup Summary for details.
   ATTENTION: RTL interpretation messages were produced during link
              of reference design.
              Verification results may disagree with a logic simulator.
--------------------------------------------------------------------------------
Reference design: r:/WORK/fir_filter
Implementation design: i:/WORK/fir_filter
436 Passing compare points
--------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF      LAT    TOTAL
--------------------------------------------------------------------------------
Passing (equivalent)           0       0       1       0      19     416        0     436
Failing (not equivalent)       0       0       0       0       0       0        0       0
********************************************************************************
```

6.2. Gate-Level Simulation Results

(Present DUT vs. REF checker results. Describe timing violations and other problems reported during simulation. Describe handling of synchronizers and other exceptions.)

Parameter	Result	Comment
DUT vs. REF	OK	Waves look the same in no timing picture, but differ in timing picture
Setup Violations	0	After removing timing checks, all ok
Hold Violations	0	After removing timing checks, all ok
Synchronizer validation	OK	No more timing violations occur after removing timing checks
Other Issues	Warning that ACK failed, twice	ACK fails in T3, mentioned already in section 4.1

Supplementary information:
From the simulation log, regarding other issues:
End time: 16:20:43 on Dec 16,2019, Elapsed time: 0:11:49
Errors: 0, Warnings: 2

7. Discussion

The observed functionality seems quite good. The correct coefficients are loaded into registers, even though one extra shift happens at the end after the load. The FIR filter algorithm should produce right answers, as they seem similar to the values from muladd module testing I did. One ACK failure occurs in T3, but I know it's there because of my own decision to rather follow the example waves instead of the instructions, as they seemed to have a small difference.

The synthesis results seem ok. No timing issues, loops or latches occurred. Gate-level simulation seems to be fine after removing the timing checks. The only thing I'm a bit worried about is the high number of sequential cells (417), because the expected number is apparently zero.

The project as a whole went well. I followed the weekly task list and managed to do everything on time. All in all, the course and the project were quite fun and the degree of difficulty was appropriate. The only negative feedback I have is that some of the instructions were a bit messy and misleading though, as they still seem to contain information from the previous years.

References

1. https://docs.google.com/document/d/1vuSITKF49bXKN0hhZbH-nUa5Wg-MJ1L0JwP89B8yYbY/edit#

2. https://docs.google.com/spreadsheets/d/1rFYapxCLaStsE4z1cSbiRZlyDEcg6NCiMil7N74g8ZI/edit#gid=650118843

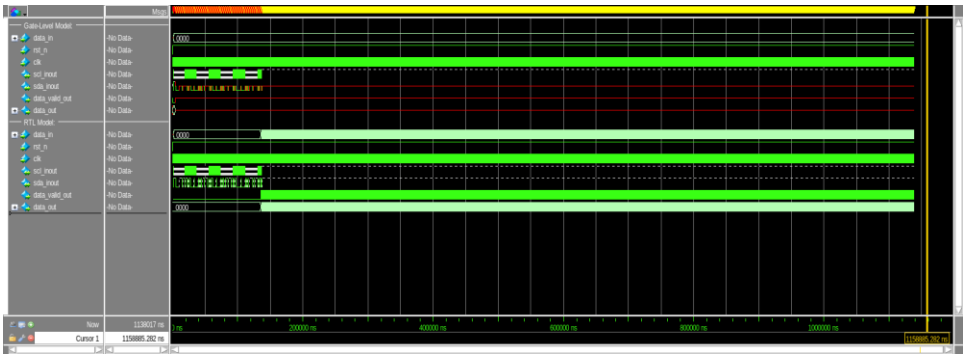
3. https://docs.google.com/spreadsheets/d/1tmOndxA0QvZQl9MPxZktwfqF9Ep6v4i0W25dAm2H1jI/edit#gid=709574858

4. https://en.wikipedia.org/wiki/Three-state_logic

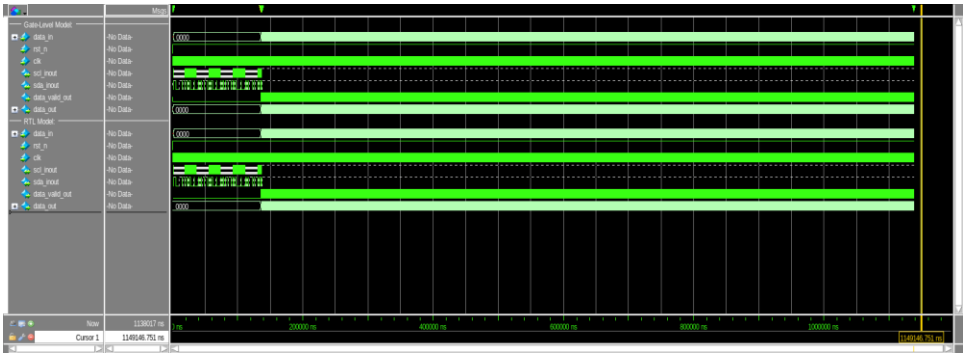
Appendices

A1. RTL Simulation Waveforms

Timing



No timing



A2. Questa Autocheck Summary Report

(From reports/3_qautocheck_fir_filter_check_report.txt)

```
AutoCheck Compile Summary
-------------------------------------------------------------------------------
Check                      Evaluations         Found        Waived
-------------------------------------------------------------------------------
ASSIGN_IMPLICIT_CONSTANT           33             0             0
CASE_DUPLICATE                      4             0             0
CLK_DELAY                          20             0             0
CLK_IN_DATA                        80             0             0
COMBO_LOOP                        104             0             0
DECLARATION_UNDRIVEN               50             0             0
DECLARATION_UNUSED                 50             0             0
DECLARATION_UNUSED_UNDRIVEN         0             0             0
FUNCTION_INCOMPLETE_ASSIGN          0             0             0
INDEX_UNREACHABLE                   0             0             0
LATCH_INFERRED                     32             0             0
LOGIC_UNDRIVEN                     50             0             0
LOGIC_UNUSED                        0             0             0
PORT_UNDRIVEN                     114             0             0
PORT_UNUSED                       114             0             0
REG_MIXED_ASSIGNS                  52             0             0
REG_NO_RESET                       20             0             0
REG_RACE                            0             0             0
REG_VARIABLE_ARESET                40             0             0
RESET_HIGH_LOW                      1             0             0
RESET_SYNC_ASYNC                    1             0             0
SLIST_INCOMPLETE                   32             0             0
X_ASSIGN_REACHABLE                  0             0             0
-------------------------------------------------------------------------------
AC Total                          797             0             0
-------------------------------------------------------------------------------


AutoCheck Verify Summary
-------------------------------------------------------------------------------
Check                      Evaluations         Found        Waived
-------------------------------------------------------------------------------
ARITH_OVERFLOW_SUB                  0             0             0
ARITH_OVERFLOW_VAL                  4             1             0
ARITH_ZERO_DIV                      0             0             0
ARITH_ZERO_MOD                      0             0             0
BLOCK_UNREACHABLE                 132             3             0
BUS_MULTIPLY_DRIVEN                 0             0             0
BUS_UNDRIVEN                        0             0             0
BUS_VALUE_CONFLICT                  0             0             0
CASE_DEFAULT                        2             0             0
CASE_FULL                           0             0             0
CASE_PARALLEL                       0             0             0
FSM_DEADLOCK_STATE                 19             0             0
FSM_LOCKOUT_STATE                  19             0             0
FSM_STUCK_BIT                       9             0             0
FSM_UNREACHABLE_STATE              19             0             0
FSM_UNREACHABLE_TRANS              46             1             0
INDEX_ILLEGAL                       3             0             0
INIT_X_OPTIMISM                    20             0             0
```

```
INIT_X_PESSIMISM                    0             0             0
INIT_X_UNRESOLVED                   0             0             0
INIT_X_UNRESOLVED_MEM               0             0             0
ONE_COLD                            0             0             0
ONE_HOT                             0             0             0
REG_MULTIPLY_DRIVEN                 0             0             0
REG_STUCK_AT                       17             0             0
REG_TOGGLE_VIOLATION               10             1             0
-------------------------------------------------------------------------------
AC Total                          300             6             0
-------------------------------------------------------------------------------


------------------------------------------------------------
AutoCheck Details
------------------------------------------------------------

Type      : ARITH_OVERFLOW_VAL
Severity  : Caution
Status    : Uninspected
Module    : i2c_ctr3
Name      : ctr3_r
Instance  : i2c_slave_1.i2c_ctr3_1
Location  : /home/so/tiileino/DT2_2019/project/workdir/input/i2c_ctr3.sv:29
Assignment Width: 3
Waveform Distance: 21

Type      : BLOCK_UNREACHABLE
Severity  : Caution
Status    : Uninspected
Module    : cregs
Location  : /home/so/tiileino/DT2_2019/project/workdir/input/cregs.sv:36

Type      : BLOCK_UNREACHABLE
Severity  : Caution
Status    : Uninspected
Module    : dregs
Location  : /home/so/tiileino/DT2_2019/project/workdir/input/dregs.sv:43

Type      : BLOCK_UNREACHABLE
Severity  : Caution
Status    : Uninspected
Module    : filter_unit_control
Location  : /home/so/tiileino/DT2_2019/project/workdir/input/filter_unit_control.sv:53

Type      : FSM_UNREACHABLE_TRANS
Severity  : Caution
Status    : Uninspected
Module    : filter_unit_control
Instance  : filter_unit_1.filter_unit_control_1
FSM       : state_r
Transition: READ->STOPPED
Location  : /home/so/tiileino/DT2_2019/project/workdir/input/filter_unit_control.sv:54

Type      : REG_TOGGLE_VIOLATION
Severity  : Caution
Status    : Uninspected
Module    : reset_sync
```

```
Signal    : srst_n
Instance  : reset_sync_1
Toggle    : 1'b1 -> 1'b0

------------------------------------------------------------


-------------------------------------------------------------------------------
CPU Time per Check Type
-------------------------------------------------------------------------------
%   Seconds    Check
-------------------------------------------------------------------------------
0.0%      0    ARITH_OVERFLOW_SUB
0.2%      0    ARITH_OVERFLOW_VAL
0.0%      0    ARITH_ZERO_DIV
0.0%      0    ARITH_ZERO_MOD
5.3%      8    BLOCK_UNREACHABLE
0.0%      0    BUS_MULTIPLY_DRIVEN
0.0%      0    BUS_UNDRIVEN
0.0%      0    BUS_VALUE_CONFLICT
0.0%      0    CASE_DEFAULT
0.0%      0    CASE_FULL
0.0%      0    CASE_PARALLEL
13.0%     20    FSM_DEADLOCK_STATE
35.7%     57    FSM_LOCKOUT_STATE
0.9%      1    FSM_STUCK_BIT
1.2%      1    FSM_UNREACHABLE_STATE
2.8%      4    FSM_UNREACHABLE_TRANS
0.0%      0    INDEX_ILLEGAL
0.0%      0    INIT_X_OPTIMISM
0.0%      0    INIT_X_PESSIMISM
0.0%      0    INIT_X_UNRESOLVED
0.0%      0    INIT_X_UNRESOLVED_MEM
0.0%      0    ONE_COLD
0.0%      0    ONE_HOT
0.0%      0    REG_MULTIPLY_DRIVEN
40.5%     65    REG_STUCK_AT
0.5%      0    REG_TOGGLE_VIOLATION
-------------------------------------------------------------------------------


-------------------------------------------------------------------------------
Unused autocheck_report Directives
-------------------------------------------------------------------------------
<none>
-------------------------------------------------------------------------------




--------- Process Statistics ----------
Elapsed Time                       46 s
-------- Orchestration Process --------
------- kataja2.oulu.fi:158796 --------
CPU Time                            3 s
Peak Memory                       0.4 GB
---------- Engine Processes -----------
------- kataja2.oulu.fi:158864 --------
CPU Time                           31 s
Peak Memory                       0.3 GB
CPU Utilization                   100 %
------- kataja2.oulu.fi:158866 --------
```

```
CPU Time                          31 s
Peak Memory                      0.3 GB
CPU Utilization                  100 %
------- kataja2.oulu.fi:158875 --------
CPU Time                          48 s
Peak Memory                      0.3 GB
CPU Utilization                  100 %
------- kataja2.oulu.fi:158877 --------
CPU Time                          48 s
Peak Memory                      0.2 GB
CPU Utilization                  100 %
---------------------------------------
```

A3. Synthesis Area Results Report

(From reports/4_dc_fir_filter_gatelevel_area.txt)

```
****************************************
Report : area
Design : fir_filter
Version: P-2019.03-SP4
Date   : Mon Dec 16 15:31:02 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    NangateOpenCellLibrary (File:
/usr/local/contrib/nangate/NANGate_45nm/Synopsys/NLDM/NangateOpenCellLibrary_typical.db)

Number of ports:                          333
Number of nets:                          2481
Number of cells:                         1753
Number of combinational cells:           1329
Number of sequential cells:               417
Number of macros/black boxes:               0
Number of buf/inv:                        170
Number of references:                       6

Combinational area:               2134.650031
Buf/Inv area:                      103.740000
Noncombinational area:            2215.780071
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  4350.430103
Total area:                 undefined

Hierarchical area distribution
------------------------------

                                  Global cell area          Local cell area
                                  ------------------  ----------------------------
Hierarchical cell                 Absolute   Percent  Combi-     Noncombi-  Black-
                                  Total      Total    national   national   boxes   Design
-------------------------------  ---------  -------  ---------  ---------  ------  --------
----
fir_filter                        4350.4301    100.0     3.9900     0.0000  0.0000
fir_filter
control_unit_1                      90.9720      2.1    48.4120    42.5600  0.0000
control_unit
filter_unit_1                     3398.6821     78.1  1893.1220  1505.5600  0.0000
filter_unit
```

```
i2c_slave_1                          844.2840     19.4   187.7960   624.5680  0.0000
i2c_slave
i2c_slave_1/i2c_sync_1                31.9200      0.7     0.0000    31.9200  0.0000  i2c_sync
reset_sync_1                          12.5020      0.3     1.3300    11.1720  0.0000
reset_sync
--------------------------------  ---------  -------  ---------  ---------  ------  --------
----
Total                                                  2134.6500  2215.7801  0.0000


Area of detected synthetic parts
--------------------------------
  No DW parts to report!

Estimated area of ungrouped synthetic parts
-------------------------------------------
                                      Estimated  Perc. of
  Module               Implem.  Count       Area cell area
  -------------------- -------  ----- ---------- ---------
  DP_OP_292J1_122_8099     str      1  1085.8296     25.0%
  DW01_inc             apparch      2     2.3196      0.1%
  DW_cmp               apparch      3     8.5120      0.2%
  -------------------- -------  ----- ---------- ---------
  DP_OP Subtotal:                   1  1085.8296     25.0%
  Total:                            6  1096.6612     25.2%

Subtotal of datapath(DP_OP) cell area:  1085.8296  25.0%  (estimated)
Total synthetic cell area:              1096.6612  25.2%  (estimated)

1
```

A4. Synthesis Timing Report

(From reports/4_dc_fir_filter_gatelevel_timing_setup.txt)

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fir_filter
Version: P-2019.03-SP4
Date   : Mon Dec 16 15:31:02 2019
****************************************

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: reset_sync_1/srst_n_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: filter_unit_1/cregs_1/cregs_r_reg[1][15]
            (rising-edge recovery check against clock clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fir_filter         5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  reset_sync_1/srst_n_reg/CK (DFFR_X2)                    0.00       0.00 r
  reset_sync_1/srst_n_reg/Q (DFFR_X2)                     0.13       0.13 r
  reset_sync_1/U5/ZN (INV_X1)                             0.02       0.15 f
  reset_sync_1/U4/ZN (INV_X2)                             0.17       0.32 r
  reset_sync_1/srst_n (reset_sync)                        0.00       0.32 r
  filter_unit_1/rst_n (filter_unit)                       0.00       0.32 r
  filter_unit_1/U32/Z (CLKBUF_X1)                         0.23       0.55 r
  filter_unit_1/U33/Z (CLKBUF_X1)                         0.22       0.77 r
  filter_unit_1/cregs_1/cregs_r_reg[1][15]/RN (DFFR_X1)
                                                          0.03       0.80 r
  data arrival time                                                  0.80

  clock clk (rise edge)                                   6.00       6.00
  clock network delay (ideal)                             0.00       6.00
  filter_unit_1/cregs_1/cregs_r_reg[1][15]/CK (DFFR_X1)
                                                          0.00       6.00 r
  library recovery time                                   0.03       6.03
  data required time                                                 6.03
  --------------------------------------------------------------------------
  data required time                                                 6.03
  data arrival time                                                 -0.80
  --------------------------------------------------------------------------
  slack (MET)                                                        5.23
```

```
Startpoint: sda_inout (input port clocked by clk)
Endpoint: i2c_slave_1/i2c_sync_1/sda_sff1_r_reg
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk_in2reg
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
fir_filter         5K_hvratio_1_1        NangateOpenCellLibrary

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.00       0.00
input external delay                                     1.20       1.20 f
sda_inout (inout)                                        0.00       1.20 f
i2c_slave_1/sda_inout (i2c_slave)                        0.00       1.20 f
i2c_slave_1/i2c_sync_1/sda_in (i2c_sync)                 0.00       1.20 f
i2c_slave_1/i2c_sync_1/sda_sff1_r_reg/D (DFFS_X1)        0.01       1.21 f
data arrival time                                                   1.21

clock clk (rise edge)                                    6.00       6.00
clock network delay (ideal)                              0.00       6.00
i2c_slave_1/i2c_sync_1/sda_sff1_r_reg/CK (DFFS_X1)       0.00       6.00 r
library setup time                                      -0.04       5.96
data required time                                                  5.96
-----------------------------------------------------------------------------
data required time                                                  5.96
data arrival time                                                  -1.21
-----------------------------------------------------------------------------
slack (MET)                                                        4.75


Startpoint: i2c_slave_1/i2c_fsm_1/state_r_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: sda_inout (output port clocked by clk)
Path Group: clk_reg2out
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
fir_filter         5K_hvratio_1_1        NangateOpenCellLibrary

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                    0.00       0.00
clock network delay (ideal)                              0.00       0.00
i2c_slave_1/i2c_fsm_1/state_r_reg[0]/CK (DFFS_X1)        0.00       0.00 r
i2c_slave_1/i2c_fsm_1/state_r_reg[0]/Q (DFFS_X1)         0.09       0.09 f
i2c_slave_1/U29/ZN (NOR2_X1)                             0.07       0.16 r
i2c_slave_1/valid_out (i2c_slave)                        0.00       0.16 r
control_unit_1/i2c_valid_in (control_unit)               0.00       0.16 r
control_unit_1/U32/ZN (INV_X1)                           0.03       0.20 f
control_unit_1/U33/ZN (NOR4_X1)                          0.10       0.29 r
control_unit_1/U34/ZN (NAND2_X1)                         0.04       0.33 f
control_unit_1/U35/ZN (NOR2_X1)                          0.06       0.39 r
control_unit_1/U40/ZN (INV_X1)                           0.02       0.41 f
control_unit_1/U41/ZN (NOR3_X1)                          0.06       0.47 r
```

```
control_unit_1/U42/ZN (AOI221_X1)                       0.03       0.50 f
control_unit_1/ack_out (control_unit)                   0.00       0.50 f
i2c_slave_1/ack_in (i2c_slave)                          0.00       0.50 f
i2c_slave_1/U42/ZN (OR3_X1)                             0.09       0.60 f
i2c_slave_1/sda_inout_tri/Z (TBUF_X1)                   0.06       0.65 r
i2c_slave_1/sda_inout (i2c_slave)                       0.00       0.65 r
sda_inout (inout)                                       0.00       0.65 r
data arrival time                                                  0.65

clock clk (rise edge)                                   6.00       6.00
clock network delay (ideal)                             0.00       6.00
output external delay                                  -1.20       4.80
data required time                                                 4.80
--------------------------------------------------------------------------
data required time                                                 4.80
data arrival time                                                 -0.65
--------------------------------------------------------------------------
slack (MET)                                                        4.15


Startpoint: filter_unit_1/filter_unit_control_1/state_r_reg[2]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: filter_unit_1/acc_1/acc_r_reg[37]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk_reg2reg
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
fir_filter         5K_hvratio_1_1        NangateOpenCellLibrary

Point                                                   Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
filter_unit_1/filter_unit_control_1/state_r_reg[2]/CK (DFFR_X1)
                                                        0.00       0.00 r
filter_unit_1/filter_unit_control_1/state_r_reg[2]/Q (DFFR_X1)
                                                        0.10       0.10 f
filter_unit_1/U9/ZN (NOR2_X1)                           0.09       0.19 r
filter_unit_1/U29/ZN (NAND2_X1)                         0.12       0.31 f
filter_unit_1/U28/ZN (INV_X1)                           0.07       0.38 r
filter_unit_1/U31/ZN (NAND2_X1)                         0.04       0.42 f
filter_unit_1/U44/ZN (INV_X2)                           0.16       0.57 r
filter_unit_1/U11/ZN (NOR2_X1)                          0.11       0.68 f
filter_unit_1/U1/Z (CLKBUF_X1)                          0.18       0.86 f
filter_unit_1/U83/ZN (NAND2_X1)                         0.07       0.93 r
filter_unit_1/U84/ZN (NAND4_X1)                         0.20       1.13 f
filter_unit_1/U12/ZN (INV_X2)                           0.22       1.35 r
filter_unit_1/U16/ZN (AOI22_X2)                         0.15       1.50 f
filter_unit_1/U15/ZN (OAI221_X2)                        0.14       1.63 r
filter_unit_1/U126/ZN (INV_X1)                          0.04       1.68 f
filter_unit_1/U127/ZN (OAI221_X1)                       0.04       1.72 r
filter_unit_1/U128/ZN (OAI21_X1)                        0.05       1.77 f
filter_unit_1/U163/S (HA_X1)                            0.09       1.85 f
filter_unit_1/U164/S (FA_X1)                            0.13       1.99 f
filter_unit_1/U165/CO (FA_X1)                           0.11       2.09 f
filter_unit_1/U193/CO (FA_X1)                           0.09       2.19 f
filter_unit_1/U222/CO (FA_X1)                           0.09       2.28 f
```

```
  filter_unit_1/U254/CO (FA_X1)                          0.09       2.37 f
  filter_unit_1/U284/CO (FA_X1)                          0.09       2.46 f
  filter_unit_1/U318/CO (FA_X1)                          0.09       2.55 f
  filter_unit_1/U351/CO (FA_X1)                          0.09       2.64 f
  filter_unit_1/U388/CO (FA_X1)                          0.09       2.73 f
  filter_unit_1/U426/CO (FA_X1)                          0.09       2.82 f
  filter_unit_1/U467/CO (FA_X1)                          0.09       2.91 f
  filter_unit_1/U507/CO (FA_X1)                          0.09       3.00 f
  filter_unit_1/U809/CO (FA_X1)                          0.09       3.09 f
  filter_unit_1/U893/CO (FA_X1)                          0.09       3.18 f
  filter_unit_1/U889/CO (FA_X1)                          0.09       3.27 f
  filter_unit_1/U885/CO (FA_X1)                          0.09       3.36 f
  filter_unit_1/U881/CO (FA_X1)                          0.09       3.45 f
  filter_unit_1/U877/CO (FA_X1)                          0.09       3.55 f
  filter_unit_1/U873/CO (FA_X1)                          0.09       3.64 f
  filter_unit_1/U869/CO (FA_X1)                          0.09       3.73 f
  filter_unit_1/U865/CO (FA_X1)                          0.09       3.82 f
  filter_unit_1/U861/CO (FA_X1)                          0.09       3.91 f
  filter_unit_1/U857/CO (FA_X1)                          0.09       4.00 f
  filter_unit_1/U853/CO (FA_X1)                          0.09       4.09 f
  filter_unit_1/U849/CO (FA_X1)                          0.09       4.18 f
  filter_unit_1/U845/CO (FA_X1)                          0.09       4.27 f
  filter_unit_1/U841/CO (FA_X1)                          0.09       4.36 f
  filter_unit_1/U837/CO (FA_X1)                          0.09       4.45 f
  filter_unit_1/U833/CO (FA_X1)                          0.09       4.54 f
  filter_unit_1/U830/CO (FA_X1)                          0.09       4.63 f
  filter_unit_1/U827/CO (FA_X1)                          0.09       4.72 f
  filter_unit_1/U824/CO (FA_X1)                          0.09       4.81 f
  filter_unit_1/U821/CO (FA_X1)                          0.09       4.90 f
  filter_unit_1/U818/CO (FA_X1)                          0.09       5.00 f
  filter_unit_1/U815/CO (FA_X1)                          0.09       5.08 f
  filter_unit_1/U810/ZN (XNOR2_X1)                       0.06       5.14 f
  filter_unit_1/U811/ZN (XNOR2_X1)                       0.06       5.20 f
  filter_unit_1/U812/ZN (AOI22_X1)                       0.06       5.26 r
  filter_unit_1/U814/ZN (NAND2_X1)                       0.03       5.29 f
  filter_unit_1/acc_1/acc_r_reg[37]/D (DFFR_X1)          0.01       5.30 f
  data arrival time                                                 5.30

  clock clk (rise edge)                                  6.00       6.00
  clock network delay (ideal)                            0.00       6.00
  filter_unit_1/acc_1/acc_r_reg[37]/CK (DFFR_X1)         0.00       6.00 r
  library setup time                                    -0.04       5.96
  data required time                                                5.96
  ------------------------------------------------------------------------
  data required time                                                5.96
  data arrival time                                                -5.30
  ------------------------------------------------------------------------
  slack (MET)                                                       0.66


1
```

A5. Synthesis Reference Report

(From eports/4_dc_fir_filter_gatelevel_reference.txt)

```
****************************************
Report : reference
Design : fir_filter
Version: P-2019.03-SP4
Date   : Mon Dec 16 15:31:02 2019
****************************************

Attributes:
    b - black box (unknown)
   bo - allows boundary optimization
    d - dont_touch
   mo - map_only
    h - hierarchical
    n - noncombinational
    r - removable
    s - synthetic operator
    u - contains unmapped logic

Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
INV_X1             NangateOpenCellLibrary
                                  0.532000       3      1.596000
INV_X8             NangateOpenCellLibrary
                                  2.394000       1      2.394000
control_unit                     90.972002       1     90.972002  h, n
filter_unit                    3398.682075       1   3398.682075  h, n
i2c_slave                       844.284026       1    844.284026  h, n
reset_sync                       12.502000       1     12.502000  h, n
--------------------------------------------------------------------------------
Total 6 references                                  4350.430103

****************************************
Design: control_unit
****************************************
Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
AND4_X1            NangateOpenCellLibrary
                                  1.596000       1      1.596000
AOI21_X1           NangateOpenCellLibrary
                                  1.064000       3      3.192000
AOI22_X1           NangateOpenCellLibrary
                                  1.330000       4      5.320000
AOI211_X1          NangateOpenCellLibrary
                                  1.330000       1      1.330000
AOI221_X1          NangateOpenCellLibrary
                                  1.596000       2      3.192000
DFFR_X1            NangateOpenCellLibrary
```

```
                                5.320000        8     42.560001  n
INV_X1              NangateOpenCellLibrary
                                0.532000        8      4.256000
NAND2_X1            NangateOpenCellLibrary
                                0.798000        8      6.384000
NAND3_X1            NangateOpenCellLibrary
                                1.064000        3      3.192000
NAND4_X1            NangateOpenCellLibrary
                                1.330000        2      2.660000
NOR2_X1             NangateOpenCellLibrary
                                0.798000        5      3.990000
NOR3_X1             NangateOpenCellLibrary
                                1.064000        3      3.192000
NOR4_X1             NangateOpenCellLibrary
                                1.330000        2      2.660000
OAI21_X1            NangateOpenCellLibrary
                                1.064000        4      4.256000
OR3_X1              NangateOpenCellLibrary
                                1.330000        1      1.330000
OR4_X2              NangateOpenCellLibrary
                                1.862000        1      1.862000
------------------------------------------------------------------------------
Total 16 references                                    90.972002

**************************************
Design: filter_unit
**************************************
Reference           Library       Unit Area   Count    Total Area   Attributes
------------------------------------------------------------------------------
AND2_X2             NangateOpenCellLibrary
                                1.330000        1      1.330000
AND4_X1             NangateOpenCellLibrary
                                1.596000        1      1.596000
AOI21_X1            NangateOpenCellLibrary
                                1.064000        3      3.192000
AOI21_X2            NangateOpenCellLibrary
                                1.862000        1      1.862000
AOI21_X4            NangateOpenCellLibrary
                                3.458000        1      3.458000
AOI22_X1            NangateOpenCellLibrary
                                1.330000      252    335.160011
AOI22_X2            NangateOpenCellLibrary
                                2.394000        5     11.970000
AOI221_X1           NangateOpenCellLibrary
                                1.596000        9     14.364000
AOI222_X1           NangateOpenCellLibrary
                                2.128000       15     31.920000
CLKBUF_X1           NangateOpenCellLibrary
                                0.798000       27     21.545999
CLKBUF_X2           NangateOpenCellLibrary
                                1.064000        2      2.128000
DFFR_X1             NangateOpenCellLibrary
```

```
                                5.320000     282   1500.240048  n
DFFS_X1            NangateOpenCellLibrary
                                5.320000       1      5.320000  n
FA_X1              NangateOpenCellLibrary
                                4.256000     155    659.680007  r
HA_X1              NangateOpenCellLibrary
                                2.660000       9     23.940001  r
INV_X1             NangateOpenCellLibrary
                                0.532000     104     55.328001
INV_X2             NangateOpenCellLibrary
                                0.798000       3      2.394000
MUX2_X1            NangateOpenCellLibrary
                                1.862000     126    234.611999
NAND2_X1           NangateOpenCellLibrary
                                0.798000      67     53.465999
NAND3_X1           NangateOpenCellLibrary
                                1.064000       5      5.320000
NAND4_X1           NangateOpenCellLibrary
                                1.330000      33     43.890001
NOR2_X1            NangateOpenCellLibrary
                                0.798000      28     22.343999
NOR3_X1            NangateOpenCellLibrary
                                1.064000       2      2.128000
NOR4_X1            NangateOpenCellLibrary
                                1.330000       3      3.990000
OAI21_X1           NangateOpenCellLibrary
                                1.064000      39     41.496000
OAI22_X1           NangateOpenCellLibrary
                                1.330000     211    280.630009
OAI211_X2          NangateOpenCellLibrary
                                2.394000       1      2.394000
OAI221_X1          NangateOpenCellLibrary
                                1.596000       7     11.172000
OAI221_X2          NangateOpenCellLibrary
                                2.926000       5     14.630001
OR2_X1             NangateOpenCellLibrary
                                1.064000       1      1.064000
OR3_X1             NangateOpenCellLibrary
                                1.330000       1      1.330000
XNOR2_X1           NangateOpenCellLibrary
                                1.596000       3      4.788000
--------------------------------------------------------------------------------
Total 32 references                            3398.682075

****************************************
Design: i2c_slave
****************************************
Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
AOI21_X1           NangateOpenCellLibrary
                                1.064000       3      3.192000
AOI22_X1           NangateOpenCellLibrary
```

```
                                1.330000     112    148.960005
CLKBUF_X1          NangateOpenCellLibrary
                                0.798000       6      4.788000
CLKBUF_X2          NangateOpenCellLibrary
                                1.064000       1      1.064000
DFFR_X1            NangateOpenCellLibrary
                                5.320000     116    617.120020  n
DFFS_X1            NangateOpenCellLibrary
                                5.320000       1      5.320000  n
INV_X1             NangateOpenCellLibrary
                                0.532000      13      6.916000
MUX2_X1            NangateOpenCellLibrary
                                1.862000       1      1.862000
NAND2_X1           NangateOpenCellLibrary
                                0.798000       3      2.394000
NAND3_X1           NangateOpenCellLibrary
                                1.064000       1      1.064000
NOR2_X1            NangateOpenCellLibrary
                                0.798000       3      2.394000
NOR3_X1            NangateOpenCellLibrary
                                1.064000       3      3.192000
NOR3_X2            NangateOpenCellLibrary
                                1.862000       1      1.862000
OAI21_X1           NangateOpenCellLibrary
                                1.064000       1      1.064000
OAI22_X1           NangateOpenCellLibrary
                                1.330000       3      3.990000
OR2_X1             NangateOpenCellLibrary
                                1.064000       2      2.128000
OR3_X1             NangateOpenCellLibrary
                                1.330000       1      1.330000
TBUF_X1            NangateOpenCellLibrary
                                2.128000       1      2.128000  n
XNOR2_X1           NangateOpenCellLibrary
                                1.596000       1      1.596000
i2c_sync                       31.920001       1     31.920001  h, n
--------------------------------------------------------------------------------
Total 20 references                                  844.284026

****************************************
Design: i2c_sync
****************************************
Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
DFFS_X1            NangateOpenCellLibrary
                                5.320000       6     31.920001  n
--------------------------------------------------------------------------------
Total 1 references                                    31.920001

****************************************
Design: reset_sync
****************************************
```

```
Reference           Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
DFFR_X1             NangateOpenCellLibrary
                                  5.320000       1      5.320000  n
DFFR_X2             NangateOpenCellLibrary
                                  5.852000       1      5.852000  n
INV_X1              NangateOpenCellLibrary
                                  0.532000       1      0.532000
INV_X2              NangateOpenCellLibrary
                                  0.798000       1      0.798000
--------------------------------------------------------------------------------
Total 4 references                                      12.502000
1
```

A6. Formal Logic Equivalence Check Status Report

(From: reports/5_formality_fir_filter_gatelevel_status_report.txt)

```
*********************************************
Report         : status

Reference      : r:/WORK/fir_filter
Implementation : i:/WORK/fir_filter
Version        : N-2017.09-SP3
Date           : Mon Dec 16 15:33:12 2019
*********************************************

*************************** Synopsys Auto Setup Summary ****************************

!!! Synopsys Auto Setup Mode was enabled. !!!
!!! Verification results are valid assuming the following setup constraints: !!!

### RTL Interpretation Setup
   set hdlin_ignore_parallel_case false
   set hdlin_ignore_full_case false
   set hdlin_error_on_mismatch_message false
   set hdlin_ignore_embedded_configuration true

### Undriven Signal Handling Setup
   set verification_set_undriven_signals synthesis

### Test Logic Setup
   set verification_verify_directly_undriven_output false
   For details see report_dont_verify_points and report_constants


For further details on Synopsys Auto Setup Mode: Type man synopsys_auto_setup
*******************************************************************************



****************************** Verification Results ******************************
Verification SUCCEEDED
   ATTENTION: synopsys_auto_setup mode was enabled.
              See Synopsys Auto Setup Summary for details.
   ATTENTION: RTL interpretation messages were produced during link
              of reference design.
              Verification results may disagree with a logic simulator.
---------------------------------------------------------------------
Reference design: r:/WORK/fir_filter
Implementation design: i:/WORK/fir_filter
436 Passing compare points
-------------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT   TOTAL
-------------------------------------------------------------------------------------
Passing (equivalent)           0       0       1       0      19     416       0     436
Failing (not equivalent)       0       0       0       0       0       0       0       0
*************************************************************************************
1
```