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\*/

/\* $Id: iom328p.h 2444 2014-08-11 22:10:47Z joerg\_wunsch $ \*/

/\* avr/iom328p.h - definitions for ATmega328P. \*/

/\* This file should only be included from <avr/io.h>, never directly. \*/

#ifndef \_AVR\_IO\_H\_

#  error "Include <avr/io.h> instead of this file."

#endif

#ifndef \_AVR\_IOXXX\_H\_

#  define \_AVR\_IOXXX\_H\_ "iom328p.h"

#else

#  error "Attempt to include more than one <avr/ioXXX.h> file."

#endif

#ifndef \_AVR\_IOM328P\_H\_

#define \_AVR\_IOM328P\_H\_ 1

/\* Registers and associated bit numbers \*/

#define PINB \_SFR\_IO8(0x03)

#define PINB0 0

#define PINB1 1

#define PINB2 2

#define PINB3 3

#define PINB4 4

#define PINB5 5

#define PINB6 6

#define PINB7 7

#define DDRB \_SFR\_IO8(0x04)

#define DDB0 0

#define DDB1 1

#define DDB2 2

#define DDB3 3

#define DDB4 4

#define DDB5 5

#define DDB6 6

#define DDB7 7

#define PORTB \_SFR\_IO8(0x05)

#define PORTB0 0

#define PORTB1 1

#define PORTB2 2

#define PORTB3 3

#define PORTB4 4

#define PORTB5 5

#define PORTB6 6

#define PORTB7 7

#define PINC \_SFR\_IO8(0x06)

#define PINC0 0

#define PINC1 1

#define PINC2 2

#define PINC3 3

#define PINC4 4

#define PINC5 5

#define PINC6 6

#define DDRC \_SFR\_IO8(0x07)

#define DDC0 0

#define DDC1 1

#define DDC2 2

#define DDC3 3

#define DDC4 4

#define DDC5 5

#define DDC6 6

#define PORTC \_SFR\_IO8(0x08)

#define PORTC0 0

#define PORTC1 1

#define PORTC2 2

#define PORTC3 3

#define PORTC4 4

#define PORTC5 5

#define PORTC6 6

#define PIND \_SFR\_IO8(0x09)

#define PIND0 0

#define PIND1 1

#define PIND2 2

#define PIND3 3

#define PIND4 4

#define PIND5 5

#define PIND6 6

#define PIND7 7

#define DDRD \_SFR\_IO8(0x0A)

#define DDD0 0

#define DDD1 1

#define DDD2 2

#define DDD3 3

#define DDD4 4

#define DDD5 5

#define DDD6 6

#define DDD7 7

#define PORTD \_SFR\_IO8(0x0B)

#define PORTD0 0

#define PORTD1 1

#define PORTD2 2

#define PORTD3 3

#define PORTD4 4

#define PORTD5 5

#define PORTD6 6

#define PORTD7 7

#define TIFR0 \_SFR\_IO8(0x15)

#define TOV0 0

#define OCF0A 1

#define OCF0B 2

#define TIFR1 \_SFR\_IO8(0x16)

#define TOV1 0

#define OCF1A 1

#define OCF1B 2

#define ICF1 5

#define TIFR2 \_SFR\_IO8(0x17)

#define TOV2 0

#define OCF2A 1

#define OCF2B 2

#define PCIFR \_SFR\_IO8(0x1B)

#define PCIF0 0

#define PCIF1 1

#define PCIF2 2

#define EIFR \_SFR\_IO8(0x1C)

#define INTF0 0

#define INTF1 1

#define EIMSK \_SFR\_IO8(0x1D)

#define INT0 0

#define INT1 1

#define GPIOR0 \_SFR\_IO8(0x1E)

#define GPIOR00 0

#define GPIOR01 1

#define GPIOR02 2

#define GPIOR03 3

#define GPIOR04 4

#define GPIOR05 5

#define GPIOR06 6

#define GPIOR07 7

#define EECR \_SFR\_IO8(0x1F)

#define EERE 0

#define EEPE 1

#define EEMPE 2

#define EERIE 3

#define EEPM0 4

#define EEPM1 5

#define EEDR \_SFR\_IO8(0x20)

#define EEDR0 0

#define EEDR1 1

#define EEDR2 2

#define EEDR3 3

#define EEDR4 4

#define EEDR5 5

#define EEDR6 6

#define EEDR7 7

#define EEAR \_SFR\_IO16(0x21)

#define EEARL \_SFR\_IO8(0x21)

#define EEAR0 0

#define EEAR1 1

#define EEAR2 2

#define EEAR3 3

#define EEAR4 4

#define EEAR5 5

#define EEAR6 6

#define EEAR7 7

#define EEARH \_SFR\_IO8(0x22)

#define EEAR8 0

#define EEAR9 1

#define \_EEPROM\_REG\_LOCATIONS\_ 1F2021

#define GTCCR \_SFR\_IO8(0x23)

#define PSRSYNC 0

#define PSRASY 1

#define TSM 7

#define TCCR0A \_SFR\_IO8(0x24)

#define WGM00 0

#define WGM01 1

#define COM0B0 4

#define COM0B1 5

#define COM0A0 6

#define COM0A1 7

#define TCCR0B \_SFR\_IO8(0x25)

#define CS00 0

#define CS01 1

#define CS02 2

#define WGM02 3

#define FOC0B 6

#define FOC0A 7

#define TCNT0 \_SFR\_IO8(0x26)

#define TCNT0\_0 0

#define TCNT0\_1 1

#define TCNT0\_2 2

#define TCNT0\_3 3

#define TCNT0\_4 4

#define TCNT0\_5 5

#define TCNT0\_6 6

#define TCNT0\_7 7

#define OCR0A \_SFR\_IO8(0x27)

#define OCR0A\_0 0

#define OCR0A\_1 1

#define OCR0A\_2 2

#define OCR0A\_3 3

#define OCR0A\_4 4

#define OCR0A\_5 5

#define OCR0A\_6 6

#define OCR0A\_7 7

#define OCR0B \_SFR\_IO8(0x28)

#define OCR0B\_0 0

#define OCR0B\_1 1

#define OCR0B\_2 2

#define OCR0B\_3 3

#define OCR0B\_4 4

#define OCR0B\_5 5

#define OCR0B\_6 6

#define OCR0B\_7 7

#define GPIOR1 \_SFR\_IO8(0x2A)

#define GPIOR10 0

#define GPIOR11 1

#define GPIOR12 2

#define GPIOR13 3

#define GPIOR14 4

#define GPIOR15 5

#define GPIOR16 6

#define GPIOR17 7

#define GPIOR2 \_SFR\_IO8(0x2B)

#define GPIOR20 0

#define GPIOR21 1

#define GPIOR22 2

#define GPIOR23 3

#define GPIOR24 4

#define GPIOR25 5

#define GPIOR26 6

#define GPIOR27 7

#define SPCR \_SFR\_IO8(0x2C)

#define SPR0 0

#define SPR1 1

#define CPHA 2

#define CPOL 3

#define MSTR 4

#define DORD 5

#define SPE 6

#define SPIE 7

#define SPSR \_SFR\_IO8(0x2D)

#define SPI2X 0

#define WCOL 6

#define SPIF 7

#define SPDR \_SFR\_IO8(0x2E)

#define SPDR0 0

#define SPDR1 1

#define SPDR2 2

#define SPDR3 3

#define SPDR4 4

#define SPDR5 5

#define SPDR6 6

#define SPDR7 7

#define ACSR \_SFR\_IO8(0x30)

#define ACIS0 0

#define ACIS1 1

#define ACIC 2

#define ACIE 3

#define ACI 4

#define ACO 5

#define ACBG 6

#define ACD 7

#define SMCR \_SFR\_IO8(0x33)

#define SE 0

#define SM0 1

#define SM1 2

#define SM2 3

#define MCUSR \_SFR\_IO8(0x34)

#define PORF 0

#define EXTRF 1

#define BORF 2

#define WDRF 3

#define MCUCR \_SFR\_IO8(0x35)

#define IVCE 0

#define IVSEL 1

#define PUD 4

#define BODSE 5

#define BODS 6

#define SPMCSR \_SFR\_IO8(0x37)

#define SELFPRGEN 0 /\* only for backwards compatibility with previous

         \* avr-libc versions; not an official name \*/

#define SPMEN 0

#define PGERS 1

#define PGWRT 2

#define BLBSET 3

#define RWWSRE 4

#define SIGRD 5

#define RWWSB 6

#define SPMIE 7

#define WDTCSR \_SFR\_MEM8(0x60)

#define WDP0 0

#define WDP1 1

#define WDP2 2

#define WDE 3

#define WDCE 4

#define WDP3 5

#define WDIE 6

#define WDIF 7

#define CLKPR \_SFR\_MEM8(0x61)

#define CLKPS0 0

#define CLKPS1 1

#define CLKPS2 2

#define CLKPS3 3

#define CLKPCE 7

#define PRR \_SFR\_MEM8(0x64)

#define PRADC 0

#define PRUSART0 1

#define PRSPI 2

#define PRTIM1 3

#define PRTIM0 5

#define PRTIM2 6

#define PRTWI 7

#define \_\_AVR\_HAVE\_PRR  ((1<<PRADC)|(1<<PRUSART0)|(1<<PRSPI)|(1<<PRTIM1)|(1<<PRTIM0)|(1<<PRTIM2)|(1<<PRTWI))

#define \_\_AVR\_HAVE\_PRR\_PRADC

#define \_\_AVR\_HAVE\_PRR\_PRUSART0

#define \_\_AVR\_HAVE\_PRR\_PRSPI

#define \_\_AVR\_HAVE\_PRR\_PRTIM1

#define \_\_AVR\_HAVE\_PRR\_PRTIM0

#define \_\_AVR\_HAVE\_PRR\_PRTIM2

#define \_\_AVR\_HAVE\_PRR\_PRTWI

#define OSCCAL \_SFR\_MEM8(0x66)

#define CAL0 0

#define CAL1 1

#define CAL2 2

#define CAL3 3

#define CAL4 4

#define CAL5 5

#define CAL6 6

#define CAL7 7

#define PCICR \_SFR\_MEM8(0x68)

#define PCIE0 0

#define PCIE1 1

#define PCIE2 2

#define EICRA \_SFR\_MEM8(0x69)

#define ISC00 0

#define ISC01 1

#define ISC10 2

#define ISC11 3

#define PCMSK0 \_SFR\_MEM8(0x6B)

#define PCINT0 0

#define PCINT1 1

#define PCINT2 2

#define PCINT3 3

#define PCINT4 4

#define PCINT5 5

#define PCINT6 6

#define PCINT7 7

#define PCMSK1 \_SFR\_MEM8(0x6C)

#define PCINT8 0

#define PCINT9 1

#define PCINT10 2

#define PCINT11 3

#define PCINT12 4

#define PCINT13 5

#define PCINT14 6

#define PCMSK2 \_SFR\_MEM8(0x6D)

#define PCINT16 0

#define PCINT17 1

#define PCINT18 2

#define PCINT19 3

#define PCINT20 4

#define PCINT21 5

#define PCINT22 6

#define PCINT23 7

#define TIMSK0 \_SFR\_MEM8(0x6E)

#define TOIE0 0

#define OCIE0A 1

#define OCIE0B 2

#define TIMSK1 \_SFR\_MEM8(0x6F)

#define TOIE1 0

#define OCIE1A 1

#define OCIE1B 2

#define ICIE1 5

#define TIMSK2 \_SFR\_MEM8(0x70)

#define TOIE2 0

#define OCIE2A 1

#define OCIE2B 2

#ifndef \_\_ASSEMBLER\_\_

#define ADC     \_SFR\_MEM16(0x78)

#endif

#define ADCW    \_SFR\_MEM16(0x78)

#define ADCL \_SFR\_MEM8(0x78)

#define ADCL0 0

#define ADCL1 1

#define ADCL2 2

#define ADCL3 3

#define ADCL4 4

#define ADCL5 5

#define ADCL6 6

#define ADCL7 7

#define ADCH \_SFR\_MEM8(0x79)

#define ADCH0 0

#define ADCH1 1

#define ADCH2 2

#define ADCH3 3

#define ADCH4 4

#define ADCH5 5

#define ADCH6 6

#define ADCH7 7

#define ADCSRA \_SFR\_MEM8(0x7A)

#define ADPS0 0

#define ADPS1 1

#define ADPS2 2

#define ADIE 3

#define ADIF 4

#define ADATE 5

#define ADSC 6

#define ADEN 7

#define ADCSRB \_SFR\_MEM8(0x7B)

#define ADTS0 0

#define ADTS1 1

#define ADTS2 2

#define ACME 6

#define ADMUX \_SFR\_MEM8(0x7C)

#define MUX0 0

#define MUX1 1

#define MUX2 2

#define MUX3 3

#define ADLAR 5

#define REFS0 6

#define REFS1 7

#define DIDR0 \_SFR\_MEM8(0x7E)

#define ADC0D 0

#define ADC1D 1

#define ADC2D 2

#define ADC3D 3

#define ADC4D 4

#define ADC5D 5

#define DIDR1 \_SFR\_MEM8(0x7F)

#define AIN0D 0

#define AIN1D 1

#define TCCR1A \_SFR\_MEM8(0x80)

#define WGM10 0

#define WGM11 1

#define COM1B0 4

#define COM1B1 5

#define COM1A0 6

#define COM1A1 7

#define TCCR1B \_SFR\_MEM8(0x81)

#define CS10 0

#define CS11 1

#define CS12 2

#define WGM12 3

#define WGM13 4

#define ICES1 6

#define ICNC1 7

#define TCCR1C \_SFR\_MEM8(0x82)

#define FOC1B 6

#define FOC1A 7

#define TCNT1 \_SFR\_MEM16(0x84)

#define TCNT1L \_SFR\_MEM8(0x84)

#define TCNT1L0 0

#define TCNT1L1 1

#define TCNT1L2 2

#define TCNT1L3 3

#define TCNT1L4 4

#define TCNT1L5 5

#define TCNT1L6 6

#define TCNT1L7 7

#define TCNT1H \_SFR\_MEM8(0x85)

#define TCNT1H0 0

#define TCNT1H1 1

#define TCNT1H2 2

#define TCNT1H3 3

#define TCNT1H4 4

#define TCNT1H5 5

#define TCNT1H6 6

#define TCNT1H7 7

#define ICR1 \_SFR\_MEM16(0x86)

#define ICR1L \_SFR\_MEM8(0x86)

#define ICR1L0 0

#define ICR1L1 1

#define ICR1L2 2

#define ICR1L3 3

#define ICR1L4 4

#define ICR1L5 5

#define ICR1L6 6

#define ICR1L7 7

#define ICR1H \_SFR\_MEM8(0x87)

#define ICR1H0 0

#define ICR1H1 1

#define ICR1H2 2

#define ICR1H3 3

#define ICR1H4 4

#define ICR1H5 5

#define ICR1H6 6

#define ICR1H7 7

#define OCR1A \_SFR\_MEM16(0x88)

#define OCR1AL \_SFR\_MEM8(0x88)

#define OCR1AL0 0

#define OCR1AL1 1

#define OCR1AL2 2

#define OCR1AL3 3

#define OCR1AL4 4

#define OCR1AL5 5

#define OCR1AL6 6

#define OCR1AL7 7

#define OCR1AH \_SFR\_MEM8(0x89)

#define OCR1AH0 0

#define OCR1AH1 1

#define OCR1AH2 2

#define OCR1AH3 3

#define OCR1AH4 4

#define OCR1AH5 5

#define OCR1AH6 6

#define OCR1AH7 7

#define OCR1B \_SFR\_MEM16(0x8A)

#define OCR1BL \_SFR\_MEM8(0x8A)

#define OCR1BL0 0

#define OCR1BL1 1

#define OCR1BL2 2

#define OCR1BL3 3

#define OCR1BL4 4

#define OCR1BL5 5

#define OCR1BL6 6

#define OCR1BL7 7

#define OCR1BH \_SFR\_MEM8(0x8B)

#define OCR1BH0 0

#define OCR1BH1 1

#define OCR1BH2 2

#define OCR1BH3 3

#define OCR1BH4 4

#define OCR1BH5 5

#define OCR1BH6 6

#define OCR1BH7 7

#define TCCR2A \_SFR\_MEM8(0xB0)

#define WGM20 0

#define WGM21 1

#define COM2B0 4

#define COM2B1 5

#define COM2A0 6

#define COM2A1 7

#define TCCR2B \_SFR\_MEM8(0xB1)

#define CS20 0

#define CS21 1

#define CS22 2

#define WGM22 3

#define FOC2B 6

#define FOC2A 7

#define TCNT2 \_SFR\_MEM8(0xB2)

#define TCNT2\_0 0

#define TCNT2\_1 1

#define TCNT2\_2 2

#define TCNT2\_3 3

#define TCNT2\_4 4

#define TCNT2\_5 5

#define TCNT2\_6 6

#define TCNT2\_7 7

#define OCR2A \_SFR\_MEM8(0xB3)

#define OCR2\_0 0

#define OCR2\_1 1

#define OCR2\_2 2

#define OCR2\_3 3

#define OCR2\_4 4

#define OCR2\_5 5

#define OCR2\_6 6

#define OCR2\_7 7

#define OCR2B \_SFR\_MEM8(0xB4)

#define OCR2\_0 0

#define OCR2\_1 1

#define OCR2\_2 2

#define OCR2\_3 3

#define OCR2\_4 4

#define OCR2\_5 5

#define OCR2\_6 6

#define OCR2\_7 7

#define ASSR \_SFR\_MEM8(0xB6)

#define TCR2BUB 0

#define TCR2AUB 1

#define OCR2BUB 2

#define OCR2AUB 3

#define TCN2UB 4

#define AS2 5

#define EXCLK 6

#define TWBR \_SFR\_MEM8(0xB8)

#define TWBR0 0

#define TWBR1 1

#define TWBR2 2

#define TWBR3 3

#define TWBR4 4

#define TWBR5 5

#define TWBR6 6

#define TWBR7 7

#define TWSR \_SFR\_MEM8(0xB9)

#define TWPS0 0

#define TWPS1 1

#define TWS3 3

#define TWS4 4

#define TWS5 5

#define TWS6 6

#define TWS7 7

#define TWAR \_SFR\_MEM8(0xBA)

#define TWGCE 0

#define TWA0 1

#define TWA1 2

#define TWA2 3

#define TWA3 4

#define TWA4 5

#define TWA5 6

#define TWA6 7

#define TWDR \_SFR\_MEM8(0xBB)

#define TWD0 0

#define TWD1 1

#define TWD2 2

#define TWD3 3

#define TWD4 4

#define TWD5 5

#define TWD6 6

#define TWD7 7

#define TWCR \_SFR\_MEM8(0xBC)

#define TWIE 0

#define TWEN 2

#define TWWC 3

#define TWSTO 4

#define TWSTA 5

#define TWEA 6

#define TWINT 7

#define TWAMR \_SFR\_MEM8(0xBD)

#define TWAM0 0

#define TWAM1 1

#define TWAM2 2

#define TWAM3 3

#define TWAM4 4

#define TWAM5 5

#define TWAM6 6

#define UCSR0A \_SFR\_MEM8(0xC0)

#define MPCM0 0

#define U2X0 1

#define UPE0 2

#define DOR0 3

#define FE0 4

#define UDRE0 5

#define TXC0 6

#define RXC0 7

#define UCSR0B \_SFR\_MEM8(0xC1)

#define TXB80 0

#define RXB80 1

#define UCSZ02 2

#define TXEN0 3

#define RXEN0 4

#define UDRIE0 5

#define TXCIE0 6

#define RXCIE0 7

#define UCSR0C \_SFR\_MEM8(0xC2)

#define UCPOL0 0

#define UCSZ00 1

#define UCPHA0 1

#define UCSZ01 2

#define UDORD0 2

#define USBS0 3

#define UPM00 4

#define UPM01 5

#define UMSEL00 6

#define UMSEL01 7

#define UBRR0 \_SFR\_MEM16(0xC4)

#define UBRR0L \_SFR\_MEM8(0xC4)

#define UBRR0\_0 0

#define UBRR0\_1 1

#define UBRR0\_2 2

#define UBRR0\_3 3

#define UBRR0\_4 4

#define UBRR0\_5 5

#define UBRR0\_6 6

#define UBRR0\_7 7

#define UBRR0H \_SFR\_MEM8(0xC5)

#define UBRR0\_8 0

#define UBRR0\_9 1

#define UBRR0\_10 2

#define UBRR0\_11 3

#define UDR0 \_SFR\_MEM8(0xC6)

#define UDR0\_0 0

#define UDR0\_1 1

#define UDR0\_2 2

#define UDR0\_3 3

#define UDR0\_4 4

#define UDR0\_5 5

#define UDR0\_6 6

#define UDR0\_7 7

/\* Interrupt Vectors \*/

/\* Interrupt Vector 0 is the reset vector. \*/

#define INT0\_vect\_num     1

#define INT0\_vect         \_VECTOR(1)   /\* External Interrupt Request 0 \*/

#define INT1\_vect\_num     2

#define INT1\_vect         \_VECTOR(2)   /\* External Interrupt Request 1 \*/

#define PCINT0\_vect\_num   3

#define PCINT0\_vect       \_VECTOR(3)   /\* Pin Change Interrupt Request 0 \*/

#define PCINT1\_vect\_num   4

#define PCINT1\_vect       \_VECTOR(4)   /\* Pin Change Interrupt Request 0 \*/

#define PCINT2\_vect\_num   5

#define PCINT2\_vect       \_VECTOR(5)   /\* Pin Change Interrupt Request 1 \*/

#define WDT\_vect\_num      6

#define WDT\_vect          \_VECTOR(6)   /\* Watchdog Time-out Interrupt \*/

#define TIMER2\_COMPA\_vect\_num 7

#define TIMER2\_COMPA\_vect \_VECTOR(7)   /\* Timer/Counter2 Compare Match A \*/

#define TIMER2\_COMPB\_vect\_num 8

#define TIMER2\_COMPB\_vect \_VECTOR(8)   /\* Timer/Counter2 Compare Match A \*/

#define TIMER2\_OVF\_vect\_num   9

#define TIMER2\_OVF\_vect   \_VECTOR(9)   /\* Timer/Counter2 Overflow \*/

#define TIMER1\_CAPT\_vect\_num  10

#define TIMER1\_CAPT\_vect  \_VECTOR(10)  /\* Timer/Counter1 Capture Event \*/

#define TIMER1\_COMPA\_vect\_num 11

#define TIMER1\_COMPA\_vect \_VECTOR(11)  /\* Timer/Counter1 Compare Match A \*/

#define TIMER1\_COMPB\_vect\_num 12

#define TIMER1\_COMPB\_vect \_VECTOR(12)  /\* Timer/Counter1 Compare Match B \*/

#define TIMER1\_OVF\_vect\_num   13

#define TIMER1\_OVF\_vect   \_VECTOR(13)  /\* Timer/Counter1 Overflow \*/

#define TIMER0\_COMPA\_vect\_num 14

#define TIMER0\_COMPA\_vect \_VECTOR(14)  /\* TimerCounter0 Compare Match A \*/

#define TIMER0\_COMPB\_vect\_num 15

#define TIMER0\_COMPB\_vect \_VECTOR(15)  /\* TimerCounter0 Compare Match B \*/

#define TIMER0\_OVF\_vect\_num  16

#define TIMER0\_OVF\_vect   \_VECTOR(16)  /\* Timer/Couner0 Overflow \*/

#define SPI\_STC\_vect\_num  17

#define SPI\_STC\_vect      \_VECTOR(17)  /\* SPI Serial Transfer Complete \*/

#define USART\_RX\_vect\_num 18

#define USART\_RX\_vect     \_VECTOR(18)  /\* USART Rx Complete \*/

#define USART\_UDRE\_vect\_num   19

#define USART\_UDRE\_vect   \_VECTOR(19)  /\* USART, Data Register Empty \*/

#define USART\_TX\_vect\_num 20

#define USART\_TX\_vect     \_VECTOR(20)  /\* USART Tx Complete \*/

#define ADC\_vect\_num      21

#define ADC\_vect          \_VECTOR(21)  /\* ADC Conversion Complete \*/

#define EE\_READY\_vect\_num 22

#define EE\_READY\_vect     \_VECTOR(22)  /\* EEPROM Ready \*/

#define ANALOG\_COMP\_vect\_num  23

#define ANALOG\_COMP\_vect  \_VECTOR(23)  /\* Analog Comparator \*/

#define TWI\_vect\_num      24

#define TWI\_vect          \_VECTOR(24)  /\* Two-wire Serial Interface \*/

#define SPM\_READY\_vect\_num    25

#define SPM\_READY\_vect    \_VECTOR(25)  /\* Store Program Memory Read \*/

#define \_VECTORS\_SIZE (26 \* 4)

/\* Constants \*/

#define SPM\_PAGESIZE 128

#define RAMSTART     (0x100)

#define RAMEND       0x8FF     /\* Last On-Chip SRAM Location \*/

#define XRAMSIZE     0

#define XRAMEND      RAMEND

#define E2END        0x3FF

#define E2PAGESIZE   4

#define FLASHEND     0x7FFF

/\* Fuses \*/

#define FUSE\_MEMORY\_SIZE 3

/\* Low Fuse Byte \*/

#define FUSE\_CKSEL0 (unsigned char)~\_BV(0)  /\* Select Clock Source \*/

#define FUSE\_CKSEL1 (unsigned char)~\_BV(1)  /\* Select Clock Source \*/

#define FUSE\_CKSEL2 (unsigned char)~\_BV(2)  /\* Select Clock Source \*/

#define FUSE\_CKSEL3 (unsigned char)~\_BV(3)  /\* Select Clock Source \*/

#define FUSE\_SUT0   (unsigned char)~\_BV(4)  /\* Select start-up time \*/

#define FUSE\_SUT1   (unsigned char)~\_BV(5)  /\* Select start-up time \*/

#define FUSE\_CKOUT  (unsigned char)~\_BV(6)  /\* Clock output \*/

#define FUSE\_CKDIV8 (unsigned char)~\_BV(7) /\* Divide clock by 8 \*/

#define LFUSE\_DEFAULT (FUSE\_CKSEL0 & FUSE\_CKSEL2 & FUSE\_CKSEL3 & FUSE\_SUT0 & FUSE\_CKDIV8)

/\* High Fuse Byte \*/

#define FUSE\_BOOTRST (unsigned char)~\_BV(0)

#define FUSE\_BOOTSZ0 (unsigned char)~\_BV(1)

#define FUSE\_BOOTSZ1 (unsigned char)~\_BV(2)

#define FUSE\_EESAVE    (unsigned char)~\_BV(3)  /\* EEPROM memory is preserved through chip erase \*/

#define FUSE\_WDTON     (unsigned char)~\_BV(4)  /\* Watchdog Timer Always On \*/

#define FUSE\_SPIEN     (unsigned char)~\_BV(5)  /\* Enable Serial programming and Data Downloading \*/

#define FUSE\_DWEN      (unsigned char)~\_BV(6)  /\* debugWIRE Enable \*/

#define FUSE\_RSTDISBL  (unsigned char)~\_BV(7)  /\* External reset disable \*/

#define HFUSE\_DEFAULT (FUSE\_BOOTSZ0 & FUSE\_BOOTSZ1 & FUSE\_SPIEN)

/\* Extended Fuse Byte \*/

#define FUSE\_BODLEVEL0 (unsigned char)~\_BV(0)  /\* Brown-out Detector trigger level \*/

#define FUSE\_BODLEVEL1 (unsigned char)~\_BV(1)  /\* Brown-out Detector trigger level \*/

#define FUSE\_BODLEVEL2 (unsigned char)~\_BV(2)  /\* Brown-out Detector trigger level \*/

#define EFUSE\_DEFAULT  (0xFF)

/\* Lock Bits \*/

#define \_\_LOCK\_BITS\_EXIST

#define \_\_BOOT\_LOCK\_BITS\_0\_EXIST

#define \_\_BOOT\_LOCK\_BITS\_1\_EXIST

/\* Signature \*/

#define SIGNATURE\_0 0x1E

#define SIGNATURE\_1 0x95

#if defined(\_\_AVR\_ATmega328\_\_)

#  define SIGNATURE\_2 0x14

#else /\* ATmega328P \*/

#  define SIGNATURE\_2 0x0F

#endif

#define SLEEP\_MODE\_IDLE (0x00<<1)

#define SLEEP\_MODE\_ADC (0x01<<1)

#define SLEEP\_MODE\_PWR\_DOWN (0x02<<1)

#define SLEEP\_MODE\_PWR\_SAVE (0x03<<1)

#define SLEEP\_MODE\_STANDBY (0x06<<1)

#define SLEEP\_MODE\_EXT\_STANDBY (0x07<<1)

#endif  /\* \_AVR\_IOM328P\_H\_ \*/