SAHYADRI
COLLEGE OF ENGINEERING & MANAGEMENT
An Autonomous Institution
MANGALURU

EMBEDDED SYSTEM CONCEPTS WITH ARM

(Effective from the Academic Year 2022 - 2023)

IV SEMESTER

Course Code	**21CS42**	CIA Marks	50
Number of Contact Hours/Week (L: T: P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40L + 20P	Exam Hours	03

CREDITS – 4

COURSE PREREQUISITES:

- • Fundamental knowledge of Computer Organization and Programming.

COURSE OBJECTIVES:

This course will enable students to:

- Understand the fundamentals of ARM based systems, basic hardware components, selection methods and attributes of an embedded system.
- Program ARM controller using the various instructions.
- Identify the applicability of the embedded system.
- Comprehend the real time operating system used for the embedded system

TEACHING - LEARNING STRATEGY:

Following are some sample strategies that can be incorporate for the Course Delivery

- Chalk and Talk Method/Blended Mode Method
- Power Point Presentation
- Expert Talk/Webinar/Seminar
- Video Streaming/Self-Study/Simulations
- Peer-to-Peer Activities
- Activity/Problem Based Learning
- Case Studies
- MOOC/NPTEL Courses
- Any other innovative initiatives with respect to the Course contents

COURSE CONTENTS

MODULE - I

Embedded System design concepts: Embedded Vs General computing system, History of embedded systems, Classification of Embedded systems, Major applications areas of embedded systems, purpose of embedded systems. Characteristics and Quality Attributes of Embedded Systems, Operational quality attributes, non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling, embedded firmware design and development. ***(Text book 2:Chapter 1(Sections 1.2 to 1.6); Chapter-3, Chapter-4, Chapter-7 (Sections 7.1, 7.2 only), Chapter-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only))***	**8 Hours**

MODULE - II

ARM Embedded Systems: RISC, ARM Design Philosophy, Embedded System Hardware and Software. **ARM Processor Fundamentals:** Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and Vector Table, Core Extensions. ***(Text book 1: Chapter 1 - 1.1 to 1.4, Chapter 2 - 2.1 to 2.5)***	**8 Hours**

MODULE - III

ARM Instructions Set: Data Processing Instructions, Branch Instructions, Load-Store Instructions, Software Interrupt Instructions, Program Status Register Instruction. ***(Text book 1: Chapter 3:Sections 3.1 to 3.6 (Excluding 3.5.2))***	**8 Hours**

MODULE - IV

Interfacing: Interfacing Sensors, Actuators, LED, 7 segment display, stepper motor, Keyboard, Push button switch, Timers. Communication Interface (onboard and external types), Embedded firmware, Other system components. ***(Text book 2:Chapter 2(Sections 2.1 to 2.6))***	**8 Hours**

MODULE - V

RTOS and IDE for Embedded System Design: Real time Operating System basics, how to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment. **Case Study:** VxWorks v/s Lynx OS. ***Text book 2: Chapter-10 (Sections 10.1 to 10.10 only), Chapter 12, Chapter-13 (13.1.1)***	**8 Hours**

COURSE OUTCOMES

Upon completion of this course, the students will be able to:

CO No.	Course Outcome Description	Bloom's Taxonomy Level
CO1	Describe the characteristics and quality attributes for designing an embedded system.	CL2
CO2	Illustrate the architectural features of ARM controller with assembly language program	CL3
CO3	Develop programs using Instruction Set Architecture of ARM controller.	CL3
CO4	Interface the peripheral devices with LPC2148 microcontroller.	CL3
CO5	Demonstrate the real time operating system by using VXWorks and Lynx OS.	CL3

LABORATORY COMPONENTS

Exp. No.	Experiment Description	CO No.	Bloom's Taxonomy Level
1.	Implement an ALP to (a) add two 16 bit binary numbers. (b) find factorial of a number.	CO1	CL3
2.	Implement an ALP to find the square of a number (1 to 10) using look-up table.	CO2	CL3
3.	Implement an ALP to find the largest/smallest number in an array of 32 numbers.	CO3	CL3
4.	Implement an ALP to arrange a series of 32-bit numbers in ascending/descending order.	CO3	CL3
5.	Implement an ALP to count the number of ones and zeros in two consecutive memory locations.	CO3	CL3
6.	Display "Hello World" message using Internal UART.	CO4	CL3
7.	Interface (a) Stepper motor (b) DC motor to rotate it in clockwise and anti-clockwise direction.	CO4	CL3
8.	Interface a DAC and generate the following waveforms: a. Square wave b. Triangular wave	CO4	CL3
9.	Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay in between.	CO4	CL3
10.	Demonstrate the use of an external interrupt to toggle an LED On/Off.	CO4	CL3

11.	Demonstration of embedded system applications to read • Temperature/humidity sensor	CO5	CL3

CO-PO-PSO MAPPING

CO No.	Programme Outcomes (PO)												Programme Specific Outcome (PSO)	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3	3	3									1		
CO2	3	3	3									1		
CO3	3	3	3	1	2				1			1		
CO4	3	3	3	1	2				1			1		
CO5	3	3	3							1		1		
3: Substantial (High)				2: Moderate (Medium)						1: Poor (Low)				

ASSESSMENT STRATEGY

Assessment will be both CIA and SEE. Students learning will be assessed using Direct and Indirect methods:

Sl. No.	Assessment Description	Weightage (%)	Max. Marks
1	**Continuous Internal Assessment (CIA)**	**100 %**	**50**
	Continuous Internal Evaluation (CIE)	60 %	30
	Practical Session (Laboratory Component)	40 %	20
2	**Semester End Examination (SEE)**	**100 %**	**50**

ASSESSMENT DETAILS

Continuous Internal Assessment (CIA) (50%)				Semester End Exam (SEE) (50%)
Continuous Internal Evaluation (CIE) (60%)			Practical Sessions (40%)	
I	II	III		
Syllabus Coverage			Syllabus Coverage	Syllabus Coverage
40%	30%	30%	100%	100%
MI			MI	MI
MII	MII		MII	MII
	MIII		MIII	MIII
		MIV	MIV	MIV
		MV	MV	MV

NOTE:

- Assessment will be both CIA and SEE.
- The practical sessions of the IPCC shall be for CIE only.
- The Theory component of the IPCC shall be for both CIA and SEE respectively.
- The questions from the practical sessions shall be included in Theory SEE.

Note: For Examinations (both CIE and SEE), the question papers shall contain the questions mapped to the appropriate Bloom's Level. Any COs mapped with higher cognitive Bloom's Level may also be assessed through the assignments.

SEE QUESTION PAPER PATTERN:

1. The question paper will have **TEN** full questions from **FIVE** Modules
2. There will be 2 full questions from each module. Every question will carry a maximum of 20 marks.
3. Each full question may have a maximum of four sub-questions covering all the topics under a module.
4. The students will have to answer FIVE full questions, selecting one full question from each module.

TEXT BOOKS:

1. Andrew N Sloss, Dominic Symes and Chris Wright, ARM system developers guide, Elsevier, Morgan Kaufman publishers, 2008. (Chapters: 1, 2, 3, 4, 5, 6, 7)
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education, Private Limited, 2nd edition. (Chapters: 9, 10, 12)

REFERENCE BOOKS:

1. William Hohl, Christopher Hinds ARM ASSEMBLY LANGUAGE Fundamentals and Techniques, 2nd Edition, CRC Press, 2015.
2. Gibson ARM Assembly Language An Introduction, Second Edition, 2007.
3. Steve Furber, ARM System-on-Chip Architecture, Second Edition, Pearson, 2015.
4. Raj Kamal, Embedded System, Tata McGraw-Hill Publishers, 2nd Edition, 2008.

REFERENCE WEB LINKS AND VIDEO LECTURES (E - RESOURCES):

1. https://onlinecourses.nptel.ac.in/noc22_cs93/unit?unit=17&lesson=18
2. https://onlinecourses.nptel.ac.in/noc22_cs93/unit?unit=26&lesson=27
3. https://onlinecourses.nptel.ac.in/noc22_cs93/unit?unit=43&lesson=44
4. https://onlinecourses.nptel.ac.in/noc22_cs93/unit?unit=52&lesson=53
5. https://onlinecourses.nptel.ac.in/noc22_cs93/unit?unit=75&lesson=76