Hardware Change Log

*[P80 ACU]*

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| Document Revision: |  | Date: | *05-03-2018* |
| **Comments** | | | |
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| Action | Name | Function | Signature | Date |
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| Prepared: | JOKR |  |  | 05-03-2018 |
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| Approved by: |  |  |  |  |

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# Changelog

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Revision | Author | Description |
|  |  |  |  |
| 12-12-2017 | 1 |  | Initial release first prototype - EDA build no. 17.1.9.592 |

# Purpose and Scope

This document describes the changes for each revision of the P80 ACU.

Raw PCB Number: ??

# Changes to be implemented (Pending)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
| 1 | Suggestion: VBAT switch R126 or T2, if they have a bad soldering/disconnect, a single failure can turn off VBAT\_OUT. Cheap solution is to make a redundant open collector circuit (duplicate these components) |  | X |  | JOKR |  |
| 2 | Page 3: net BOOST\_OUT and V\_BAT are connected together. Net should only have one name. |  | X |  | JOKR |  |
| 3 | VCC routing on mid-layer 5 can be removed. Vias connected through VCC plane layer 7 |  |  | X | JOKR |  |
| 4 | Brownout detector should be removed and replaced by the watchdog/brownout detector used in P80 PMU |  | X |  | BGS |  |
| 5 | One watchdog for each MCU and use the nMR input tied together for the JTAG interface |  | X |  | BGS |  |
| 6 | Change load switches, find one that is retrying and has programmable latch-up limit |  | X |  | BGS |  |
| 7 | Add input protection for the “global” comparator (U5 and U41) in each ACU200, see ACU210 |  | X |  | BGS |  |
| 8 | Maybe use a reference for the “global” comparator (U5 and U41) instead of “vboost” divided by resistors. And at the same time use precision resistors for measuring the VBAT instead of the Zener. |  | X |  | BGS |  |
| 9 | Change the stacked capacitors and coil in the converter. Note the quality issues from P60. |  | X |  | BGS |  |
| 10 | The LDO supplying the converter logics can be changed to a switcmode converter. |  | X |  | BGS |  |
| 11 | LTC6101, to be changed to LTC6106 for low voltage channels |  | X |  | BGS |  |
| 12 | R2 and D2 does not impose any protection, remove or change to TVS. |  | X |  | BGS |  |
| 13 | MCU1 Crystal serial resistor R239 not mounted | X |  |  | JOKR |  |
| 14 | MCU2 Crystal serial resistor R251 not mounted | X |  |  | JOKR |  |
| 15 | VBAT switch circuit, 1 + 2, Resistor R122 / R126 may need derating. Is exposed to 33Vdc at max VBAT. | X | X |  | JOKR |  |
| 16 | FRAM U31 I2C address shall be [A2:A0]=001. Connect A0 to Vcc |  | X |  | JOKR |  |
| 17 | FRAM U61 I2C address shall be [A2:A0]=001. Connect A0 to Vcc |  | X |  | JOKR |  |
| 18 | TVS diode 30V e.g. D7 has wrong footprint |  |  | X | JOKR |  |
| 19 | Consider tuning MCU crystal frequency. Crystal Cload specified to 10pF. Calculated load with Cstray=4pF is 7,4pF. To get Cload closer to 10pF, change the two load capacitors to app. 12pF. | X |  |  | JOKR |  |
| 20 | The resistor R227 at nRESET must be of lower value. The internal pull-up at the two MCU’s are so strong that nRESET only can be pulled down to app. 2,4V. | X | X |  | JOKR |  |
|  |  |  |  |  |  |  |

# Revision 2 changes implemented

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| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
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