Hardware Change Log

*[P80 ACU]*

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| Action | Name | Function | Signature | Date |
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# Changelog

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| --- | --- | --- | --- |
| Date | Revision | Author | Description |
|  |  |  |  |
| 12-12-2017 | 1 |  | Initial release first prototype - EDA build no. 17.1.9.592 |
| 28-08-2018 | 2 |  | Revision 2, EDA build number: 1.1.9.86 |
| 18-02-2020 |  |  | Updated changes to PCB rev 2 |

# Purpose and Scope

This document describes the changes for each revision of the P80 ACU.

Raw PCB Number: ??

# Changes to be implemented (Pending)

|  |  |  |  |  |  |  |
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| No. | Description | BOM | Schematic | Layout | Who | Status |
| 1 | Overvoltage protection circuit controlling OVLU signal should limit VBAT at 33,6V, but the overvoltage limit is 36,9V due to reverse leakage current through D4 / D42 at 25µA. |  | X |  | JKRI |  |
| 2 | VBAT no load leakage current is app. 0,80mA, equivalent to a pull down resistance of 41kohm from several voltage dividers, especially from BOOST\_OUT in the VBAT overvoltage circuit. (R14//R16 + R19) |  | X |  | JKRI |  |
| 3 | VBAT switch circuit: KS is pulled up to VBAT at the battery and Q18 FET drain connected to VBAT\_IN. When the VBAT switch have been off, the Q18 FET can get in a state where it is not possible to turn on the VBAT\_switch again, if VBAT\_IN have reached VBAT maximum, due to no load.  Also the Q18 FET Vgs threshold is in the range 1V to 3V, and Q18 can have up to 1µA gate leakage current. This result in little margin between ON and OFF state and with very high resistor values, the circuit might be turned ON/OFF by noise.  Suggestion: change to N-channel FET or use P-channel FET with higher Vgs threshold. |  | X | X | JKRI |  |
| 4 | When the transition from reduced power mode (V\_Bat range 32V-33,6V) to overvoltage mode lock out mode at V\_Bat max, huge voltage ripple occurs at interm-a (measured at C25) and the inductor L3 makes high sound noise. This behaviour can most likely be eliminated if there were a small hysteresis at the OVLU comparator U5, implemented as 1-2Mohm feedback from U5 output to IN+. This will give also result in a hysteresis af V\_Bat max threshold. |  | X |  | JKRI |  |
| 5 | Comparator circuit with hysteresis, controlling boost converter FET have periods, where the FET is triggered several times, both at turn ON and at turn OFF. The hysteresis should avoid this behavior.  This behavior is caused by Vcc ripple on the LMV762 comparator. There is too little de-coupling. Datasheet recommended de-coupling is:  "To minimize supply noise, power supplies must be decoupled by a 0.1-μF ceramic capacitor in parallel with a 10-μF capacitor”  Vboost have 2 x 100nF and 4,7µF behind the diode at buck converter output. Add at least 2µF. |  | X |  | JKRI |  |
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| 23 | **Change to PCB revision 1**:  Change HW mode vboost set point form app. 4,7V to app. 14V to get higher output power. On master schematic change R15 + R6 at resistor divider at INA- / INB- from 10k to ??k. | X |  |  | JOKR |  |
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# Revision 3 changes implemented

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| No. | Description | BOM | Schematic | Layout | Who | Status |
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# Revision 2 changes implemented

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| No. | Description | BOM | Schematic | Layout | Who | Status |
| 11 | LTC6101, to be changed to LTC6106 for low voltage channels |  | X |  | BGS | Done |
| 13 | MCU1 Crystal serial resistor R239 not mounted | X |  |  | BGS | Done |
| 14 | MCU2 Crystal serial resistor R251 not mounted | X |  |  | BGS | Done |
| 16 | FRAM U31 I2C address shall be [A2:A0]=001. Connect A0 to Vcc |  | X |  | BGS | Done |
| 17 | FRAM U61 I2C address shall be [A2:A0]=001. Connect A0 to Vcc |  | X |  | BGS | Done |
| 19 | Consider tuning MCU crystal frequency. Crystal Cload specified to 10pF. Calculated load with Cstray=4pF is 7,4pF. To get Cload closer to 10pF, change the two load capacitors to app. 12pF. | X |  |  | BGS | Done |
| 4 | Brownout detector should be removed and replaced by the watchdog/brownout detector used in P80 PMU |  | X |  | BGS | Done |
| 5 | One watchdog for each MCU and use the nMR input tied together for the JTAG interface |  | X |  | BGS | Done |
| 6 | Change load switches, find one that is retrying and has programmable latch-up limit  Missing component calculations |  | X |  | BGS | Done |
| 21 | The resistor R227 at nRESET must be of lower value. The internal pull-up at the two MCU’s are so strong that nRESET only can be pulled down to app. 2,4V.  Brownout detector changed to watchdog with built-in watchdog | X | X |  | JOKR | Done |
| 7 | Add input protection for the “global” comparator (U5 and U41) in each ACU200, see ACU210 |  | X |  | BGS | Done |
| 8 | Maybe use a reference for the “global” comparator (U5 and U41) instead of “vboost” divided by resistors. And at the same time use precision resistors for measuring the VBAT instead of the Zener. |  | X |  | BGS | Done |
| 12 | R2 and D2 does not impose any protection, remove or change to TVS.  Removed |  | X |  | BGS | Done |
| 18 | TVS diode 30V e.g. D7 has wrong footprint |  |  | X | JOKR | Done |
| 10 | The LDO supplying the converter logics can be changed to a switcmode converter. |  | X |  | BGS | Done |
| 15 | VBAT switch circuit, 1 + 2, Resistor R122 / R126 may need derating. Is exposed to 33Vdc at max VBAT.  Not relevant anymore | X | X |  | JOKR | Done |
| 29 | Update to correct GND scheme |  | X | X | BGS | Done |
| 31 | Add ESD protection to debug connector | X | X | X | BGS | Done |
| 30 | Change to new FRAM | X | X | X | BGS | Done |
| 3 | VCC routing on mid-layer 5 can be removed. Vias connected through VCC plane layer 7  PCB has to be rerouted |  |  | X | JOKR | Done |
| 1 | Suggestion: VBAT switch R126 or T2, if they have a bad soldering/disconnect, a single failure can turn off VBAT\_OUT. Cheap solution is to make a redundant open collector circuit (duplicate these components)  Not relevant anymore |  | X |  | JOKR | Done |
| 2 | Page 3: net BOOST\_OUT and V\_BAT are connected together. Net should only have one name. |  | X |  | JOKR | Done |
| 9 | Change the stacked capacitors and coil in the converter. Note the quality issues from P60. |  | X |  | BGS | Done |
| 24 | To change boost converter regulation mode change:  C4 changed to 5,2µF (2x2,2µF + 1µF)  I1 change to 15µH. 22µH  R10 = 33kohm, R14 = 3k3ohm, C9 = 10pF.  R159 changed to ??kohm (increase HW mode set point)  Removed SYNC clock, R9, R23: 1,8Mohm, C29, C30: 10pF, U9 and components around that IC.  Added 1Mohm feedback, U20A from OUTA\_C pin 1 to INA+ pin 3  Same changes to channel B | X | X | X | JOKR | Done |
| 25 | LDO supplying the converter logics should be changed to LTC3639 DC/DC converter.    Changes enable/SHDN pin from 0.3V to 0.7V threshold. Complies with KS logic. Refer to ltspice simulation for LTC3639 for component selection. Efficiency simulated from 88 to 93%. Expect nominel 85%.  Wurth Coil (74406043221)  Vripple <= 100mV (2%)  Note: Reused design from BP8 | X | X | X | CAF | Done |
| 26 | Rather than using a single LDO/Buck converter for two channels, reconfigure for adding redundancy by letting a single LDO/Buck power 4 channels and be overlapping. This allows for a single LDP/Buck to fail while ensure continued operation. Second failed LDO/Buck only causes 2 channels to discontinue operation. Overlapping could be as  Buck1: Boost[0..3]  Buck2: Boost[2..5]  Buck3: Boost[4..7]  Investigate possible fail cases.  Note: Not done as complexity is not worth it at the moment | X | X | X | CAF | Done |
| 28 | Update Killswitch circuitry to P80 Killswitch overview v3 | X | X | X | CAF | Done |
| 22 | Change boost converter regulation to CCM. On master schematic, change R3 from 10ohm to 100ohm (DAC output), I1 from 4,3µH to 10µH. Added feedback from OUTA to INA- R=10kohm. Apply changes to all converters.  Note: Implemented in 24 | X | X | X | JOKR | Done |
| 27 | Rather than OR’ing 5V with Vsun for LDO, OR output of LDO with 5V from Stack. Investigate possible fail cases  Note: Implementation following ACU210 from P60 |  |  |  |  | Done |
| 32 | Remove sync | X | X | X | BGS | Done |