Hardware Change Log

*[P80 PDU]*

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| Document Title: | PDU\_Hardware\_Change\_Log | | |
| Document Reference: |  | | |
| Document Revision: |  | Date: | *14-03-2018* |
| **Comments** | | | |
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| Action | Name | Function | Signature | Date |
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| Prepared: | JOKR |  |  | 14-03-2018 |
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| Approved by: |  |  |  |  |

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# Changelog

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Revision | Author | Description |
|  |  |  |  |
| 14-12-2017 | 1 |  | Initial release first prototype - EDA build no. 17.1.9.592 |

# Purpose and Scope

This document describes the changes for each revision of the P80 PDU.

Raw PCB Number: ??

# Changes to be implemented (Pending)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
| 1 | FRAM write protect pin connect to CPU IO pin |  | X | X | TTH |  |
| 2 | Change all GanFet to Normal N-FET |  | X | X | TTH |  |
| 3 | Change low voltage load switch to new type |  | X | X | TTH |  |
| 4 | Diode D6 and D7 missing, Set as not mounted. But there might be a problem with running these two outputs in parallel. An other solution is to only use one FET and then use one Keystone resistor to connect the two outputs together | X |  |  | JOKR |  |
| 5 | On sheet “PDU\_HV – Main” the remark at SYNC oscillator U4 state “51k=3,9MHz”. This is the master frequency. The output frequency depends on the PH setting, which is 4, thus output frequency is 980KHz. |  | X |  | JOKR |  |
| 6 | The C20 10nF capacitor loads the SYNC4 signal too much. C20 is only needed when MOD, U4 pin 14 is floating. C20 should be not mounted when R21 is mounted | X |  |  | JOKR |  |
| 7 | The Buck converter efficiency can be improved by lowering the switching frequency. Change external clock frequency from 971kHz to e.g. 667kHz by changing R19 from 51k to 75kohm. Verify LT8612 RT setting. | X |  |  | JOKR |  |
| 8 | Small stacked capacitors are a problem in production |  | X | X | TTH |  |
| 9 | CPU must be placed on top |  | X | X | TTH |  |
| 10 | Change inductor to new type |  | X | X | TTH |  |
| 11 | Connectors may change position |  |  | X | TTH |  |
| 12 | Change high voltage gate driver to LTC7000-1 |  | X | X | TTH |  |
| 13 | Current measuring point after the switch |  | X | X | TTH |  |
| 14 | ADC datasheet recommend more decoupling at ADC’s Vref pin:  “The REFP pin requires a 10-μF ceramic capacitor to meet performance specifications. Place the capacitor directly next to the device. This capacitor ground pin must be routed to the REFM pin by a very short t” |  | X |  | JOKR |  |
| 15 | Low voltage output ADC current measurement input to ADC is above the Vref voltage. ADC input voltage is adjusted down with the following changes:  R134 (Master sch.) from 100ohm to 50ohm.  R45 (master sch.) from 10kohm to 2,4kohm    **Note** the current amplifier, LT6106 output voltage high cannot go higher than app. V+ (power supply) minus 1,2V. So with 3V3 powered outputs the maximum ADC input is app. 2V. | X |  |  | JOKR |  |
| 16 |  |  |  |  |  |  |

# Revision 2 changes implemented

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| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
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