Hardware Change Log

*[P80 PDU]*

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| Document Title: | PDU\_Hardware\_Change\_Log | | |
| Document Reference: |  | | |
| Document Revision: |  | Date: | *14-03-2018* |
| **Comments** | | | |
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| Action | Name | Function | Signature | Date |
| --- | --- | --- | --- | --- |
| Prepared: | JOKR |  |  | 14-03-2018 |
| Verified by: |  |  |  |  |
| Approved by: |  |  |  |  |

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# Changelog

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Revision | Author | Description |
|  |  |  |  |
| 14-12-2017 | 1 |  | Initial release first prototype - EDA build no. 17.1.9.592 |

# Purpose and Scope

This document describes the changes for each revision of the P80 PDU.

Raw PCB Number: ??

# Changes to be implemented (Pending)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
| 1 | FRAM write protect pin connect to CPU IO pin |  | X | X | TTH |  |
| 2 | Change all GanFet to Normal N-FET |  | X | X | TTH |  |
| 3 | Change low voltage load switch to new type |  | X | X | TTH |  |
| 4 | Diode D6 and D7 missing, Set as not mounted. But there might be a problem with running these two outputs in parallel. An other solution is to only use one FET and then use one Keystone resistor to connect the two outputs together | X |  |  | JOKR |  |
| 5 | On sheet “PDU\_HV – Main” the remark at SYNC oscillator U4 state “51k=3,9MHz”. This is the master frequency. The output frequency depends on the PH setting, which is 4, thus output frequency is 980KHz. |  | X |  | JOKR |  |
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# Revision 2 changes implemented

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
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