Hardware Change Log

*[P80 PMU]*

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| Document Revision: |  | Date: | *08-03-2018* |
| **Comments** | | | |
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| Action | Name | Function | Signature | Date |
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# Changelog

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| --- | --- | --- | --- |
| Date | Revision | Author | Description |
|  |  |  |  |
| 12-12-2017 | 1 |  | Initial release first prototype - EDA build no. 17.1.9.592 |
| 24-03-2020 |  |  | Updated with rev 3 changes |

# Purpose and Scope

This document describes the changes for each revision of the P80 PMU.

Raw PCB Number: 100608

# Changes to be implemented (Pending)

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| No. | Description | BOM | Schematic | Layout | Who | Status |
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# Revision 3 changes implemented

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| No. | Description | BOM | Schematic | Layout | Who | Status |
| 1 | Add CAN termination  Changed R65, R66, R97, C118 to mounted | X | X |  | BGS | Done |
| 2 | The watchdog cannot be tested by automatic test equipment, due to the VCC “watchdog override” circuit. The test fixture has the circuitry to activate this.  Not relevant, as the Vcc\_JTAG current measurement circuit have been removed. The WDI external signal is going to be controlled by the automatic test equipment. |  | X |  | BGS | Done - No relevant |
| 3 | Inrush limiting in V\_DEP1/2 has to be adjusted to fit with the current limit of 0.5 A. Changing C83 and C89 will give 178 mA @ 100 uF load. C79 and C85 will probably need to be bigger to deliver enough current. C83 and C89 needs to be at least 76 V caps, hence the footprint might be too small.  Change C83 to 100nF, 100V. Footprint change from 0402 to 0603.  Change C83 to 100nF, 100V. Footprint change from 0402 to 0603.  R182 + R200 is rated to 40V (with derating to 80%). The voltage will never get close to this limit.  C79 + C85 capacity is increased to 2,2µF to have more margin when capacitance is reduced by DC biasing. Change to 2.2µF, 0402, 25V | X | X | X | BGS | Done |
| 4 | Timer capacitors in V\_DEP1/2 should be reduced to 10 pF in order handle shorts better. Results in ~3 us response time.  C82 changed to 10pF  C88 changed to 10pF | X | X |  | BGS | Done |
| 5 | PMU Vcc watchdog circuit trigger the watchdog (U27), while the MCU is flashed. The Timer circuit and the JTAG Vcc enable circuit is removed from the PMU pcb.  The Timer circuit is implemented on an external PCB and the WDI trigger signal is feed through the debug connector J5 pin 12. (the second UART is not used on the PMU)  There must be made a connection from J5 pin 12 to D14 anode. (only component not removed is Diode D14)  Resistor R74 is changed from 10k to 100kohm. (Pull-down) | X | X | X | JKRI | Sch done |
| 6 | The Vcc watchdog circuit is modified to have extended nReset low pulse time. Extent from app. 200ms to app. 500ms. This to secure that the Vcc level gets low enough to power reset the MCU.  C176 change to 3,3µF  R303 change to 100kohm  Mount D17  Add resistor in serial to D17, value 200ohm. This prevents high discharge current into U45B pin 4.  Add resistor in serial to U45 pin 6, value 200ohm. This prevents high discharge current into U45B pin 6 from C179. | X | X | X | JKRI | Sch done |
| 7 | Deployment power, add diode from LTC7000 load switch (U13+U15) pin 13 (TS) to GND to protect TS input from negative voltage in case of a short circuit of the output.  Anode to GND  Cathode to TS. | X | X | X | JKRI |  |
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# Revision 2 changes implemented

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| No. | Description | BOM | Schematic | Layout | Who | Status |
| 1 | U26 SYNC Oscillator, Pin 2 GND is connected to VCC through R142, 100kohm, Pin 3 SET is connected to GND. |  | X | X | JOKR | Done |
| 5 | Add zero ohms for RS485 connection to main bus |  | X | X | BGS | Done |
| 23 | Change net ties in main connector to 10R resistors |  | X | X | BGS | Done |
| 7 | If new MCU: add write protect capability to FRAM |  | X | X | BGS | Done |
| 8 | If new MCU: add CAN mode control |  | X | X | BGS | Done |
| 24 | Change MCU to 100 pin version | X | X | X | BGS | Done |
| 25 | Change load switches, note P60 issues  Missing component calculations | X | X | X | BGS | Done |
| 22 | Reverse GSRB connections |  | X | X | BGS | Done |
| 6 | GPIOs PB00 and PB01 are used twice: |  | X | X | BGS | Done |
| 2 | Q4 MOSFET Vgs voltage can get higher than absolute maximum rating off -20V vhen Vbat gets higher than 30V  Not relevant anymore | X | X |  | JOKR | Done |
| 3 | Low voltage loadswitches needs to be changed. |  | X | X | BGS | Done |
| 10 | R175 and R186 is not required due to DFF logic. DFF logic can be replaced with a 5V CMOS level shifter, hence R175 and R186 will prevent retry functionality as per Figure 4 in LT1910 datasheet  Not relevant anymore | X | X | X | CAF | Done |
| 15 | R26 should be 10k. | X |  |  | CAF | Done |
| 17 | Add series termination to SPI bus to reduce ringing. Possibly footprint for a load capacitor as well. | X | X | X | CAF | Done |
| 18 | R115 should be located as close as possible to the MCU to work as series termination. Ringing from RX/TX are causing crosstalk.  R115 and R118 should be changed to 100ohm. Could be more, but trimming should occur on next revision.    10 ohm series resistor    100 ohm series resistor    The result after changing to 100 ohm | X |  | X | CAF | Done |
| 19 | R131 + R134 can cause VGS max to exceede limits of +/- 20V  Not relevant anymore |  |  |  |  | Done |
| 11 | Change R130 to 1k  nReset on MCU sees a small pulse high on power on.  Ch1: Yellow VCC @ U23 pin 5  Ch2: Cyan nRESET @ U23 pin 1  Ch3: Magenta WDI @ U23 pin 4  Ch4: Blue nRESET @ U18 pin 64  On power up, RESET\_N on MCU is pulled towards VCC which is causing the glitch. Could this be an issue for an open collector?  R130 = 1k  This cannot be prevented by supervisor circuitry as it is the MCU who generate it.  Resistor changed, Open-Collector WD version is considered |  |  |  | CAF | Done |
| 12 | Supervisor circuitry generated reset (U23) could be replaced or OR’ed with PG from load switch (U42).  Not implemented |  | X | X | CAF | Done |
| ~~9~~ | ~~Change R176, R177, R187 and R188 to 100k and C152 and C165 to reduce deploy peak current from 1.8A to 18mA without load. This to ensure overcurrent is not tripped from inrush current.~~    Not relevant anymore | ~~X~~ |  |  | ~~CAF~~ | Done |
| 20 | Vref (VM5) on ADC is irrelevant.  Removed |  |  |  |  | Done |
| 14 | Is the added resolution on U3 necessary? VM\_VBAT and CM\_VBAT are both routed to U1 and U2 respectively and hence measured twice.  Circuit kept | X | X | X | CAF | Done |
| 13 | How is charge initially applied to C106 and C107 is a diode from VCC to VBAT missing? Is capacitance sufficient with self-discharge? | X | X | X | CAF | Done |
| 26 | Added PPS receiver | X | X | X | BGS | Done |
| 21 | Update Killswitch circuitry to reflect P80\_killswitch\_overview v3 | X | X | X | CAF | Done |
| 4 | GAN FET to be changed to MOSFET, or GAN Systems FET with much lower gate-source leakage. |  | X | X | BGS | Done |
| 16 | Datasheet for ADS7952 (U1 & U2) states requirement for a 10µF capacitor between REF and GND as close as possible to the IC.  Additionally the datasheet recommends 1µF at each supply pin placed as close as possible to the IC. | X | X | X | CAF | Done |
| 27 | Added ESD protection for debug | X | X | X | BGS | Done |
| 28 | Added chassis ground |  | X | X | BGS | Done |
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