Hardware Change Log

*[P80 PMU]*

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| Document Title: | PMU\_Hardware\_Change\_Log | | |
| Document Reference: |  | | |
| Document Revision: |  | Date: | *08-03-2018* |
| **Comments** | | | |
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| Action | Name | Function | Signature | Date |
| --- | --- | --- | --- | --- |
| Prepared: | JOKR |  |  | 08-03-2018 |
| Verified by: |  |  |  |  |
| Approved by: |  |  |  |  |

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# Changelog

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Revision | Author | Description |
|  |  |  |  |
| 12-12-2017 | 1 |  | Initial release first prototype - EDA build no. 17.1.9.592 |

# Purpose and Scope

This document describes the changes for each revision of the P80 PMU.

Raw PCB Number: 100608

# Changes to be implemented (Pending)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
| 1 | U26 SYNC Oscillator, Pin 2 GND is connected to VCC through R142, 100kohm, Pin 3 SET is connected to GND. |  | X | X | JOKR |  |
| 2 | Q4 MOSFET Vgs voltage can get higher than absolute maximum rating off -20V vhen Vbat gets higher than 30V | X | X |  | JOKR |  |
| 3 | Low voltage loadswitches needs to be changed. |  | X | X | BGS |  |
| 4 | GAN FET to be changed to MOSFET, or GAN Systems FET with much lower gate-source leakage. |  | X | X | BGS |  |
| 5 | Add zero ohms for RS485 connection to main bus |  | X | X | BGS |  |
| 6 | GPIOs PB00 and PB01 are used twice: |  | X | X | BGS |  |
| 7 | If new MCU: add write protect capability to FRAM |  | X | X | BGS |  |
| 8 | If new MCU: add CAN mode control |  | X | X | BGS |  |
| 9 | Change R176, R177, R187 and R188 to 100k and C152 and C165 to reduce deploy peak current from 1.8A to 18mA without load. This to ensure overcurrent is not tripped from inrush current. | X |  |  | CAF |  |
| 10 | R175 and R186 is not required due to DFF logic. DFF logic can be replaced with a 5V CMOS level shifter, hence R175 and R186 will prevent retry functionality as per Figure 4 in LT1910 datasheet | X | X | X | CAF |  |
| 11 | nReset on MCU sees a small pulse high on power on.  Ch1: Yellow VCC @ U23 pin 5  Ch2: Cyan nRESET @ U23 pin 1  Ch3: Magenta WDI @ U23 pin 4  Ch4: Blue nRESET @ U18 pin 64  On power up, RESET\_N on MCU is pulled towards VCC which is causing the glitch. Could this be an issue for an open collector?  R130 = 1k  This cannot be prevented by supervisor circuitry as it is the MCU who generate it. |  | X |  | CAF |  |
| 12 | Supervisor circuitry generated reset could be replaced or OR’ed with PG from load switch. |  | X | X | CAF |  |
| 13 | How is charge initially applied to C106 and C107 is a diode from VCC to VBAT missing? Is capacitance sufficient with self-discharge? | X | X | X | CAF |  |
| 14 |  |  |  |  |  |  |
| 15 |  |  |  |  |  |  |
| 16 |  |  |  |  |  |  |

# Revision 2 changes implemented

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| No. | Description | BOM | Schematic | Layout | Who | Status |
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