Both active-high x and active-low y* are asserted. Which one below is true?

A. x=1, y*=0

B. x=0, y*=1

C. x=1, y*=1

D. x=0, y*=0

Both active-high x and active-low y* are negated. Which one below is true?

A. x=1, y*=0

B. x=0, y*=1

C. x=1, y*=1

D. x=0, y*=0

Interpretation of logic expressions

Example 1: all signals active high

F = A' B (C+D)

F is asserted iff

- **A is asserted / negated , and**
- **B is asserted / negated , and**
- **either C or D is asserted / negated**

Interpretation of logic expressions

Example 2: all signals active low

G* = A*’ B* (C*+D*)

G* = 0

G* is asserted iff

- **A* is asserted / negated , or**
- **B* is asserted / negated , or**
- **C* and D* are both asserted / negated**

A* = 1

B* = 0

C* + D* = 0

Interpretation of logic expressions

Example 3: mixed signals

W = A*’ B’ (C+D*)

W=1

W is asserted iff

A* = 0

- **A* is asserted / negated , and**
- **B is asserted / negated , and**

B = 0

- **either C is asserted / negated or D* is asserted / negated**

C+D* = 1

Interpretation of logic expressions

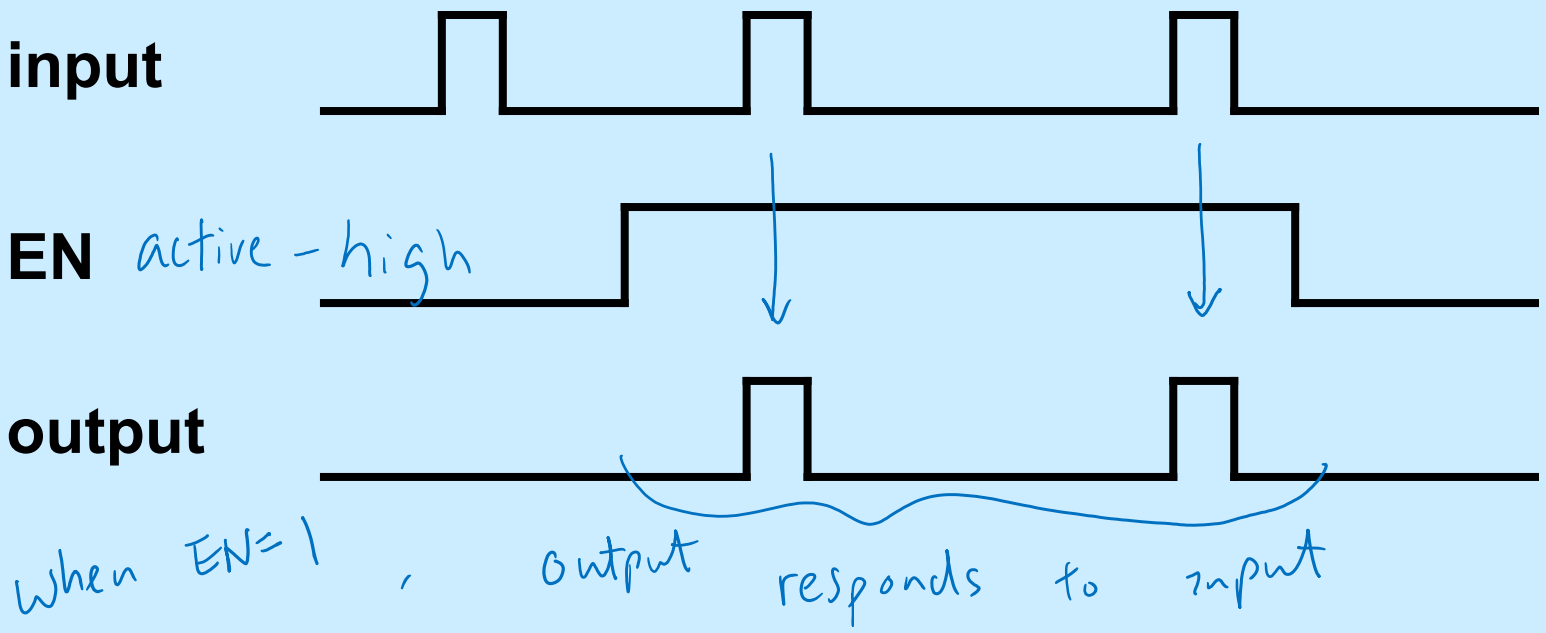
Example 4: mixed signals

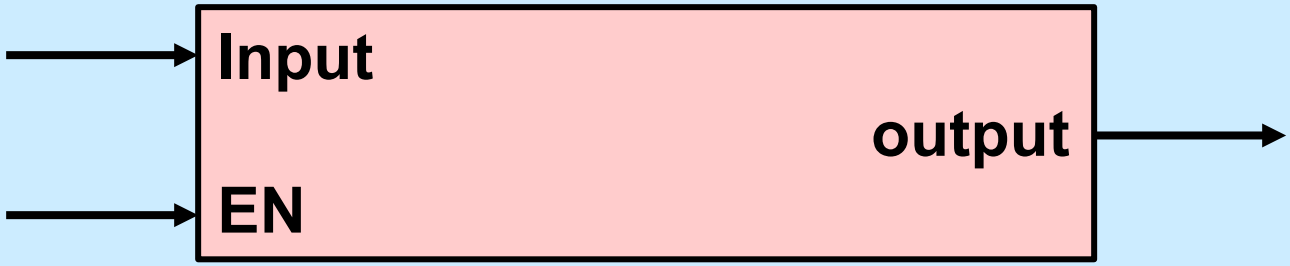
V* = A*' B' + C + D*

V* is asserted iff

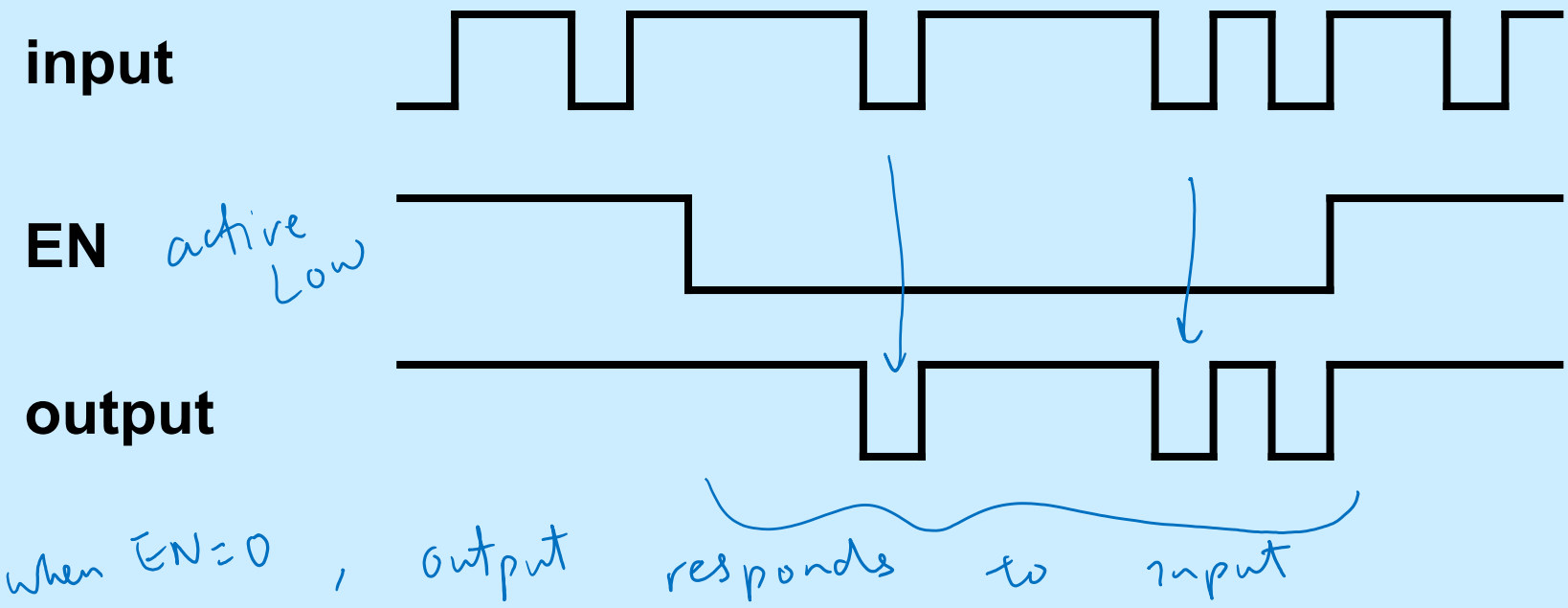
- **A* is asserted / negated or B is asserted / negated , and**
- **C is asserted / negated , and**
- **D* is asserted / negated**

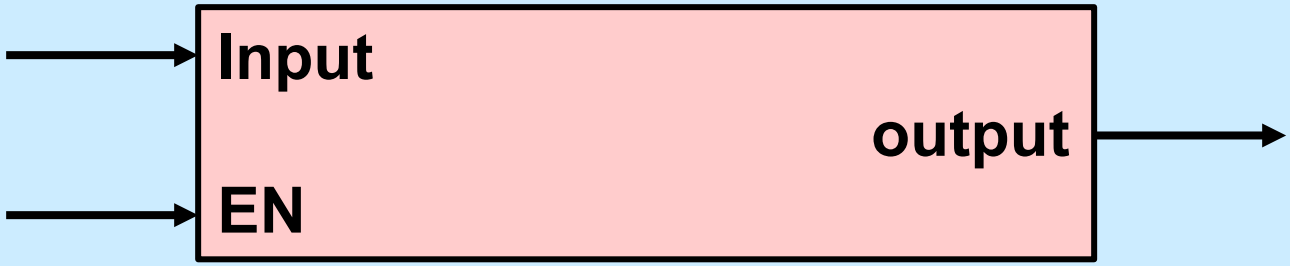
Enable input EN: active high or active low?





Enable input EN: active high or active low?





Inputs A, B, C*, D* and output F.
F is only asserted when either A or C* is asserted (but not both), and either B or D* is negated (but not both).
F(A,B,C*,D*)=

A. $\sum m(0, 2, 8, 12)$

B. $\sum m(0, 5, 10, 15)$ 

C. $\sum m(0, 6, 12, 15)$

A asserted

or

C* asserted

but not both

and

B negated

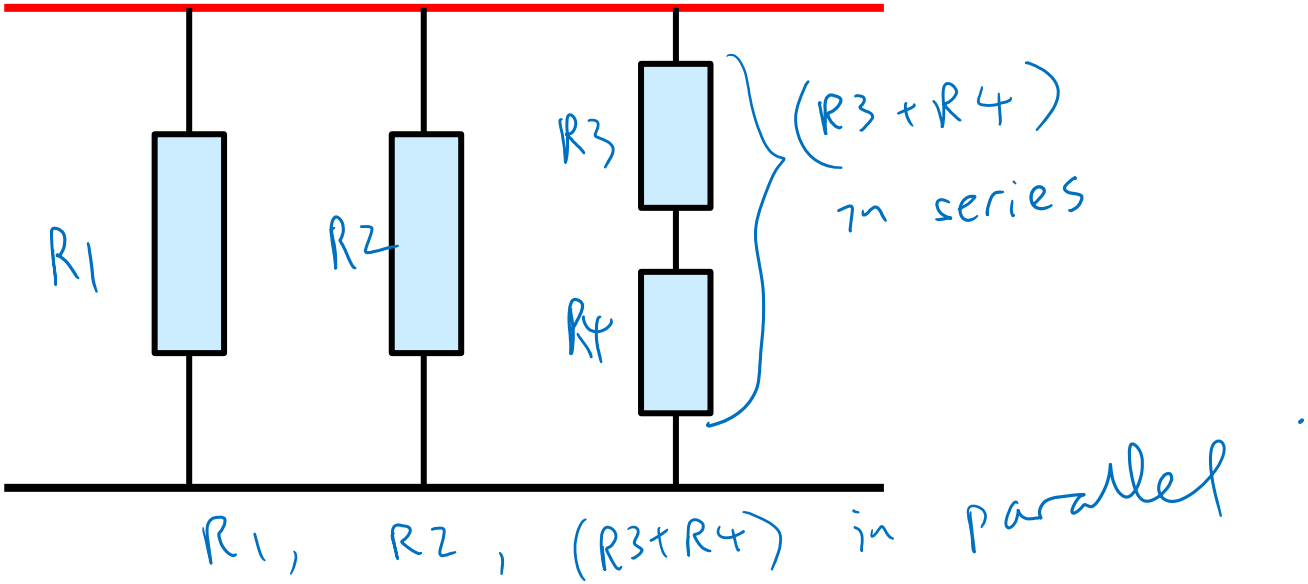
or

D* negated

but not both

A	B	C*	D*	F	
0	0	0	0		m0
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		m5
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		m10
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		m15

How many parallel paths and serial paths are formed by the resistors?



A. 2 parallel, 1 serial

B. 3 parallel, 2 serial

✓ C. 3 parallel, 1 serial

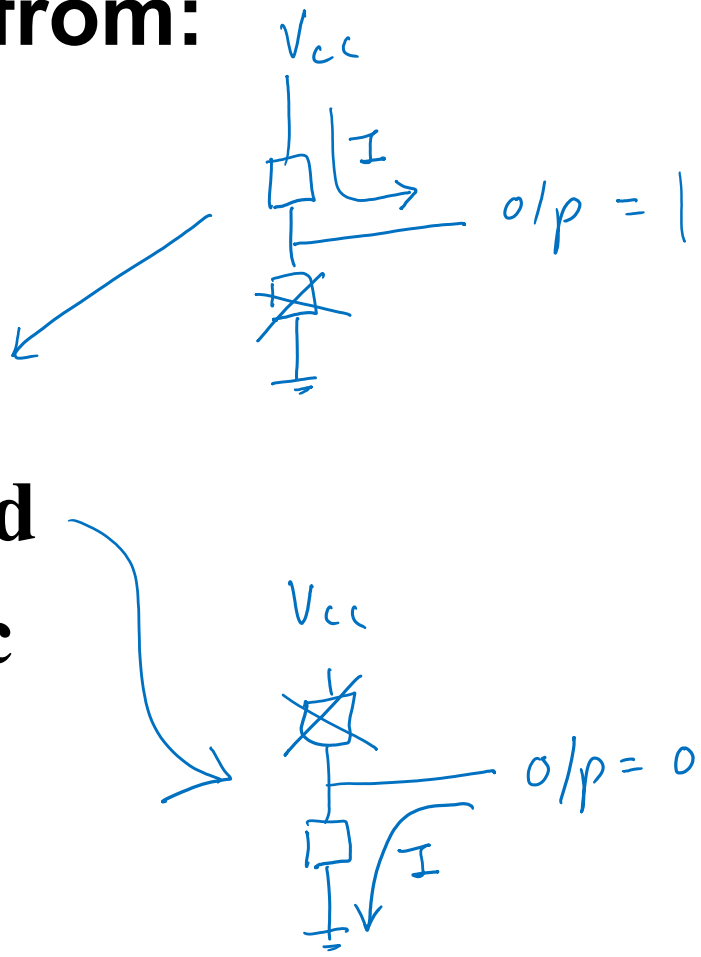
For a logic output to go high, current must flow from:

A. Vcc to Gnd

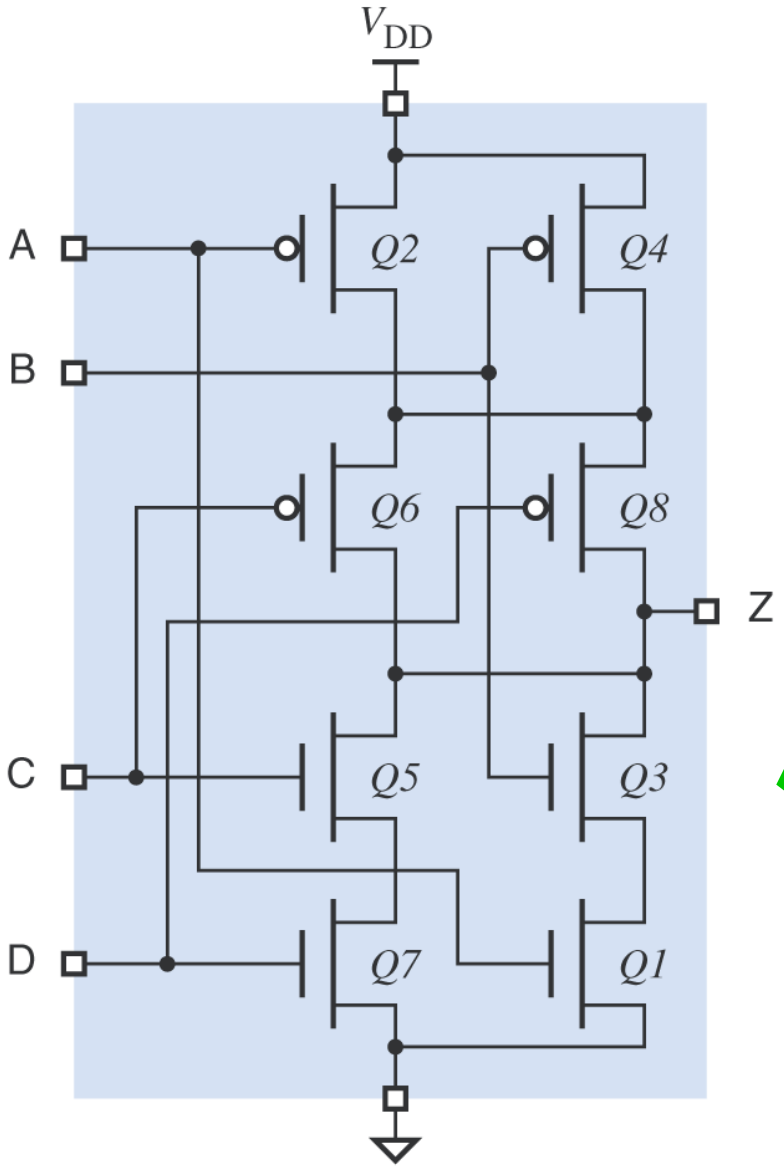
B. Vcc to output

C. Output to Gnd

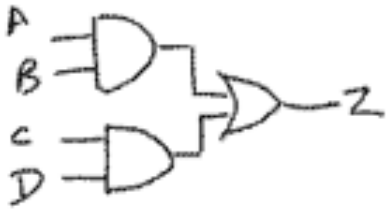
D. Output to Vcc



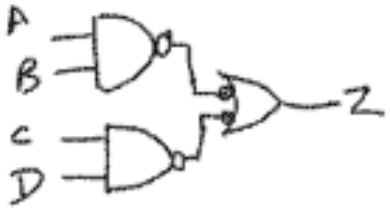
Which circuit does it implement?



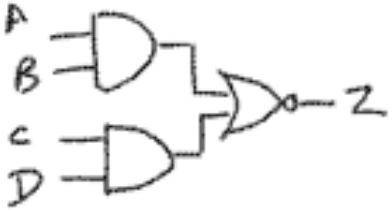
A.



B.



C.



D.

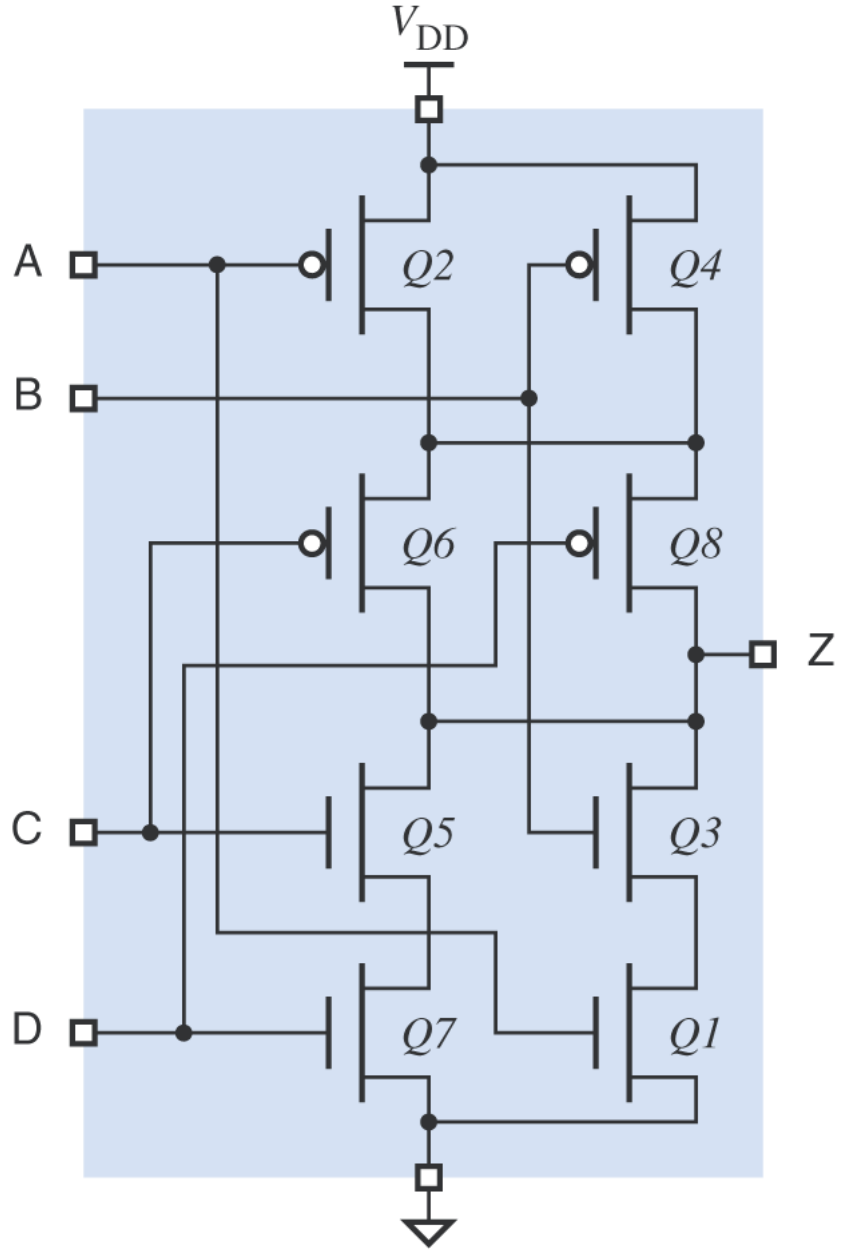


Fig. 3-20 Wakerly

For Z=0
Both Q3 & Q1 must be ON, or
Both Q5 and Q7 must be ON
Q2,Q4,Q6,Q8 must be OFF
i.e. A=B=1, or C=D=1

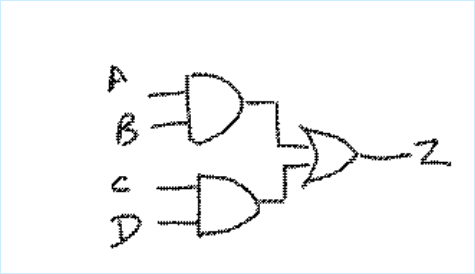
For Z=1
Q2 or Q4 must be ON, and
Q6 or Q8 must be ON
Q1,Q3,Q5,Q7 must be OFF
i.e. A=0 or B=0, and
C=0 or D=0

For Z=0
Both Q3 & Q1 must be ON, or
Both Q5 and Q7 must be ON
i.e. A=B=1, or C=D=1

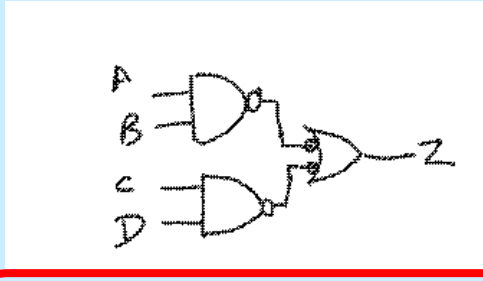
For Z=1
Q2 or Q4 must be ON, and
Q6 or Q8 must be ON
i.e. A=0 or B=0, and C=0 or D=0

Which circuit does it implement?

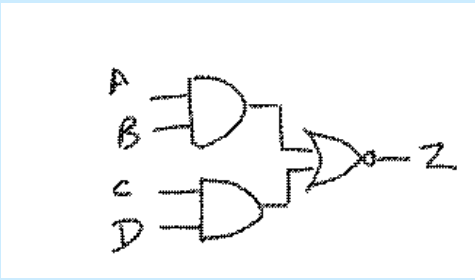
(A)



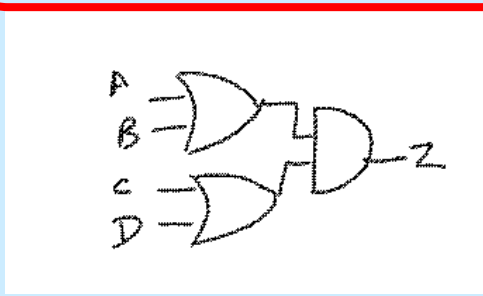
(B)



(C)



(D)



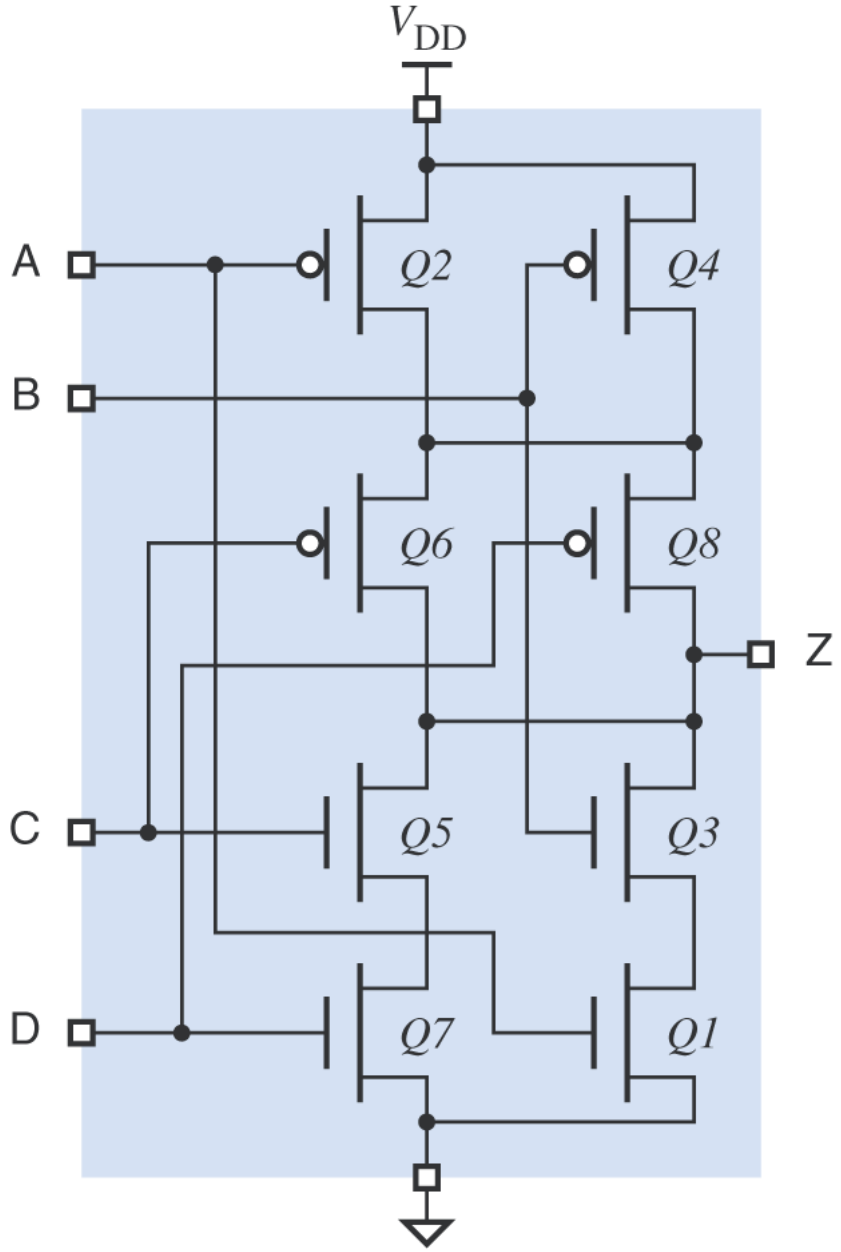
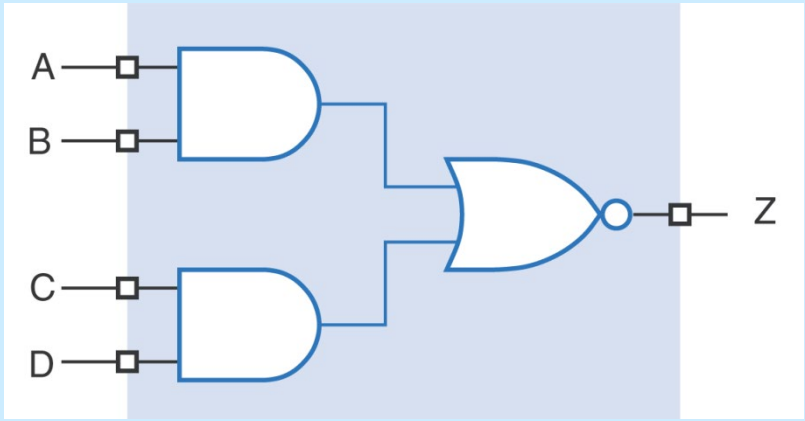


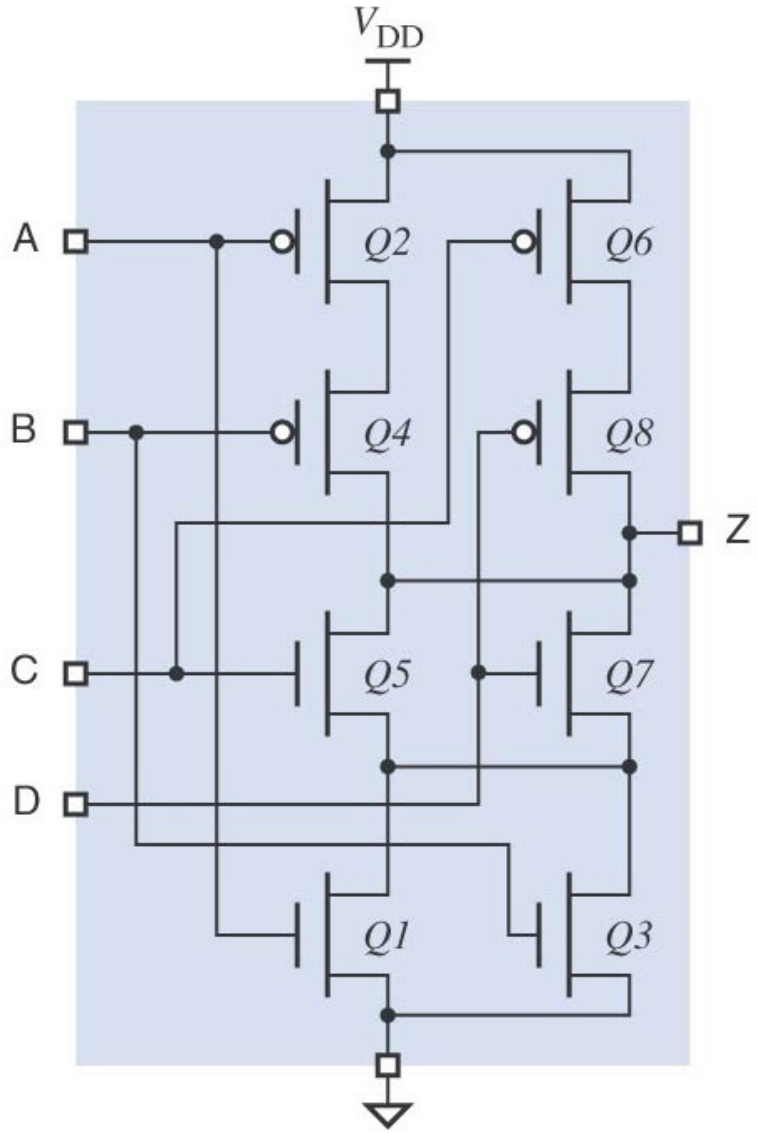
Fig. 3-20 Wakerly

When A=B=1,
Q2 and Q4 OFF,
Q1 and Q3 ON
Z=0
Similarly when C=D=1,
Q6 and Q8 OFF,
Q5 and Q7 ON
Z=0



Z = (AB + CD)'

Which circuit does it implement?

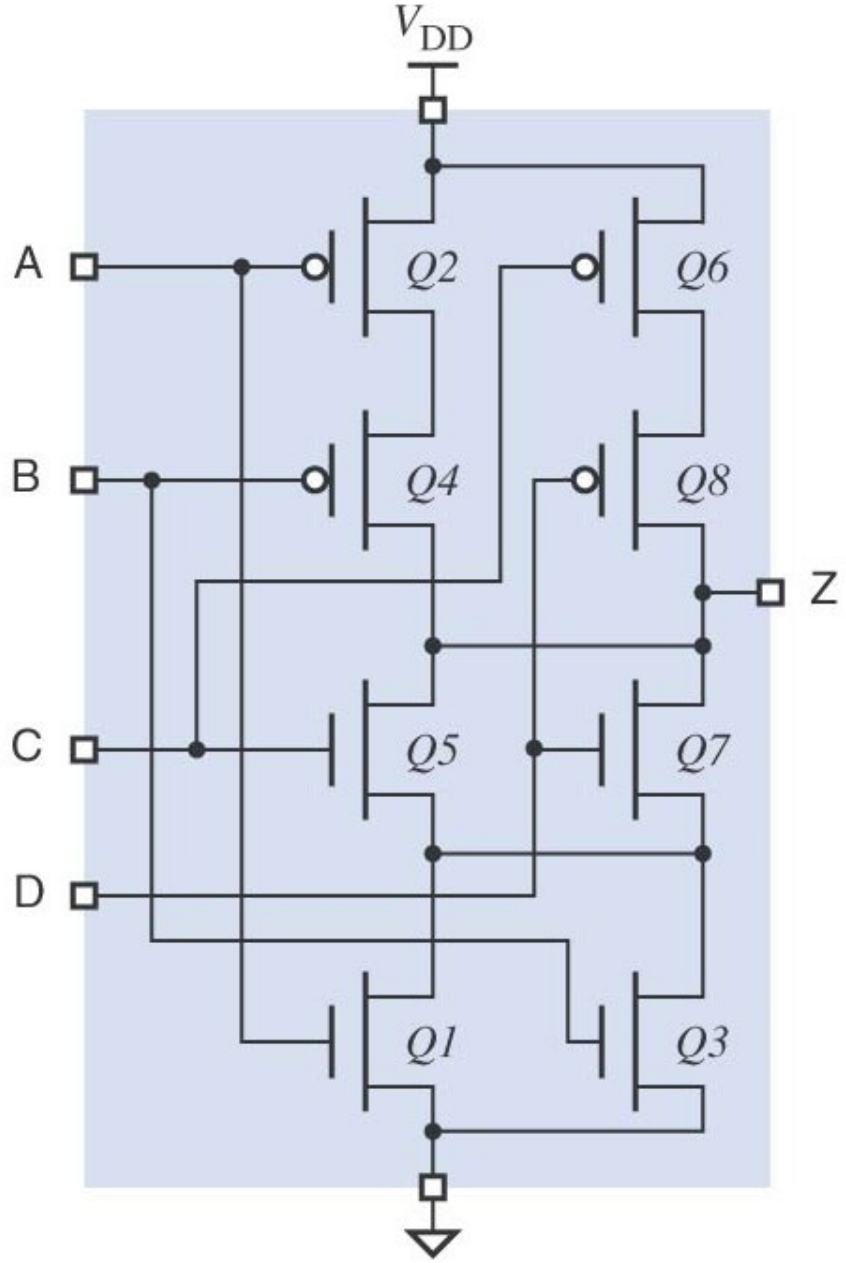


A. Z = (A+B)' (C+D)'

B. Z = (A'+B') (C'+D')

C. Z = (AB + CD)'

D. Z = [(A+B) (C+D)]'



For Z=1
Both Q2 & Q4 must be ON, or
Both Q6 and Q8 must be ON
Q1,Q3,Q5,Q7 must be OFF
i.e. A=B=0, or C=D=0

For Z=0
Q1 or Q3 must be ON, and
Q5 or Q7 must be ON
Q2,Q4,Q6,Q8 must be OFF
i.e. A=1 or B=1, and
C=1 or D=1

For Z=1
Both Q2 & Q4 must be ON, or
Both Q6 and Q8 must be ON
i.e. A=B=0, or C=D=0

For Z=0
Q1 or Q3 must be ON, and
Q5 or Q7 must be ON
i.e. A=1 or B=1, and C=1 or D=1

Which circuit does it implement?

(A) Z = (A+B)' (C+D)'

(B) Z = (A'+B') (C'+D')

(C) Z = (AB + CD)'

(D) Z = [(A+B) (C+D)]'

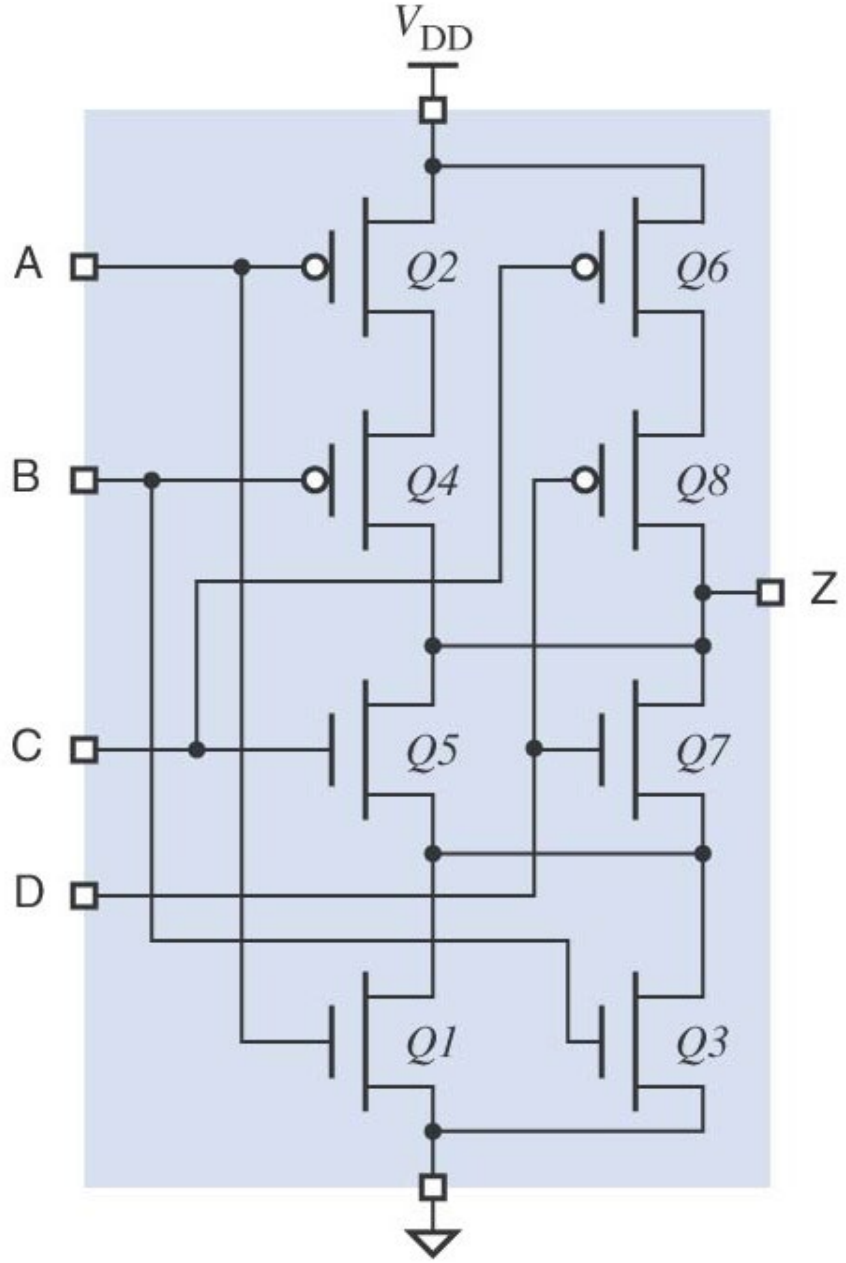
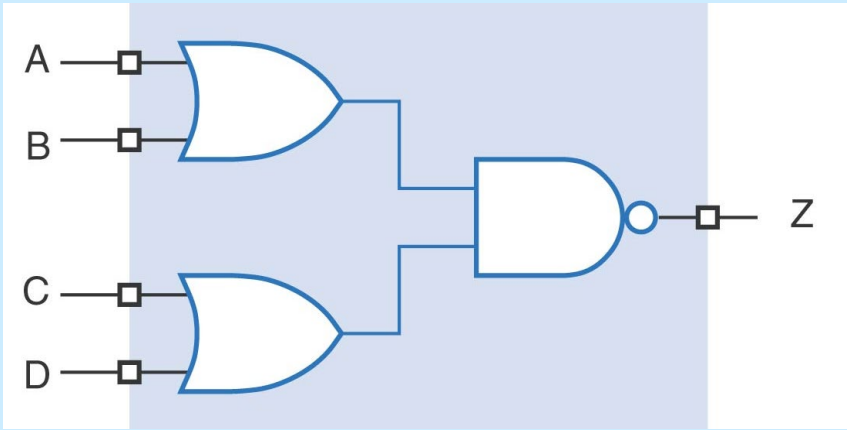


Fig. 3-22 Wakerly

When A=B=0,
Q2 and Q4 ON,
Q1 and Q3 OFF
Z=1
Similarly when C=D=0,
Q6 and Q8 ON,
Q5 and Q7 OFF
Z=1



Z = [(A+B) (C+D)]'