IEEE/ANSI Standard Logic Symbols

- use rectangular symbols
- bubbles replaced by small triangles or wedges (think 0)
- You are required to recognise these symbols but not required to draw these symbols

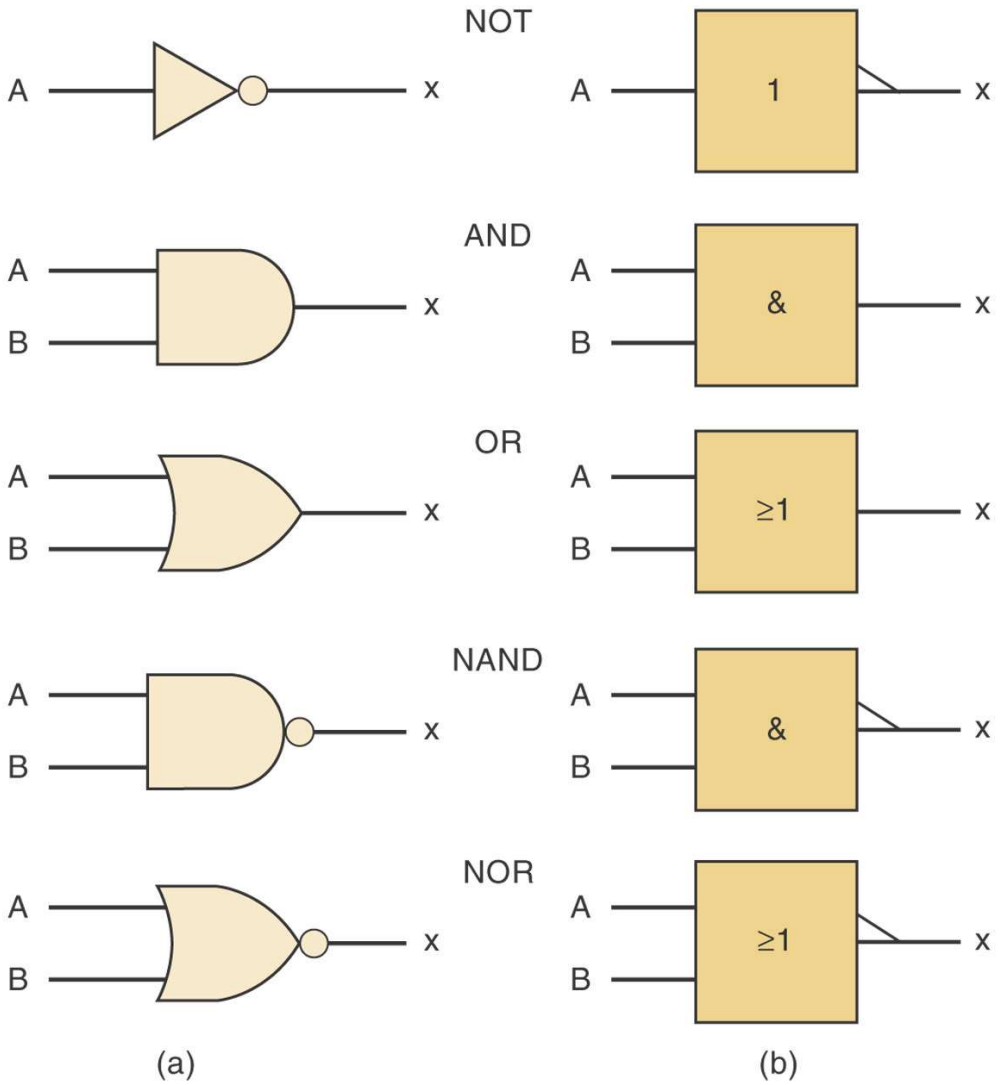
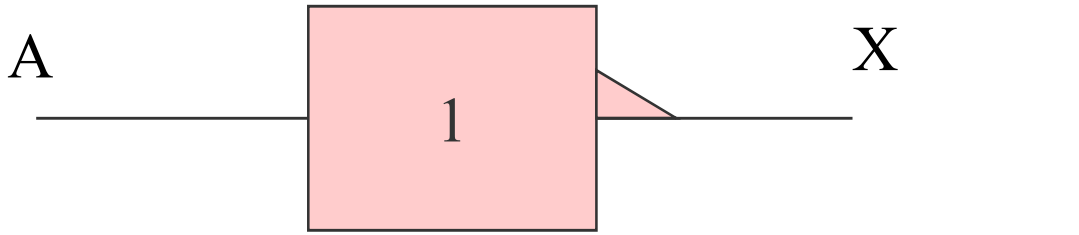


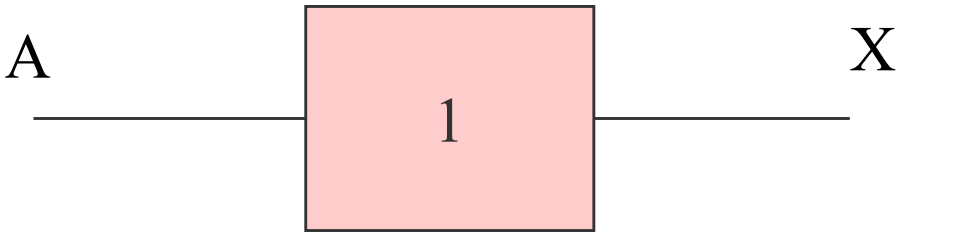
Fig. 3-41: Traditional and IEEE logic symbols (Tocci 10th ed)

Output is 0 when “the single input” is 1



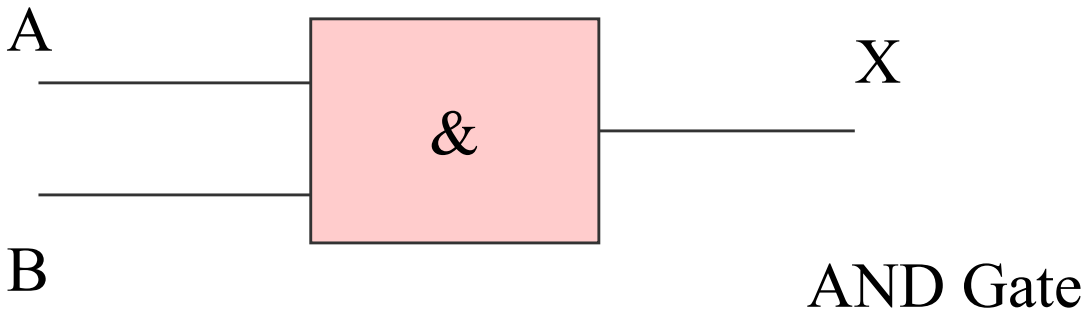
NOT Gate

Output is 1 when “the single input” is 1

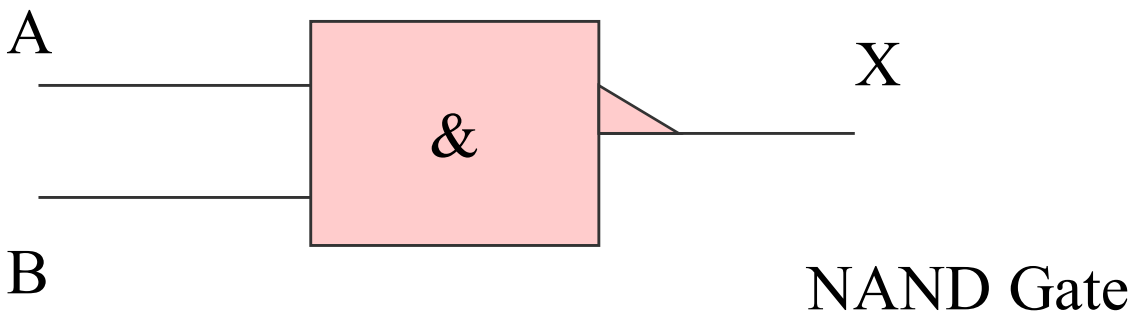


Buffer

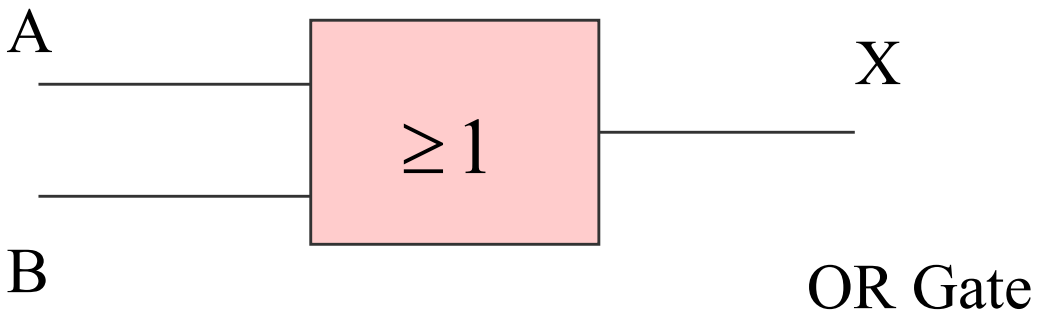
Output is 1 when “all the inputs” are 1



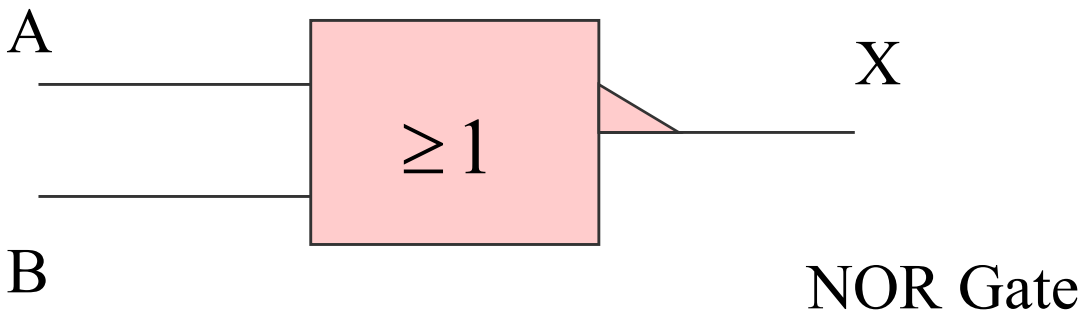
Output is 0 when “all the inputs” are 1



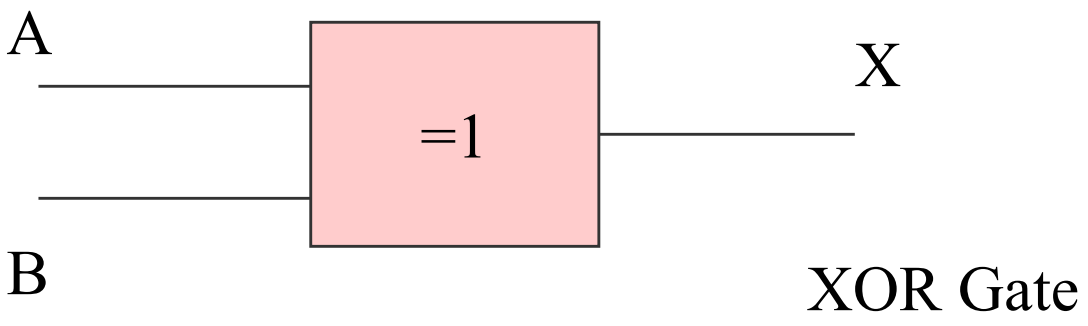
Output is 1 when “at least one input is” 1



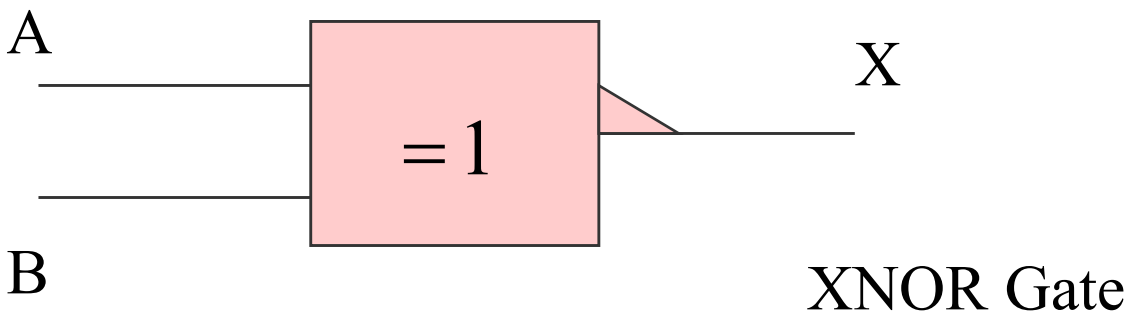
Output is 0 when “at least one input” is 1



Output is 1 when “exactly one input” is 1



Output is 0 when “exactly one input” is 1



IEEE/ANSI Standard Logic Symbols

The symbol inside the rectangle specifies the requirement on the inputs

- & : “all the inputs”
- 1 : “the single input” – only true for a buffer or an inverter
- ≥ 1 : “at least one input”
- =1 : “exactly one input” – e.g. on a 2-input XOR gate