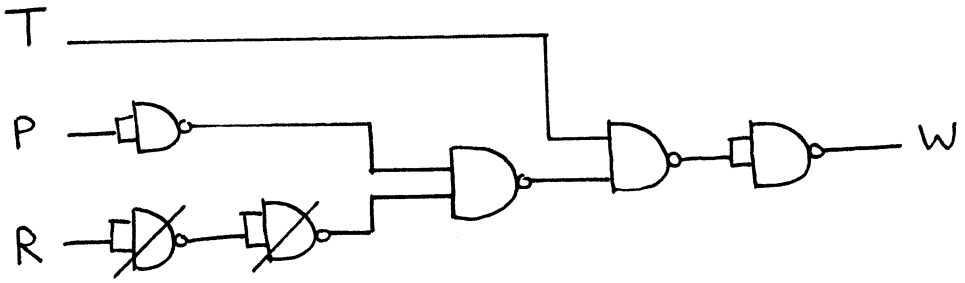
SC1005 Digital Logic Revision Practice (answers)

1. a) W = T • (P + R')
Therefore, warning light is activated when temperature is ≥ 200°F **AND** (Either pressure is ≥ 220 psi **OR** speed is < 4800 rpm)

b)



2. ALARM = PANIC + (ACTIVATE • EXITING' • SECURE')

SECURE = WINDOW • DOOR • GARAGE

∴ ALARM = PANIC +
[ACTIVATE • EXITING' • (WINDOW • DOOR • GARAGE)']

3. Redeem = Above50 (Sunday + After5)

Redeem = 1 only when Above50=1, and either Sunday=1 or After5=1

Redeem* = Above50* + (Sunday*)(After5*)

Redeem* = 0 only when Above50*=0, and either Sunday*=0 or After5*=0

4. NASA logic circuit.

G = 1 when
A = X, and
B = Y, and
C = Z.

Apply A and X to a 2-input XNOR gate, the output will be HIGH when A = X. Similarly, apply B and Y to another 2-input XNOR gate, C and Z to the third 2-input XNOR gate.

G is simply obtained by ANDing the three XNOR outputs together.

Assuming that XYZ = 110 represents 600 psi to 699 psi, and XYZ = 111 represents 700 to 799 psi, R should go HIGH when XY = 1.

Hence R = XY

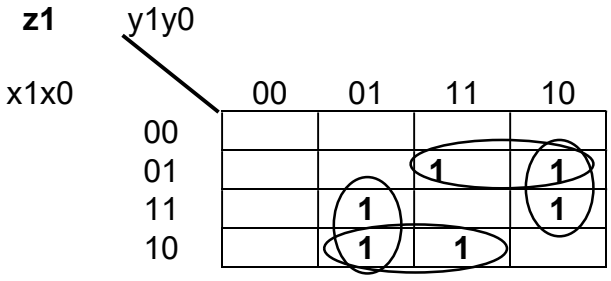
5. Multiplier circuit.

Truth table:

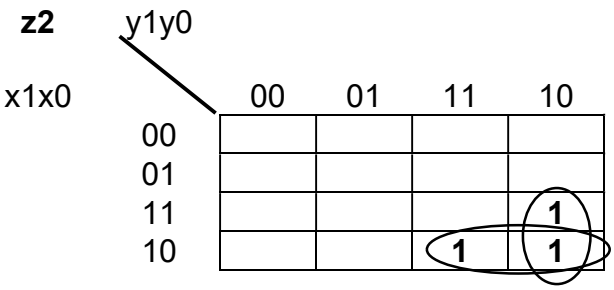
Inputs				Outputs			
x1	**x0**	**y1**	**y0**	**z3**	**z2**	**z1**	**z0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

From observation, **z3 = x1.x0.y1.y0**

z0 = x0.y0

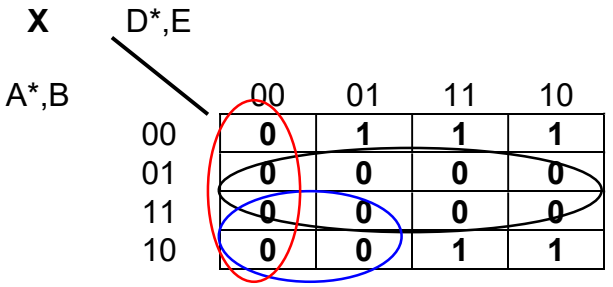


z1 = x1.y1'.y0 + x1.x0'.y0 + x1'.x0.y1 + x0.y1.y0'
= x1.y0.(y1' + x0') + y1.x0.(x1' + y0')



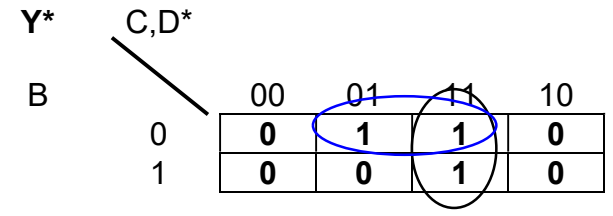
z2 = x1.x0'.y1 + x1.y1.y0'
= x1.y1.(x0' + y0')

6. K-map for X (loop for POS)



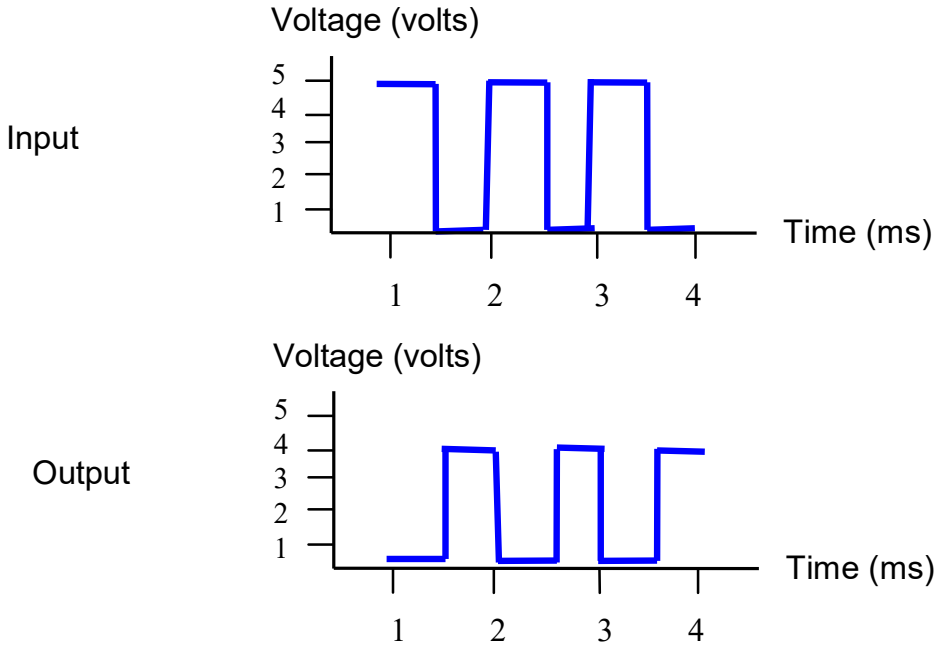
X = B' (A*' + D*) (D* + E)

K-map for Y* (loop for SOP)



Y* = D*B' + D*C

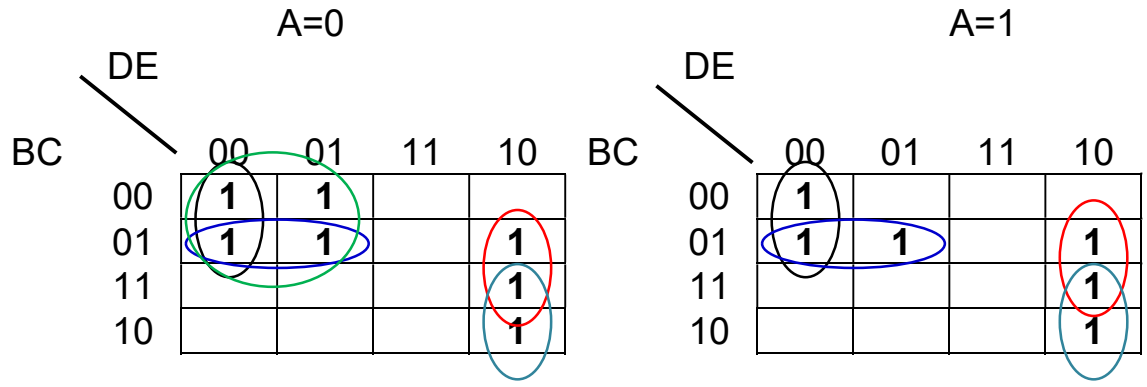
7. The input of a TTL inverter is a 1 kHz squarewave. The following timing diagram is supposed to show the observed input and output. Point out and correct the three errors in the timing diagram.



Errors corrected:
1. frequency: 1 kHz => period is 1 ms.
2. Voltage range for TTL logic 0 output is 0 – 0.8 V.
3. output of inverter should be opposite of input at all time.

8.

5-variable k-map



Z = A'B'D' + B'D'E' + B'CD' + CDE' + BDE'