Accessing Verilog Tools from home

The following Verilog resources are available to assist you with your Verilog skills. I would recommend you restrict your options to one of the first 3, which are listed below.

1. Use **Vivado 2018** from the School (SCSE) virtual desktop. This will enable you to use the full Xilinx tool chain up to where you need to programme the device (that is design entry, simulation, synthesis, place & route and bitstream generation). You will need to use Citrix Receiver to access the SCSE virtual computing service (see Content-> Laboratory materials, then open the "Instructions for Citrix Receiver" document). You will also need to VPN in if outside the University. When you access the virtual desktop, make sure you select Vivado 2018 and NOT Vivado 2012.

2. Alternatively, you could use an on-line tool, such as: https://www.edaplayground.com/. This is the easiest to use as you just need a browser. It will allow you to compile and simulate your Verilog code. In the left panel, select "System Verilog/Verilog", none, none. In Tools & Simulators select one of the free simulators (I tried Icarus Verilog 0.10.0 and it worked OK). Tick the box "Open EPWave after run". To run EPWave, you will need to generate the waveform files during your run. The easiest way to do this is by adding a second initial block to your testbench file with the following system calls:

```
initial begin
        $dumpfile("dump.vcd");
        $dumpvars(1);
end
```

3. You could download and install Vivado on your own machine. The installation is available at https://www.xilinx.com/support/download.html. Note that the current version is Vivado 2021.1. We use Vivado 2018.3 in the lab (as the older versions tend to be a bit more stable and the newer versions support newer devices which we do not use). To get 2018.3 go to "Vivado Archive" in the left panel.
Note that you will need to register and use the free webpack version. This will also allow you to perform design entry, simulation, synthesis, place & route and bitstream generation, but not use the hardware (unless you buy a Basys 3 board). The code package size is very large.

4. you could use a standalone package (but you will need to install these) such as:
   Icarus Verilog for offline simulation: http://iverilog.icarus.com/
   Verilator: https://www.veripool.org/verilator/
   There are other less stable tools, such as ghdl and cver but I do not recommend these.

An example for EDA playground.
Enter the top module into the design window and the bottom module into the testbench window.

```
module adder #(parameter SIZE=32)(input Cin, input [SIZE-1:0] A, B, output Cout, output [SIZE-1:0] Sum);
	assign {Cout, Sum} = A + B + Cin;
endmodule


module adder_tb ();
	parameter SIZE = 32;
	reg CIN;
	reg [SIZE-1:0] A, B;
	wire CO;
	wire [SIZE-1:0] Sum;

	adder uut1 (.Cin(CIN), . A(A), .B(B), .Cout(CO), .Sum(Sum));

	initial begin
		A=0; B=0; CIN=0;
		#10 A=2;
		#10 B=3;
		#10 CIN=1;
		#10 A=7;
		#10 B=5;
		#10;
	end

	initial begin
		$dumpfile("dump.vcd");
		$dumpvars(1);
	end
endmodule
```