

SC1005 Digital Logic

Tutorial 10

- Q1. Design a finite state machine that has a single input and single output. It outputs a 1 from the second consecutive high input, and only then outputs a zero after the second consecutive low input. Hence, two consecutive 1 inputs, get a high output, that stays until two consecutive low inputs are received.
- (a) Implement the finite state machine in Verilog using a combinational always block for the state transition logic.
 - (b) Redo the implementation using only assign statements for the state transition logic.
 - (c) Show how the state machine would respond to the following sequence of inputs:
0,1,0,1,1,0,1,1,0,0,1,0,1,1