How many different 2-input truth tables can be constructed? Assume each has 1 output.

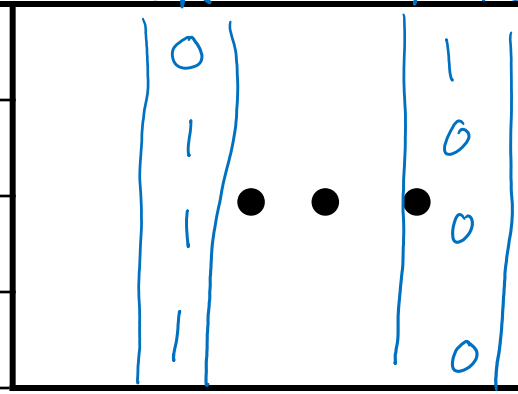
A. 4

B. 8

C. 12

D. 16

Inputs		Possible outputs								
a	b									
0	0	0	0	0					1	1
0	1	0	0	0					1	1
1	0	0	0	1					1	1
1	1	0	1	0					0	1



trivial

trivial

2^n rows

2^(2^n) columns

Commonly-used 2-input logic gates:

- **AND, NAND**
- **OR, NOR**
- **XOR, XNOR**

Can the truth table be obtained from a timing diagram?

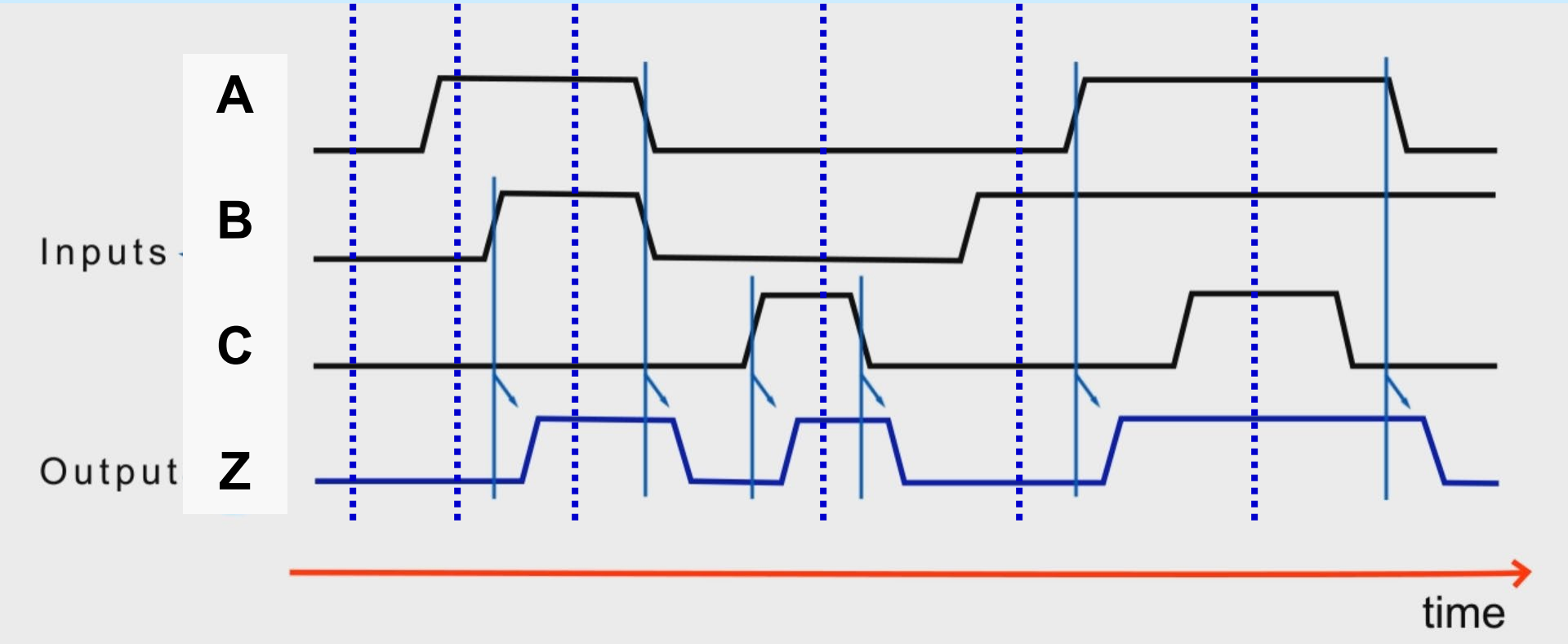


Fig. 3.17 (taken from Wakerly)

Truth table from timing diagram

inputs			output
A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Incomplete truth table

These input combinations did not happen in the timing diagram

inputs			output
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	?
1	0	0	0
1	0	1	?
1	1	0	1
1	1	1	1

A(B+C)' = AB' + AC'

True or false?

A. True

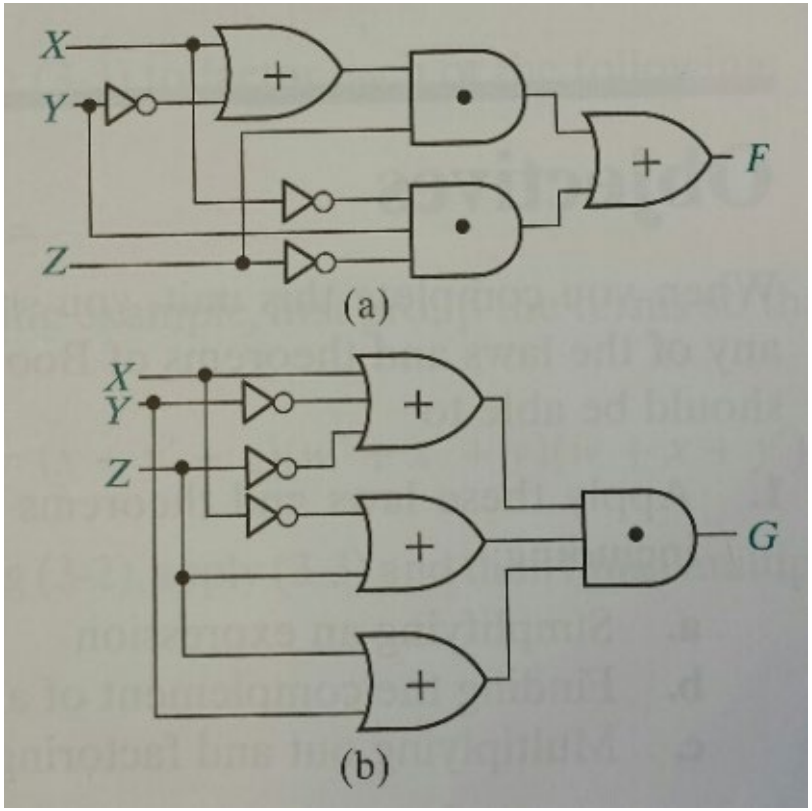
B. False

A (B + C)'
= A (B' C')
= A B' C'

Are these two circuits algebraically equivalent?

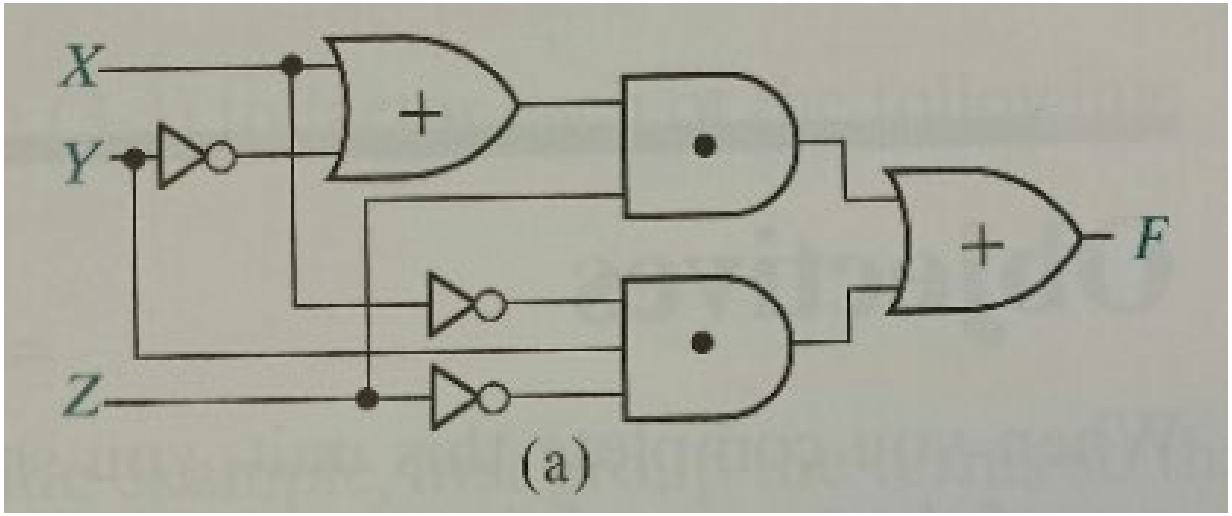
A. Yes

B. No



Source: Q2.30, p 59, Fundamentals of Logic Design, Roth & Kinney, Cengage Learning.

The answer is Yes.



F = (X+Y')Z + X'YZ'

G = (X+Y'+Z')(X'+Z)(Y+Z)

= (X+Y'+Z')(X'Y + X'Z + YZ + ZZ)

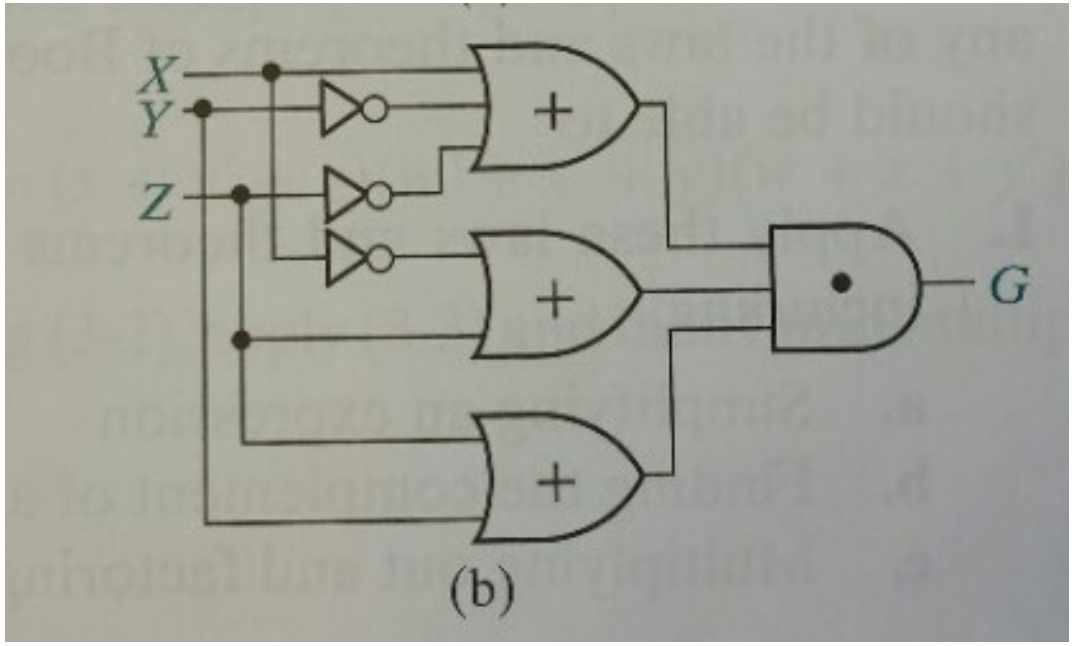
= (X+Y'+Z')[X'Y + Z(X'+Y+1)]

= (X+Y'+Z')[X'Y + Z]

= XZ + Y'Z + X'YZ'

= (X+Y')Z + X'YZ'

= F



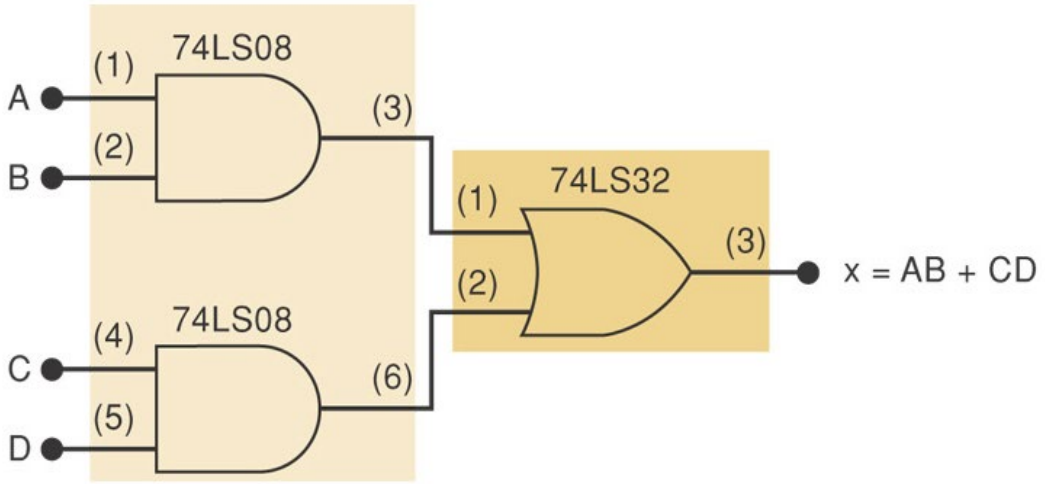
How many NAND gates are needed in total to replace all the gates?

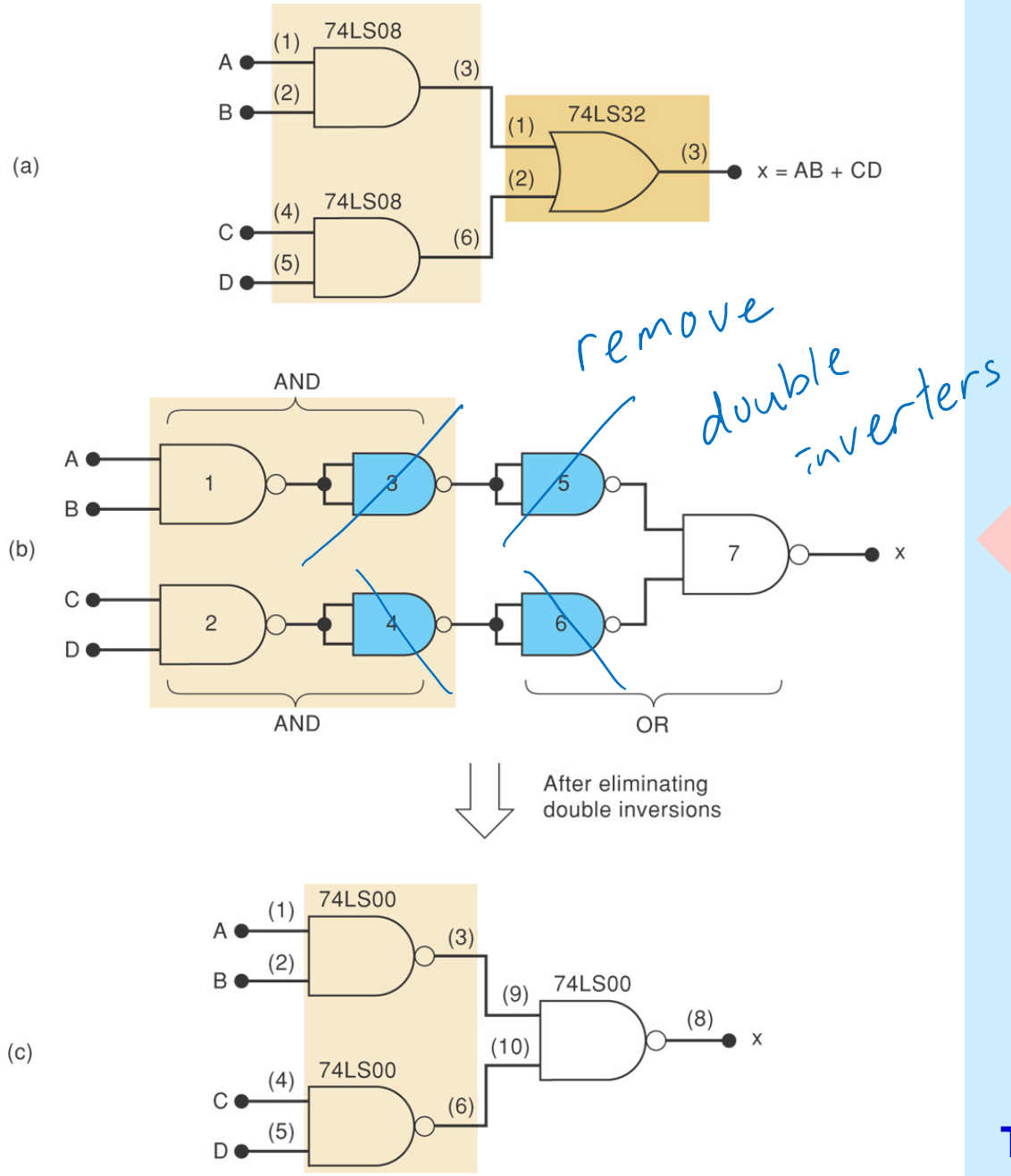
A. 3

B. 4

C. 5

D. 6





Example:

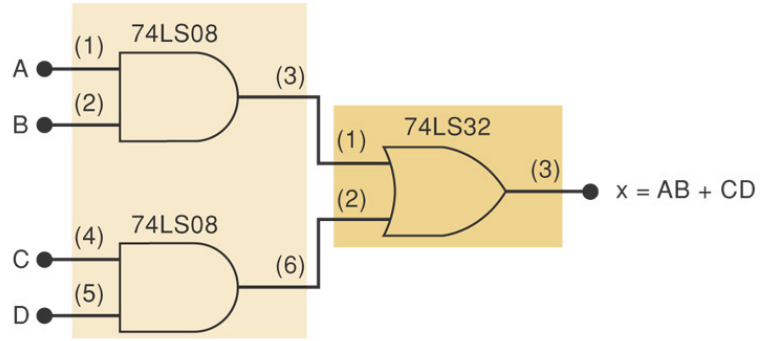
NAND gates replace AND, OR

By diagram

Figure 3-32

Tocci, Widmer, Moss. 10th ed.

(a)



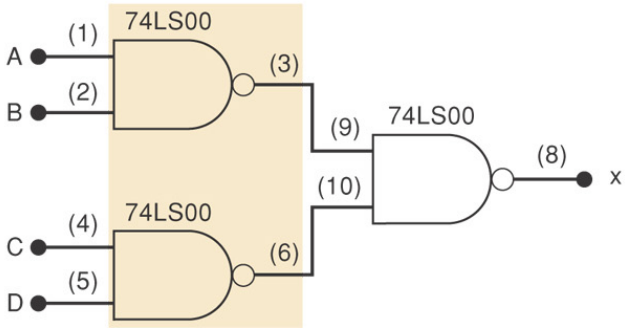
$$AB + CD = [\,(AB + CD)'\,]'$$

$$= [\,(AB)'\,(CD)'\,]'$$

NAND

NAND NAND

(c)



Example:

NAND gates replace AND, OR

By Boolean expression

Figure 3-32

Tocci, Widmer, Moss. 10th ed.

Universal gates always reduce the number of gates used. True or false?

A. True

B. False