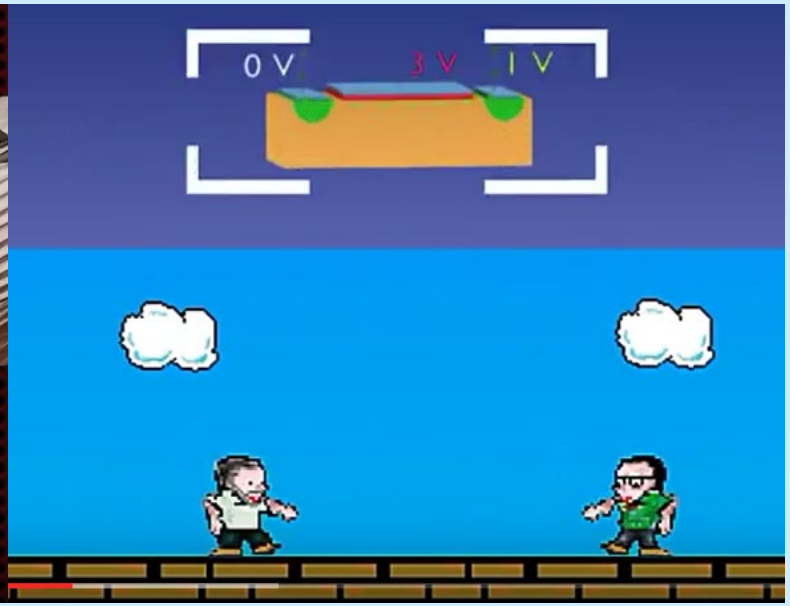
Lecture 9 key concepts

- Digital circuits: made up of resistors, diodes, transistors
- Different physical properties to represent logic
- Logic families: TTL & CMOS voltage range
- How to turn on/off transistors
- Active logic levels, asserted/negated/de-asserted – in relation to enable/disable

Which concepts are unclear to you after viewing L9?

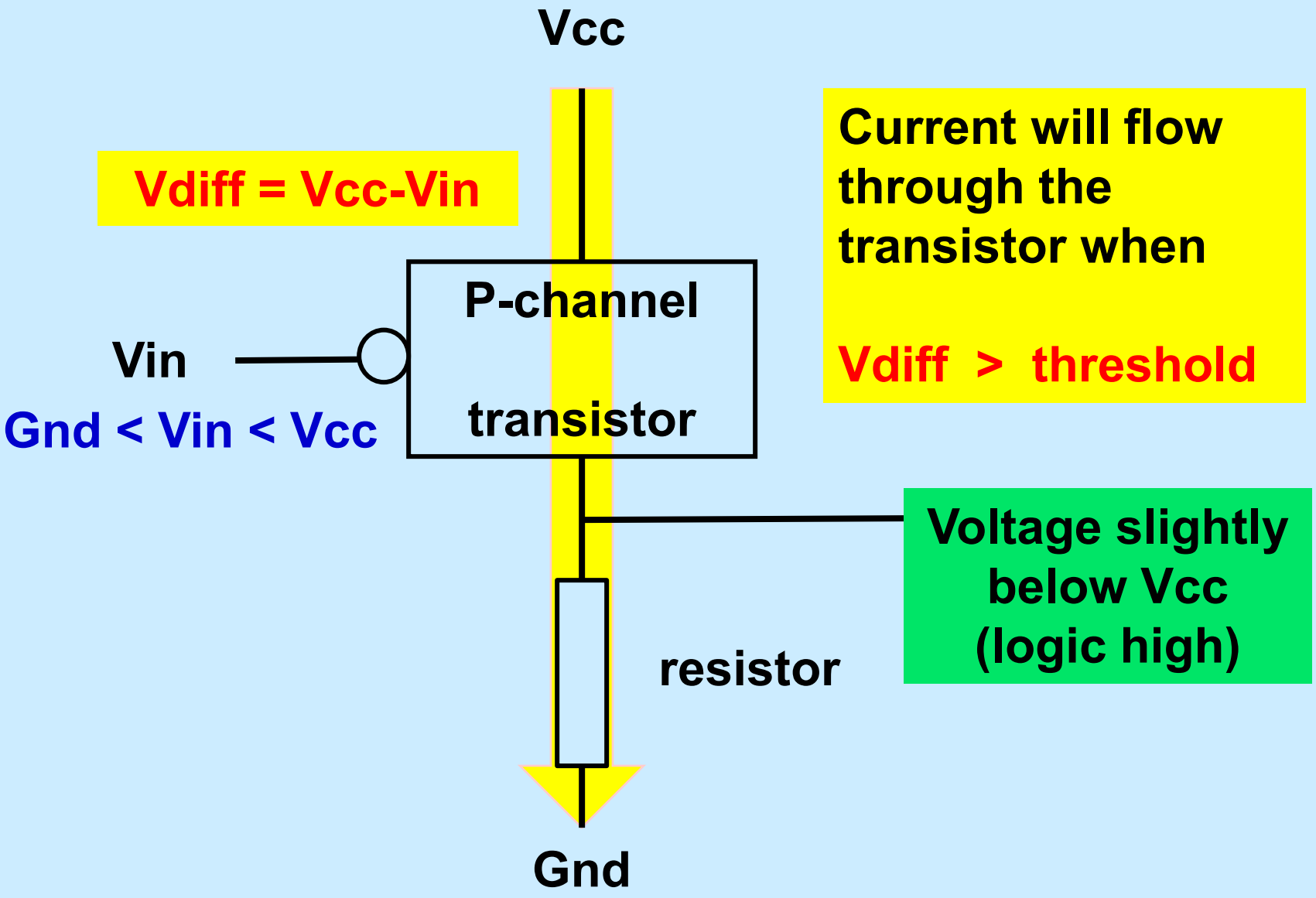
A. TTL and CMOS
B. Turning on/off a transistor
C. Active high/low and asserted/negated
D. None

youtube videos on how transistors work

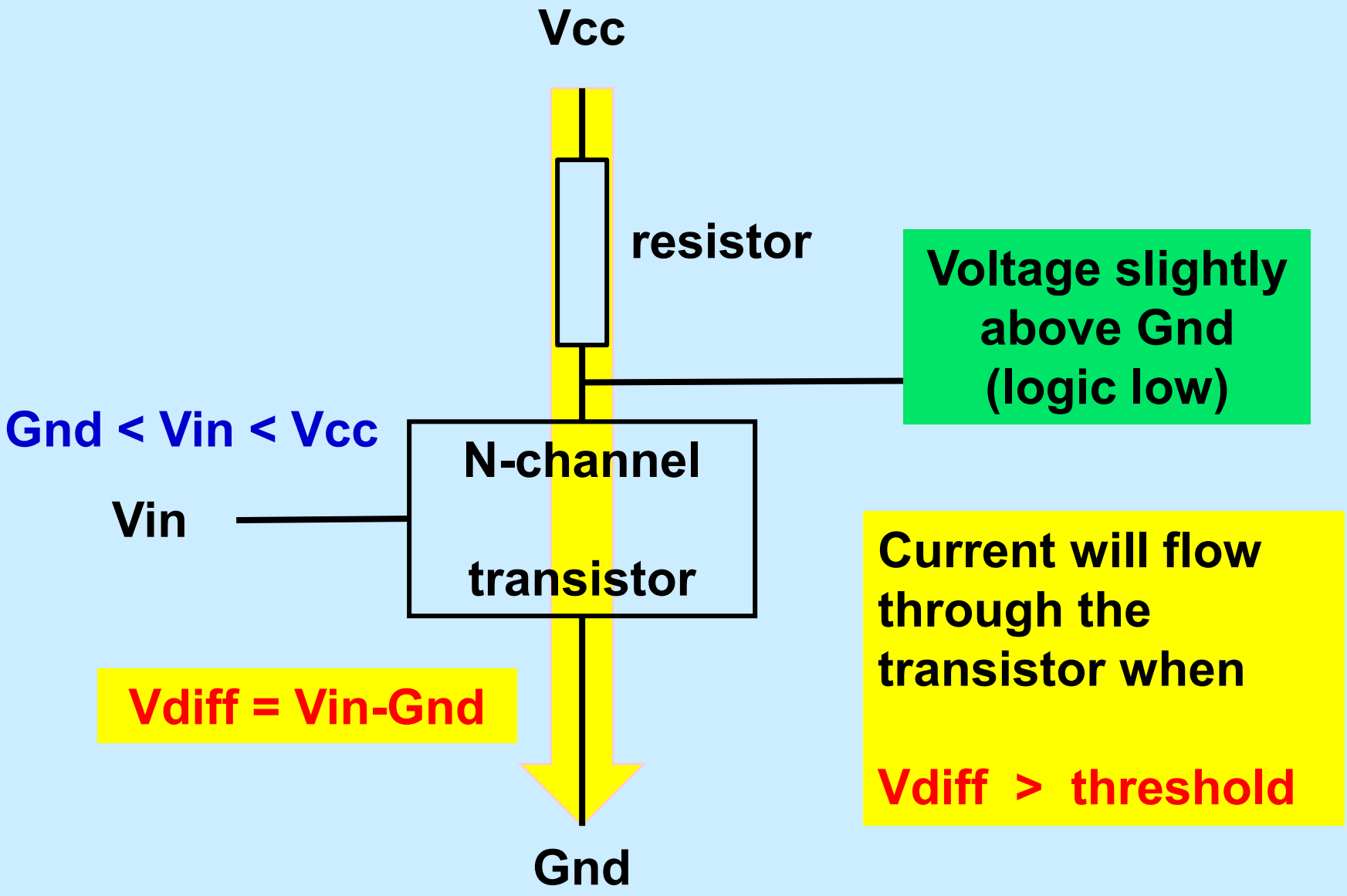


https://www.youtube.com/watch?v=IcrBqCFLHIY

https://www.youtube.com/watch?v=QO5FgM7MLGg



http://www.falstad.com/circuit/e-pmosfet.html F910-4



http://www.falstad.com/circuit/e-nmosfet.html

Both active-high x and active-low y* are asserted. Which one below is true?

A. x=1, y*=0

B. x=0, y*=1

C. x=1, y*=1

D. x=0, y*=0

Both active-high x and active-low y* are negated. Which one below is true?

A. x=1, y*=0

B. x=0, y*=1

C. x=1, y*=1

D. x=0, y*=0

Asserted and negated

- A signal is asserted when it is in its active logic level
- Otherwise, it is negated

Actual logic level	Active high Signal=1 to have effect	Active low Signal=0 to have effect
asserted	1	0
negated	0	1

Most signals are active high unless otherwise specified

Interpretation of logic expressions

Example 1: all signals active high

$$F = A' B (C+D)$$

F is asserted iff

- **A is asserted / negated , and**
- **B is asserted / negated , and**
- **either C or D is asserted / negated**

Interpretation of logic expressions

Example 2: all signals active low

$$G^* = A^{*\prime}\ B^*\ (C^*+D^*)$$

G* is <u>asserted</u> iff

- **A* is asserted / negated , or**
- **B* is asserted / negated , or**
- **C* and D* are both asserted / negated**

Interpretation of logic expressions

Example 3: mixed signals

$$W = A^{*\prime}\ B'\ (C+D^{*})$$

W is <u>asserted</u> iff

- **A* is asserted / negated , and**
- **B is asserted / negated , and**
- **either C is asserted / negated or D* is asserted / negated**

Interpretation of logic expressions

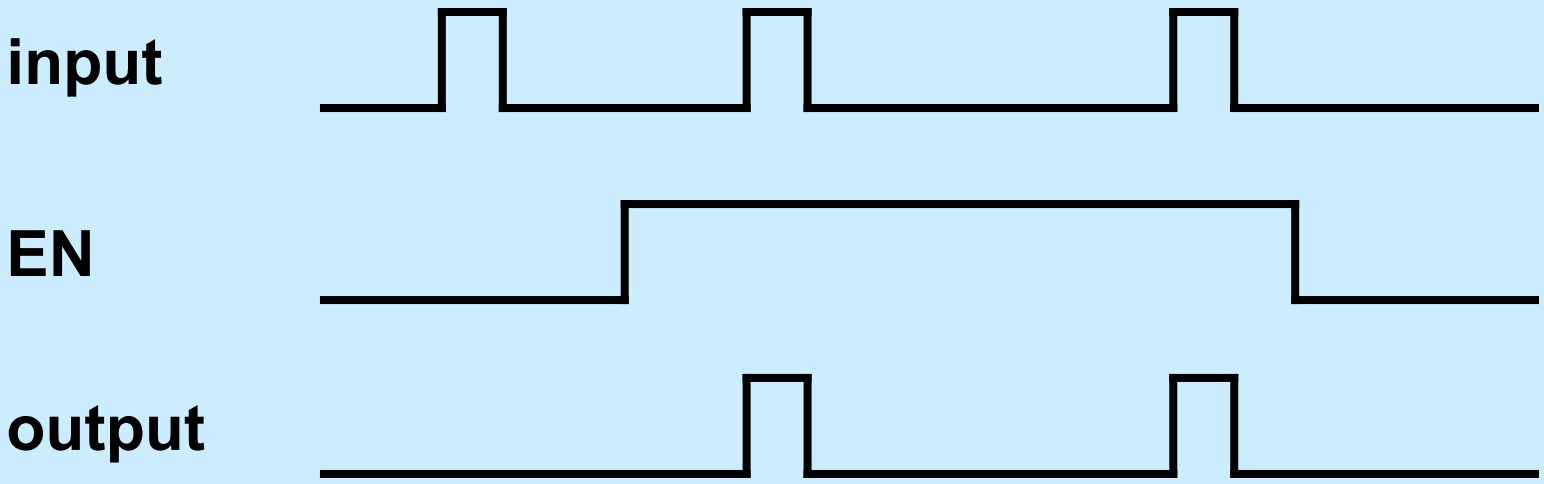
Example 4: mixed signals

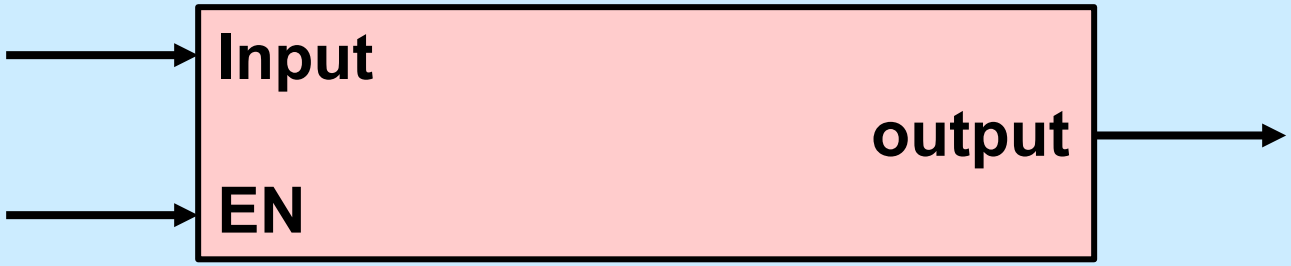
$$V^* = A^{*\prime}\, B' + C + D^*$$

V* is <u>asserted</u> iff

- **A* is asserted / negated or B is asserted / negated , and**
- **C is asserted / negated , and**
- **D* is asserted / negated**

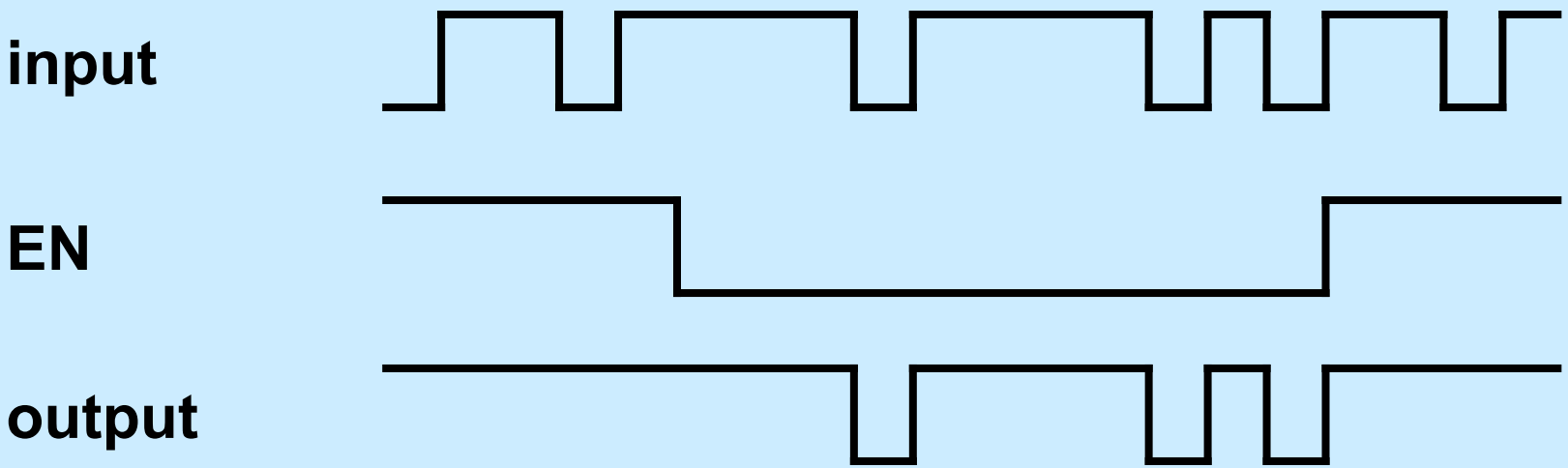
Enable input EN: active high or active low?

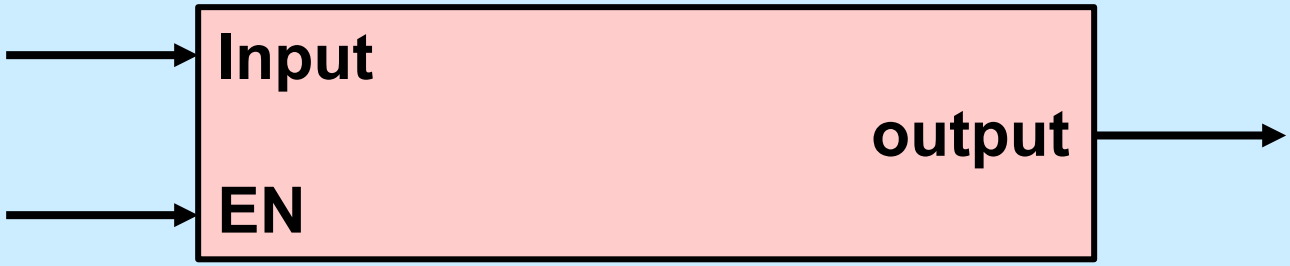




F910-13

Enable input EN: active high or active low?





F910-14

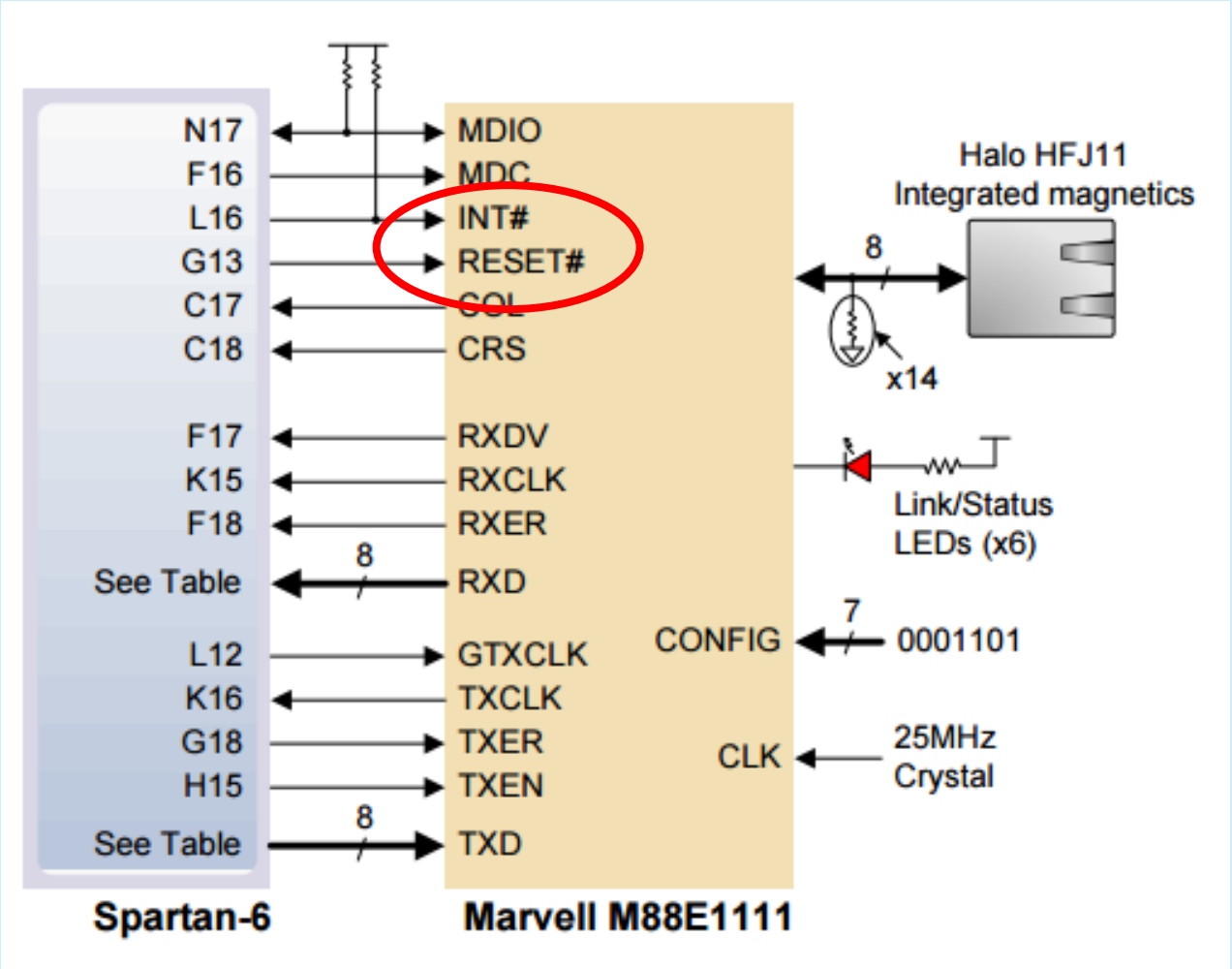
Inputs A, B, C*, D* and output F.
F is only asserted when either A or C* is asserted (but not both), and either B or D* is negated (but not both).
F(A,B,C*,D*)=

A. $\sum m(0, 2, 8, 12)$

B. $\sum m(0, 5, 10, 15)$

C. $\sum m(0, 6, 12, 15)$

Example: Active low inputs



http://electronics.stackexchange.com/questions/7664/why-are-things-like-reset-mclr-active-low-on-most-ics

End of L9 summary

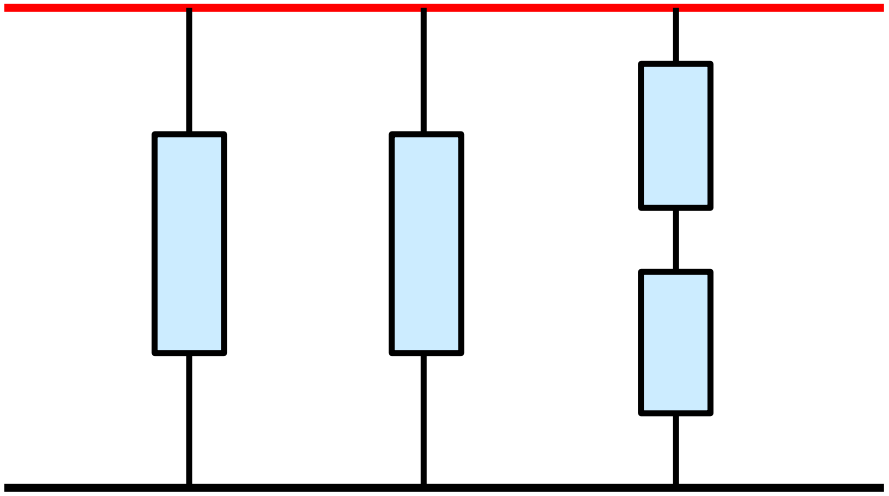
Lecture 10 key concepts

- Basic transistor switching: On/Off
- Parallel and serial current paths
- CMOS logic circuits: PMOS on top, NMOS below – only circuit analysis, no circuit design

Which concepts are unclear to you after viewing L10?

A. Parallel/series current paths
B. Producing 0/1 at logic output
C. CMOS logic circuits
D. None

How many parallel paths and serial paths are formed by the resistors?

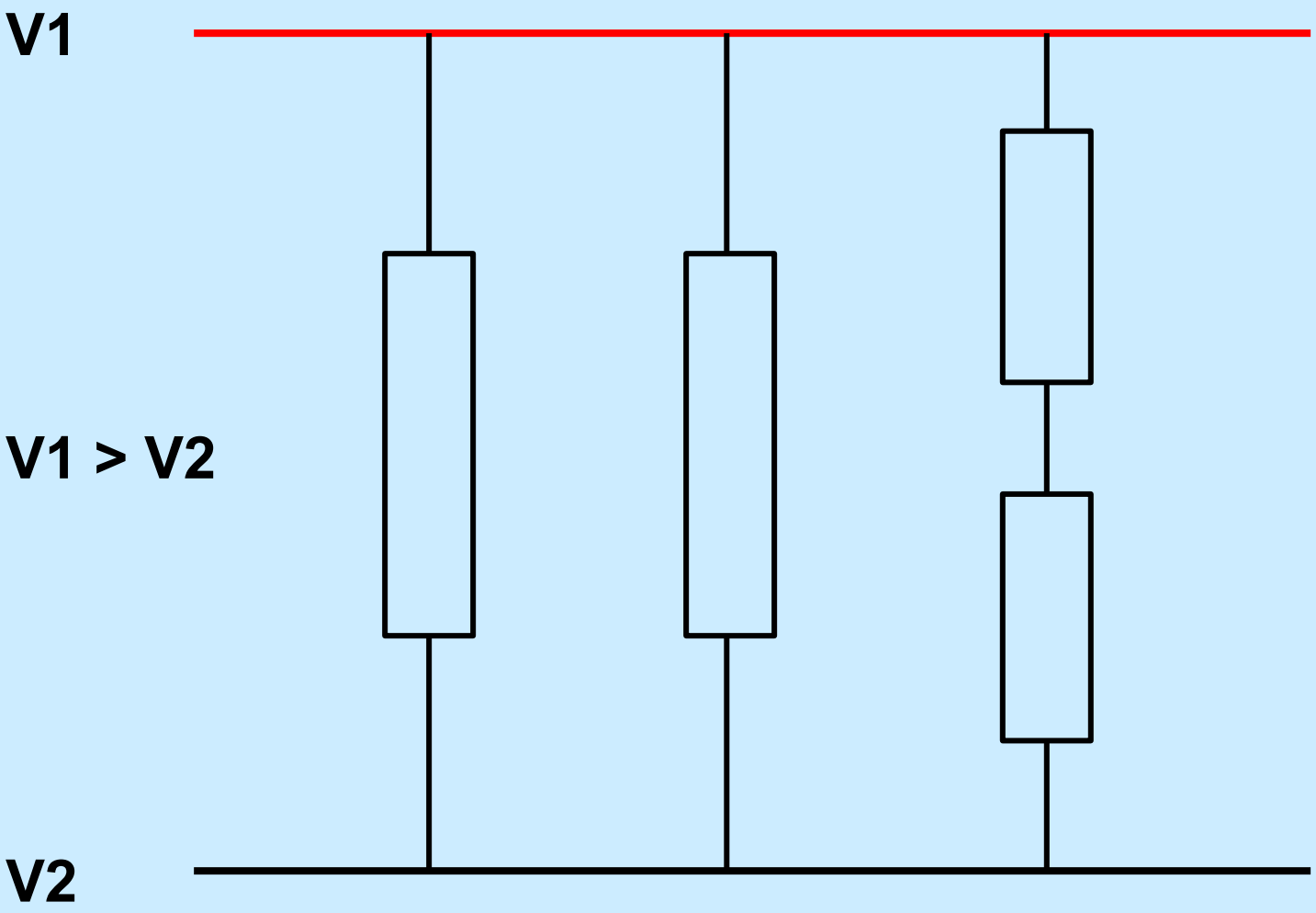


A. 2 parallel, 1 serial

B. 3 parallel, 2 serial

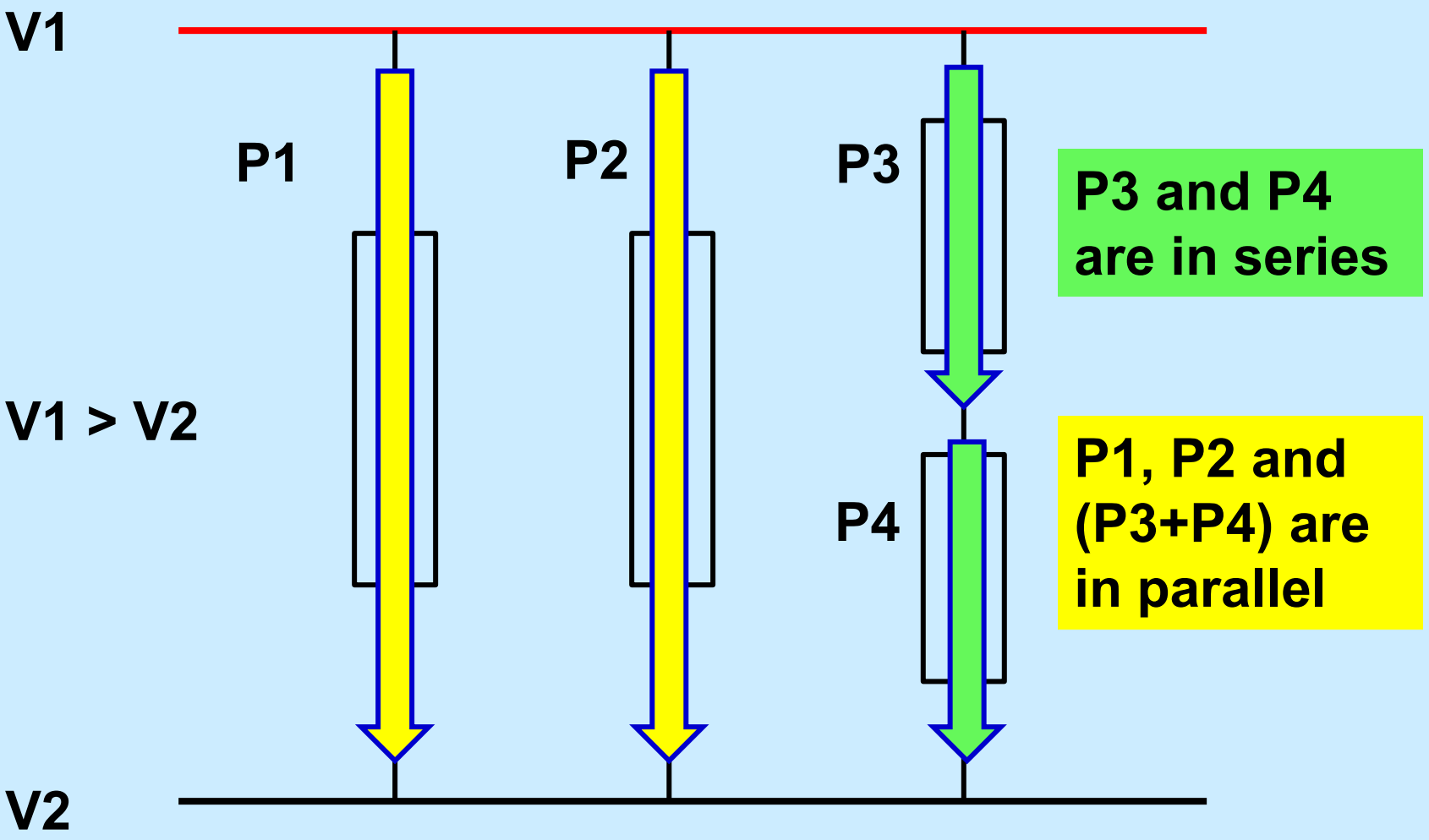
C. 3 parallel, 1 serial

Parallel and serial current paths

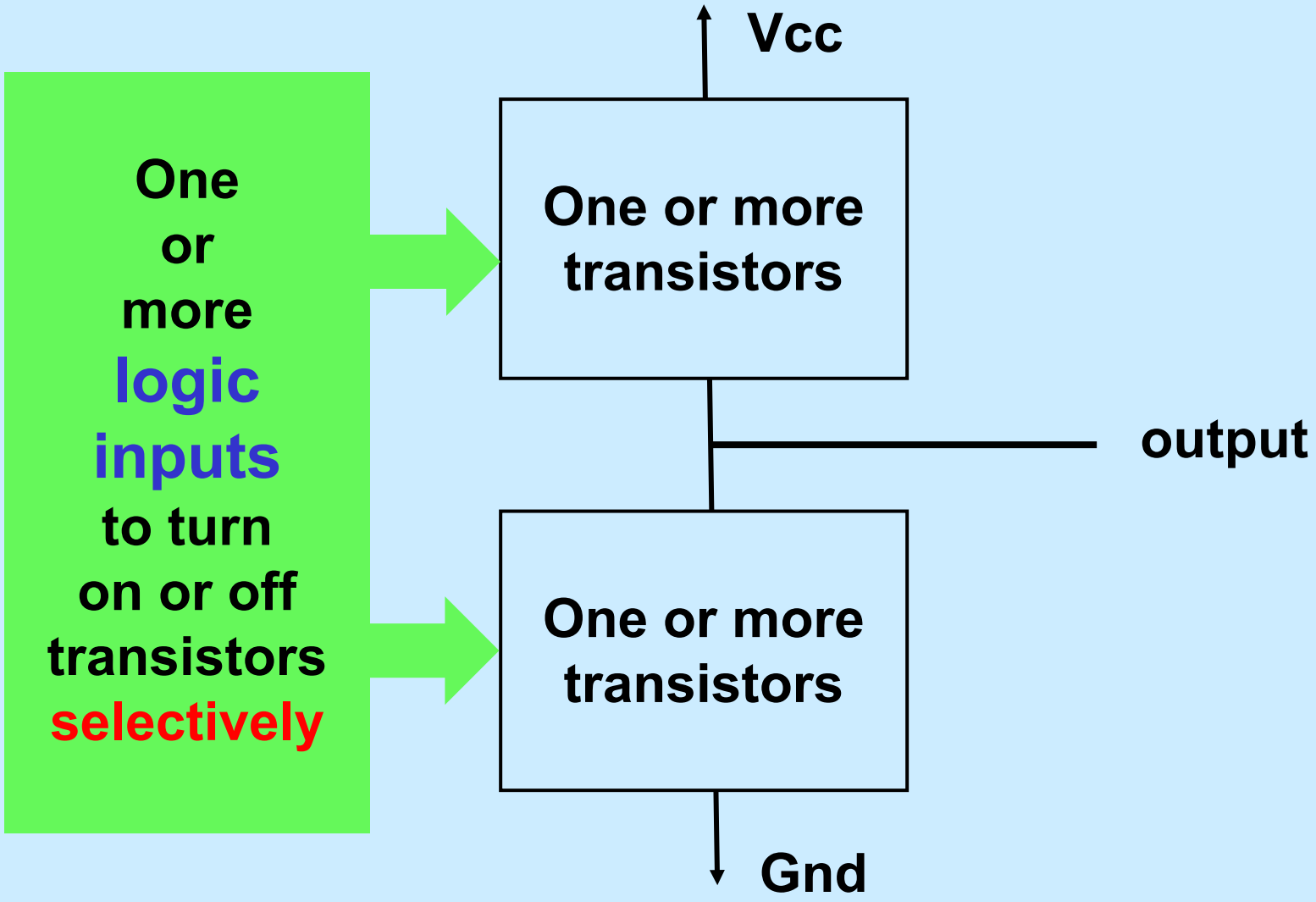


F910-21

Parallel and serial current paths



A typical logic circuit



F910-23

For a logic output to go high, current must flow from:

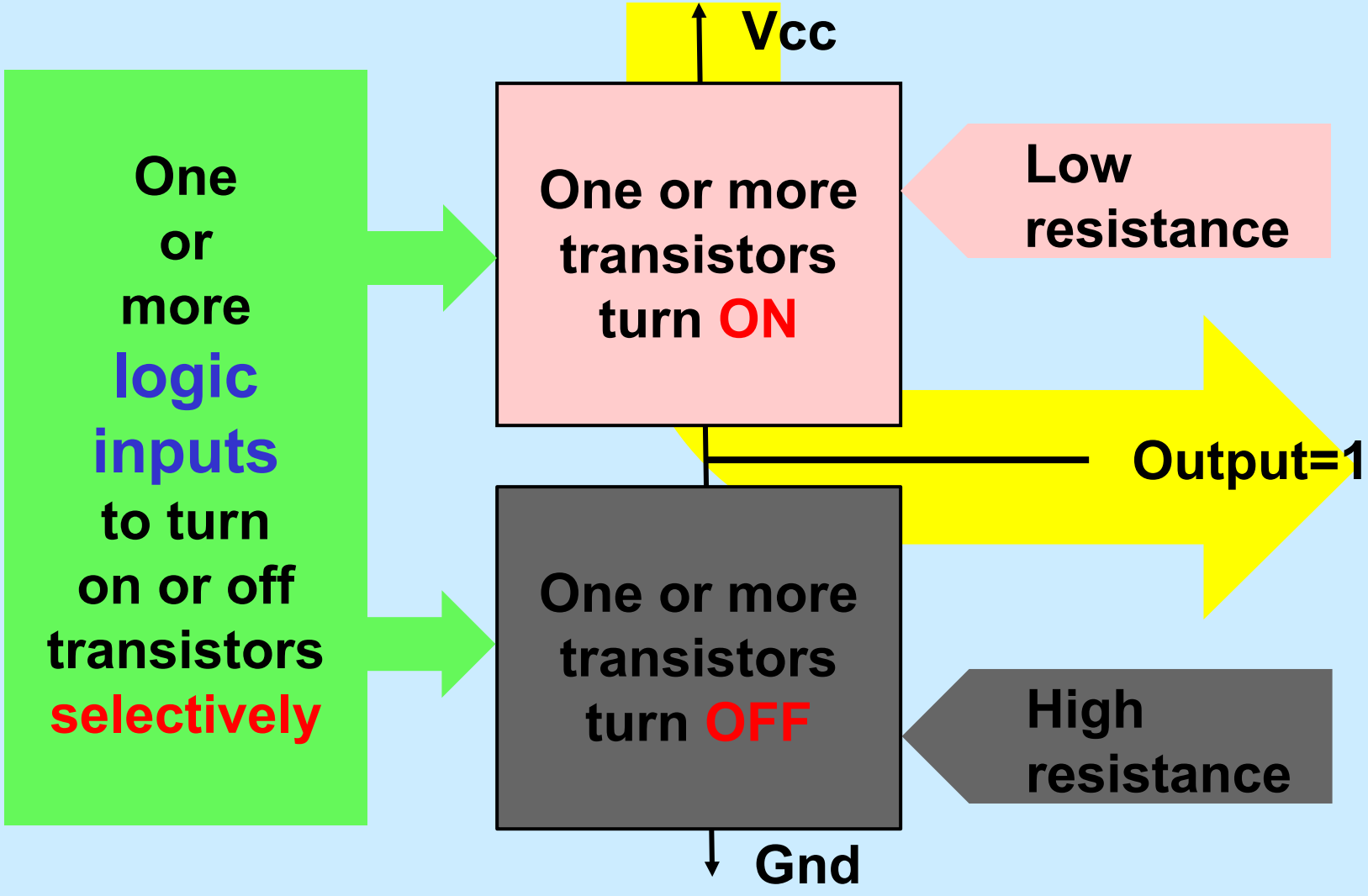
A. Vcc to Gnd

B. Vcc to output

C. Output to Gnd

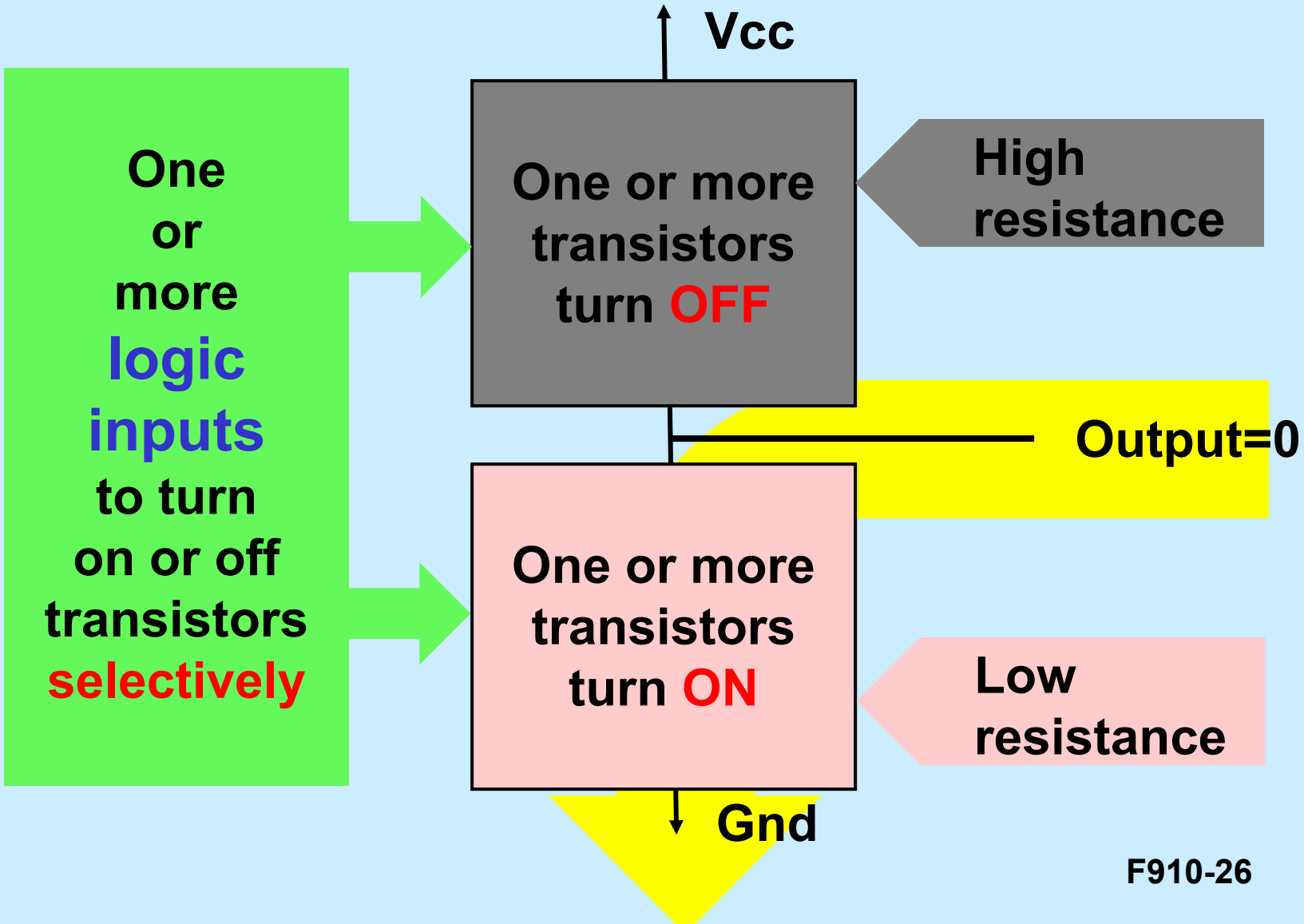
D. Output to Vcc

Making the output go High



F910-25

Making the output go Low



F910-26

Current flows from Vcc to output	Current flows from output to Gnd	Output logic level
Yes	No	1
No	Yes	0
No	No	Hi-Z
Yes	Yes	Not allowed. Excessive current may damage transistors

IMPORTANT

Only the top or the bottom current path can be turn on at any point in time, but not both. Otherwise there will be excessive current flowing through the circuit, damaging the device.

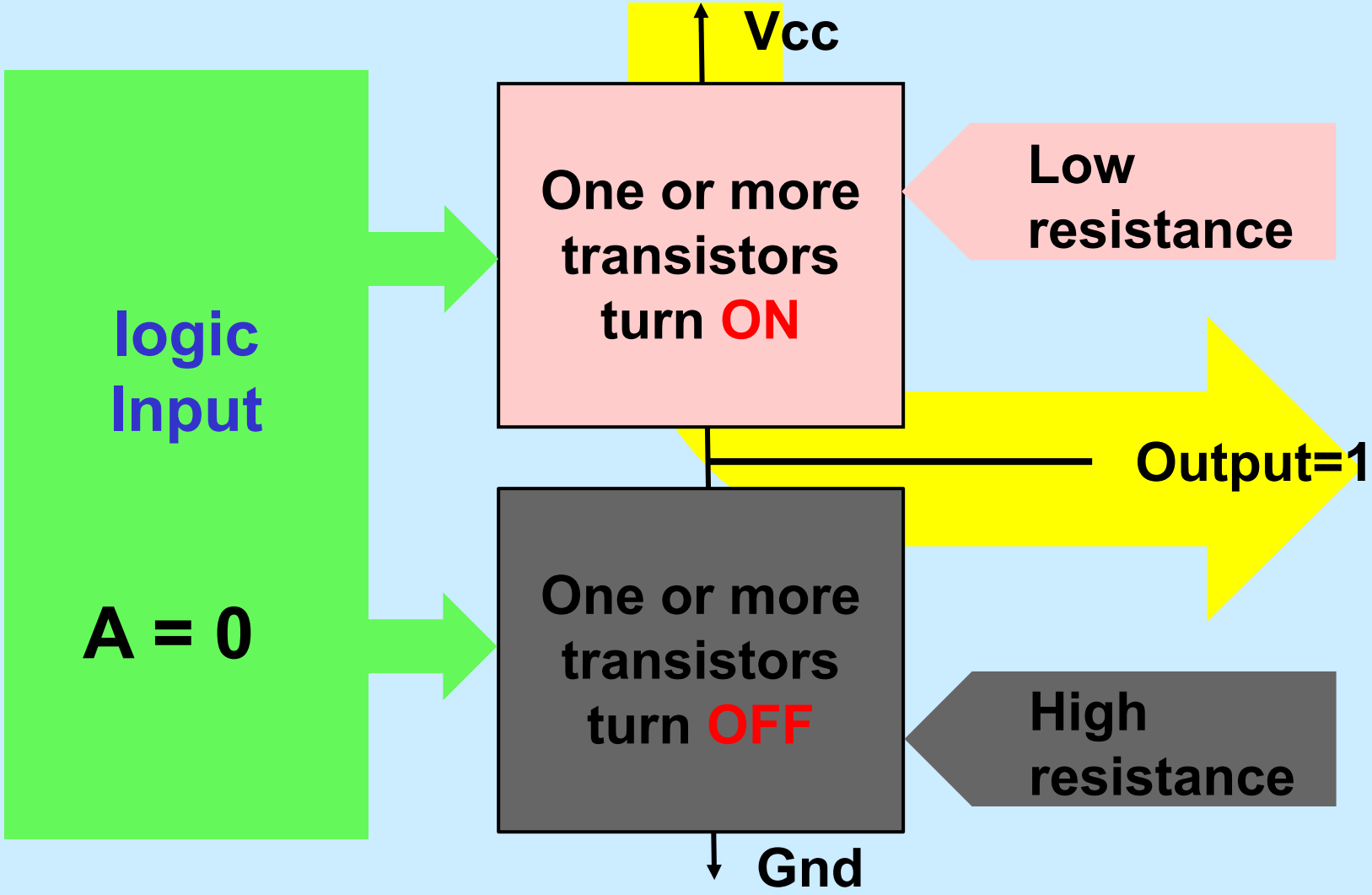
Both top and bottom off -> high-impedance (tristate output)

The logic function

How the logic inputs control when to turn on the top current path (and turn off the bottom)

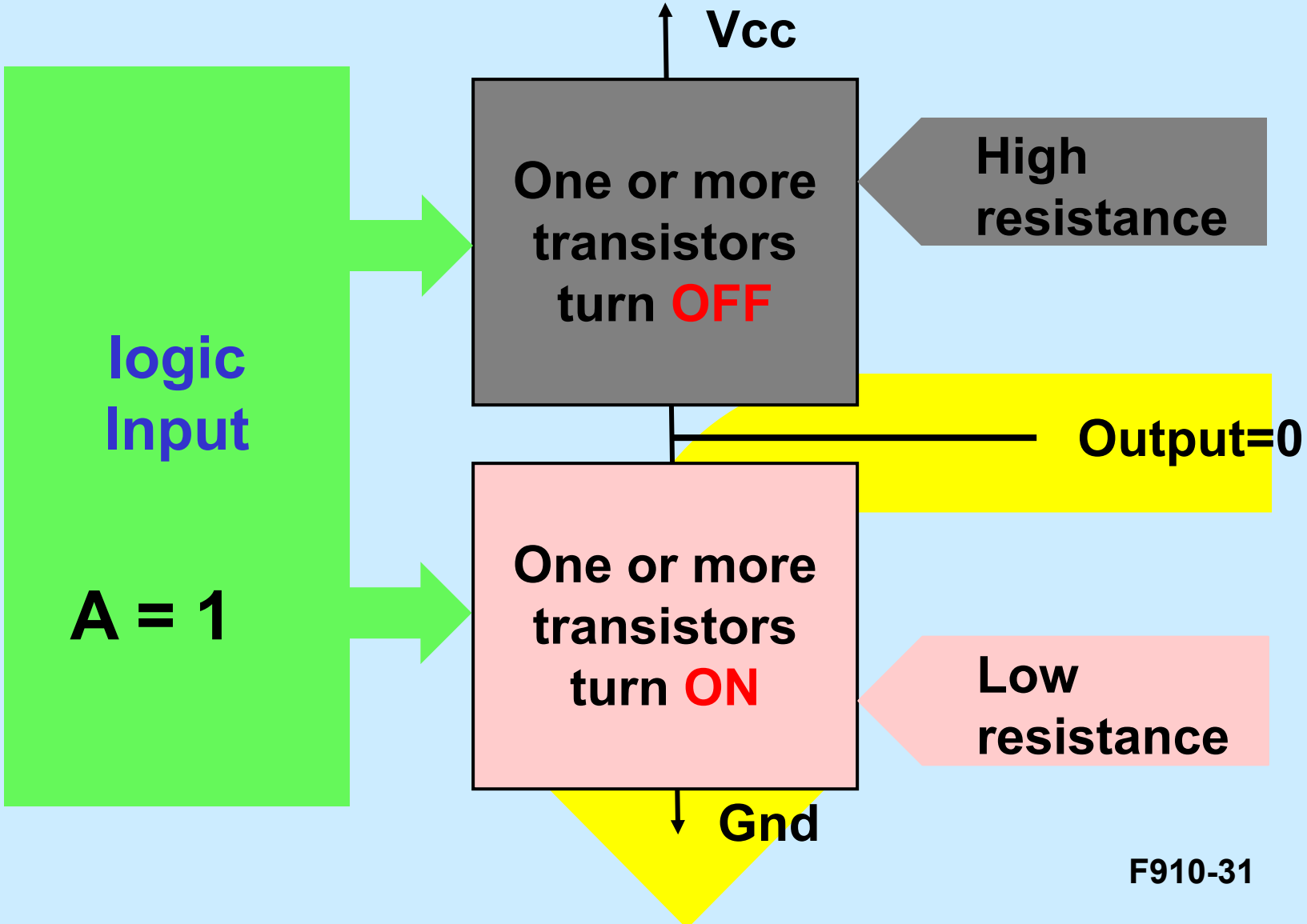
or turn on the bottom current path (and turn off the top) determines the logic function of the device.

Simplest example: NOT gate



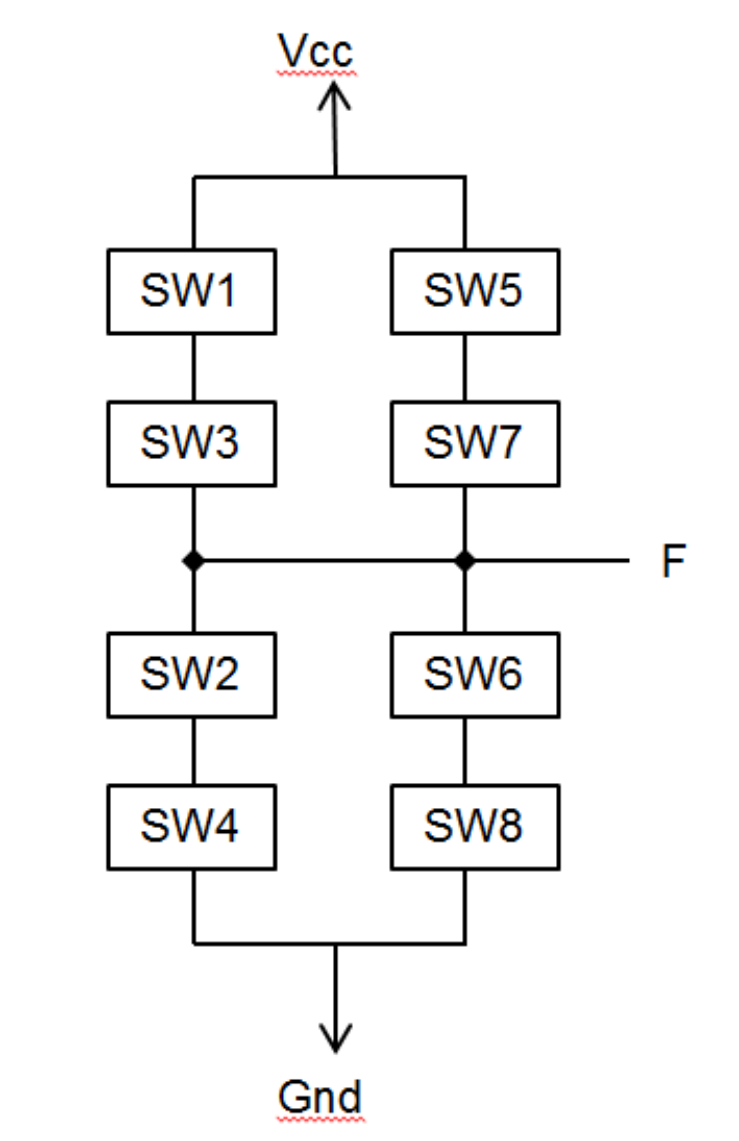
F910-30

Simplest example: NOT gate

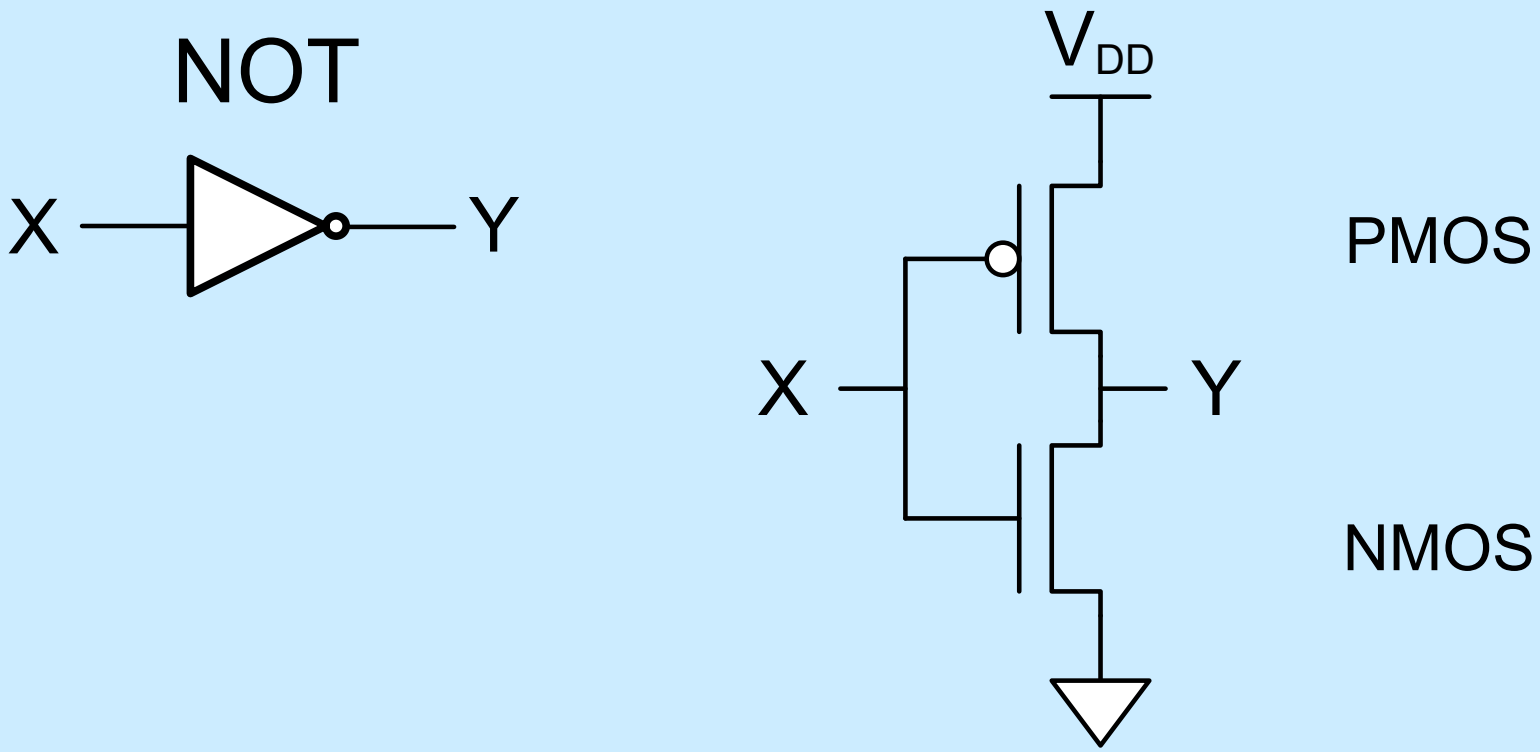


F910-31

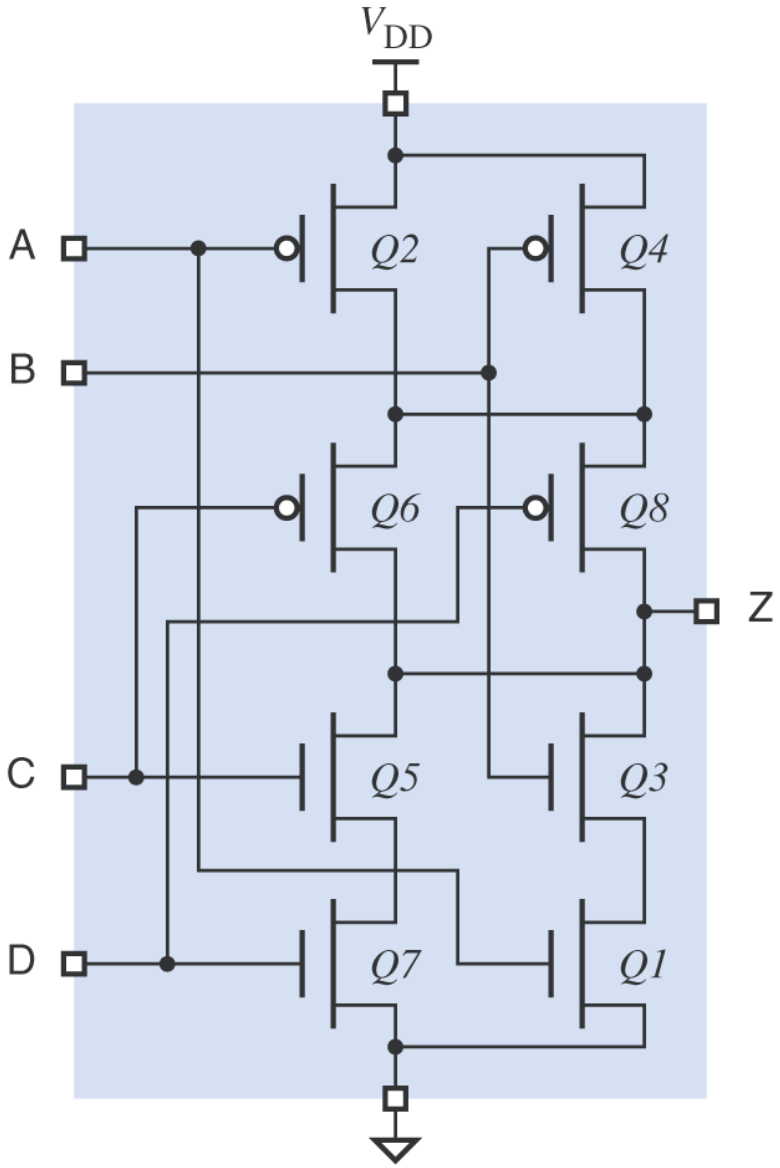
Transistors in parallel/series



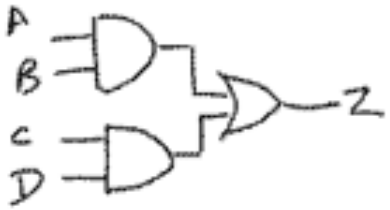
CMOS inverter



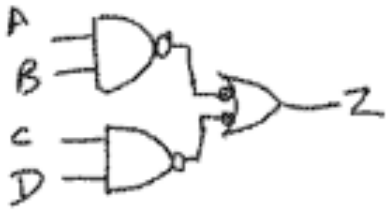
Which circuit does it implement?



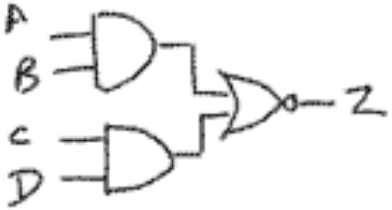
a.



b.

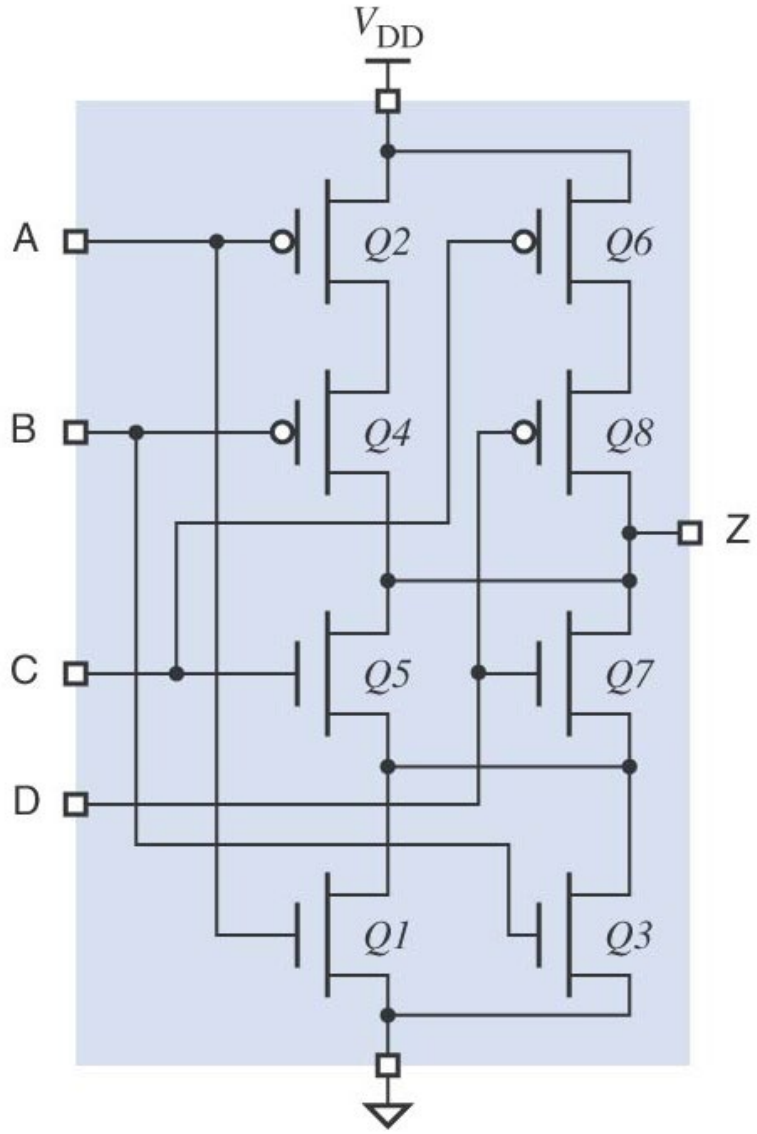


c.



d.

Which circuit does it implement?



a. Z = (A+B)' (C+D)'

b. Z = (A'+B') (C'+D')

c. Z = (AB + CD)'

d. Z = [(A+B) (C+D)]'

End of L10 summary