Course contents

**Design with Hardware Description Language:
Structural and behavioural Verilog**

Combinational logic circuits	**Sequential logic circuits**
Encoder, decoder, multiplexer	Counter, register, finite state machine

Digital circuits	**Flip-flops**

Number systems and codes	**Logic gates**	**Boolean algebra**	**Digital arithmetic**	**Boolean expression simplification**

Lecture 11 key concepts

- Digital circuits transfer characteristic
- Voltage parameters and noise margins
- Current parameters and fan-out
- Power dissipation, switching speed and propagation delay
- Rise time and fall time
- Tri-state output
- Open-drain output

Which concepts are unclear to you after viewing L11?

A. Voltage/current parameters
B. Noise margin and fan-out
C. Power dissipation
D. Timing parameters
E. Tristate output
F. Open drain output
G. none

Static characteristics

Static

- When outputs are not changing

Voltage/current parameters

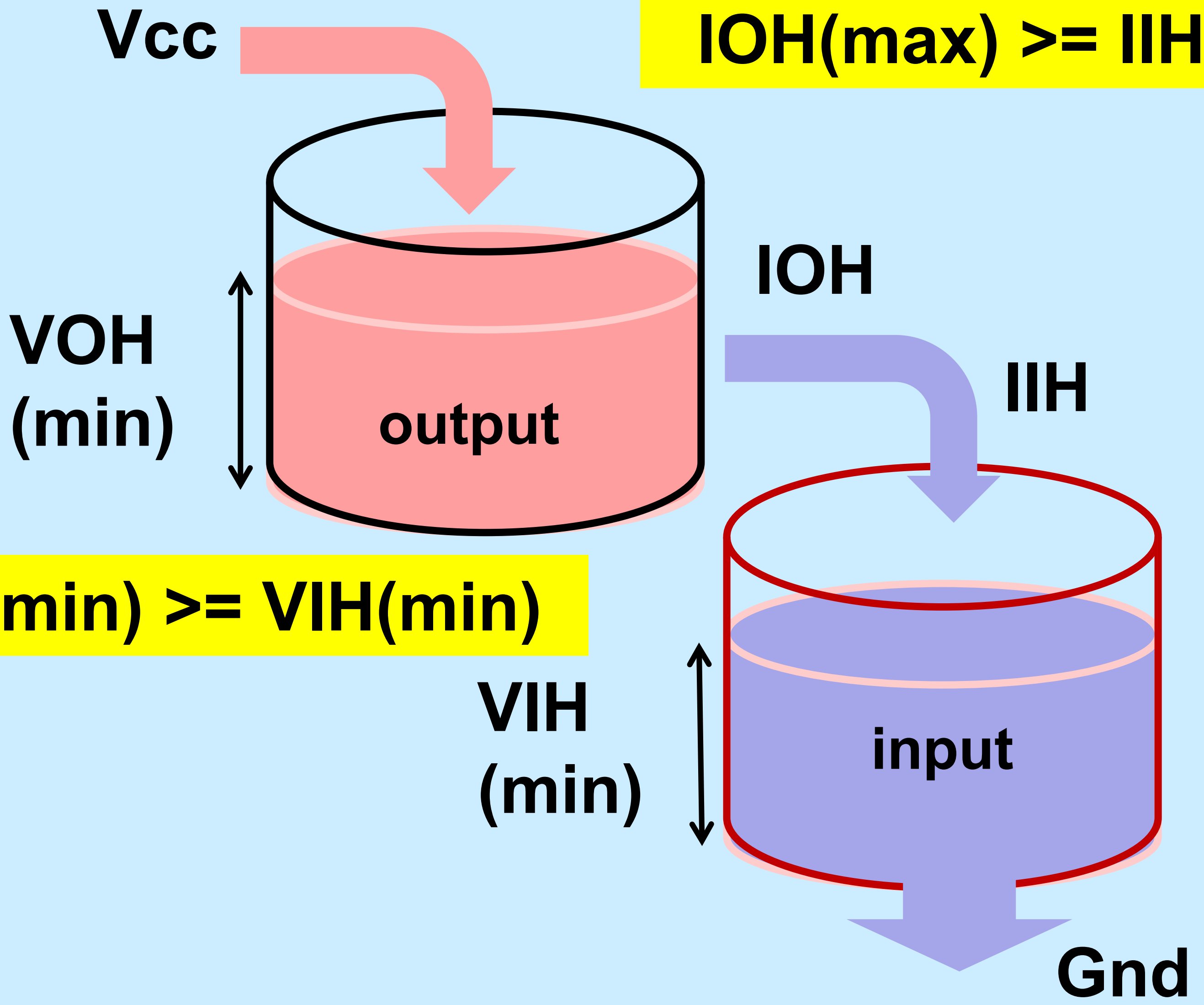
DC noise margin =

$$\min \{ V_{OH}(\min) - V_{IH}(\min),\ V_{IL}(\max) - V_{OL}(\max) \}$$

DC fan-out = $\min \{ I_{OH} / I_{IH},\ I_{OL} / I_{IL} \}$

VOH, IOH, VIH, IIH

IOH(max) >= IIH(max)



VOH(min) >= VIH(min)

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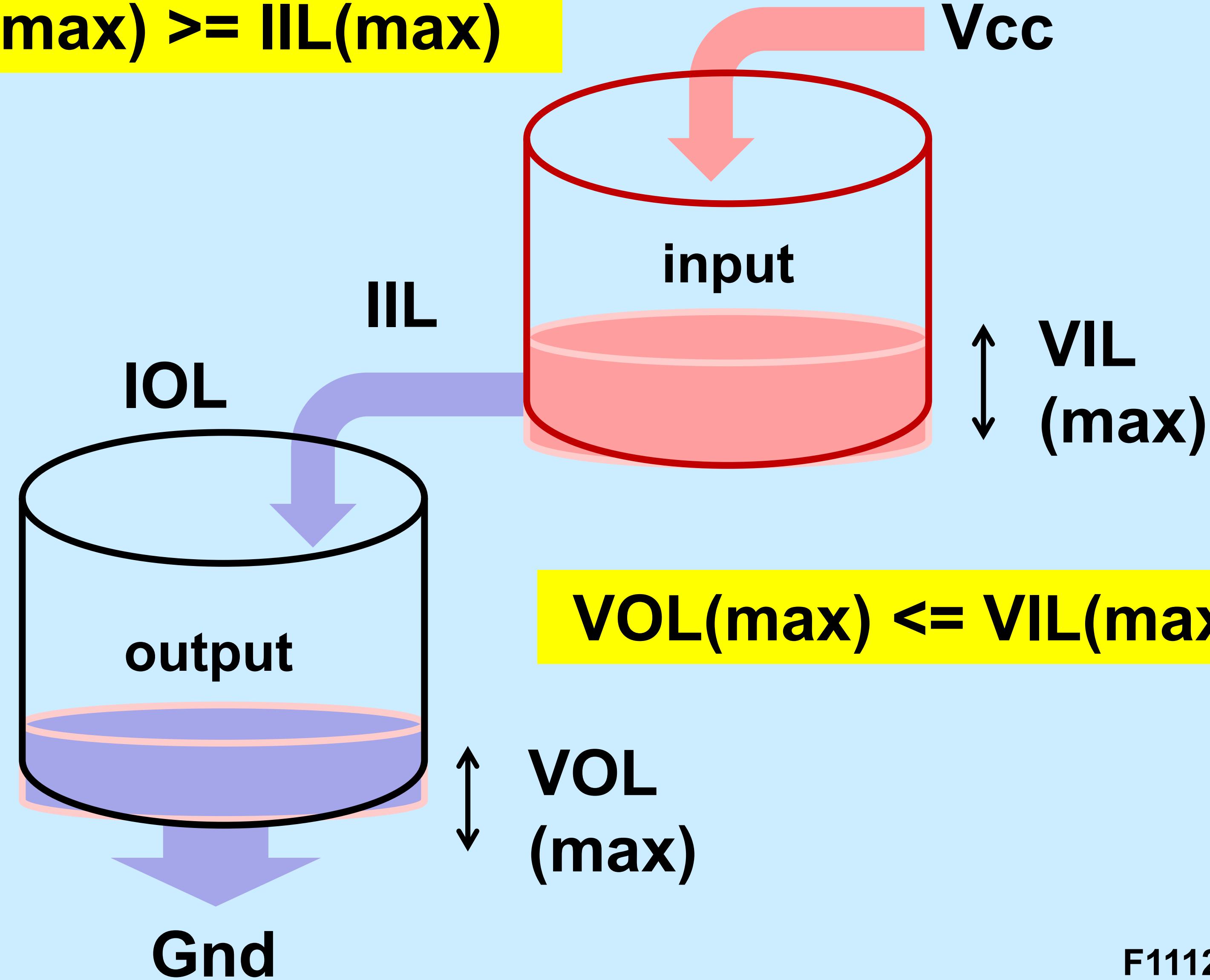
VOL, IOL, VIL, IIL

IOL(max) >= IIL(max)



VOL(max) <= VIL(max)

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Requirements for device A to drive device B:

A's output provides	**≤ / ≥ ?**	**B's input requires**
V_{OH}(min)		V_{IH}(min)
I_{OH}(max)		I_{IH}(max)
V_{OL}(max)		V_{IL}(max)
I_{OL}(max)		I_{IL}(max)

DC noise margin = min(Difference in input/output voltages)

DC fan-out = min(Ratio of output/input currents)

Dynamic characteristics

Dynamic

- When outputs are changing

Low is better:

Power dissipation, propagation delay,
rise time and fall time

High is better:

Switching speed

Tristate output

Enabled output: 0, 1

Disable output: H-Z (High-impedance)

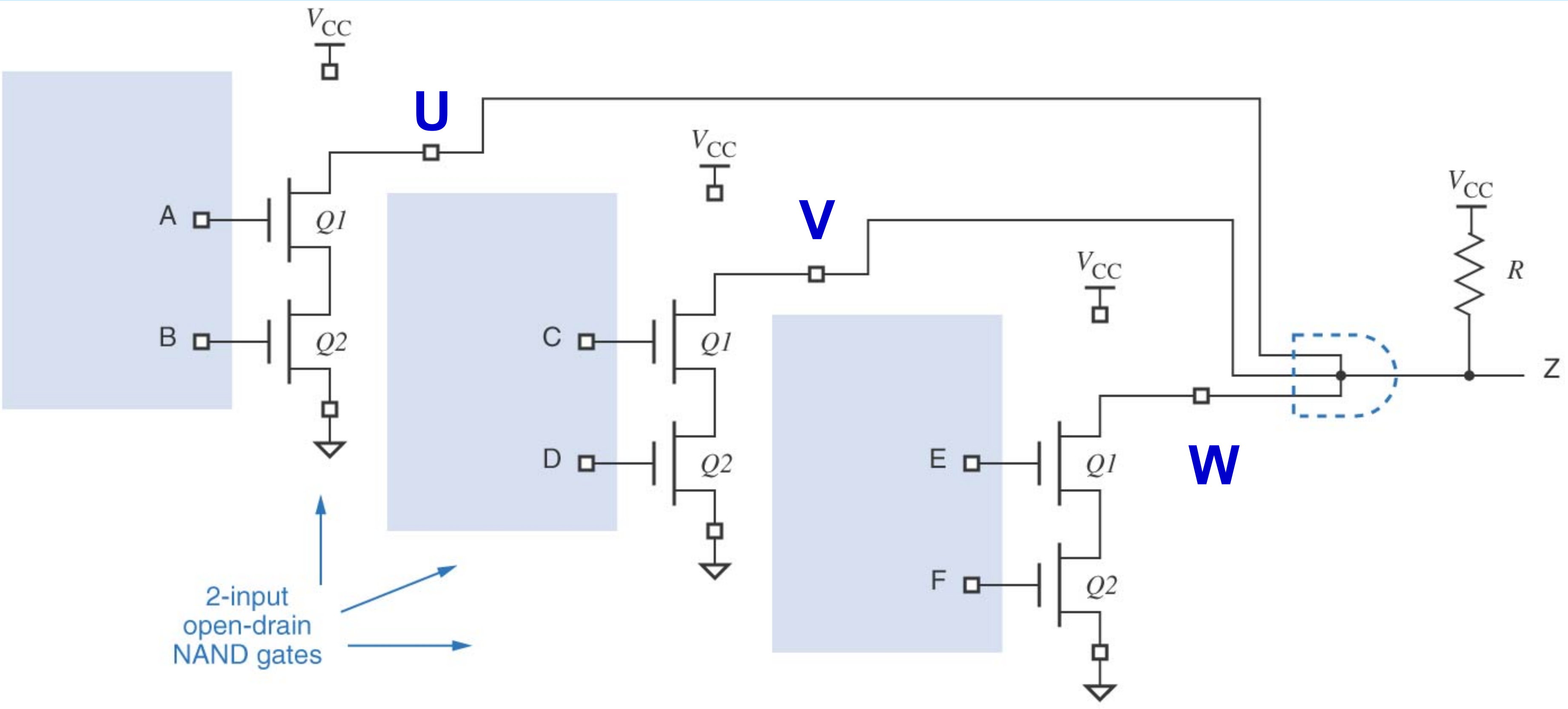
Connected tristate outputs:

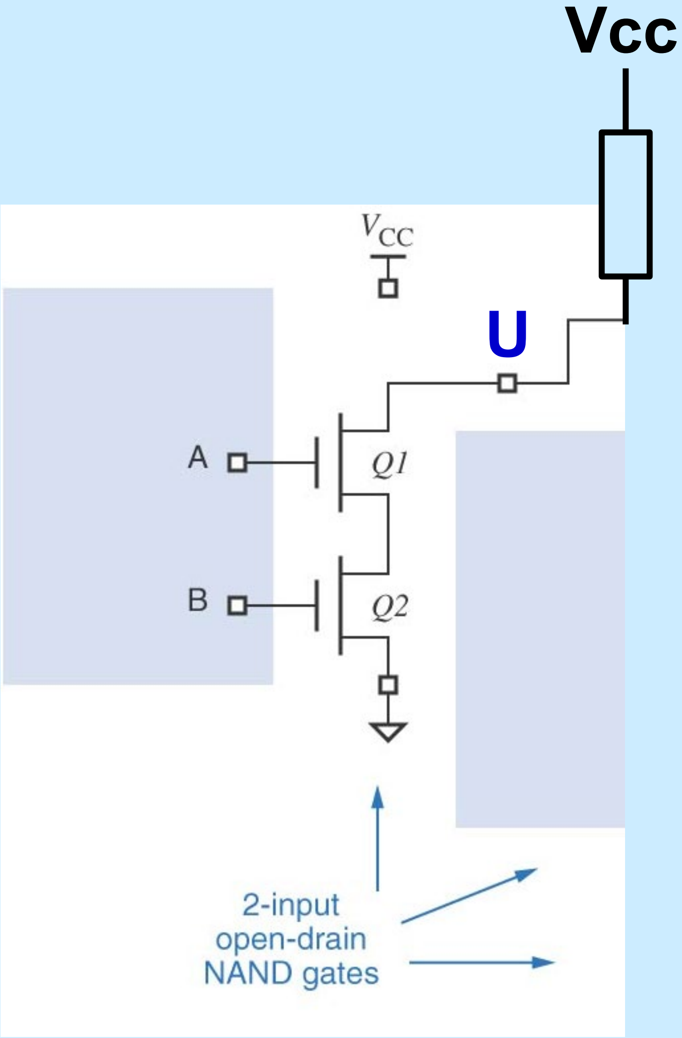
Why not more than one output can be enabled?

Question: which is which?

(a)	(b)
Outputs can be connected together	
Does not require external pull-up resistor	Requires external pull-up resistor
Has enable input	Does not have enable input
At most one individual output can produce High or Low (i.e. enabled) at any time. The rest must be Hi-Z.	Each individual output can produce High or Low at any time.
Common output follows enabled output; Hi-Z when all outputs are disabled	Common output is wire-AND of individual outputs

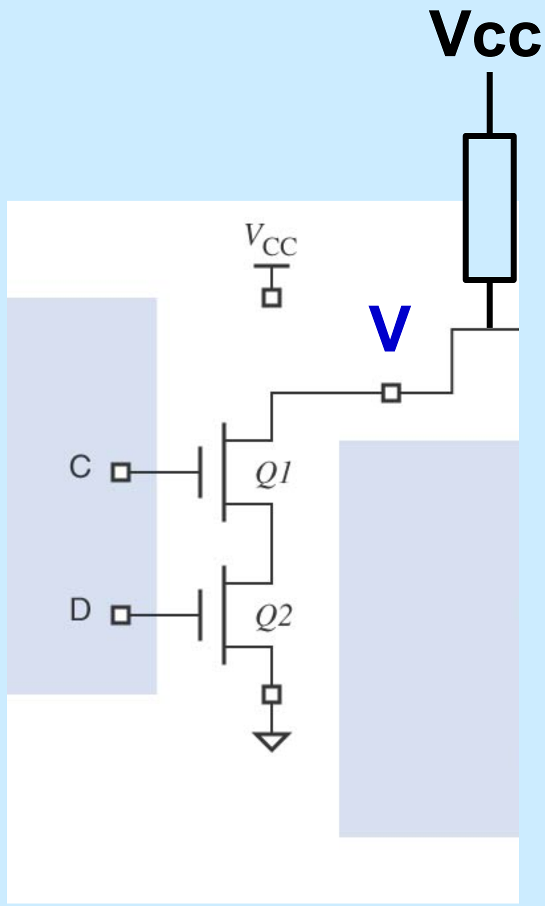
Connected open-drain outputs





U = (AB)’

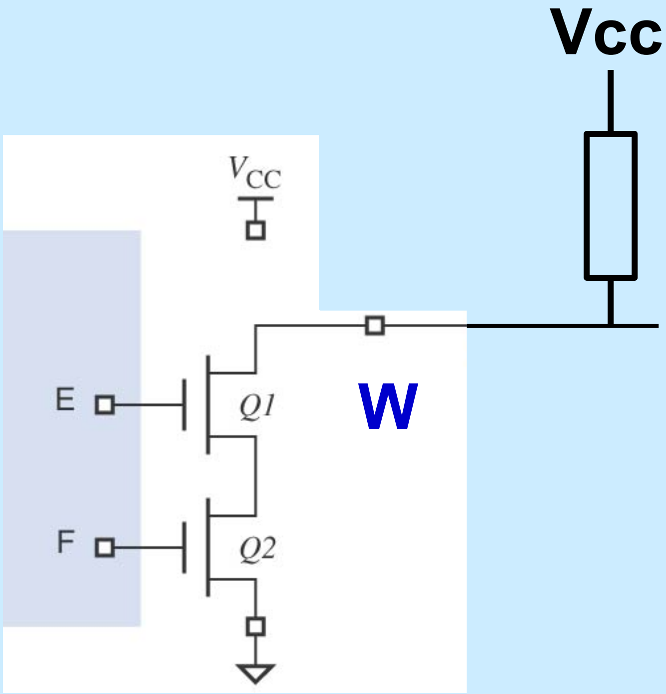
Each NAND gate can work on its own with a pull-up resistor



V = (CD)’

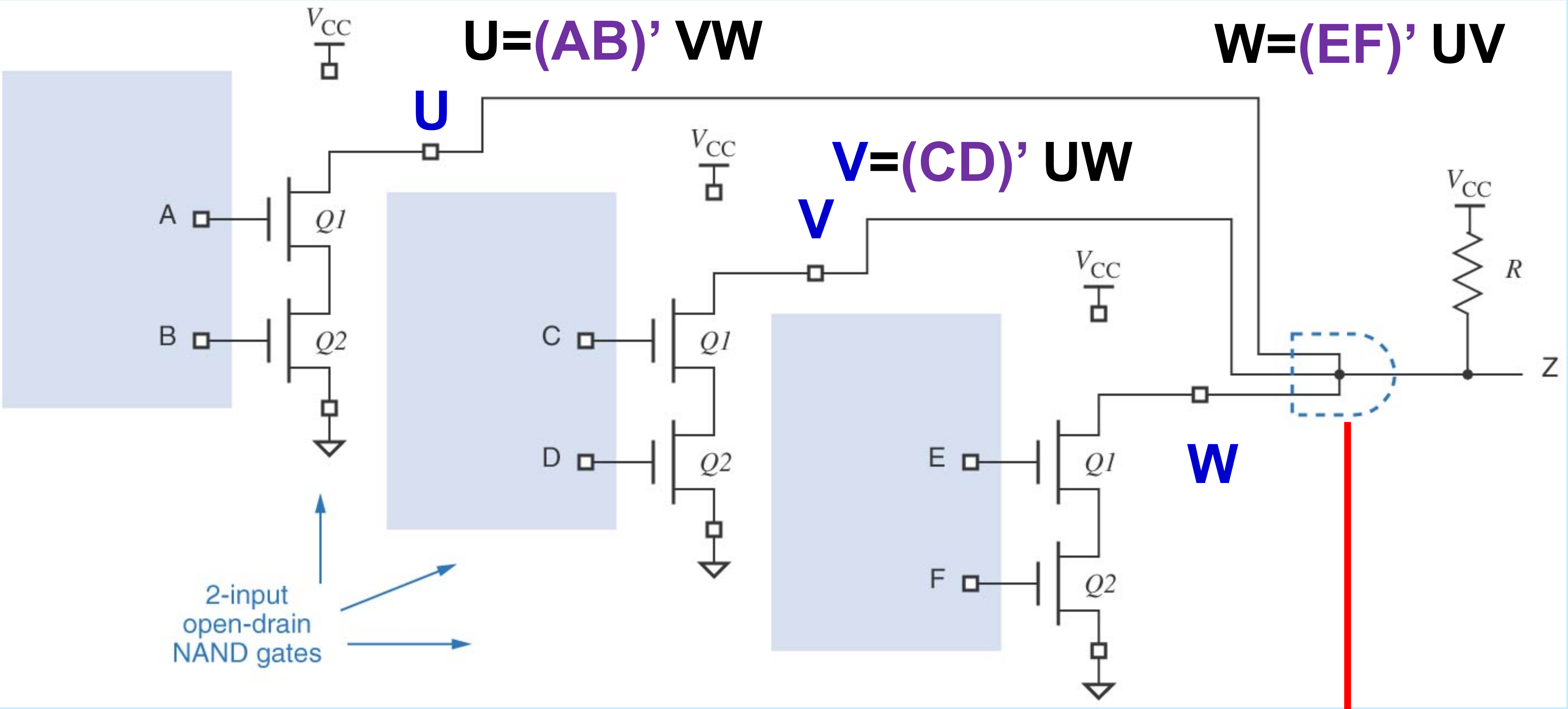
Each NAND gate can work on its own with a pull-up resistor

$W = (EF)'$



Each NAND gate can work on its own with a pull-up resistor

Wired-AND output



Wired-And: is a behavior, not an AND gate

Z = 0 if U=0, or V=0 or W=0

End of L11 summary

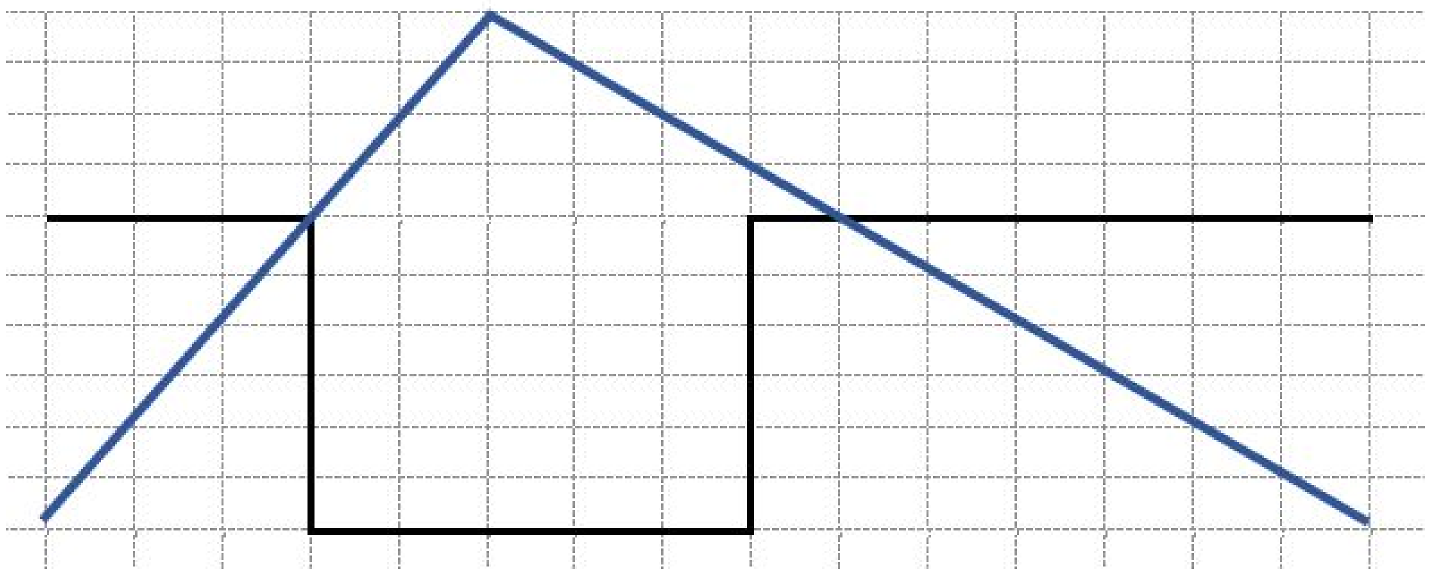
Lecture 12 key concepts

- **Schmitt-trigger inputs**
  Key parameters: VT-, VT+
- **Programmable Logic Arrays**
  Implement SOP with some flexibility
- **Fixed point and floating point numbers -**
  Pros and cons

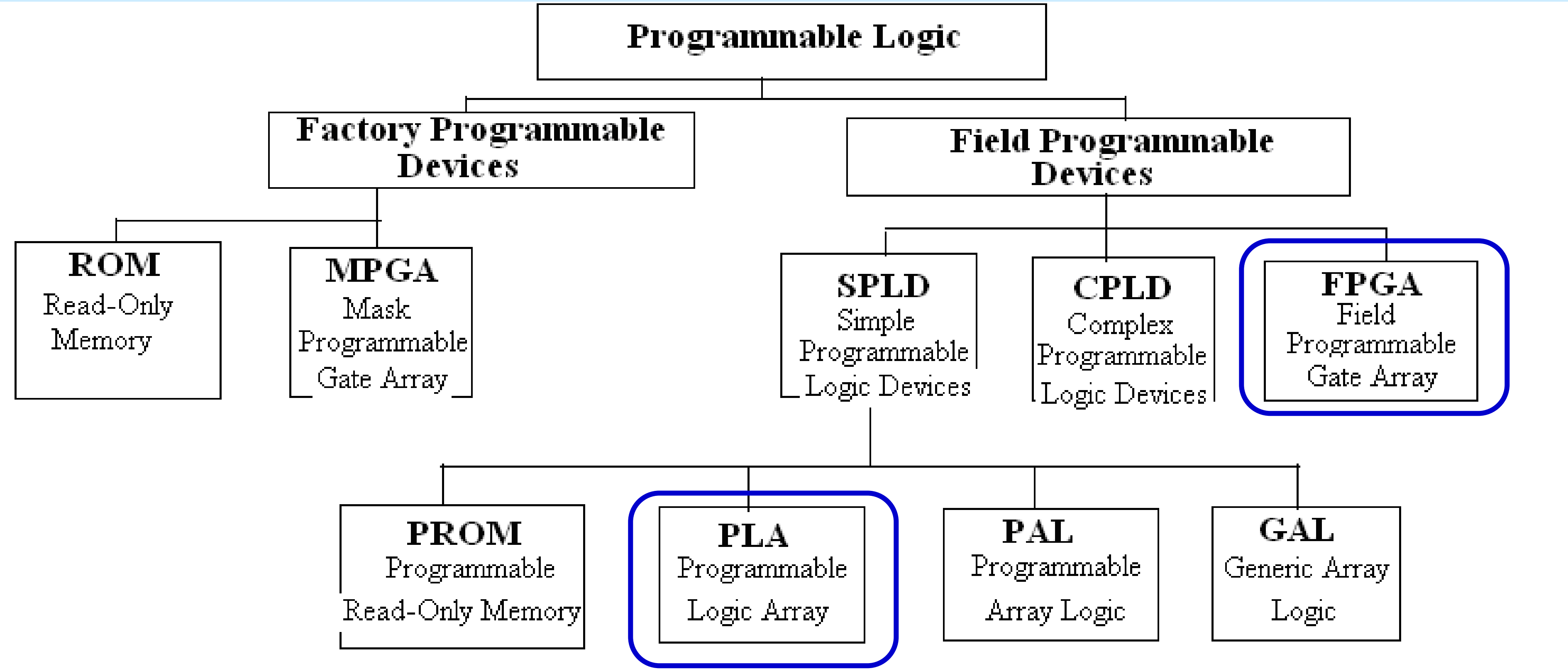
Which concepts are unclear to you after viewing L12?

A. Schmitt-trigger input
B. Programmable logic array
C. Floating point number
D. none

Are these input/output waveforms of a Schmitt-trigger buffer or inverter?

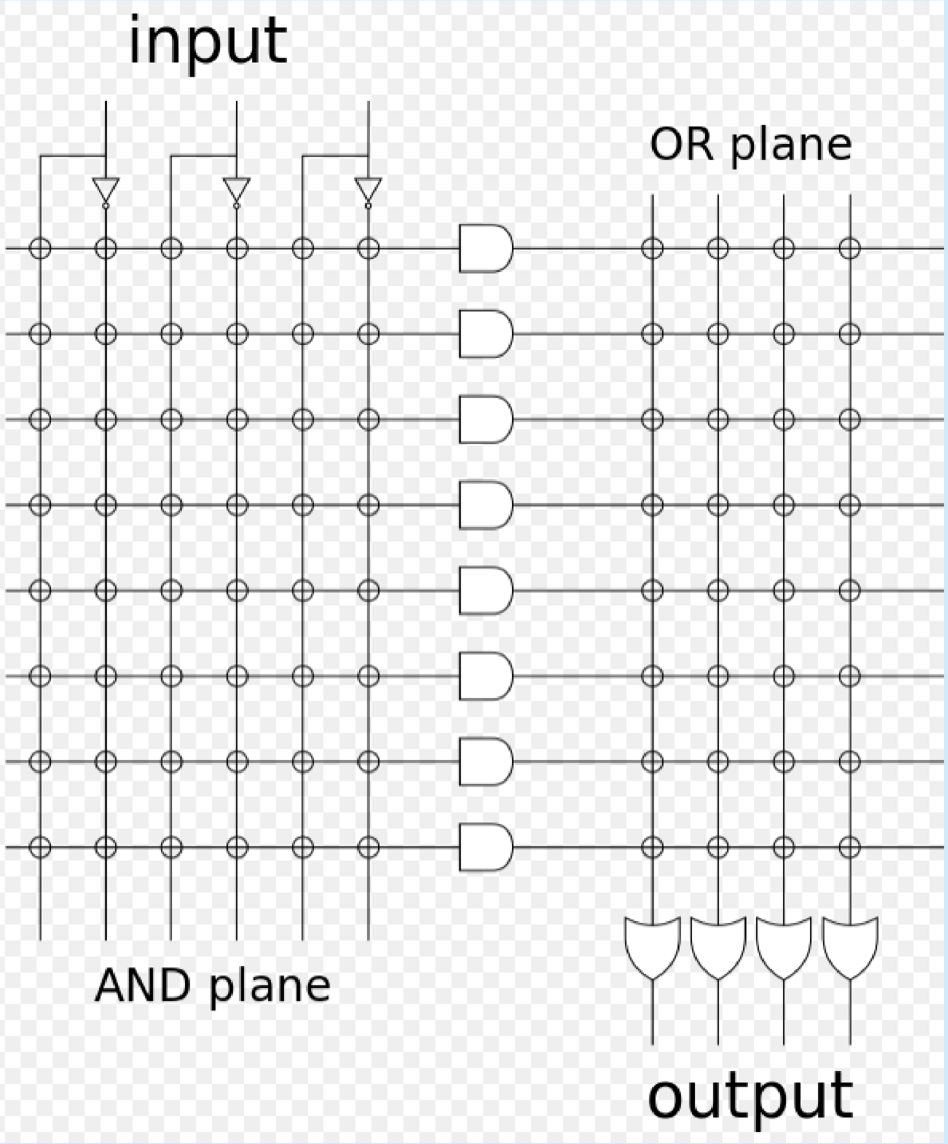


Programmable Logic Devices



Digital Systems Design Using Verilog, Roth, John, Lee. Cengage 2016.

Programmable Logic Arrays



Both AND plane and OR plane are programmable

What circuit is implemented?

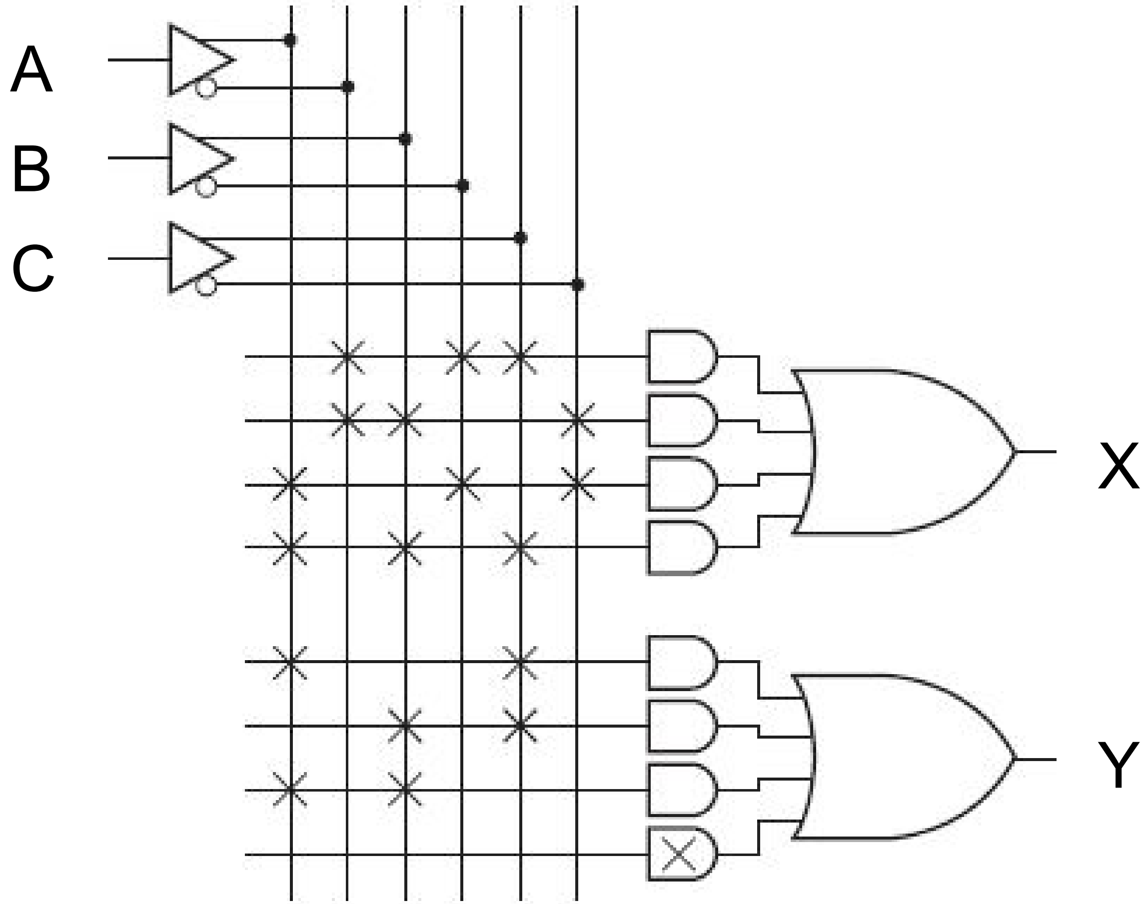


Fig. 9.33 from Fundamentals of Logic Design by Roth and Kinney

Fixed/floating point example

Store the unsigned decimal value 15.9375

15.9375(dec) = 1111.1111(bin)

Fixed point:

1111 1111

●

is not stored

Floating point:

0011 1111

1111.1111 = 1.1111111x2^3

4-bit significand=1111

4-bit exponent=0011

1. is not stored

Range of values

Compare largest value represented

Fixed point:

1111 . 1111

= 15.9375(dec)

Floating point:

0111 1111

= 1.1111 x 2^(+7)

= 1111 1000(bin)

= 248(dec)

Given the same number of bits, floating point can represent a much wider range of values than fixed point but is more complex.

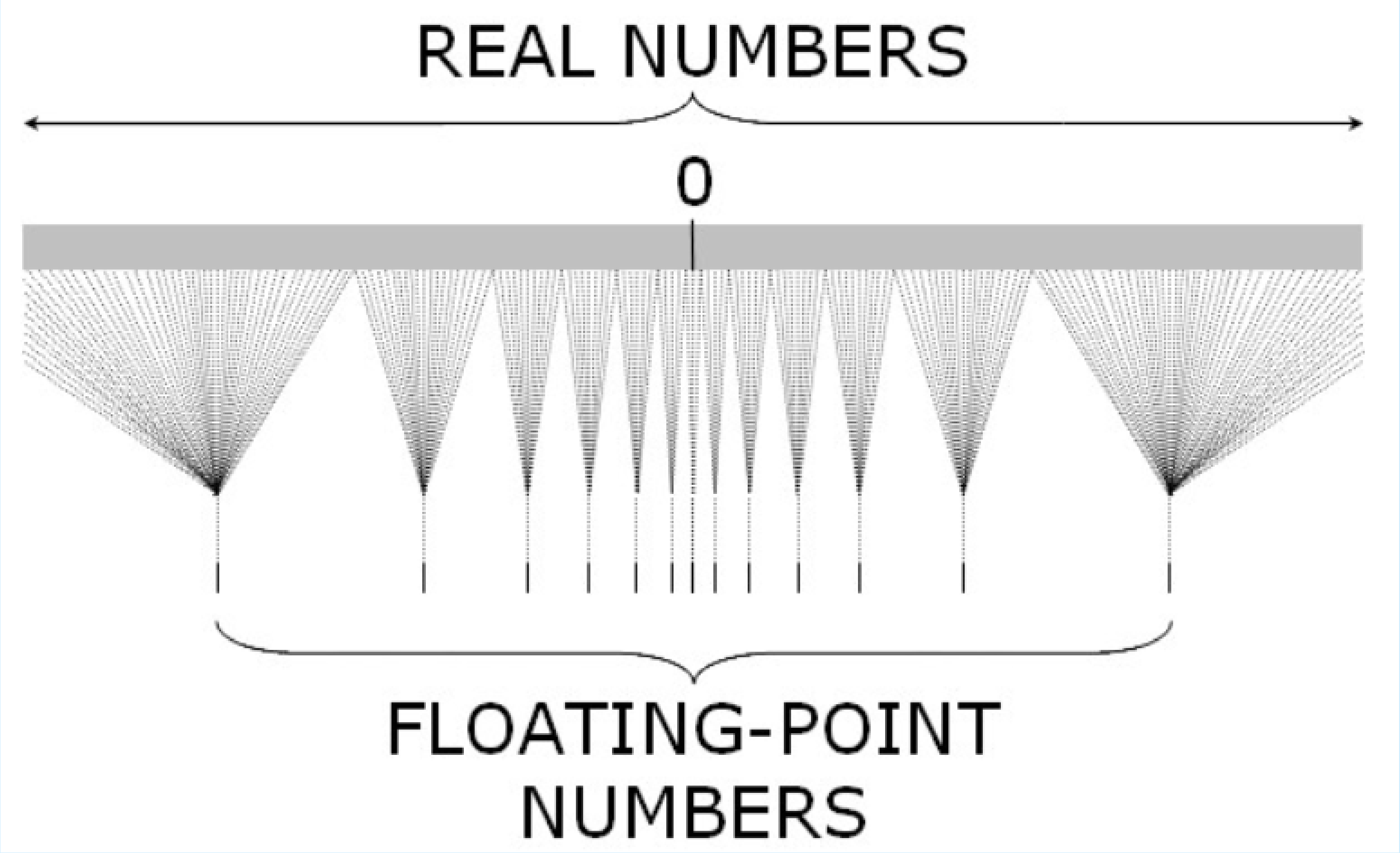
Disadvantage of fixed point

e.g. Multiply 0.0010 with 0.0011 = 0.<u>0000</u>011

Fixed point result:	Floating point result:
0000 . <u>0000</u>	1010 1000
	= 1.1000 x 2^(-6)

Fixed-point arithmetic such as multiplication may result in a loss of significant bits.

Disadvantage of floating point



http://jasss.soc.surrey.ac.uk/9/4/4.html

End of L12 summary