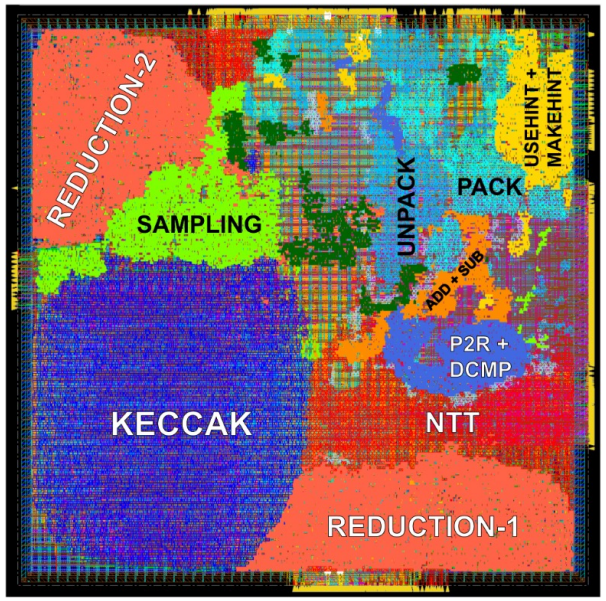

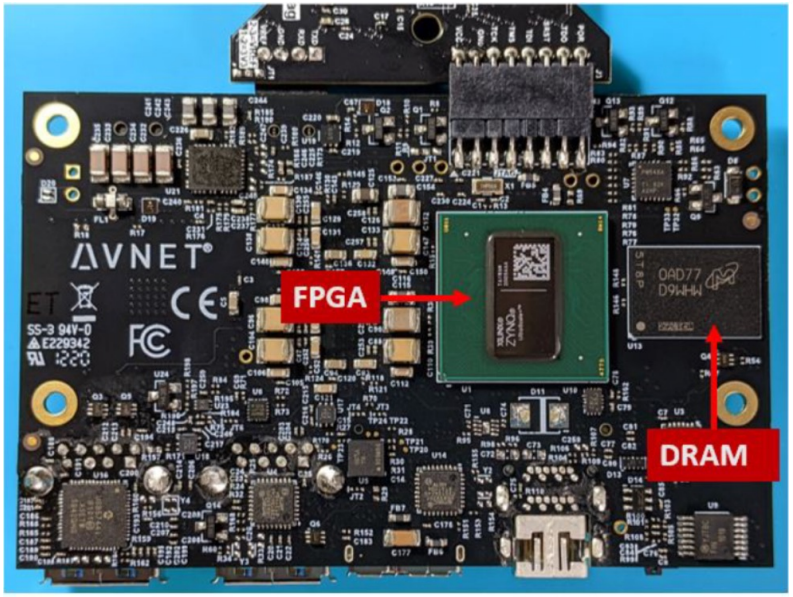

15-250X Faster than Software Implementation

Contact Information

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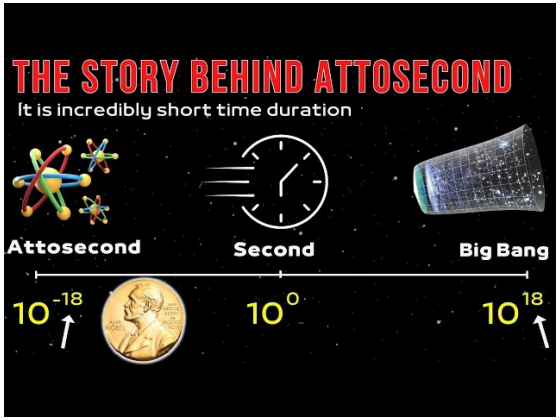


Attoseconds

Plan for the 2nd half of the semester

NANYANG TECHNOLOGICAL UNIVERSITY

- Full-Time Course

Week	Pre-Recorded Lectures	Monday (LT19A) 830-920	Thursday (Zoom) 1630-1720	Tutorial	Lab
7	L13-L14				
Recess Week					
8	L15-L16	L13-L14 Summary	Online Consultation (Zoom)	Tutorial 6	+ quiz 3
9	L17-L18	L15-L16 Summary		Tutorial 7	Experiment 4 + quiz 4
10	L19-L20	L17-L18 Summary		Tutorial 8	
11	L21-L22	L19-L20 Summary (**Zoom**)		Tutorial 9	Experiment 5 + quiz 5
12	L23	L21-L22 Summary		Tutorial 10	
13		*Public holiday*			

Plan for the 2nd half of the semester *(contd.)*

NANYANG TECHNOLOGICAL UNIVERSITY

- Part-Time Course

Week	Pre-Recorded Lectures	Tuesday (LT11) 1830-2130		Lab
7	L13-L14			
Recess Week				
8	L15-L16	L13-L14 Summary	Tutorial 6	
9	L17-L18	L15-L16 Summary	Tutorial 7, 8	
10	L19-L20	L17-L19 Summary	Tutorial 9	
11	L21-L22			Experiment 4 + quiz 4
12	L23	L20-L22 Summary	Tutorial 10	
13				Experiment 5 + quiz 5

Plan for the 2nd half of the semester *(contd.)*

NANYANG TECHNOLOGICAL UNIVERSITY

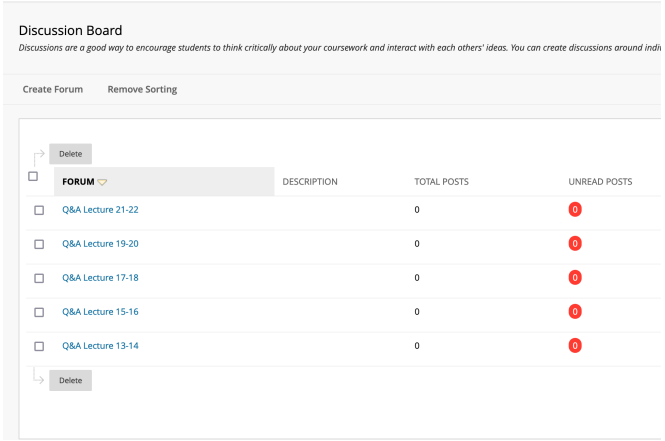
- Online Tasks for L13 to L22
  - Will not be graded

- Discussion lectures (Monday, 8:30-9:20 AM, LT19A)
  - You are required to view the pre-recorded lectures
  - Recap and discussion (slides to be uploaded afterwards)
  - Additional examples and exercises
  - Polls through Wooclap (QR code in respective slides)

Plan for the 2nd half of the semester *(contd.)*

NANYANG TECHNOLOGICAL UNIVERSITY

- Participation in Course
  - Use NTULearn Discussion Forum to ask follow-up questions



- Consultation Slots on (Thursday, 4:30-5:20 PM, Zoom)
  - Limit yourself to 3 questions
  - Avoid the clarification on tutorial
  - https://ntu-sg.zoom.us/j/81954891824
    Meeting ID: 819 5489 1824
    Passcode: 364003

SC1005
Digital Logic

Recap and Discussion

Lecture 17

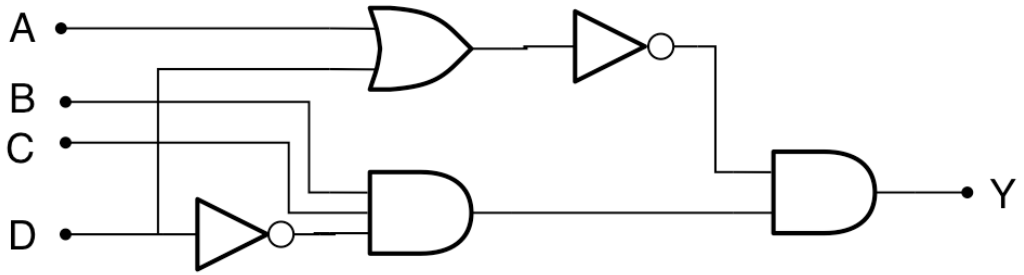
Sequential Circuits

Summary of Lecture 17

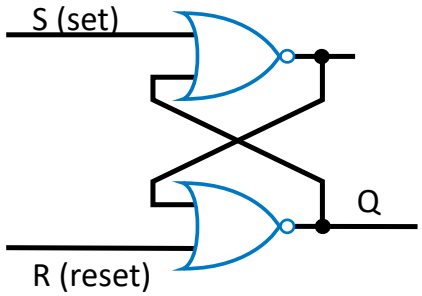
- Sequential Circuits
  - Set-Reset (SR) Latch
  - Transparent D-Latch
  - Clock and Timing

Recap: Combinational vs. Sequential Circuits

- The output of a combinational circuit is purely a function of the present inputs to it
  - *output = f(input)*



- The output of a sequential circuit depends on both the *current* and *previous* inputs.



Exercise 1

- Consider two styles of fan speed control:
  - Dial-based (0,1,2,3,4,5)
  - Button-based (+,–)
- Which of the following correctly define the type of circuit used for implementing the fan control for L and R?

L

R

L – Combinational
R – Combinational

L – Sequential
R – Combinational

L – Combinational
R – Sequential

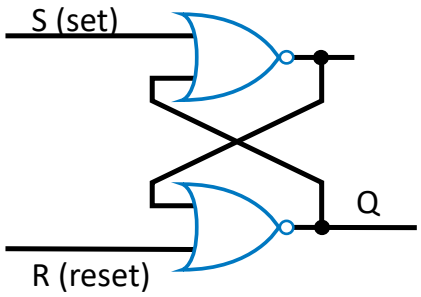
L – Sequential
R – Sequential

1 Go to wooclap.com
2 Enter the event code in the top banner

Event code
CAOAZX

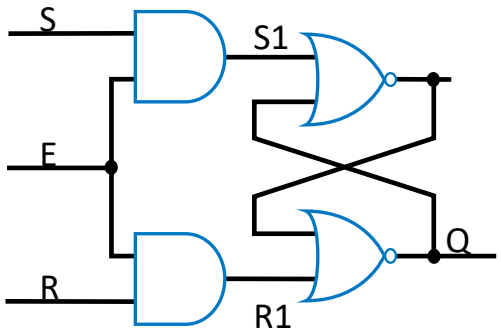
Recap: Latches

Set-Reset (SR) Latch



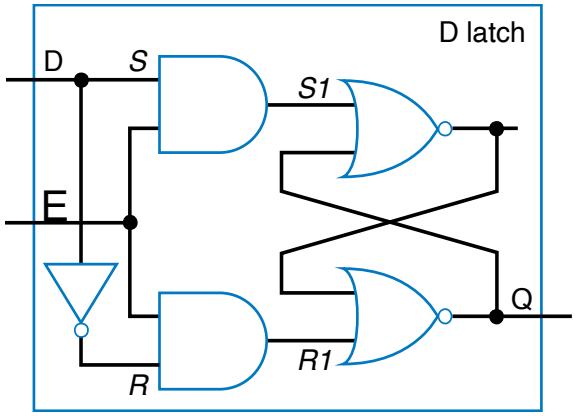
S	R	Q+	Function
0	0	Q	Store
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

Enabled SR Latch



E	S	R	Q+	Function
0	X	X	Q	Store
1	0	0	Q	Store
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	?	Undefined

D Latch

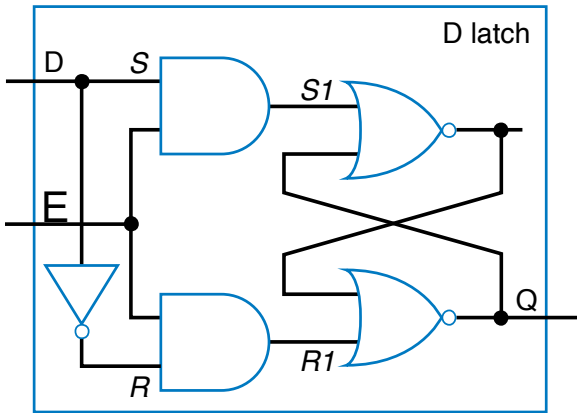


E	D	Q+
0	X	Q
1	0	0
1	1	1

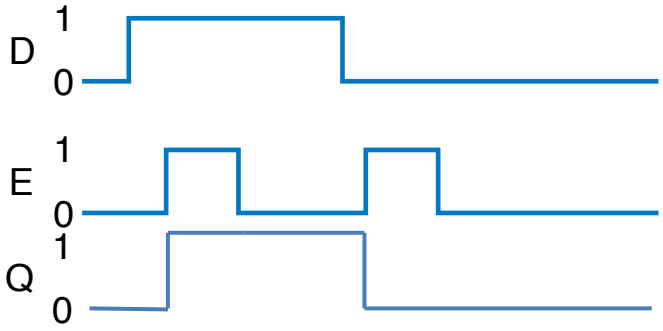
Problem: When both S and R are asserted and then de-asserted at the same time, we may get output oscillation.

Recap: Transparent D Latch

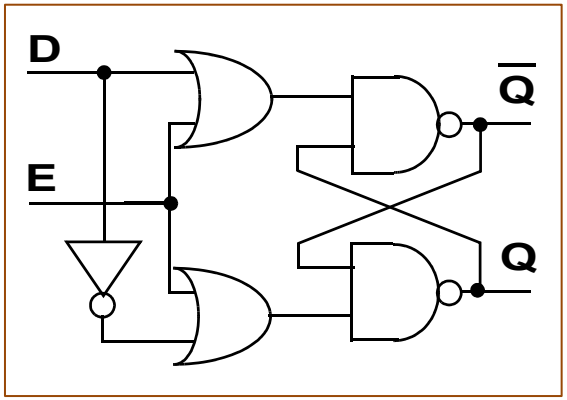
Active-High D Latch



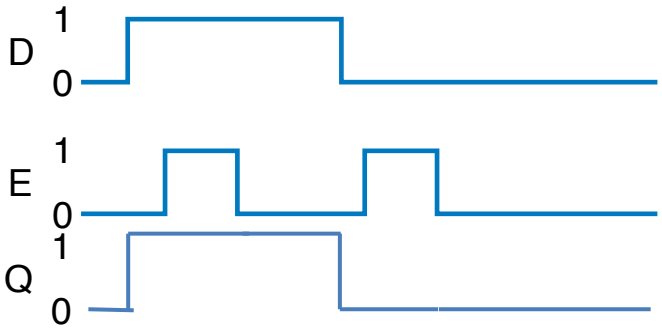
E	D	Q+	Function
0	X	Q	Store
1	0	0	Transparent
1	1	1	Transparent



Active-Low D Latch

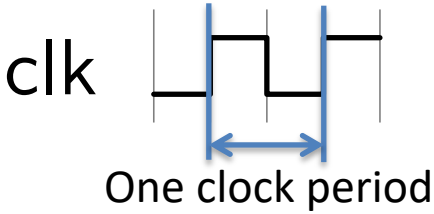


E	D	Q+	Function
1	X	Q	Store
0	0	0	Transparent
0	1	1	Transparent



The Clock

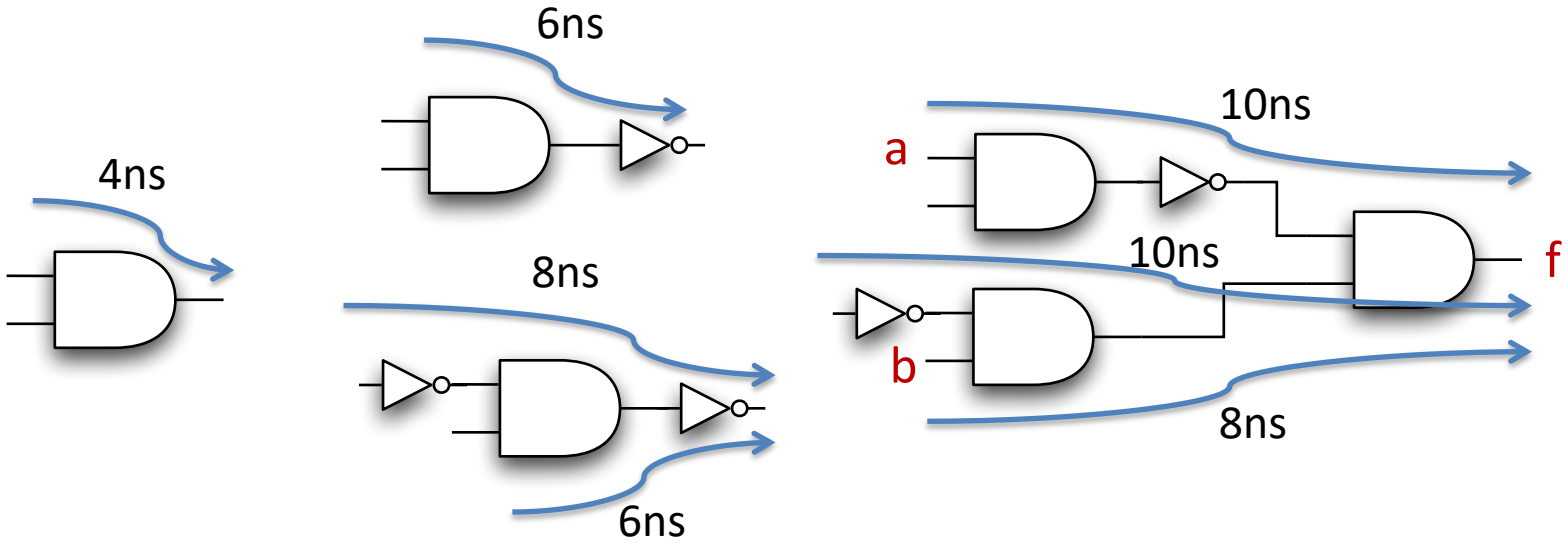
- In digital systems, sequential components are connected to what we call a "clock"
- The clock is a signal that continuously toggles between 0 and 1 at a fixed rate:



- The period of the clock is the time it takes to complete one complete cycle – we call this a cycle
- The frequency is the inverse of the period:
  - 10ns period = 10×10^{-9}s, $1/10 \times 10^{-9} = 10^{8}$Hz = 100MHz
  - 1ns period = 1×10^{-9}s, $1/1 \times 10^{-9} = 10^{9}$Hz = 1GHz

Timing in Circuits

- Assume an **and** gate has a delay of 4ns and an **inverter** has a delay of 2ns:



- The propagation delay, t_p, may differ between different inputs and outputs in the same circuit
- If we report a single number, we always use the worst (i.e. longest path)

SC1005
Digital Logic

Recap and Discussion

Lecture 18

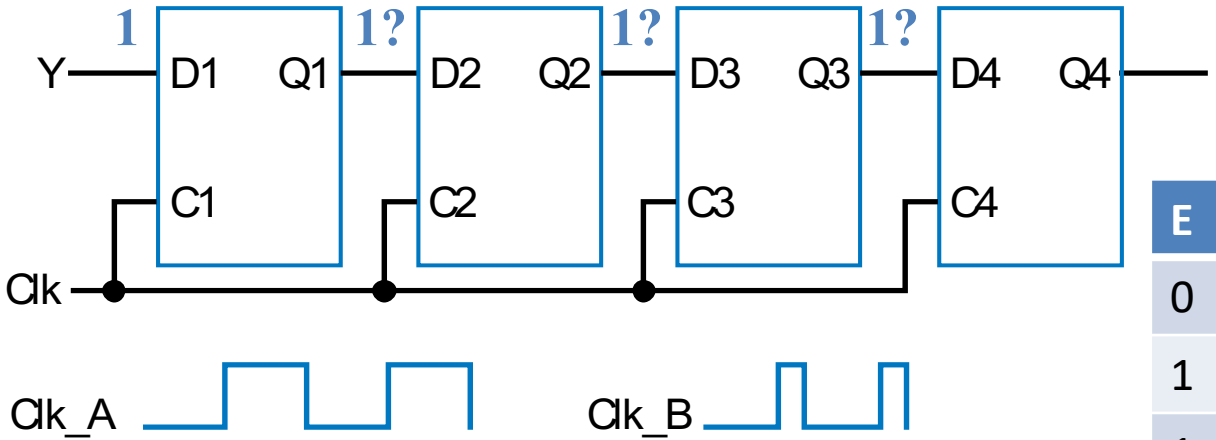
Sequential Circuits

Summary of Lecture 18

- Introduction to Verilog HDL
  - Gated/Enabled S-R Latch
  - Transparent D-Latch
  - Edge-Triggered Flip-Flop

Timing of Latches

- Consider a chain of latches:

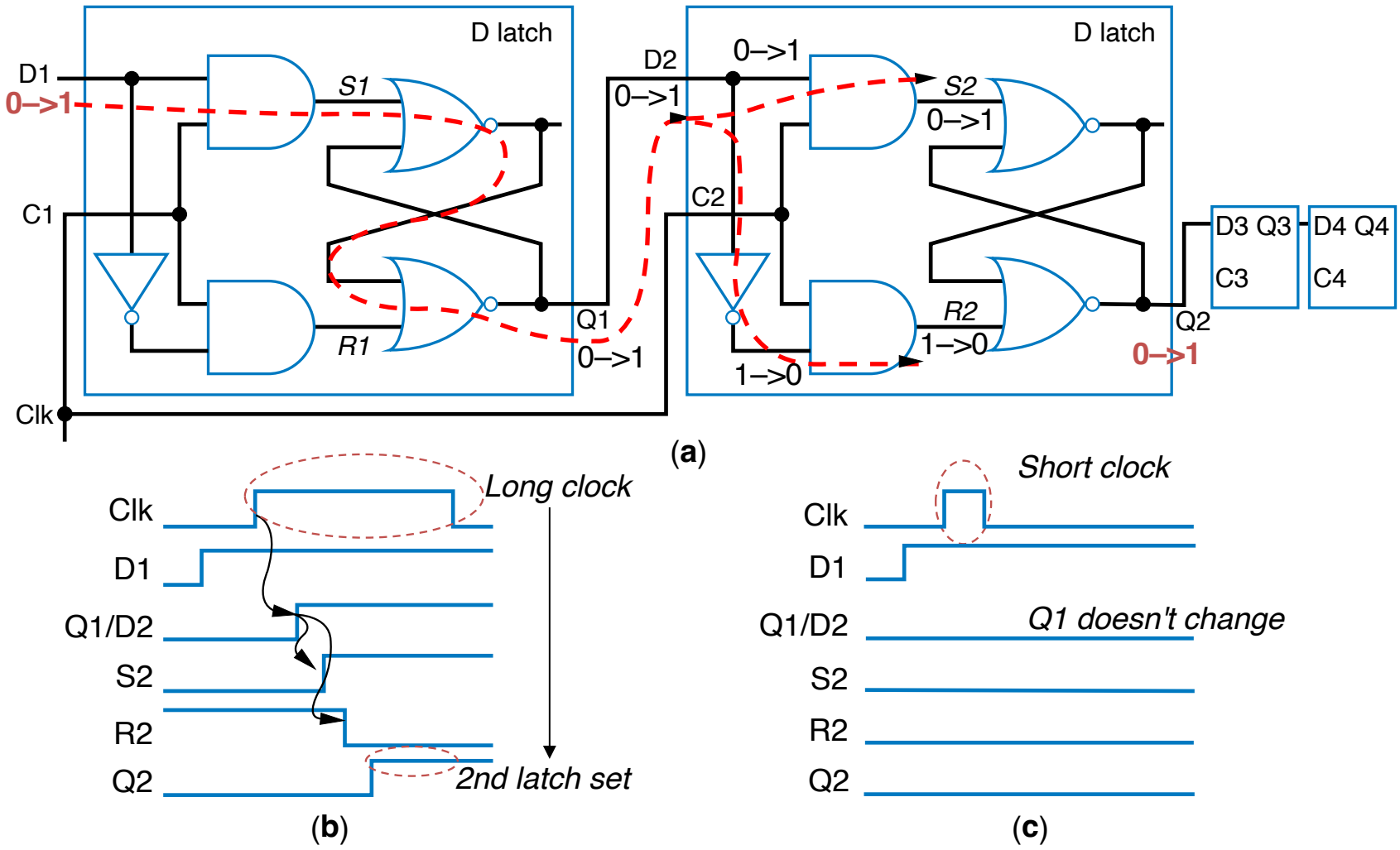


Truth table of a D Latch

E	D	Q+	Function
0	X	Q	Store
1	0	0	Transparent
1	1	1	Transparent

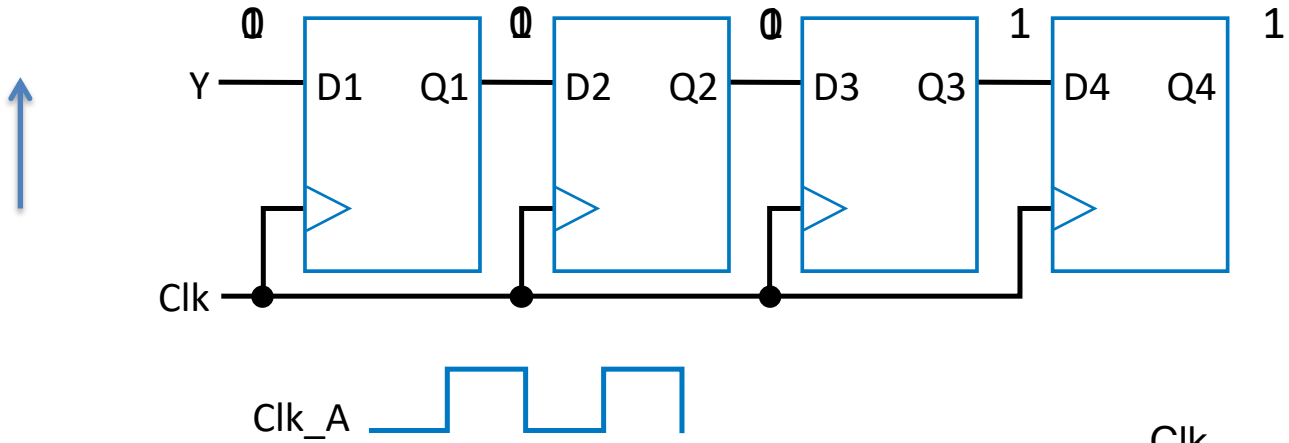
- When Clk_A is 1, how many latches will the input pass through?
- With Clk_A, it may be more, Clk_B, fewer

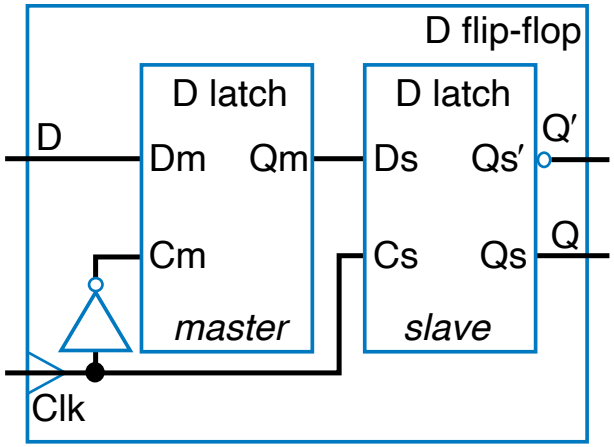
Timing of Latches



Recap: Edge Triggered Flip-Flops

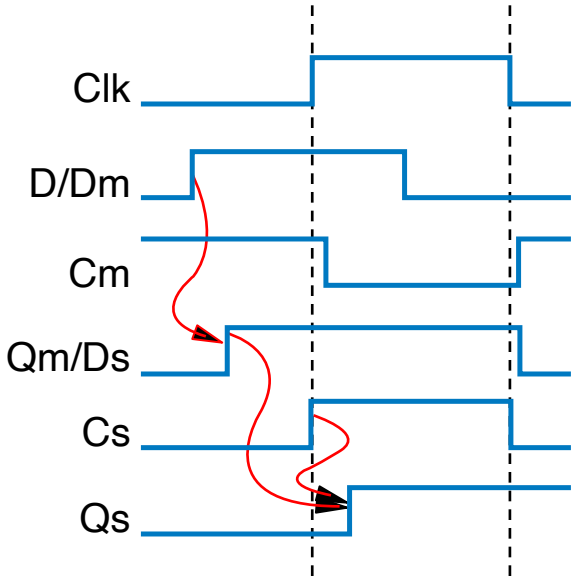
- Use edge triggered flip-flop to overcome the limitation of latches





Truth table of a D Latch

E	D	Q+	Function
0	X	Q	Store
1	0	0	Transparent
1	1	1	Transparent

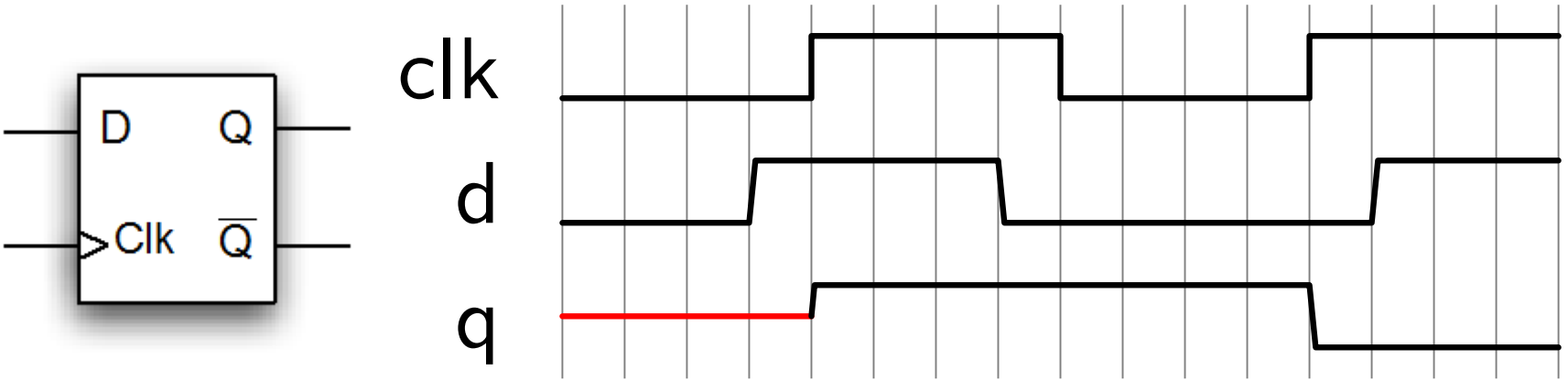


Edge-Triggered Flip-Flops

- Master-Slave implies two latch stages:
  - Master stage is enabled when control is low, and samples the current input, while slave is disabled, locking it in the middle
  - When control goes high, the master is disabled, and the slave uses the value from the middle to determine its output
- Hence, the only time an output will change is at the rising edge
  - *For a negative-edge triggered setup, the master responds to high enable, and the slave to low enable*

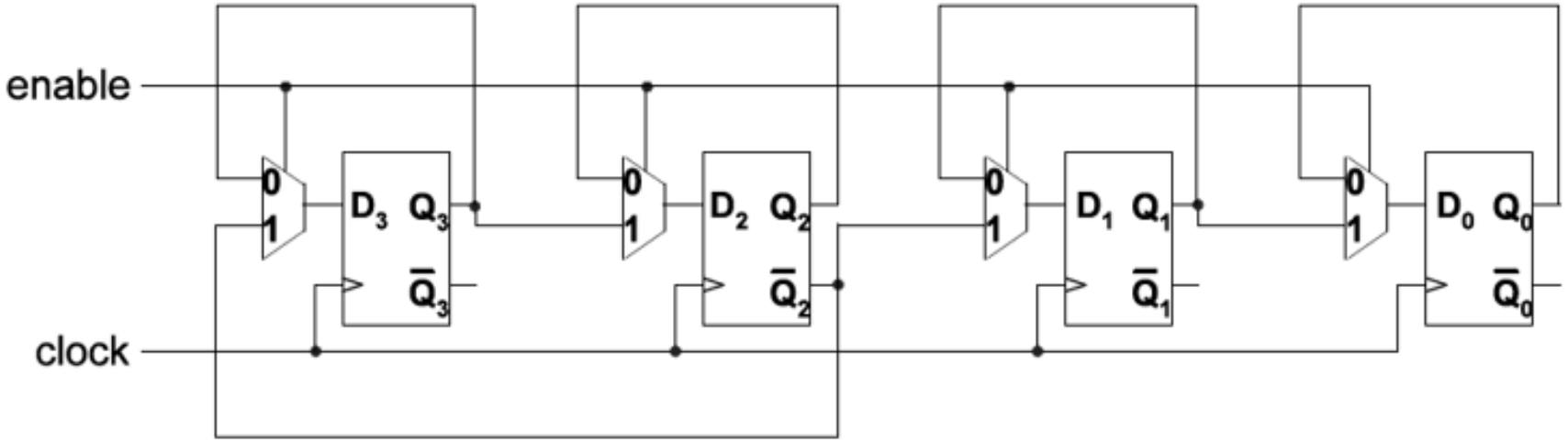
Edge-Triggered Flip-Flops

- The timing diagram for for a D-type flip-flop is as follows:



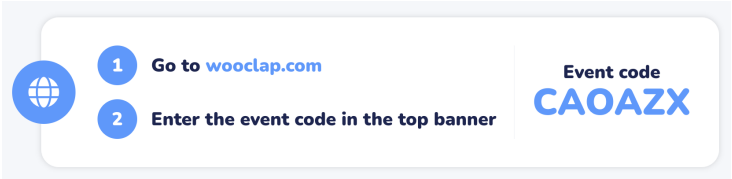
- Note transitions on the output only occur at the (rising) clock edge

Exercise 2



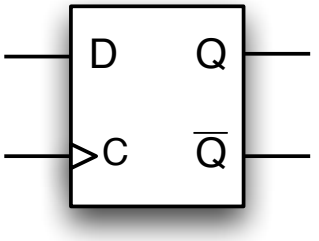
If *enable* = 1 and the current state of the circuit is $Q_3Q_2Q_1Q_0$ = 0101, what is the next state?

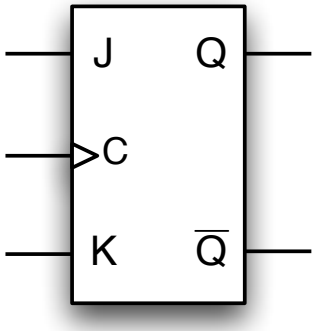
1111
1010
1100
0011
0000

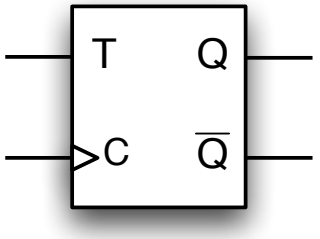


Edge-Triggered Flip-Flops

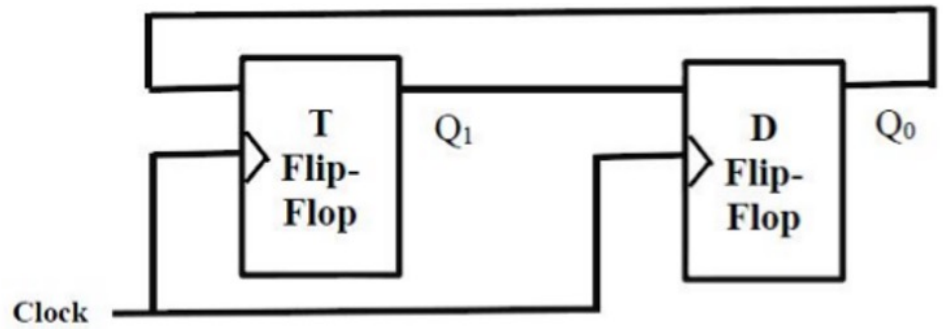
- We've seen the D flip-flop:
  - Q takes the value on D at the rising edge of C
- There's also a J-K flip-flop:
  - Q becomes 1 if J is asserted at the rising edge and 0 if K is asserted
  - If both J and K are asserted, the output toggles at the rising edge
- And a T flip-flop:
  - Q toggles at the rising edge if T=1
- (Also a lesser seen SR flip-flop)







Exercise 3

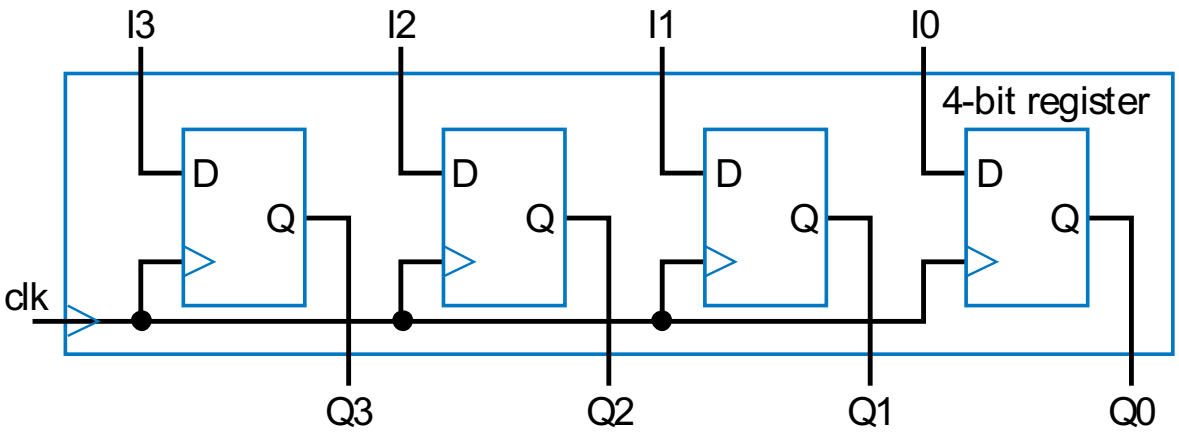


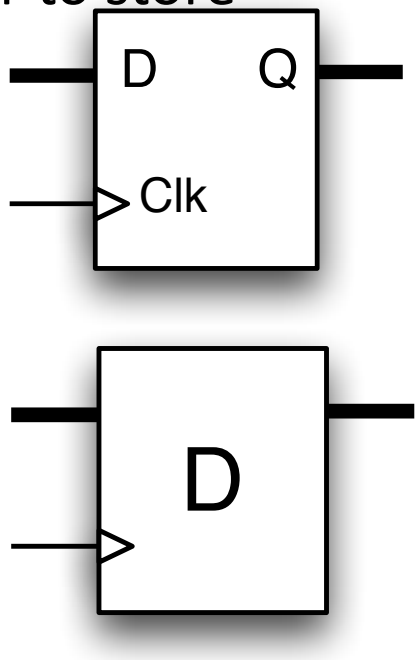
Initially both Q_0 and Q_1 are set to 1 (before the first clock cycle). The outputs

3^{rd} clock cycle, $Q_1Q_0 = 11$; 4^{th} clock cycle, $Q_1Q_0 = 00$;
3^{rd} clock cycle, $Q_1Q_0 = 11$; 4^{th} clock cycle, $Q_1Q_0 = 01$;
3^{rd} clock cycle, $Q_1Q_0 = 00$; 4^{th} clock cycle, $Q_1Q_0 = 11$;
3^{rd} clock cycle, $Q_1Q_0 = 01$; 4^{th} clock cycle, $Q_1Q_0 = 01$;

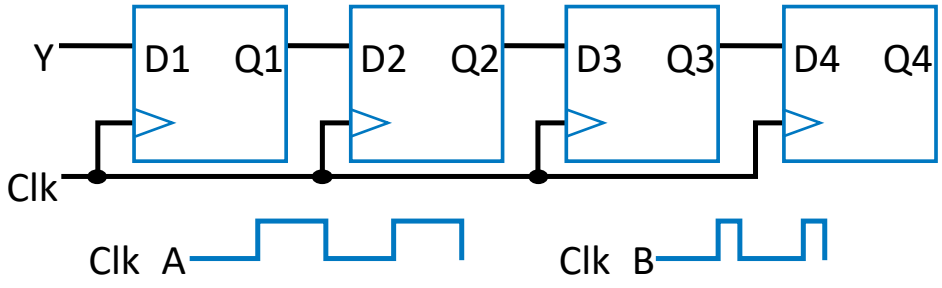
Registers

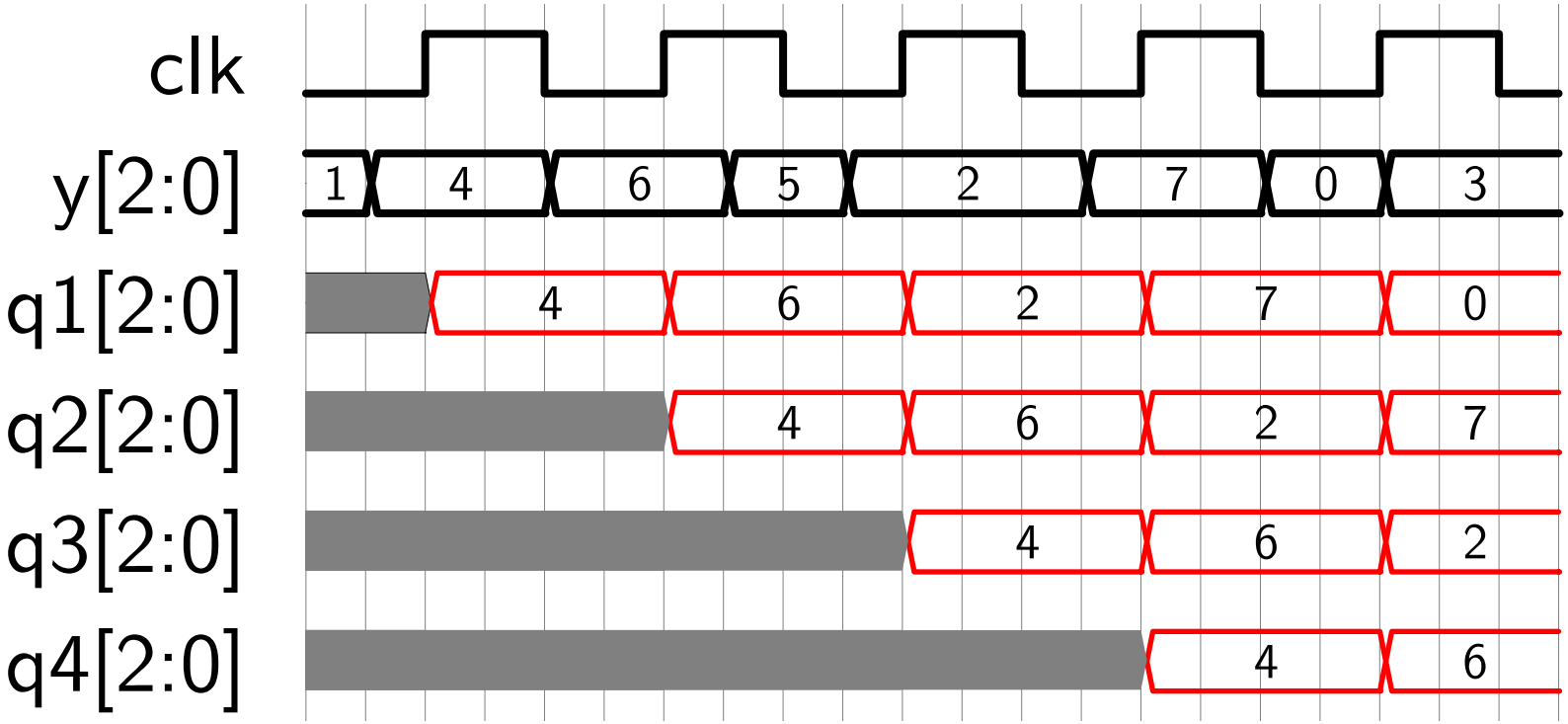
- Flip-flop is a circuit that changes outputs only at the control signal's edges; positive edge-triggered or negative edge-triggered
- The D-type flip-flop is the fundamental building block in synchronous design
- But we often deal with multi-bit signals
- When we combine multiple D flip-flops together to store multiple bits, we call this a **register**:





Shift Register





END OF L17,L18 SUMMARY