Lecture 3 key concepts

- Alternate logic symbols can be used to describe logic circuits more clearly
- With bubble: interpret as 0; without bubble: interpret as 1
- AND shape: interpret as “and”; OR shape: interpret as “or”
- XOR, XNOR, bitwise comparison, parity circuit
- Logic ICs: circuit connection diagram - physical pinout, power and ground
- Applied in Experiment 1

Which concepts are unclear to you after viewing L3?

A. Alternate logic symbols
B. XOR, XNOR
C. Parity circuit
D. Logic circuit connections
E. None

Its output is 0 when at least one of its input is 0. What gate is it?

A. NOT
B. OR
C. AND

Will you be attending the concert?

"I won't attend if I don't have a free ticket <u>and</u> no one goes with me"

- Alternate symbol for 2-input OR gate

Alternatively, it is the same as
"I will attend if I have a free ticket <u>or</u> someone goes with me"

- Standard symbol for 2-input OR gate

Alternate symbols example 1

Given X = [(ABC)’ (A+D)]’

How to draw the logic circuit diagram?

3 ways:

a) Use standard logic symbols only

b) Show clearly how X can go Low using appropriate symbols

c) Show clearly how X can go High using appropriate symbols

a) X = [(ABC)’ (A+D)]’

b) X=0 requires (either A=0, or B=0, or C=0) and (A=1 or D=1)

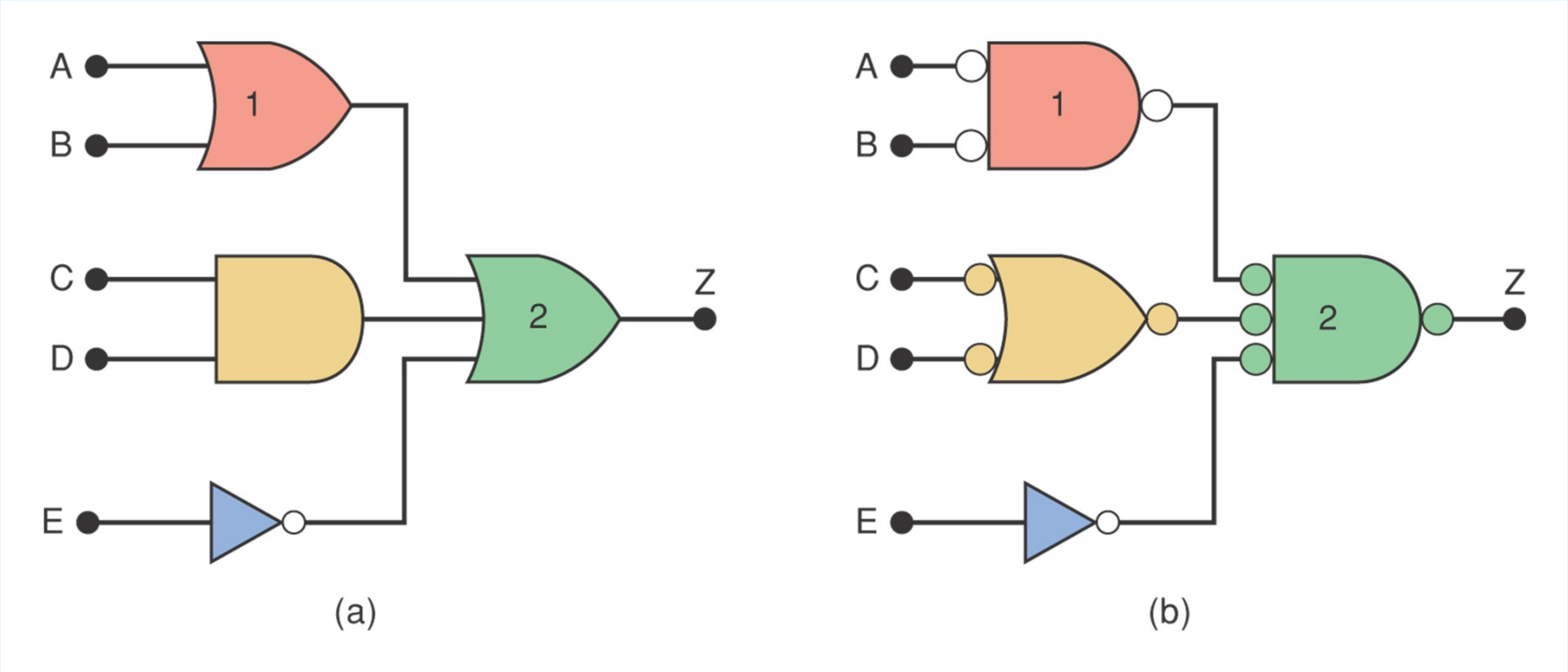
c) X=1 requires (A=B=C=1) or (A=D=0)

Alternate symbols example 2

Given another circuit Z = (A+B)+CD+E’

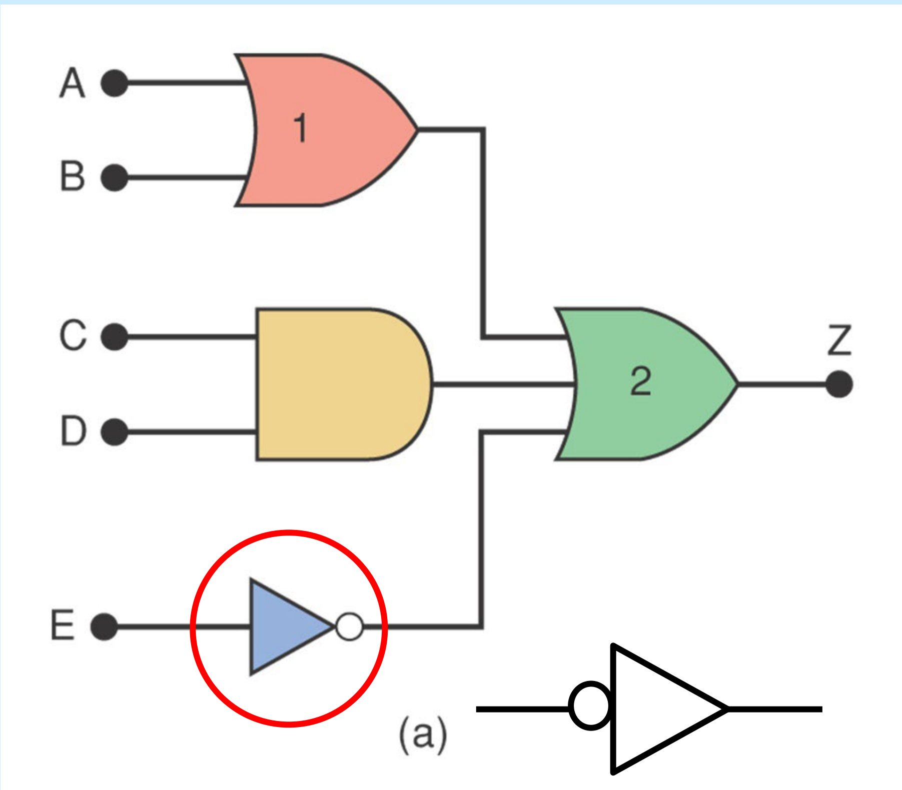
Figure shows how to make output Z goes

(a) High **(b) Low**



Example 2 (cont)

Interpretation of circuit diagram (a):



Z = 1 when

A=1 <u>or</u> B=1,

<u>or</u>

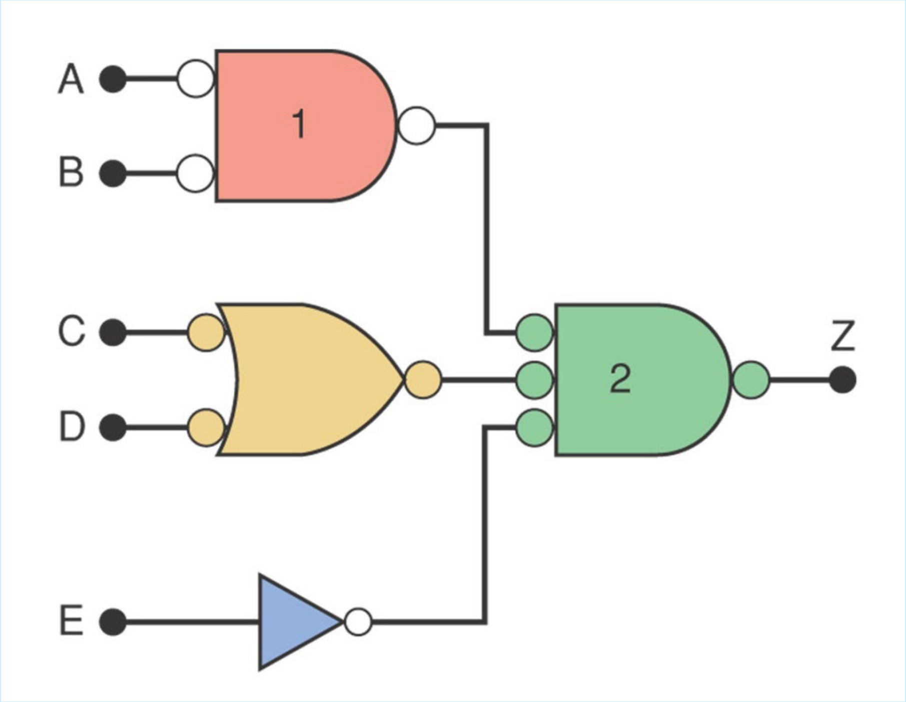
C=1 <u>and</u> D=1,

<u>or</u>

E=0

Example 2 (cont)

Interpretation of circuit diagram (b):



Z = 0 when

A=0 <u>and</u> B=0,

<u>and</u>

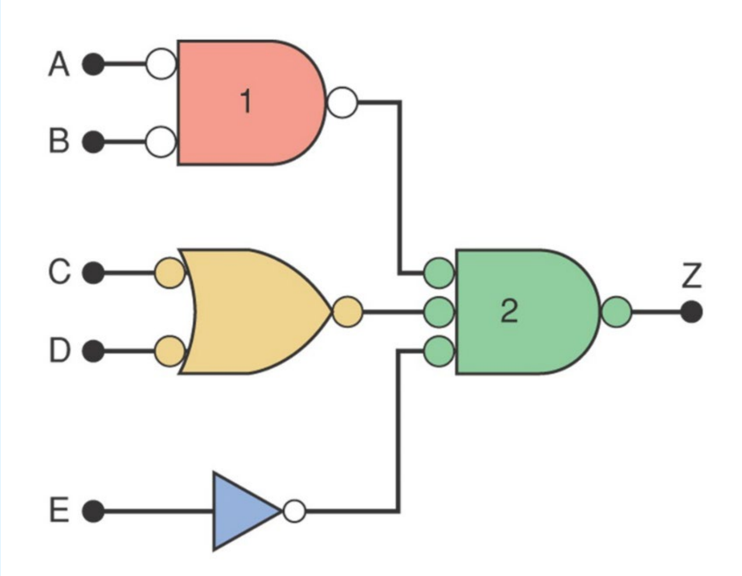
C=0 <u>or</u> D=0,

<u>and</u>

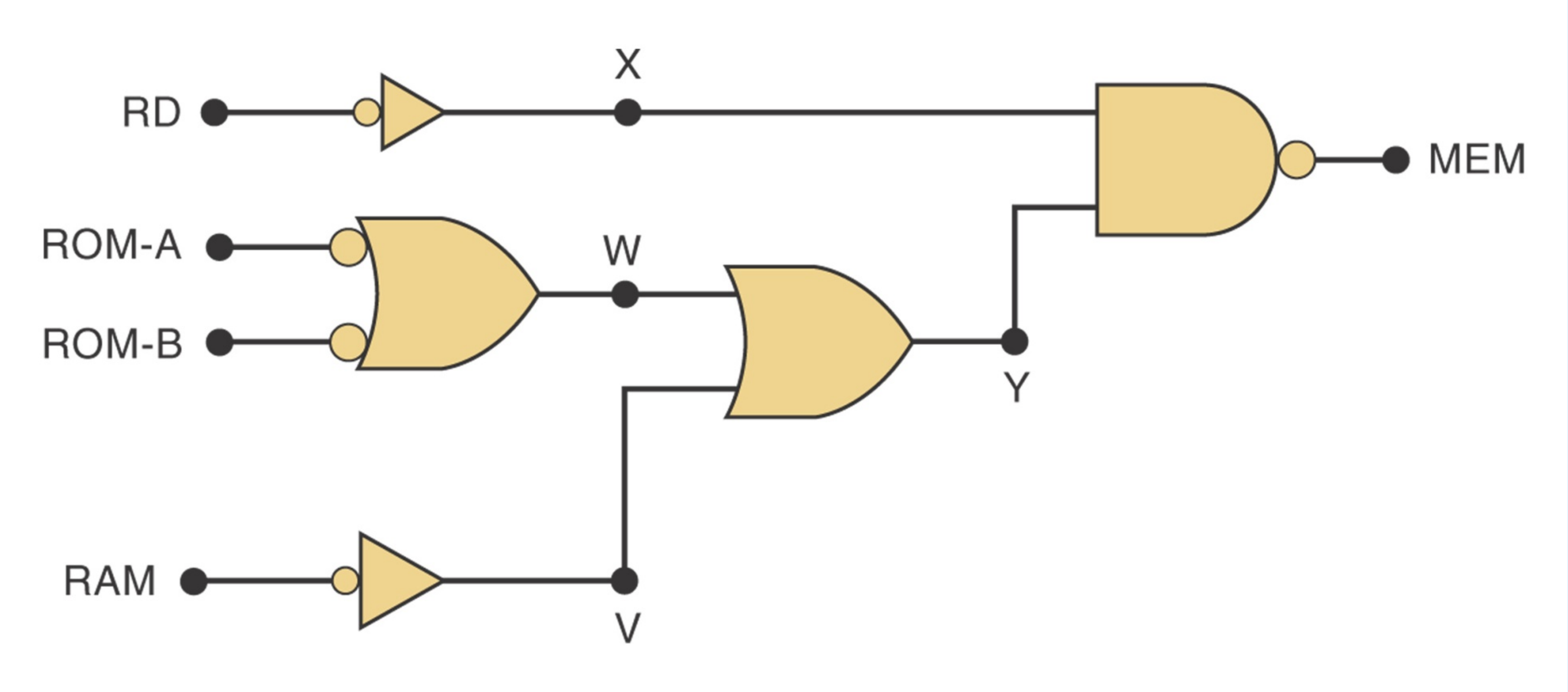
E=1

Example 2 (cont)

What if we remove pairs of matched-bubbles?



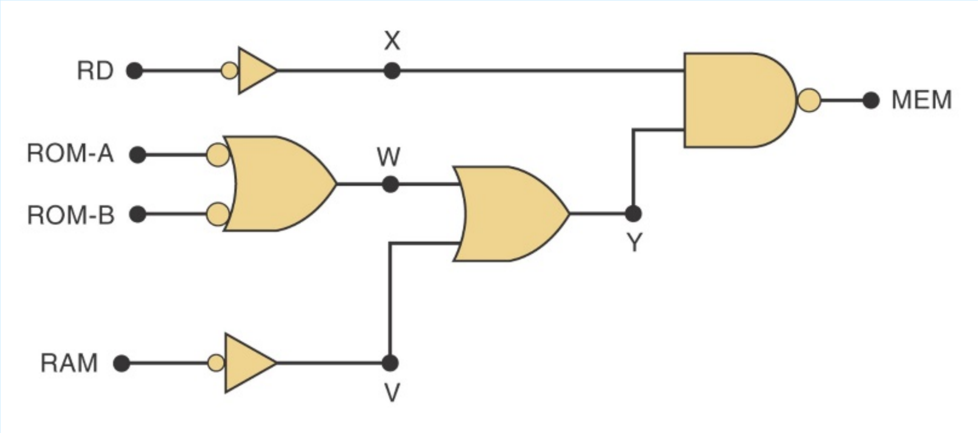
Alternate symbols example 3



RD=0 and (ROM-A=0 or ROM-B=0 or RAM=0) **will make MEM = 0**

Figure 3-39 Tocci, Widmer, Moss. 10th ed.

Possible to draw simpler diagram



Exclusive OR/NOR

$A \text{ XOR } B = AB' + A'B = A \oplus B$

$A \text{ XNOR } B = A'B' + AB = (A \oplus B)'$

$$A \text{ XOR } B \text{ XOR } C = (A \oplus B) \oplus C$$
$$= A \oplus (B \oplus C)$$

XOR is commutative and associative

$$(A \oplus B)' = A \oplus B' = A' \oplus B$$

True or false?

A. True

B. False

Example: Construct the truth table for F:

$F = W\,(X \oplus Y \oplus Z \oplus W') + (X \oplus Y \oplus Z)$

W	X	Y	Z	F
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

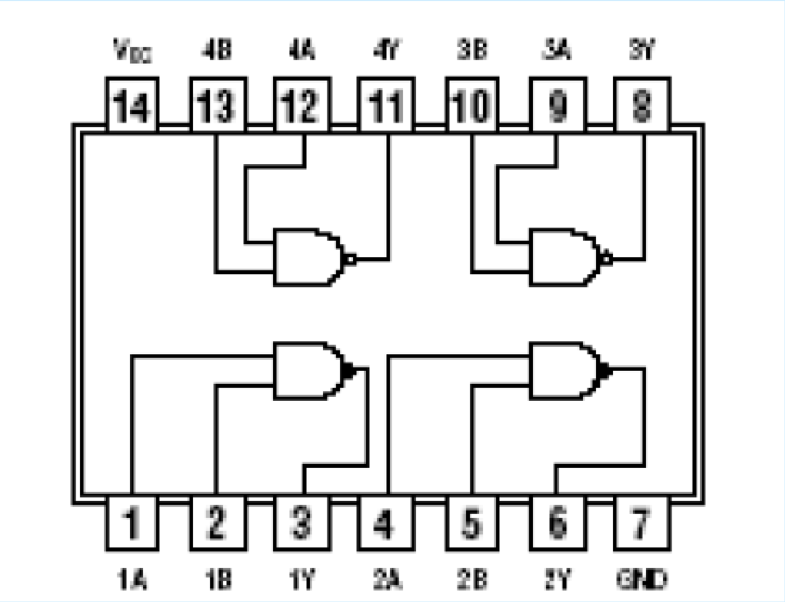
How many 2-input XOR gates are needed to generate the parity bit from an 8-bit data?

A. 4
B. 6
C. 8
D. 10

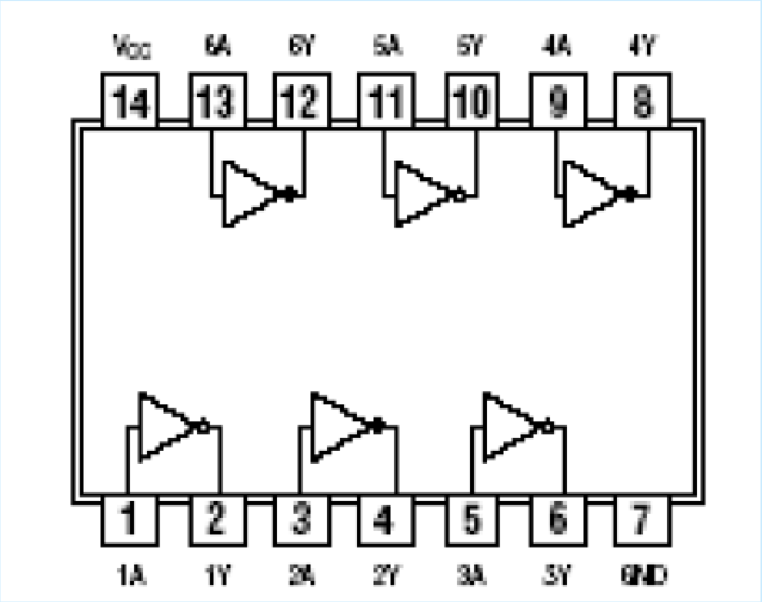
Logic devices

Component pin assignment

Quad-NAND



Hex-NOT



Logic devices (cont)

Circuit connection diagram

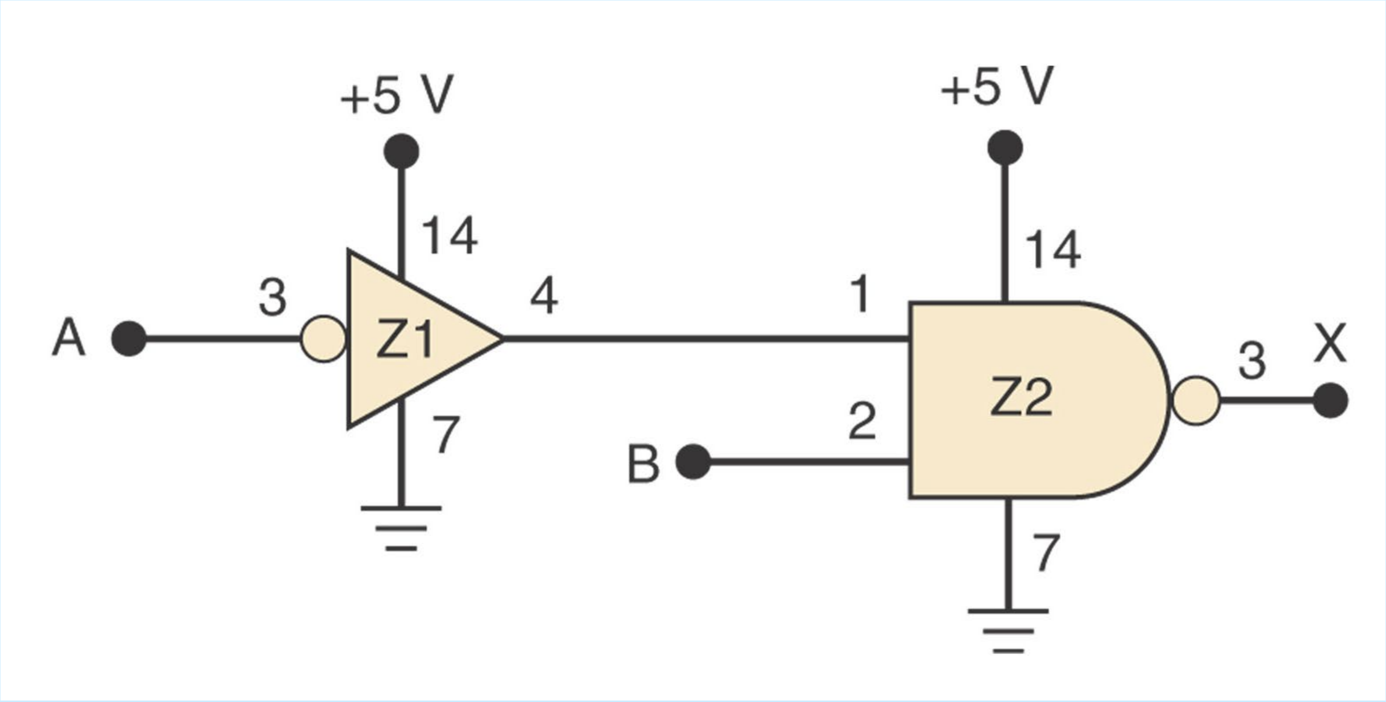


Figure 4-36 Tocci, Widmer, Moss. 10th ed.

Lecture 4 key concepts

- Binary addition and subtraction
- Half adder and full adder
- Carry and sum
- 4-bit parallel adder with 4 full adders
- Carry propagation
- Sign-magnitude representation
- 2’s complement representation
- http://www.falstad.com/circuit/e-fulladd.html

Which concepts are unclear to you after viewing L4?

A. Half adder, full adder
B. Parallel adders
C. Carry propagation
D. Sign-magnitude
E. 2’s complement
F. None

Carry and Sum

Logical addition and arithmetic addition are different:

1 + 1 = 1	Logical addition
1 + 1 = 1 0	Arithmetic addition
1 + 1 + 1 = 1 1	Arithmetic addition

e.g. 21(dec) + 7(dec) = 28(dec)

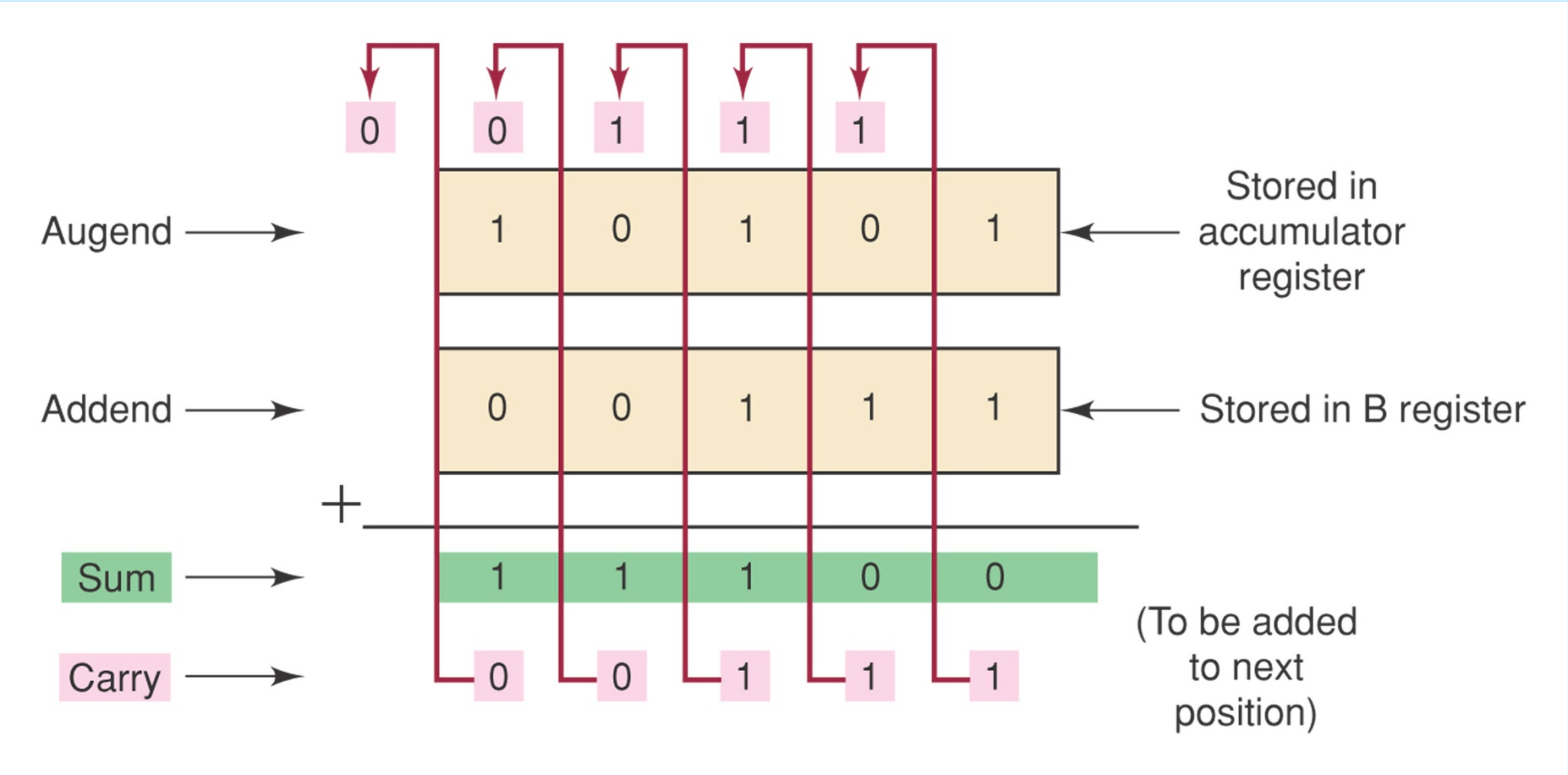


Figure 6-5 Tocci, Widmer, Moss. 10th ed.

e.g. 9(dec) + 7(dec) = 16(dec)

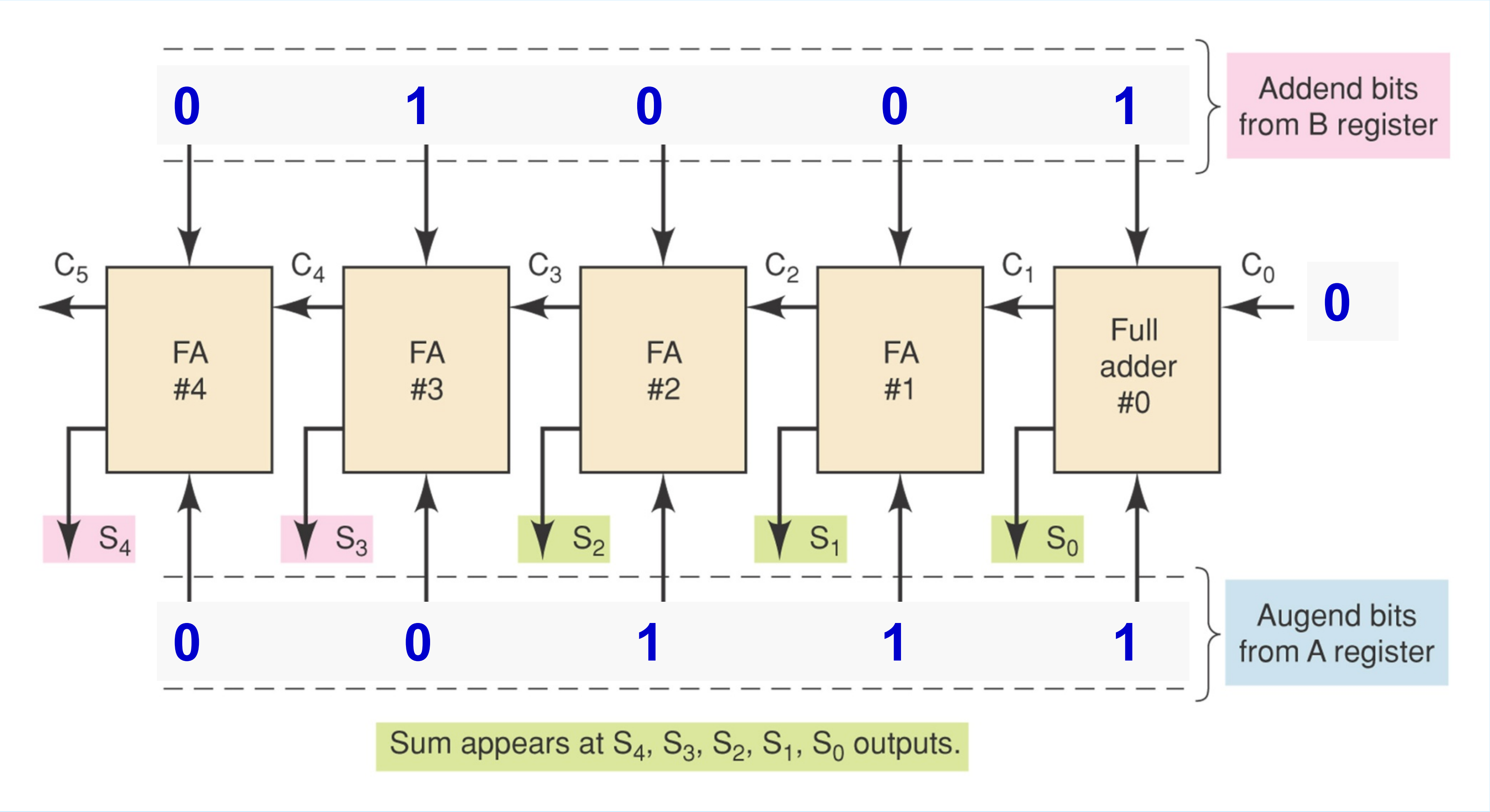


Figure 6-6 Tocci, Widmer, Moss. 10th ed.

e.g. 9(dec) + 7(dec) = 16(dec)

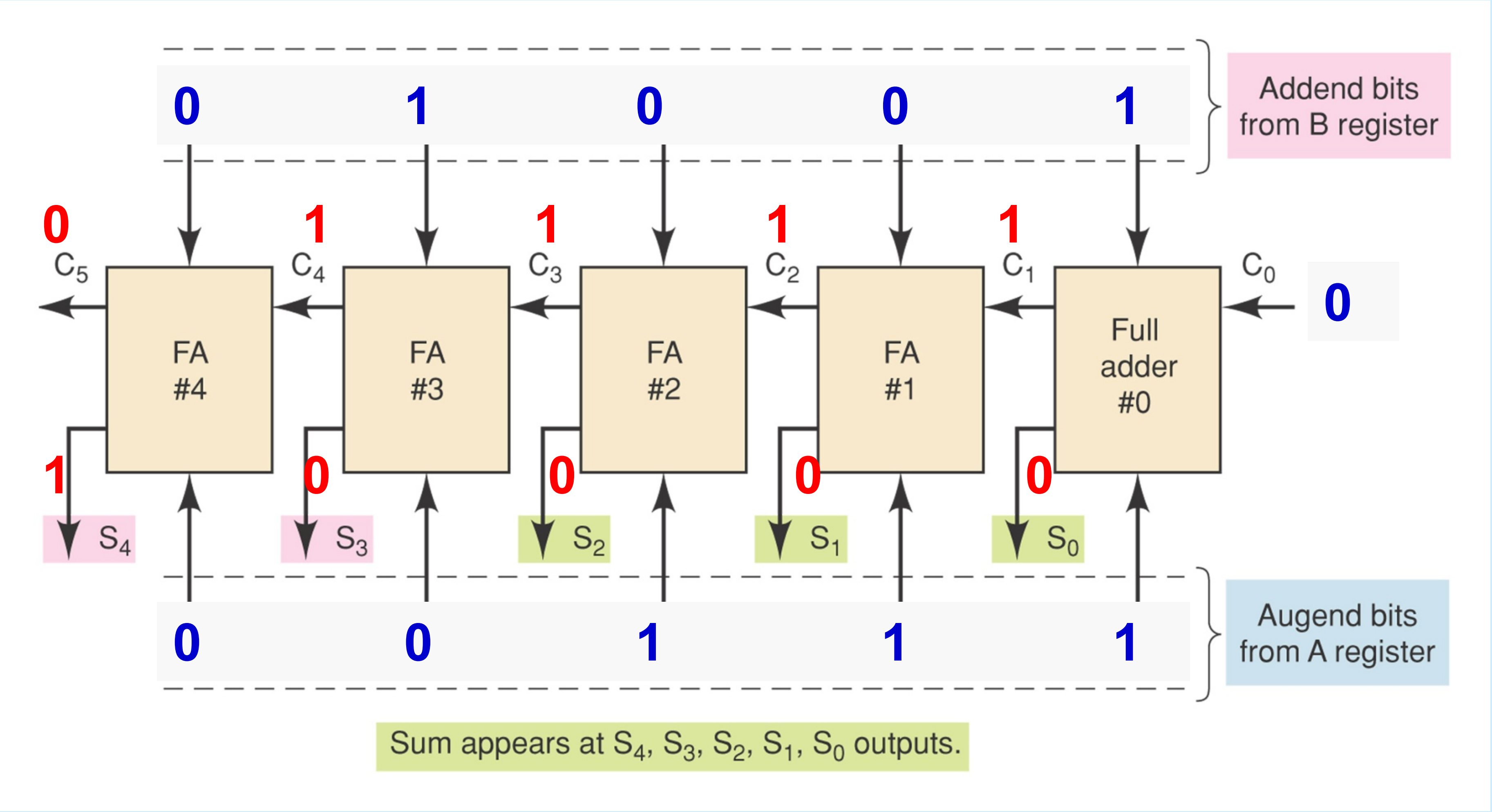


Figure 6-6 Tocci, Widmer, Moss. 10th ed.

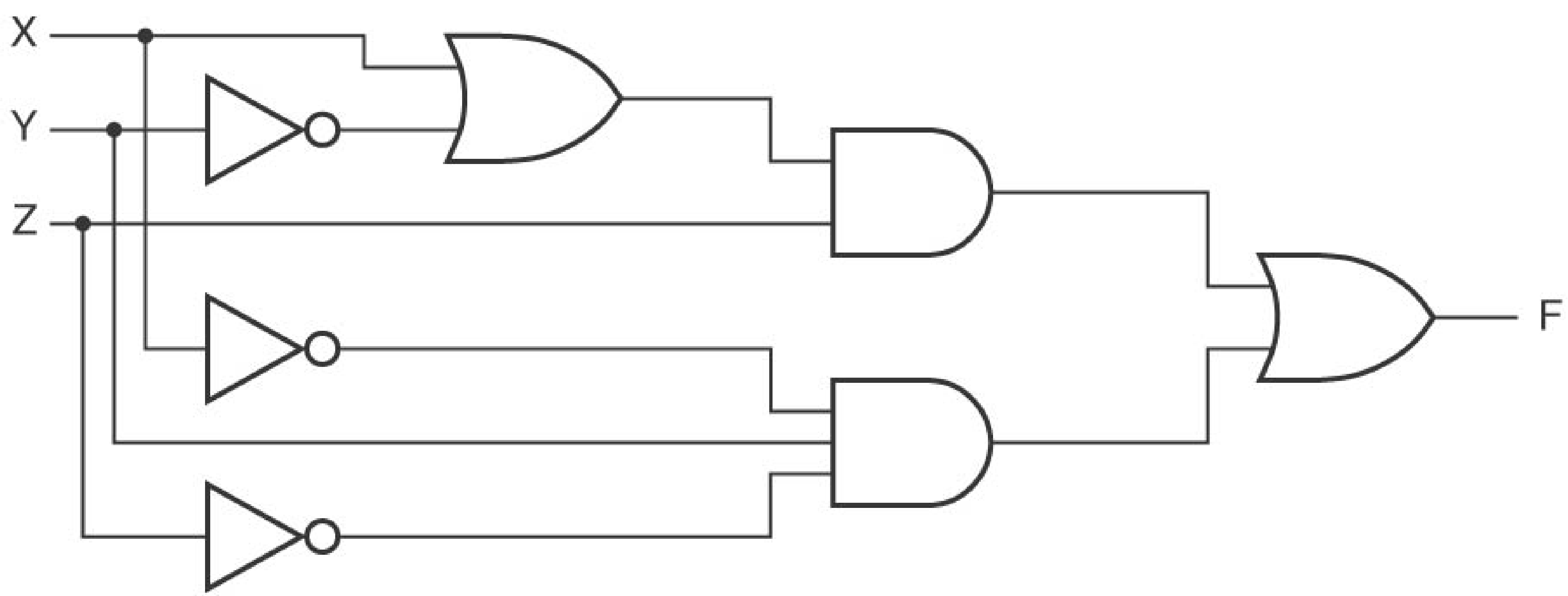
Re-write the following in hexadecimal:

$$\boxed{9(\text{dec}) + 7(\text{dec}) = 16(\text{dec})}$$

$$\boxed{21(\text{dec}) + 7(\text{dec}) = 28(\text{dec})}$$

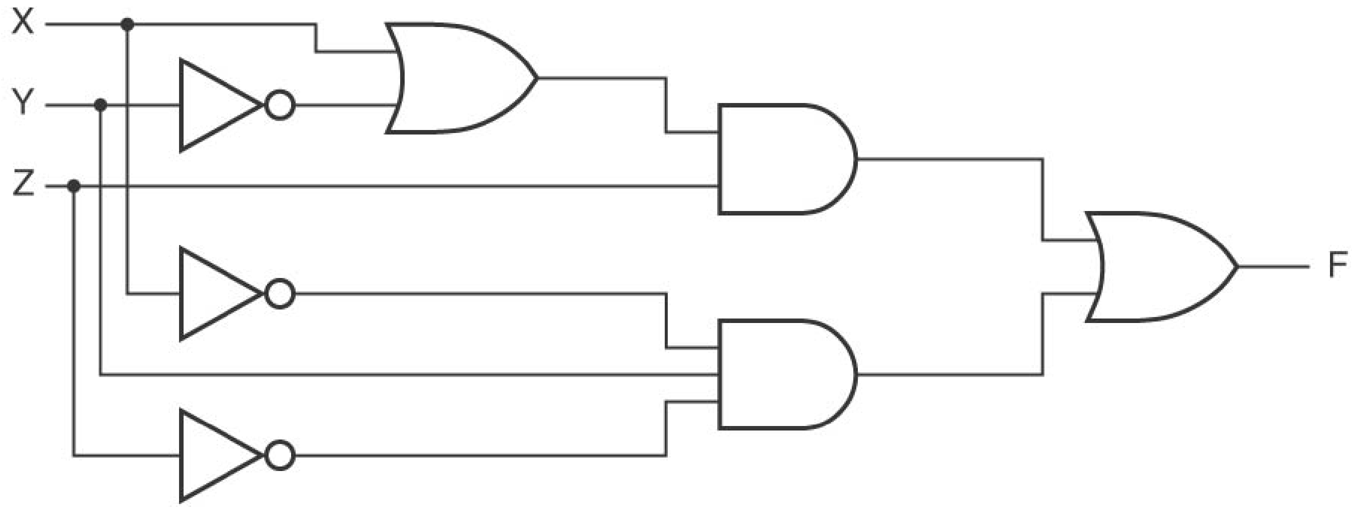
Propagation delay example

How many units of gate delays in total from inputs X, Y, Z to output F?



From *Digital Design: Principles and Practices*, Fourth Edition, John F. Wakerly, ISBN 0-13-186389-4.

How many units of gate delay in total?



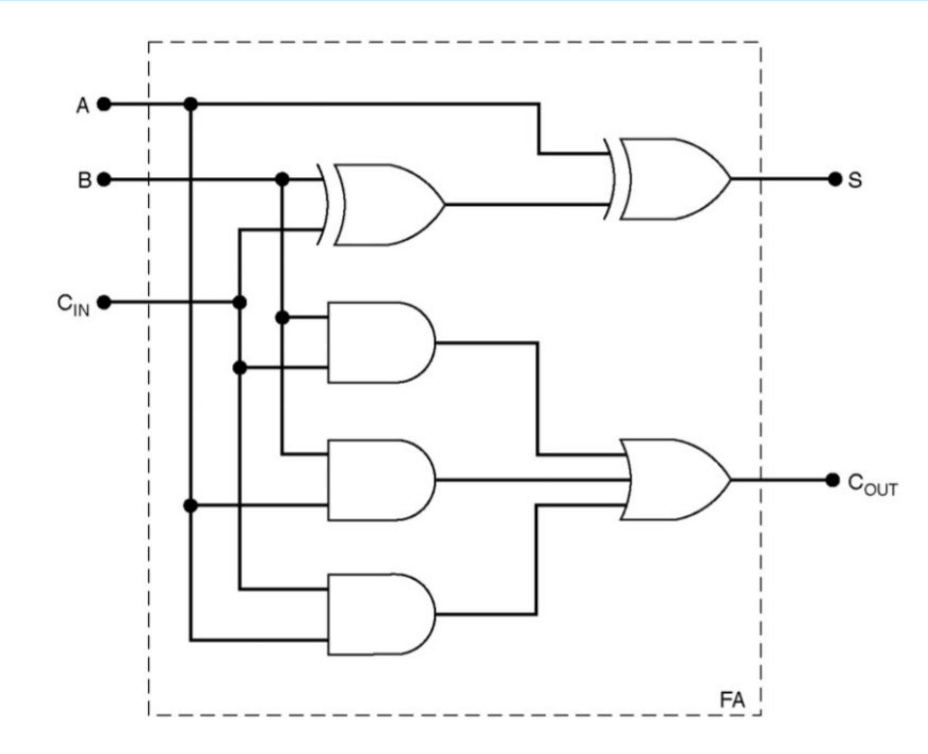
A. 4

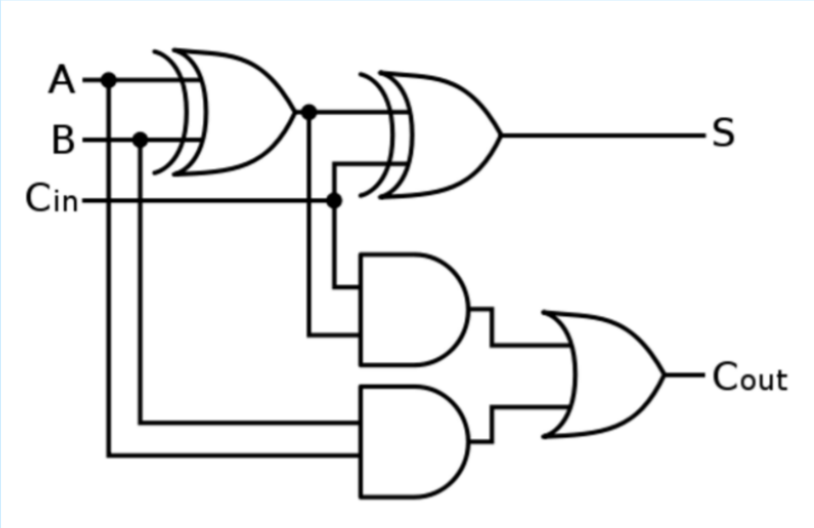
B. 5

C. 6

D. 7

Do these circuits perform the same function?
Do they have the same propagation delays?





Give the sign-magnitude/2's complement representation of +20 (dec):

A. 1 0 1 0 0
B. 0 1 1 0 0
C. 0 1 0 1 0 0
D. 1 0 1 1 0 0

Give the sign-magnitude representation of -20 (dec):

A. 1 0 1 0 0
B. 0 1 1 0 0
C. 1 0 1 1 0 0
D. 1 1 0 1 0 0

Give the 2's complement representation of -20 (dec):

A. 1 0 1 0 0
B. 0 1 1 0 0
C. 1 0 1 1 0 0
D. 1 1 0 1 0 0

End of L4 summary