智晶光電股份有限公司

UG-2864KSWMG01

UG-2864KSYMG01

UG-2864KLBMG01

Evaluation Kit User Guide

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Version: 1.0

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1. REVISION HISTORY

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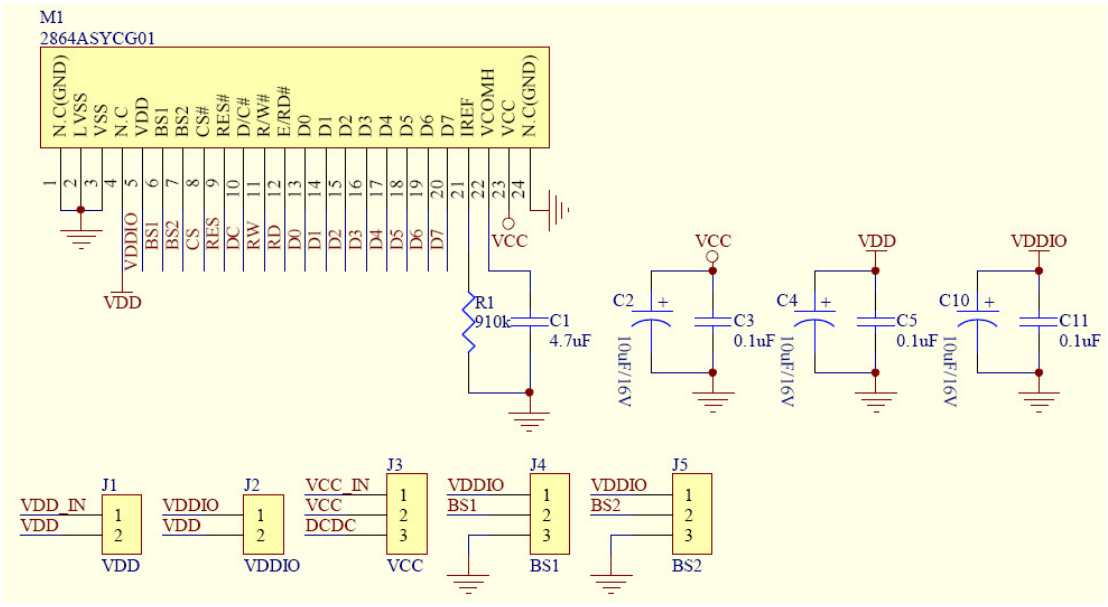
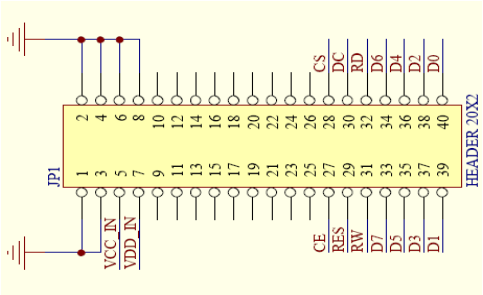
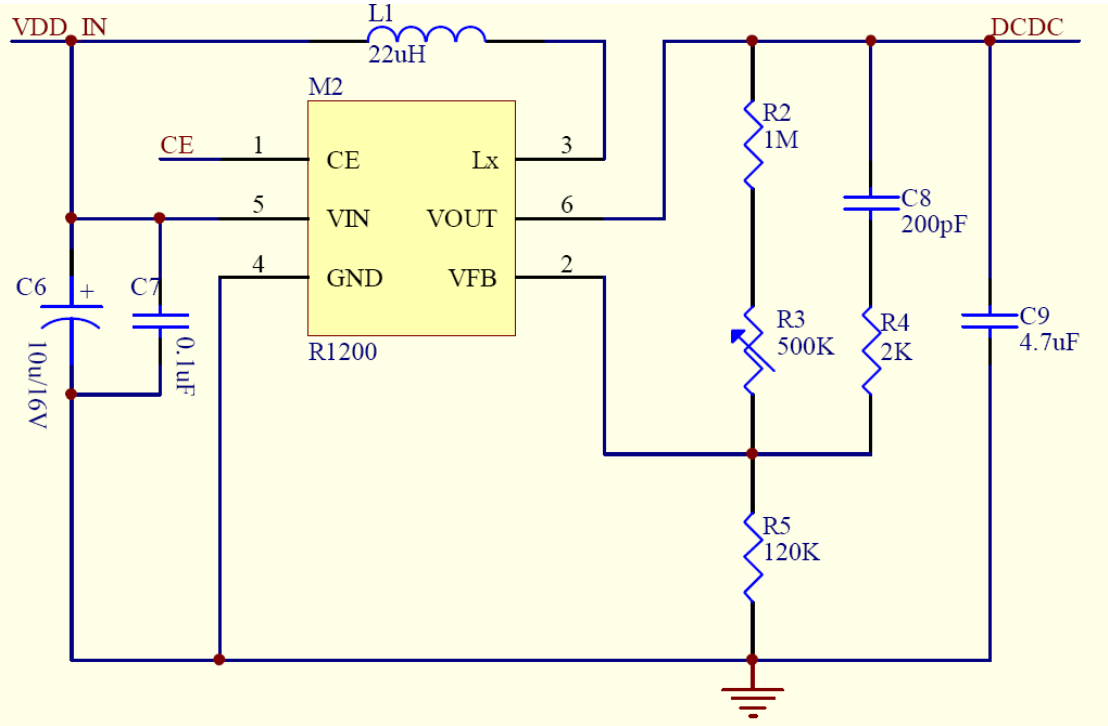
2011/10/26			1.0

2. EVK Schematic







3. Symbol define

VCC：Power supply for panel driving voltage.

VSS：This is ground pin.

VDD：Power supply for core logic operation.

VDDIO：Power supply for interface logic level. (Reserved Function not Applicable)

BS0~BS2：MUC bus interface selection pin(BS0 pulled LOW in internal).

CS：This pin is chip select input(active LOW).

RES：This pin is reset signal input(active LOW).

D/C：This is DATA/COMMAND control pin. When it is Pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register.

In I2C mode, this pin acts as SA0 for slave address select.

R/W：This is read/write control input pin connecting to the MCU interface.

When interface to a 6800-series microprocessor , Read mode will be carried out when this pin is pulled HIGH and write mode when low .

When interface to an 8080-microprocessor , this pin when be the data Write input.

When serial interface is selected, this pin must be connected to Vss.

E/RD：When interface to a 6800-series microprocessor , this pin will be used as the Enable(E) signal.

When interface to an 8080-microprocessor , this pin receives the Read(RD#)signal.

D0~D7：These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.

When serial interface mode is selected, D0(SCLK) will be the serial clock input,D1(SDIN) will be the serial data input,D2 should be left opened.

When I2C mode is selected,D1(SDA_{in}) AND D2(SDA_{out}) should be tied together,D0(SCL) is the I2Cclock input

IREF：This is segment output current reference pin.

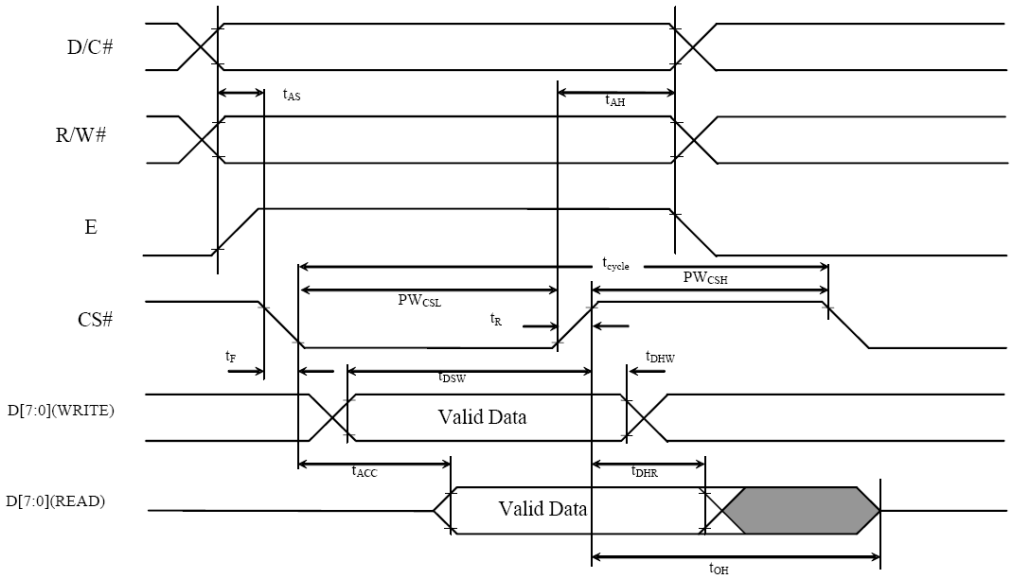
VCOMH：This pin for COM signal deselected level voltage.

4.TIMMING CHARACTERISTICS

4.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	System Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

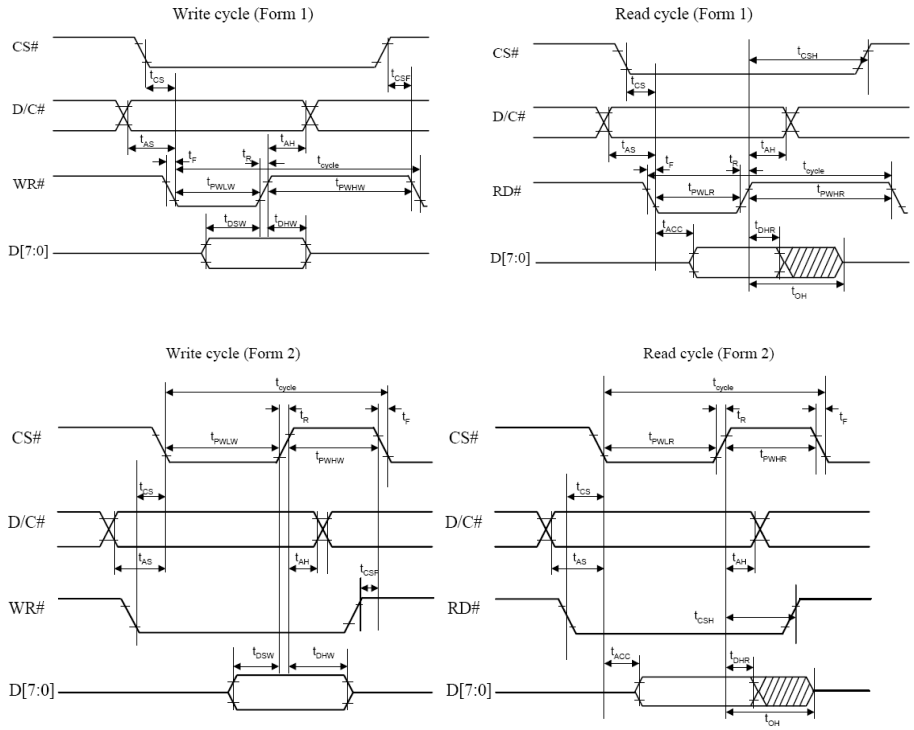
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)



4.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

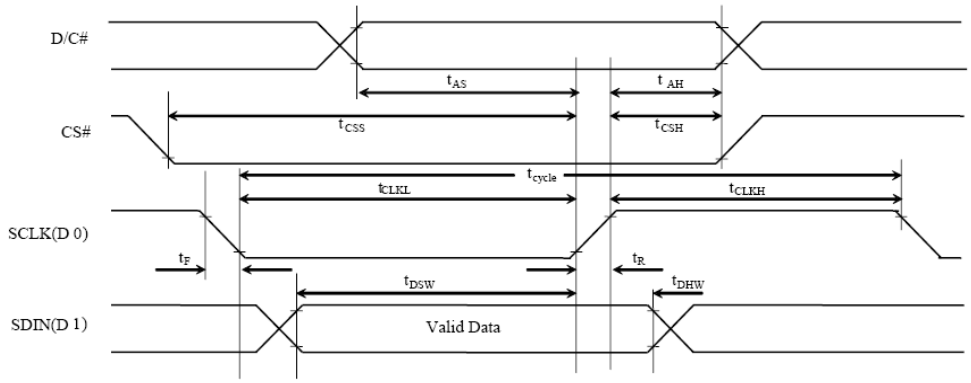
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)

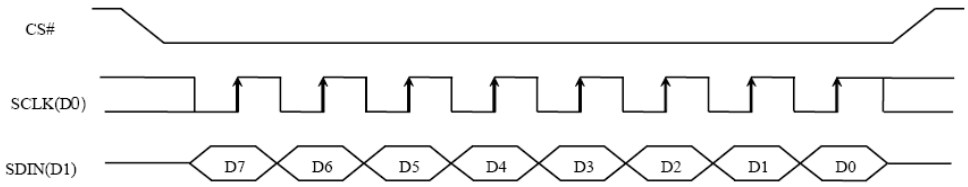


4.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	50	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Serial Clock Low Time	100	-	ns
t_{CLKH}	Serial Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)

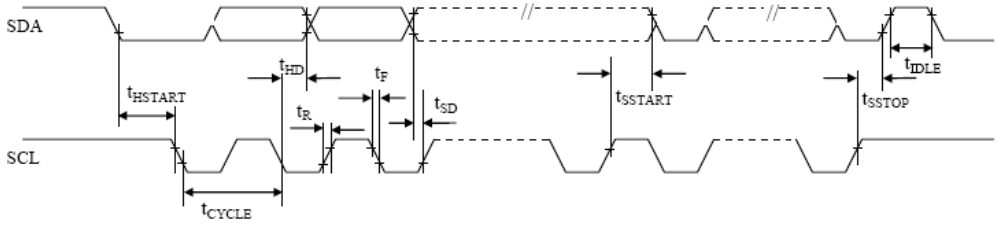




4.4 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)



5.EVK use introduction

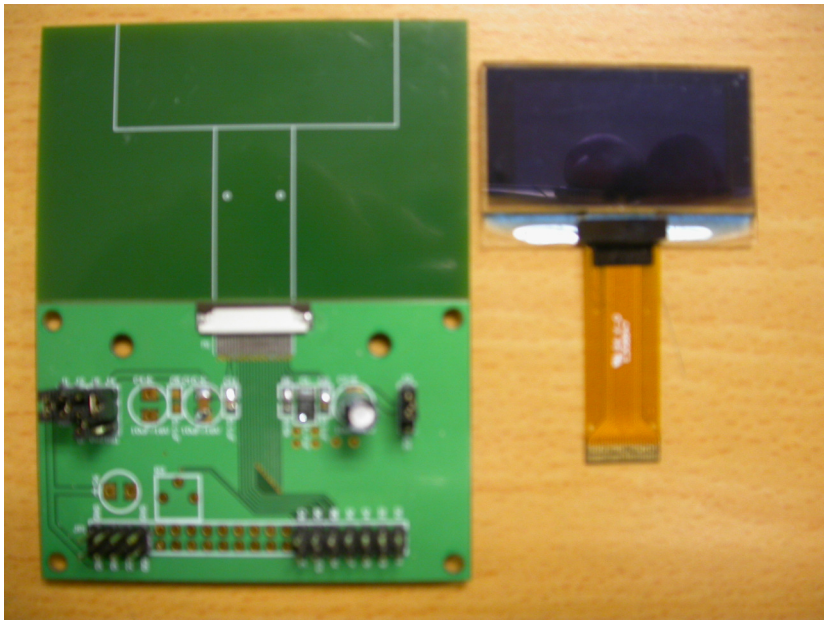


Figure 1 EVK PCB and OLED Module

UG-2864ASYCG01 is COG type module, please refer to Fig5, Fig6.User can use leading wire to connect EVK with customer's system. The example shows as Fig7.

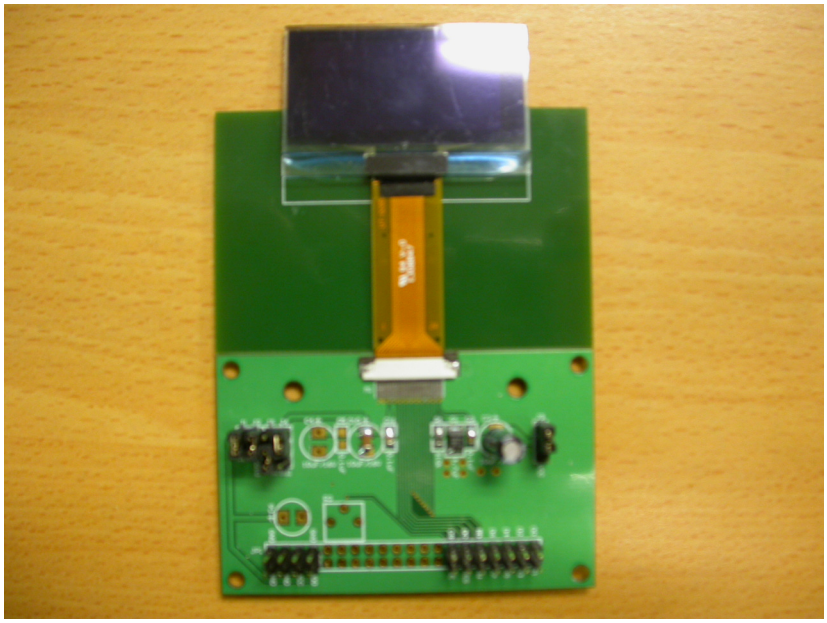


Figure 2 The combination of the module and EVK

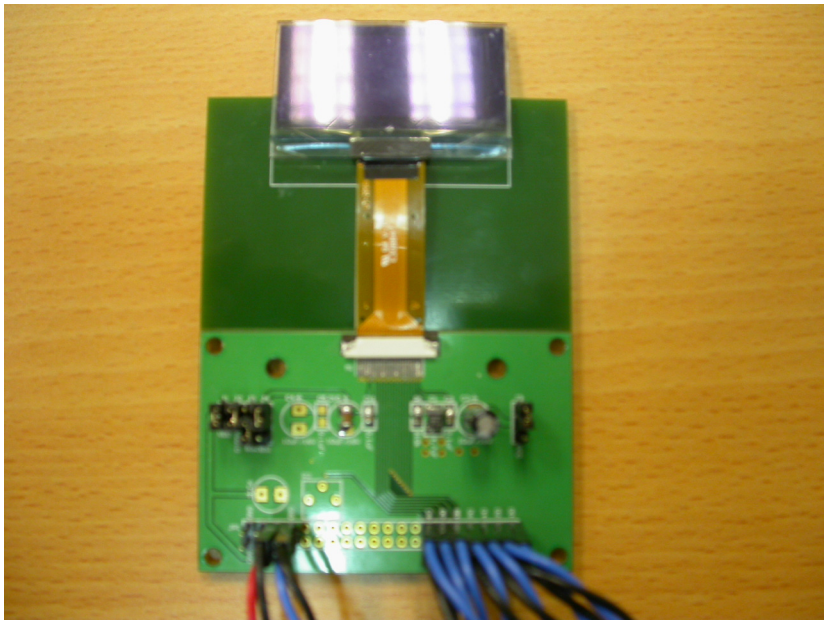


Figure 3 EVK with test platform

Note 1：It is OLED high voltage supply.

Note 2：It is logic voltage supply.

Note 3：Those are leading wire connect to control board. Those are data pin.(D0-D7)

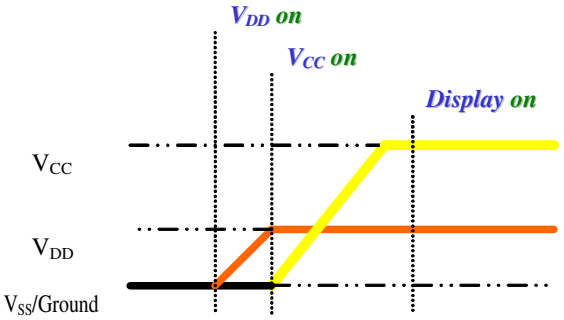
Note 4：Those are leading wire connect to control board. Those are control pin.
(DC, CS, RD, WR, RES)

6. Power down and Power up Sequence

To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DD} is stable)
7. Send Display on command



Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{DDH} is reach 0 and
   panel is completely
   discharges)
4. Power down V_{DD}