Assignment 2
Computer Organization
Deadline: 11:55pm Monday, Nov 12, 2024

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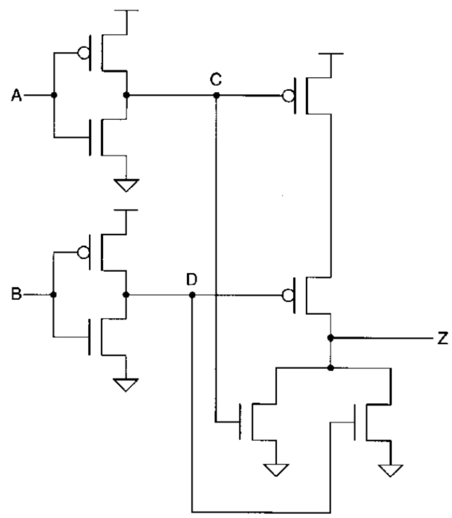
1. For the following transistor-level circuit, fill in the truth table. What is the logical expression of Z in terms of A and B? (12 points)



A	B	C	D	Z

Answer:

A	B	C	D	Z
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Z = AB

2. Fibonacci numbers are the sequence of numbers F_n defined by the linear recurrence equation $F_n = F_{n-1} + F_{n-2}$ where $F_1 = F_2 = 1$. It is conventional to define $F_0 = 0$. Given a word size of four bits, design a circuit to detect if a given input binary number $I_3I_2I_1I_0$ is a Fibonacci number or not. Show the following steps: (22 points)
   1) Write the truth table;
   2) Write the logical expression in Sum of Product form.

3) Simplify the logical expression using logical identities.
4) Simplify the logical expression using K-MAP.
5) Draw the logical circuit and verify it.

Answer:

1)

I_3	I_2	I_1	I_0	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

2) $F = \overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_3}\,\overline{I_2}\,\overline{I_1}I_0 + \overline{I_3}\,\overline{I_2}I_1\overline{I_0} + \overline{I_3}\,\overline{I_2}I_1I_0 + \overline{I_3}I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_3I_2\overline{I_1}I_0$

3)

$F = \overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_3}\,\overline{I_2}\,\overline{I_1}I_0 + \overline{I_3}\,\overline{I_2}I_1\overline{I_0} + \overline{I_3}\,\overline{I_2}I_1I_0 + \overline{I_3}I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_3I_2\overline{I_1}I_0$

$= (\overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_3}\,\overline{I_2}\,\overline{I_1}I_0) + (\overline{I_3}\,\overline{I_2}I_1\overline{I_0} + \overline{I_3}\,\overline{I_2}I_1I_0) + \overline{I_3}I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_3I_2\overline{I_1}I_0$

$= \overline{I_3}\,\overline{I_2}\,\overline{I_1}(\overline{I_0} + I_0) + \overline{I_3}\,\overline{I_2}I_1(\overline{I_0} + I_0) + \overline{I_3}I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_3I_2\overline{I_1}I_0$

$= \overline{I_3}\,\overline{I_2}\,\overline{I_1} + \overline{I_3}\,\overline{I_2}I_1 + (\overline{I_3}I_2\overline{I_1}I_0 + I_3I_2\overline{I_1}I_0) + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0}$

$= \overline{I_3}\,\overline{I_2}\,\overline{I_1} + \overline{I_3}\,\overline{I_2}I_1 + (\overline{I_3} + I_3)I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0}$

$= (\overline{I_3}\,\overline{I_2}\,\overline{I_1} + \overline{I_3}\,\overline{I_2}I_1) + I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0}$

$= \overline{I_3}\,\overline{I_2}(\overline{I_1} + I_1) + I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0}$

$= \overline{I_3}\,\overline{I_2} + I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0}$

$= (\overline{I_3}\,\overline{I_2} + \overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0}) + I_2\overline{I_1}I_0 + I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0}$

$= (I_3\overline{I_2}\,\overline{I_1}\,\overline{I_0} + \overline{I_3}\,\overline{I_2}\,\overline{I_1}\,\overline{I_0}) + I_2\overline{I_1}I_0 + \overline{I_3}\,\overline{I_2}$

$= (I_3 + \overline{I_3})\overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_2\overline{I_1}I_0 + \overline{I_3}\,\overline{I_2}$

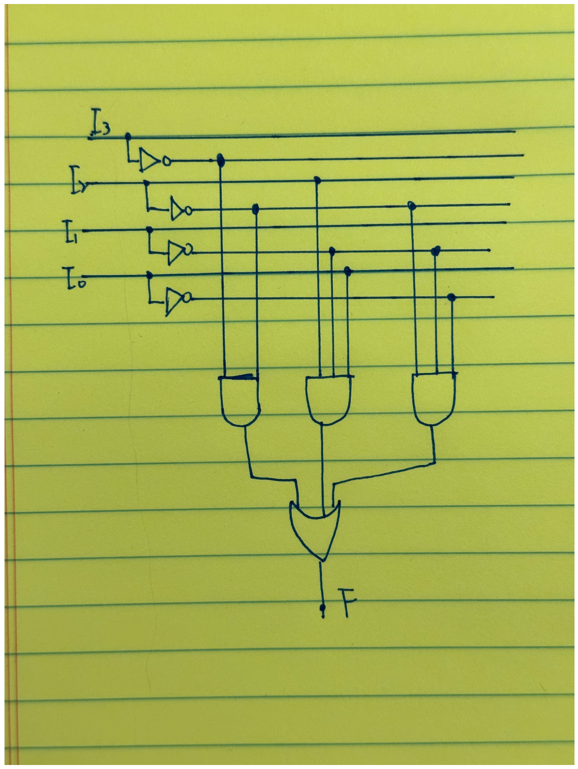
$= \overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_2\overline{I_1}I_0 + \overline{I_3}\,\overline{I_2}$

4)

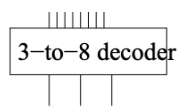
		I_3I_2			
		00	01	11	10
I_1I_0	00	1	0	0	1
	01	1	1	1	0
	11	1	0	0	0
	10	1	0	0	0

F $= \overline{I_2}\,\overline{I_1}\,\overline{I_0} + I_2\overline{I_1}I_0 + \overline{I_3}\,\overline{I_2}$

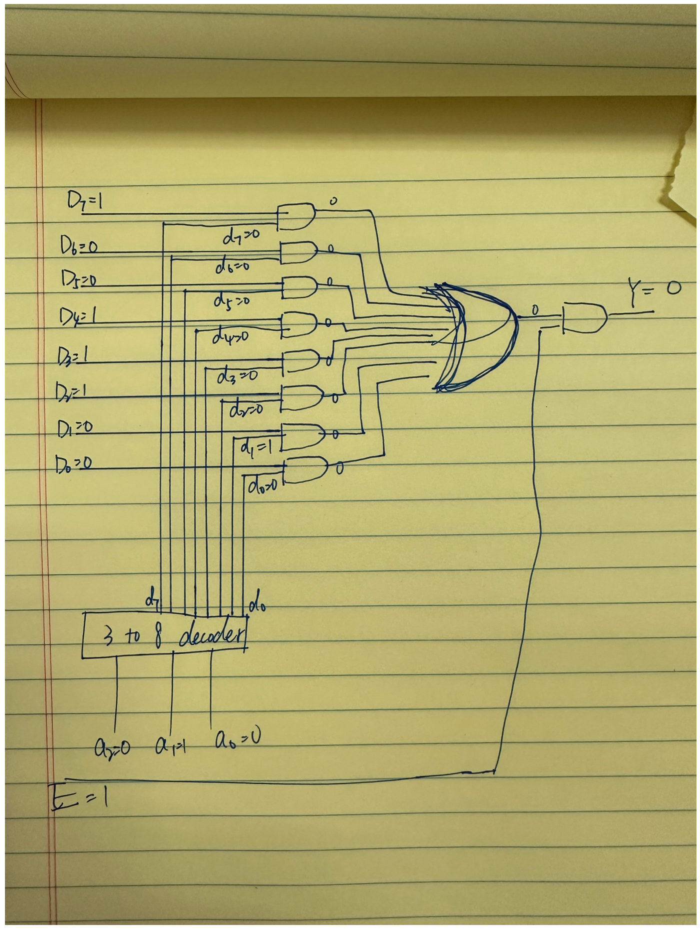
5)



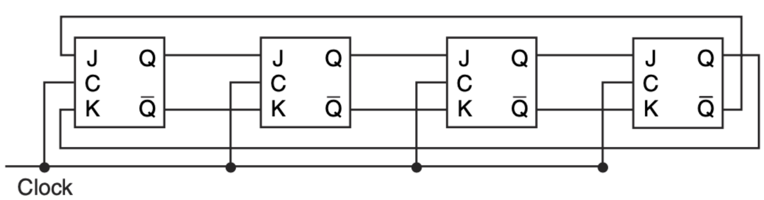
3. Draw a combinational logic circuit of an eight-input multiplexor where the inputs (D7, D6, D5, D4, D3, D2, D1, D0) are each one-bit variables. Label the values of inputs and outputs of each gate of the circuit, assuming the eight inputs have the values (1, 0, 0, 1, 1, 1, 0, 0) respectively, and assuming D1 is selected. [Note: Assume you have an 3-8 decoder to use as a black box and do not draw the decoder circuit which is part of the multiplexor.] (8 points)



(You can use this as part of your multiplexor)



4. Investigate the operation of the following circuit. Assume the initial state is 0000. Trace the outputs (the Qs) as the clock ticks and determine the purpose of the circuit. You must show your trace to complete your answer. (10 points)



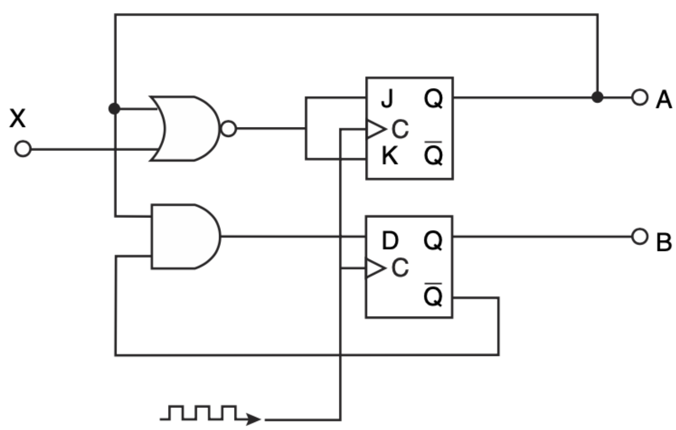
$$Q_0(t) = \overline{Q_3(t-1)}$$
$$Q_1(t) = Q_0(t-1)$$
$$Q_2(t) = Q_1(t-1)$$
$$Q_3(t) = Q_2(t-1)$$

t	$Q_3(t)$	$Q_2(t)$	$Q_1(t)$	$Q_0(t)$
0	0	0	0	0
1	0	0	0	1

2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0
8	0	0	0	0
$\ldots\ldots$	$\ldots\ldots$			
n	$Q_3(n \bmod 8)$	$Q_2(n \bmod 8)$	$Q_1(n \bmod 8)$	$Q_0(n \bmod 8)$

Purpose: 4-bit Johnson Counter (twisted ring counter) , making a "circular" or "ring" structure.

5. Complete the truth table for the following sequential circuit: (8 points)



A	B	X	Next State A	Next State B
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

A	B	X	Next State	
			A	B
0	0	0	1	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	0

1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0