

Lab5 Report

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Introduction

The fetch-decode-execute cycle, also known as the instruction cycle, is the fundamental operational process of a computer's central processing unit (CPU). During each cycle, the CPU retrieves an instruction from memory (fetch), interprets what needs to be done (decode), and performs the necessary actions to complete the instruction (execute). In this report, we analyze the fetch-decode-execute cycle for a sample ADD instruction using a simplified instruction set architecture (ISA) model.

Chosen Instruction and Initial States

Instruction: **ADD R6, R2, R6**

This instruction adds the values in registers **R2** and **R6** and stores the result in register **R6**.

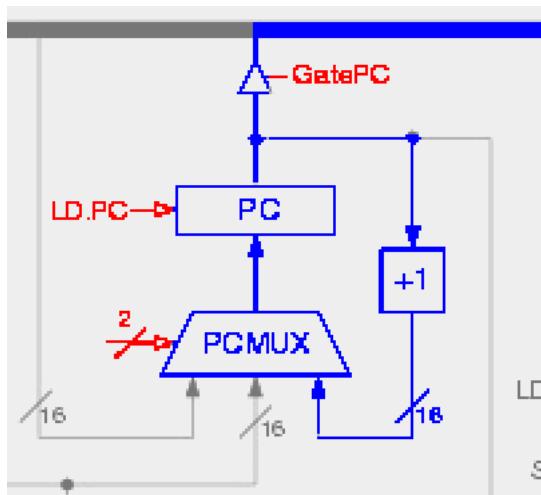
Initial Register and Memory States:

Control Registers			
PC: 3000	IR: 0000	MAR: 0000	MDR: 0000
N: 0	Z: 0	P: 0	
General Purpose Registers			
R0: 0000	R1: 0000	R2: 0000	R3: 0000
R4: 0000	R5: 0000	R6: 0000	R7: 0000

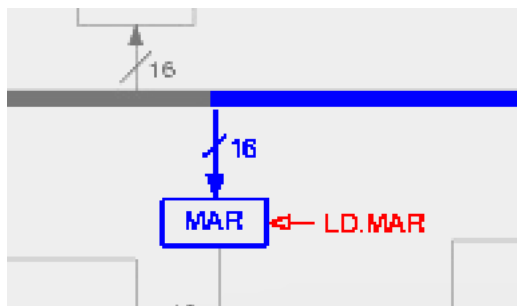
Detailed Cycle Analysis

Fetch Phase

PC becomes PC + 1

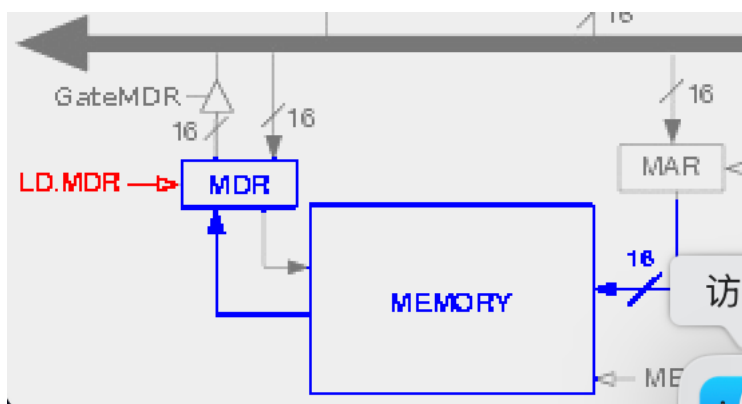


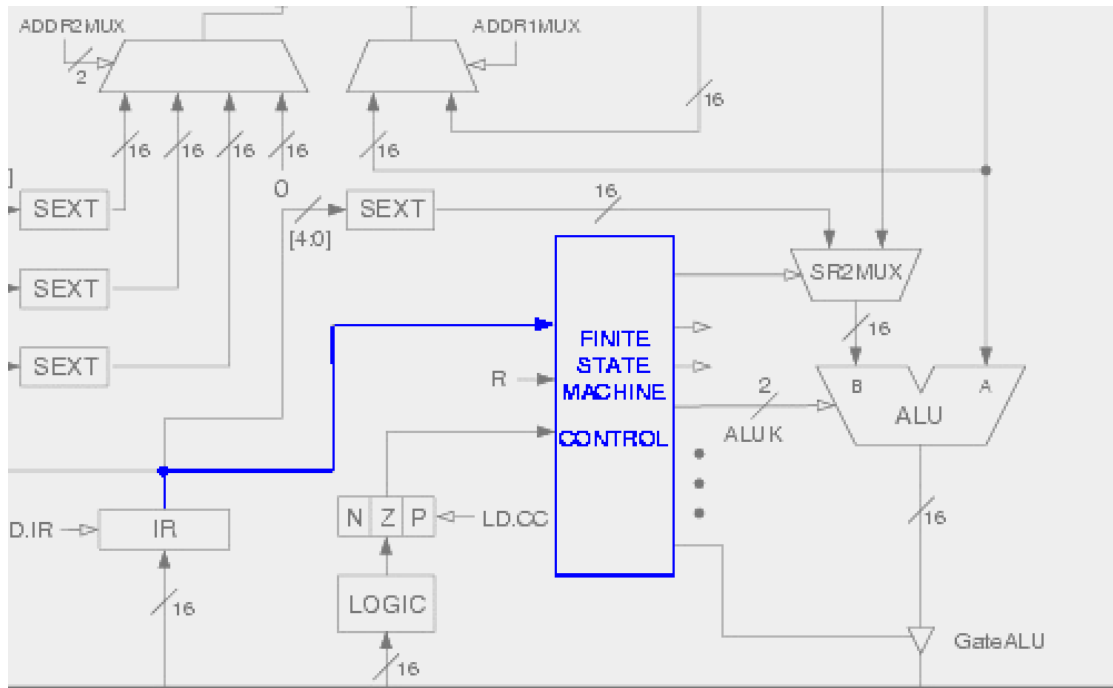
Load contents of PC into MAR, MAR become 3000



Control Registers			
PC: 3001	IR: 0000	MAR: 3000	MDR: 0000
N: 0	Z: 0	P: 0	

Send a "read" signal from MAR to memory to fetch the instruction, MDR become 1c86





Execute Phase

The ALU retrieves the values from registers R2 and R6, performs the addition ($0 + 0$), and produces the result (0), and set $Z = 1$.

Control Registers

PC: **3001**

IR: **1c86**

MAR: **3000**

MDR: **1c86**

N: **0**

Z: **1**

P: **0**

General Purpose Registers

R0: **0000**

R1: **0000**

R2: **0000**

R3: **0000**

R4: **0000**

R5: **0000**

R6: **0000**

R7: **0000**