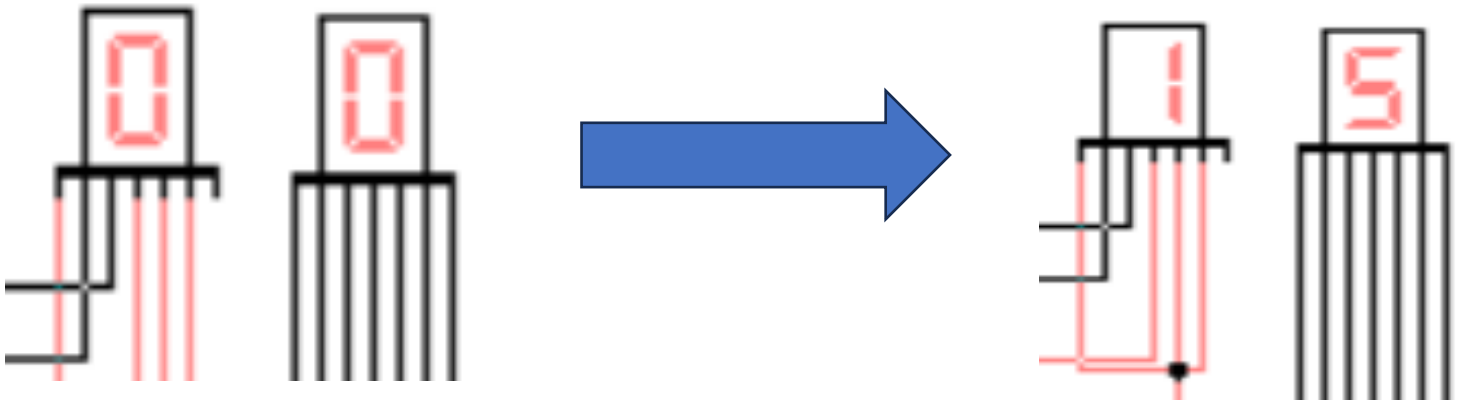
Computer Organization
Lab4
Group9

Contents

01
Design Target

Design Target

- Design a **4-bit binary counter system**
- Displays numbers ranging from 00 to 15



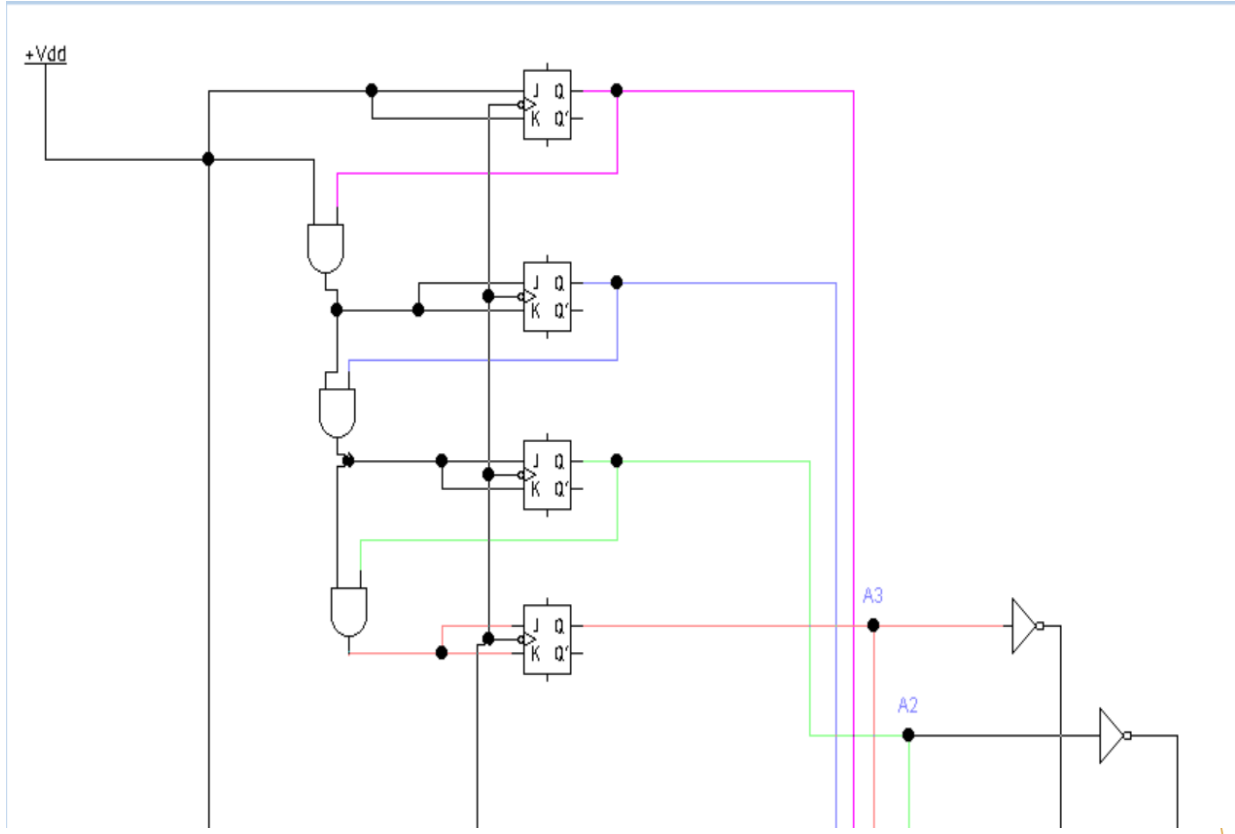
- Using **two seven-segment displays**

02

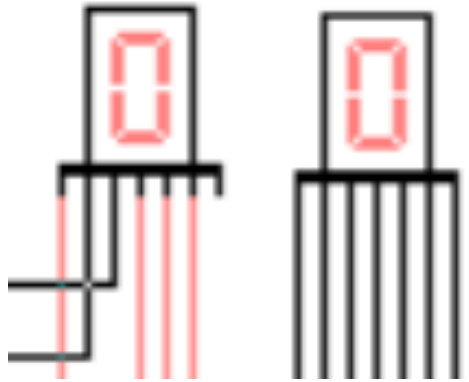
Design Progress

Key System Components —— 4-bit binary counter

- Composed of four JK flip-flops.
- Generates a 4-bit binary output (A3, A2, A1, A0), representing numbers from 0 to 15.



Key System Components —— 7-segment display



- Units Display:

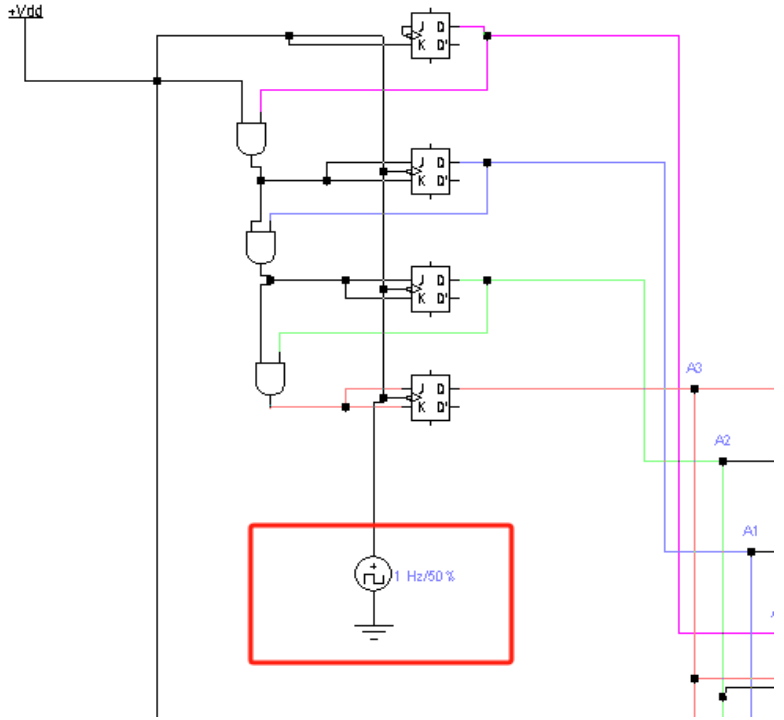
Displays values from 0 to 9 to represent the units digit of the counter value.

Driven by decoded signals (Sa, Sb, Sc, Sd, Se, Sf, Sg) generated from the 4-bit counter output (A3, A2, A1, A0).

- Tens Display:

Displays values of 0 or 1 to represent the tens digit of the counter value.

Controlled by signal N, indicating whether the current value exceeds 9.



Key System Components —— clock

we connect the output of the clock to the clock input of the counter. The counter will increase by 1 at every clock cycle.

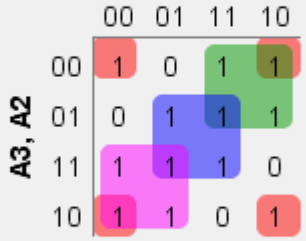
We set the clock in “1Hz/50%”, which means the frequency is 1 time/s and the duty cycle is 50%

Design Progress—— Truth Table

A3	A2	A1	A0	Sa	Sb	Sc	Sd	Se	Sf	Sg	N
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1	0
0	0	1	1	1	1	1	1	0	0	1	0
0	1	0	0	0	1	1	0	0	1	1	0
0	1	0	1	1	0	1	1	0	1	1	0
0	1	1	0	1	0	1	1	1	1	1	0
0	1	1	1	1	1	1	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	0	0	1	1	0
1	0	1	0	1	1	1	1	1	1	0	1
1	0	1	1	0	1	1	0	0	0	0	1
1	1	0	0	1	1	0	1	1	0	1	1
1	1	0	1	1	1	1	1	0	0	1	1
1	1	1	0	0	1	1	0	0	1	1	1
1	1	1	1	1	0	1	1	0	1	1	1

Design Progress—— K-Map

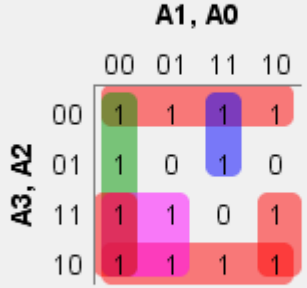
输出: Sa
格式: 积之和范式



$\overline{A2}\ \overline{A0} + \overline{A3}\ A1 + A2\ A0 + A3\ \overline{A1}$

设为表达式

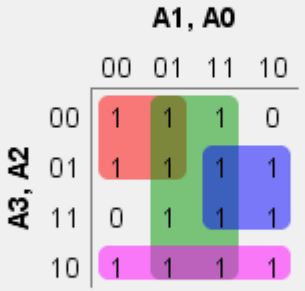
输出: Sb
格式: 积之和范式



$\overline{A2} + \overline{A1}\ \overline{A0} + \overline{A3}\ A1\ A0 + A3\ \overline{A1} + A3\ \overline{A0}$

设为表达式

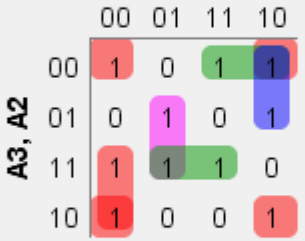
输出: Sc
格式: 积之和范式



$\overline{A3}\ \overline{A1} + A0 + A2\ A1 + A3\ \overline{A2}$

设为表达式

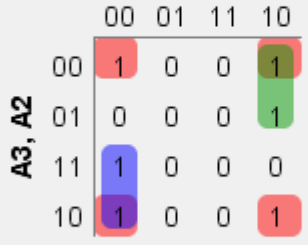
输出: Sd
格式: 积之和范式



$\overline{A2}\ \overline{A0} + \overline{A3}\ \overline{A2}\ A1 + \overline{A3}\ A1\ \overline{A0} + A2\ \overline{A1}\ A0 + A3\ \overline{A1}\ \overline{A0} + A3\ A2\ A0$

设为表达式

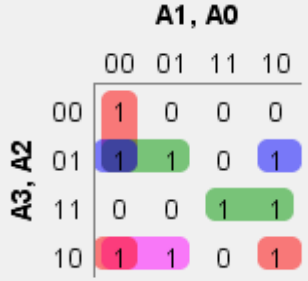
输出: Se
格式: 积之和范式



$\overline{A2}\ \overline{A0} + \overline{A3}\ A1\ \overline{A0} + A3\ \overline{A1}\ \overline{A0}$

设为表达式

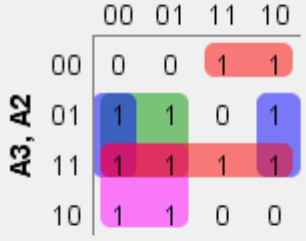
输出: Sf
格式: 积之和范式



$\overline{A3}\ \overline{A1}\ \overline{A0} + \overline{A3}\ A2\ \overline{A1} + A3\ \overline{A2}\ A0 + A3\ \overline{A2}\ \overline{A1} + A3\ A2\ \overline{A0} + A3\ A2\ A1$

设为表达式

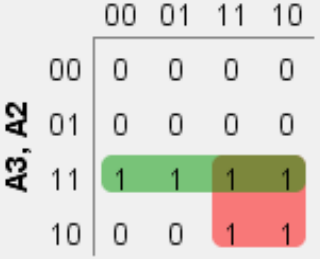
输出: Sg
格式: 积之和范式



$\overline{A3}\ \overline{A2}\ A1 + A2\ \overline{A1} + A2\ A0 + A3\ \overline{A1} + A3\ A2$

设为表达式

输出: M
格式: 积之和范式



$A3\ A1 + A3\ A2$

设为表达式

Design Progress—— Truth Table

N	Sa	Sb	Sc	Sd	Se	Sf	Sg
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0

Thank you