Objective of the Lab/Program

Implement the half adder using VHDL/Verilog.

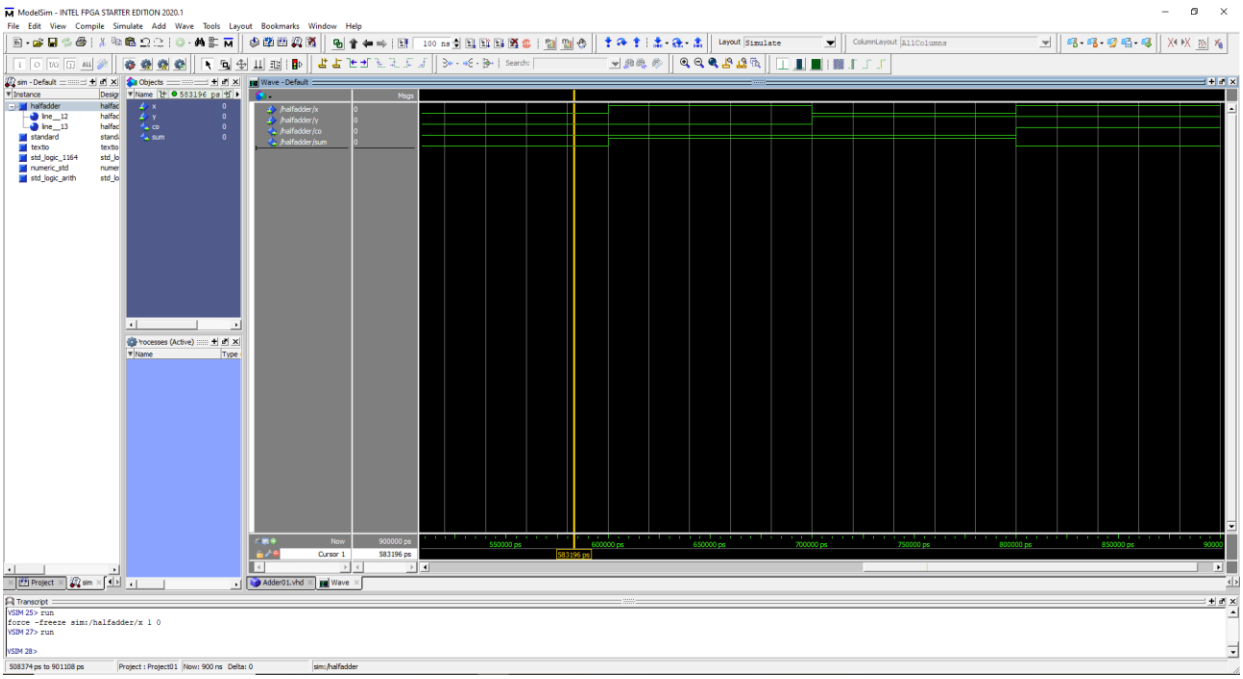
VHDL Source Code

```
library ieee; --Pre processor directives
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.std_logic_arith.all;

entity halfadder is --Defines the variables and return values
port(x,y:in bit; co,sum:out bit);
end halfadder;

architecture simple of halfadder is --how the entity behaves
begin
        sum <= (x xor y);
        co <= (x and y);
end simple;
```

Screen shot of the simulation (waveforms)



Conclusion and References

The program runs after defining the function named “halfadder”. Each change in wave form is representative of changing each variable from 0 to 1.