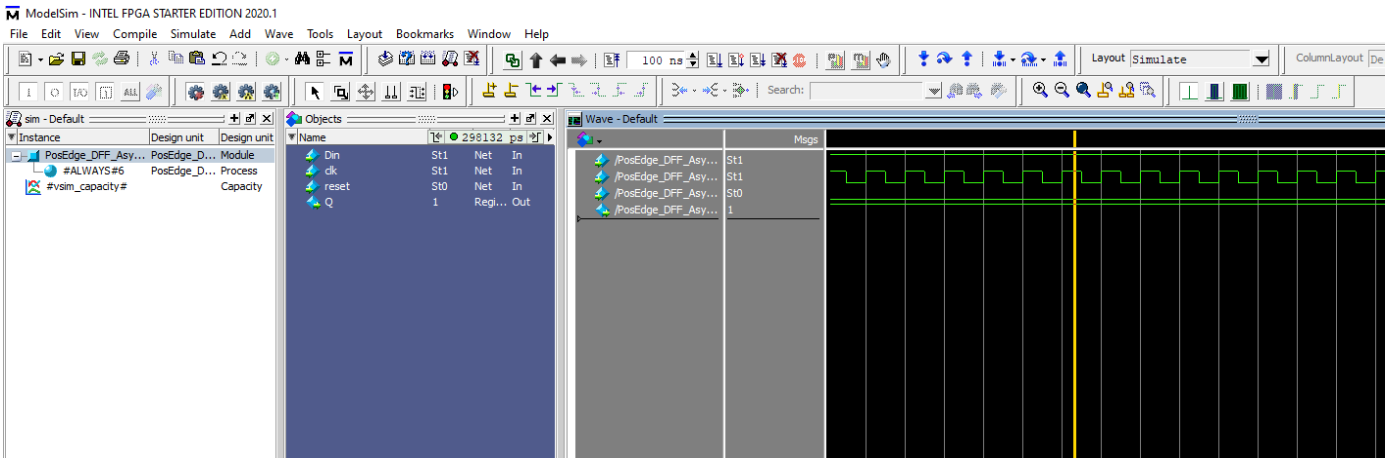
Objective of the Lab/Program

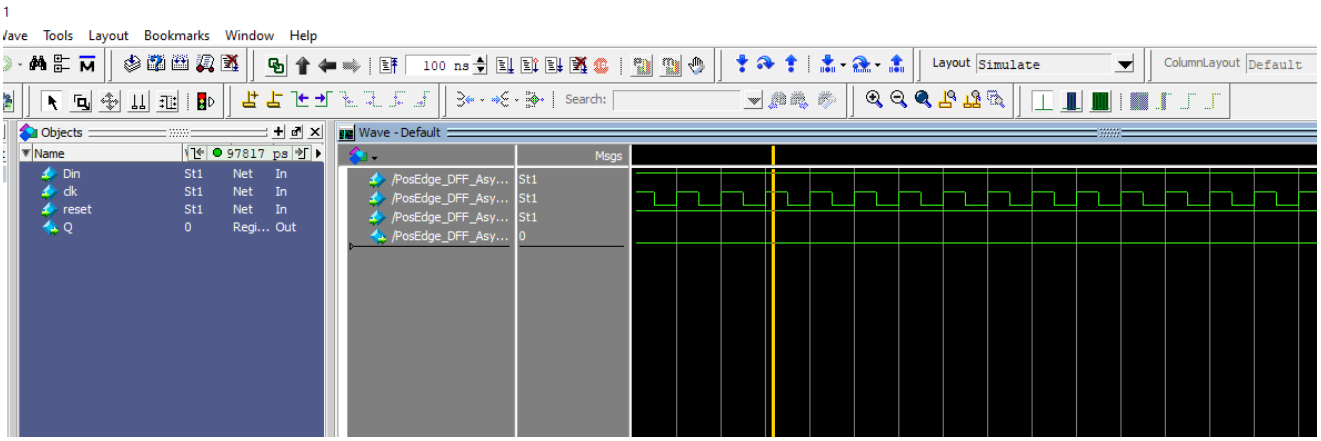
Design and Implement the positive edge triggered D flip flop with RESET signal using HDL Verilog. When RESET=1 the flip flop should be cleared. When RESET=0 the flip flop should store the input. The output follows the input when CLOCK is 1.

VHDL Source Codes

```
module PosEdge_DFF_AsyncReset(Din, clk, reset, Q);
input Din; //Data input signal
input clk; //clock input
input reset; //asynchronous reset high level - high priority
output reg Q; //output Q
always @(posedge clk or posedge reset)
begin
 if(reset==1'b1) //binary of vector one
 Q <= 1'b0;
 else
 Q <= Din;
end
endmodule
```

Screen shot of the simulation (waveforms) showing the results for the flip flop operation when RESET=0 and when RESET=1





Conclusion and References

Using Verilog had dramatically made it easier to create the D flip-flop. Only requiring one conditional statement after defining the variables. Afterwards the simulation had shown to work as intended.