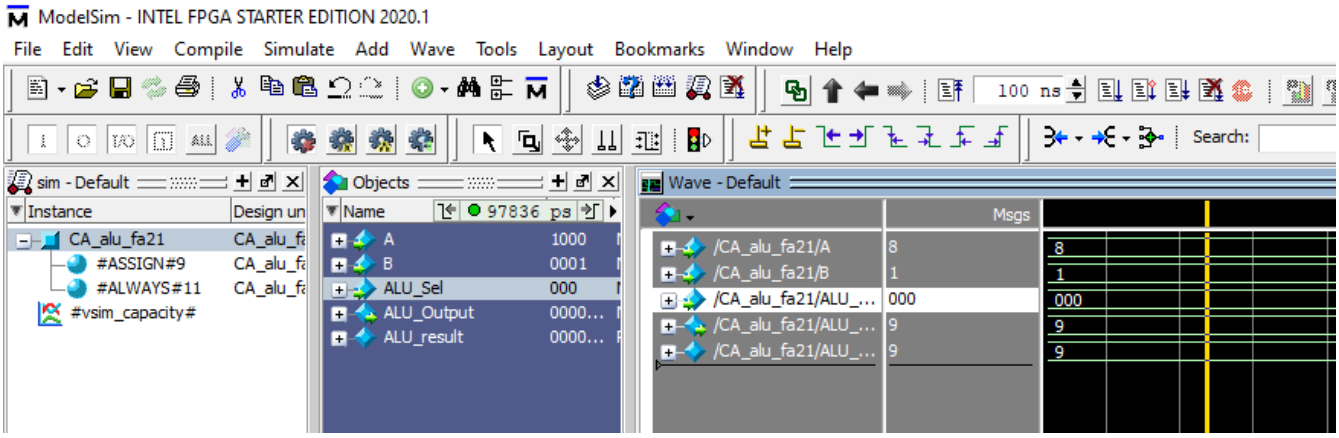
Objective of the Lab/Program

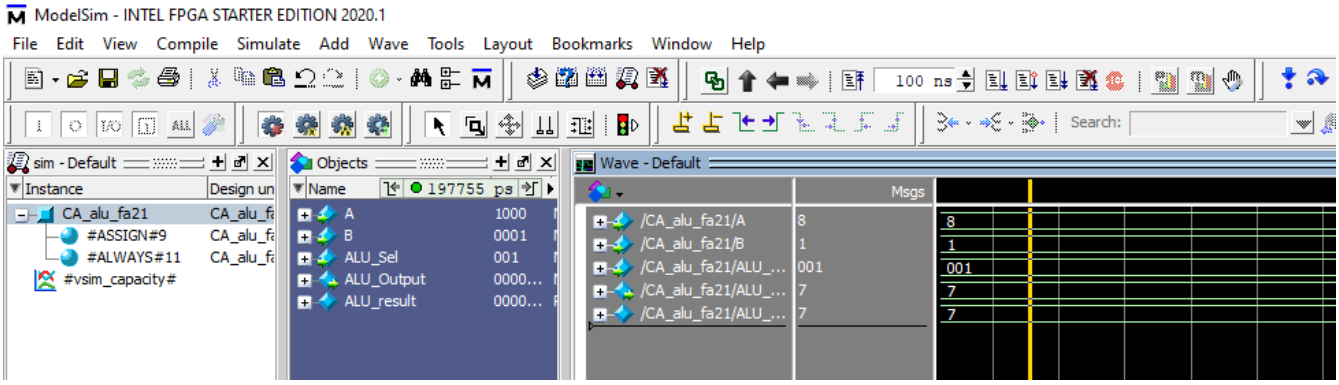
Implement the ALU using Verilog HDL. This ALU will perform seven different function, add, subtract, multiply, logical XOR, logical OR, logical AND, equals and greater than.

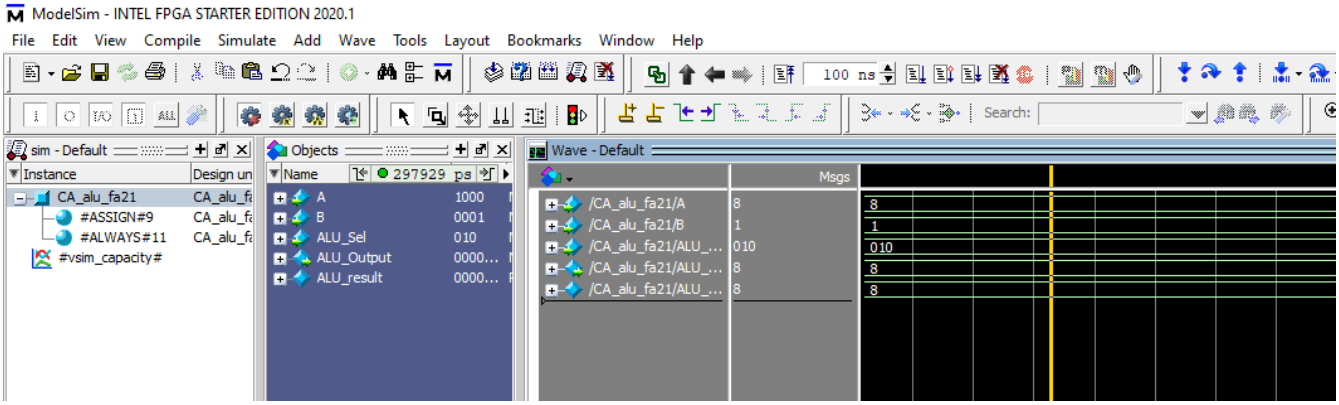
VHDL Source Code with the completed fill in the blanks

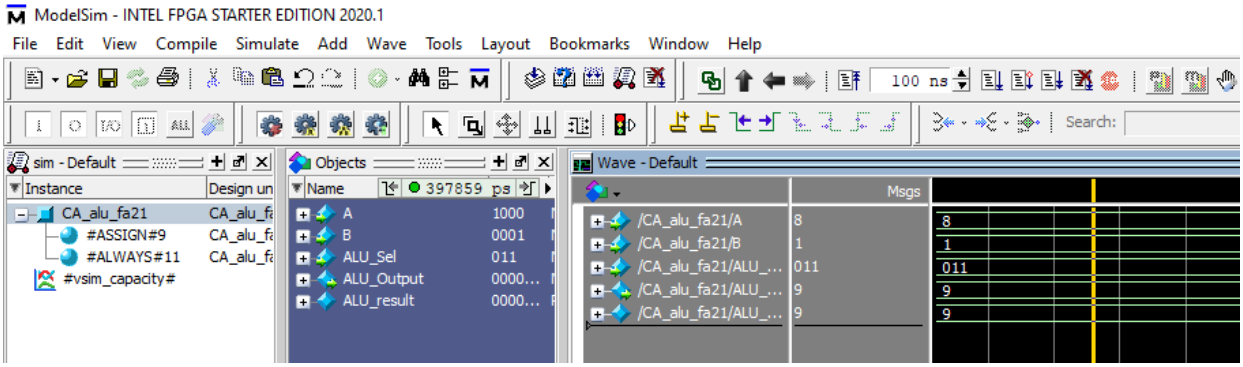
```
//ALU - Arithmetic Logic Unit similar to covered in theory

module CA_alu_fa21(
	input [3:0] A,B, //Inputs 4 bits
	input [2:0] ALU_Sel, //Select lines 3
	output [7:0] ALU_Output //8-bit Output
);
reg[7:0] ALU_result;
assign ALU_Output = ALU_result; //ALU out

always @(*)
begin
	case(ALU_Sel)
	3'b000: //Addition
	 ALU_result = A+B;
	3'b001: //Substraction
	 ALU_result = A-B;
	3'b010: //Multiplication
	 ALU_result = A*B;
	3'b011: //OR
	 ALU_result = A | B;
	3'b100: //AND
	 ALU_result = A & B;
	3'b101: //XOR
	 ALU_result = A ^ B;
	3'b110: //Equal
	 ALU_result = (A==B)?8'd1:8'd0;
	3'b111: //Greater than
	 ALU_result = (A>B)?8'd1:8'd0;
	default: ALU_result = 8'b0;

	endcase
end
endmodule
```

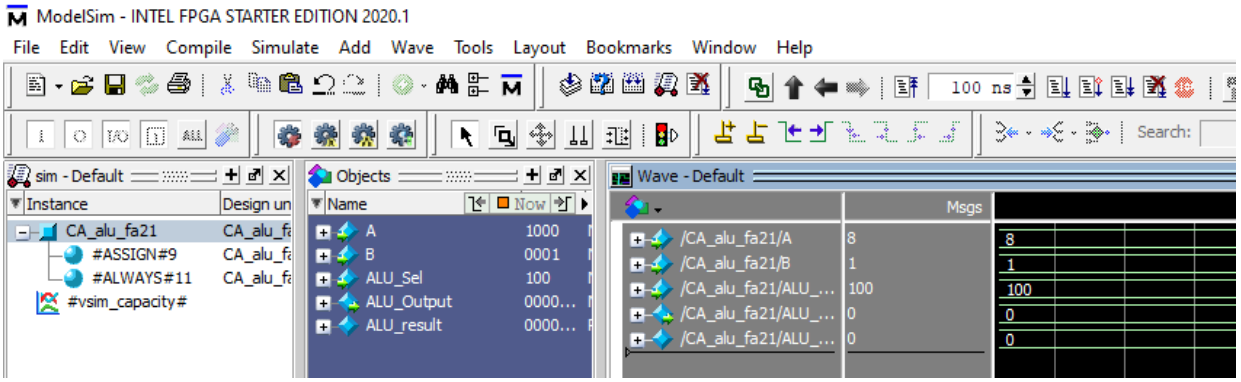
Screen shot of the simulation (waveforms) showing the results for the ALU operation for all cases

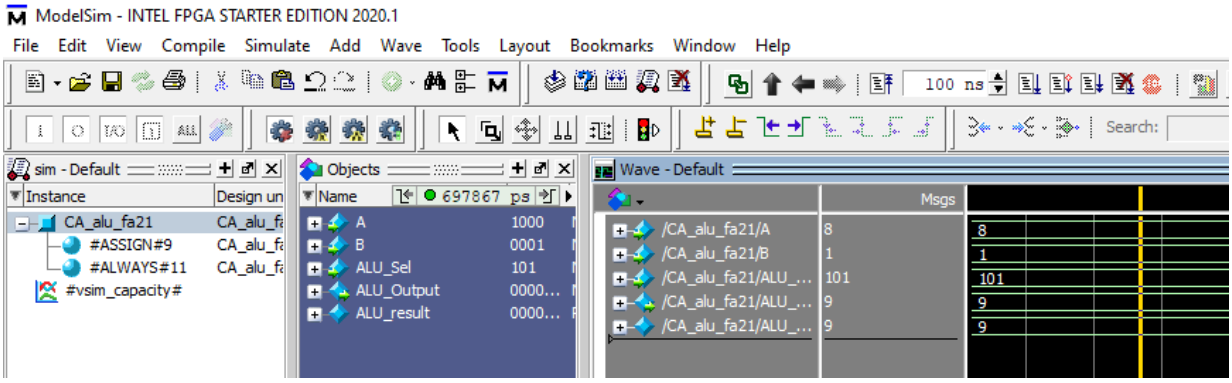


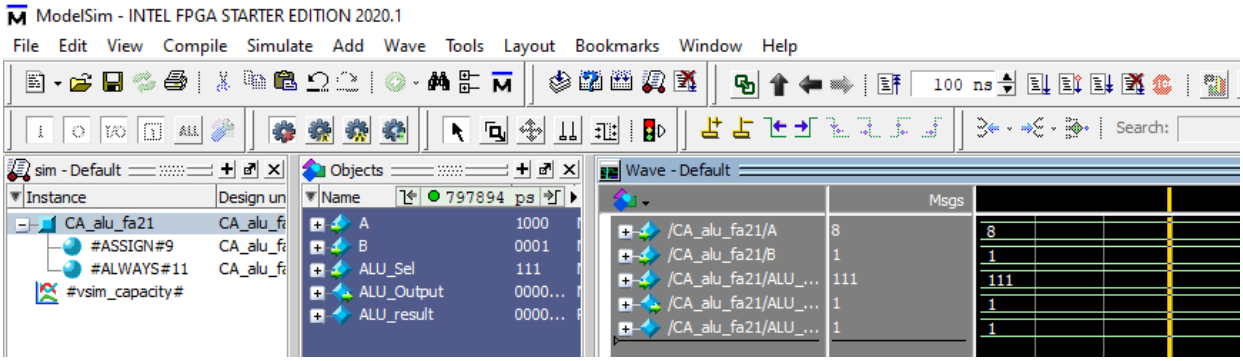





ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
CA_alu_fa21
#ASSIGN#9
#ALWAYS#11
#vsim_capacity#
Objects
Name
A 1000
B 0001
ALU_Sel 011
ALU_Output 0000...
ALU_result 0000...
Wave - Default
Msgs
/CA_alu_fa21/A 8
/CA_alu_fa21/B 1
/CA_alu_fa21/ALU_... 011
/CA_alu_fa21/ALU_... 9
/CA_alu_fa21/ALU_... 9


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
CA_alu_fa21
#ASSIGN#9
#ALWAYS#11
#vsim_capacity#
Objects
Name
A 1000
B 0001
ALU_Sel 100
ALU_Output 0000...
ALU_result 0000...
Wave - Default
Msgs
/CA_alu_fa21/A 8
/CA_alu_fa21/B 1
/CA_alu_fa21/ALU_... 100
/CA_alu_fa21/ALU_... 0
/CA_alu_fa21/ALU_... 0


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
CA_alu_fa21
#ASSIGN#9
#ALWAYS#11
#vsim_capacity#
Objects
Name
A 1000
B 0001
ALU_Sel 101
ALU_Output 0000...
ALU_result 0000...
Wave - Default
Msgs
/CA_alu_fa21/A 8
/CA_alu_fa21/B 1
/CA_alu_fa21/ALU_... 101
/CA_alu_fa21/ALU_... 9
/CA_alu_fa21/ALU_... 9


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
CA_alu_fa21
#ASSIGN#9
#ALWAYS#11
#vsim_capacity#
Objects
Name
A 1000
B 0001
ALU_Sel 111
ALU_Output 0000...
ALU_result 0000...
Wave - Default
Msgs
/CA_alu_fa21/A 8
/CA_alu_fa21/B 1
/CA_alu_fa21/ALU_... 111
/CA_alu_fa21/ALU_... 1
/CA_alu_fa21/ALU_... 1

Conclusion and References

After defining the different cases using a switch statement the ALU was able to output each operation correctly.