EE 2EI4 - Electronic Devices and Circuit I
Project IV

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Section 2A - Circuit Schematic

The circuit schematic that I used for this design utilized a total of 12 MOSFETS, 6 of which being PMos, and 6 of which being NMos. The below figures show the implementation of the XOR gate in CMOS, as well as the schematic which was used to implement an inverter. To derive the form of the PDN, I applied DeMorgan's theorem, and developed a boolean expression for XOR in that format that we saw in class…

$$Y = A \oplus B = \overline{A}B + \overline{B}A = \overline{\overline{\overline{A}B + \overline{B}A}} = \overline{\overline{\overline{A}B} + \overline{\overline{B}A}} = \overline{(A + \overline{B}) \cdot (B + \overline{A})} = \overline{AB + \overline{AB}}$$

Thus, our pull down network would consists of A in series with B, all in parallel with $\overline{A}$ in series with $\overline{B}$. We can then mirror this setup in the PUN, and develop the finalized circuit for the XOR gate.

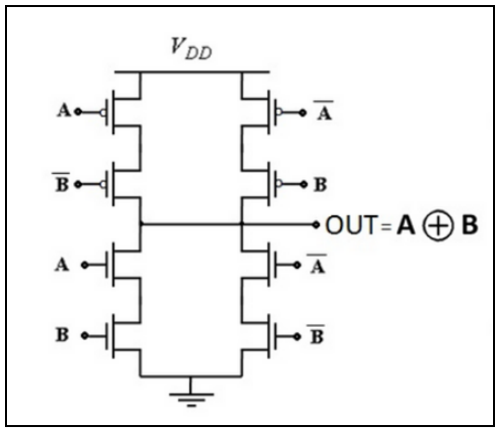


Figure 1: CMOS XOR gate

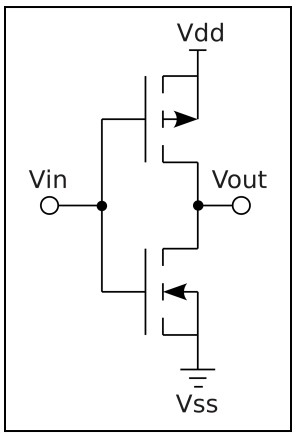


Figure 2: CMOS Inverter

The XOR gate employs 6 MOSFETS, however each input requiring an inversion requires 2 gates, thus the total circuit requires 12 MOSFETS.

Section 2B - Ideal Sizing

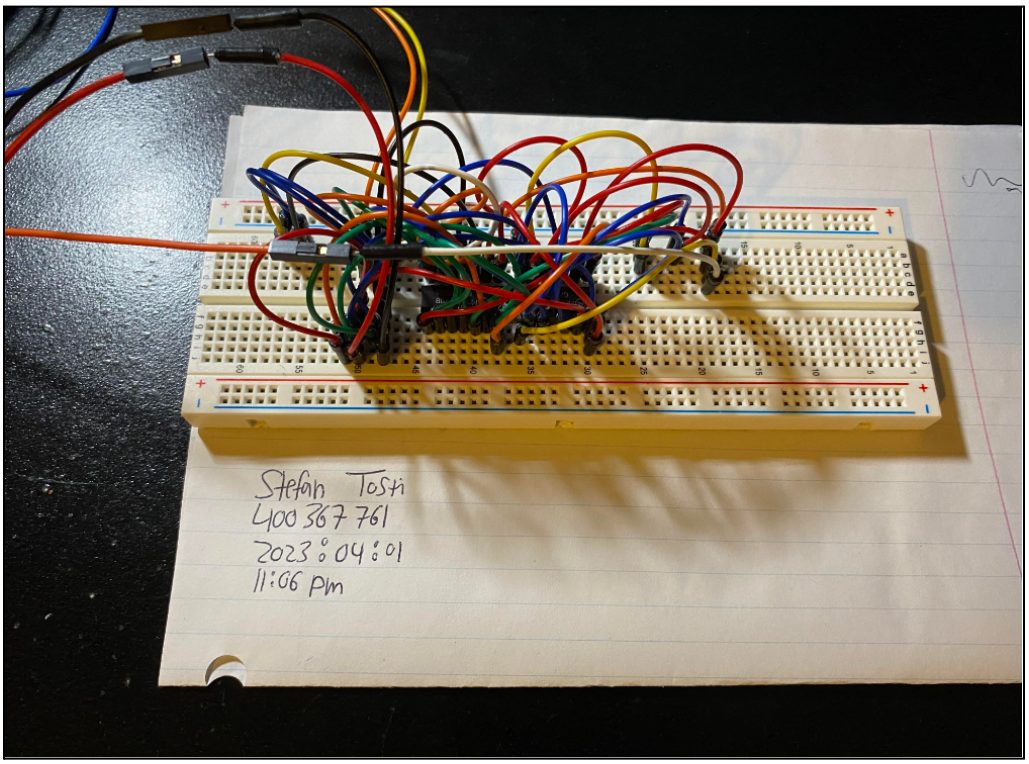
We know that the average sizing for a PMOS is $\left(\frac{W}{L}\right)_P = \frac{5}{1}$ and for an NMOS is $\left(\frac{W}{L}\right)_N = \frac{2}{1}$.

From the circuit schematic above, we can see that the longest path in both the pullup network, and the pull down network go through 2 MOSFETs. This means that R_{eq} for the total path will be $\frac{n}{2}$ (for the pull down case) and $\frac{p}{2}$ (for the pull up case). The ratio of PUN to PDN for the fastest switching time requires them to be symmetric. This ensures the time delays for both networks are the same. So the ratio is 1:1.We know that R is inversely proportional to sizing, which tells us that the sizing of each P and N mosfet should be double of that of the reference inverter. Using these two metrics, we can determine that the ideal sizing ratio between the 2 mosfet types should be, $\frac{2*PMOS}{2*NMOS} = \frac{5}{2} = 2.5$

Section 2C - Feasibility of Ideal Sizing

In this circuit, we can see that the longest path from VDD to GND has to pass through a total of 2 PMOSfets and 2 NMOSfets. This tells us that the sizing for this circuit should be $\frac{2\times PMOS}{2\times NMOS} = \frac{5}{2} = 2.5$. This is exactly the same as the ideal value that we calculated in the previous step, and thus it will be feasible to implement this sizing. For this circuit, I also believe that the symmetry of the design will play a role in the feasibility of ideal sizing implementation.

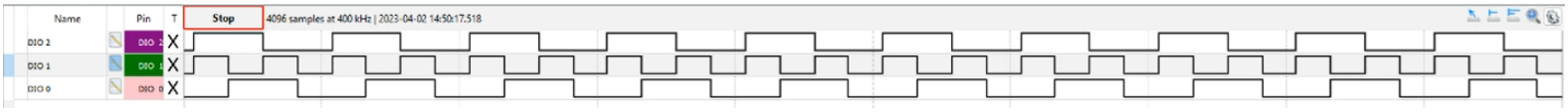
Built Circuit in Real Life



Section 2A - Functional Testing

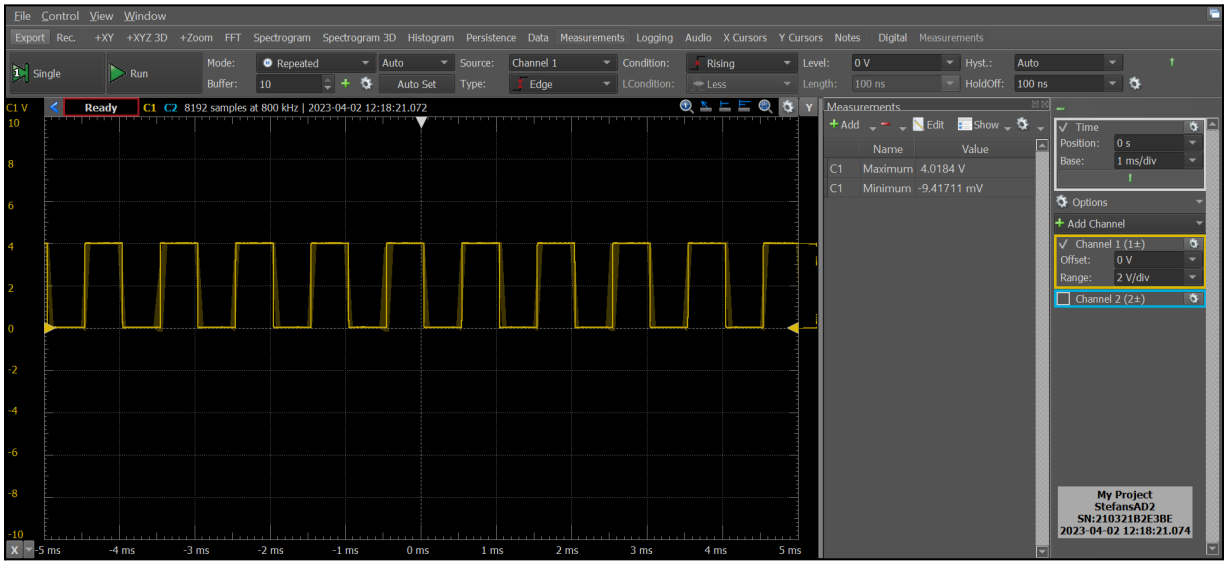
The figure to the right depicts the output of the functional testing with the AD2, via the integrated Digital IO pins. We can verify the truth table by seeing at the corresponding output to various input combinations.

DIO 0	DIO 1	DIO 2
0	0	0
0	1	1
1	0	1
1	1	0

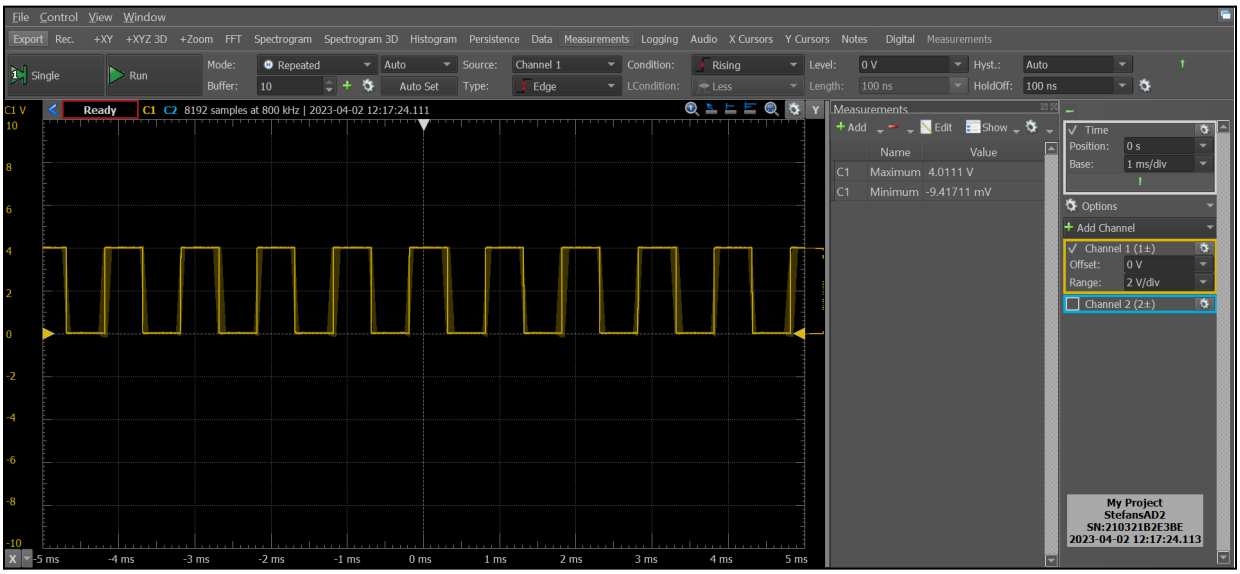


Section 2B - Static Level Testing

The first generated graph used the input A and 5V, and input B as a square wave between 0V and 5V



The second generated graph used the input B as 5V, and input A as a square wave between 0V and 5V



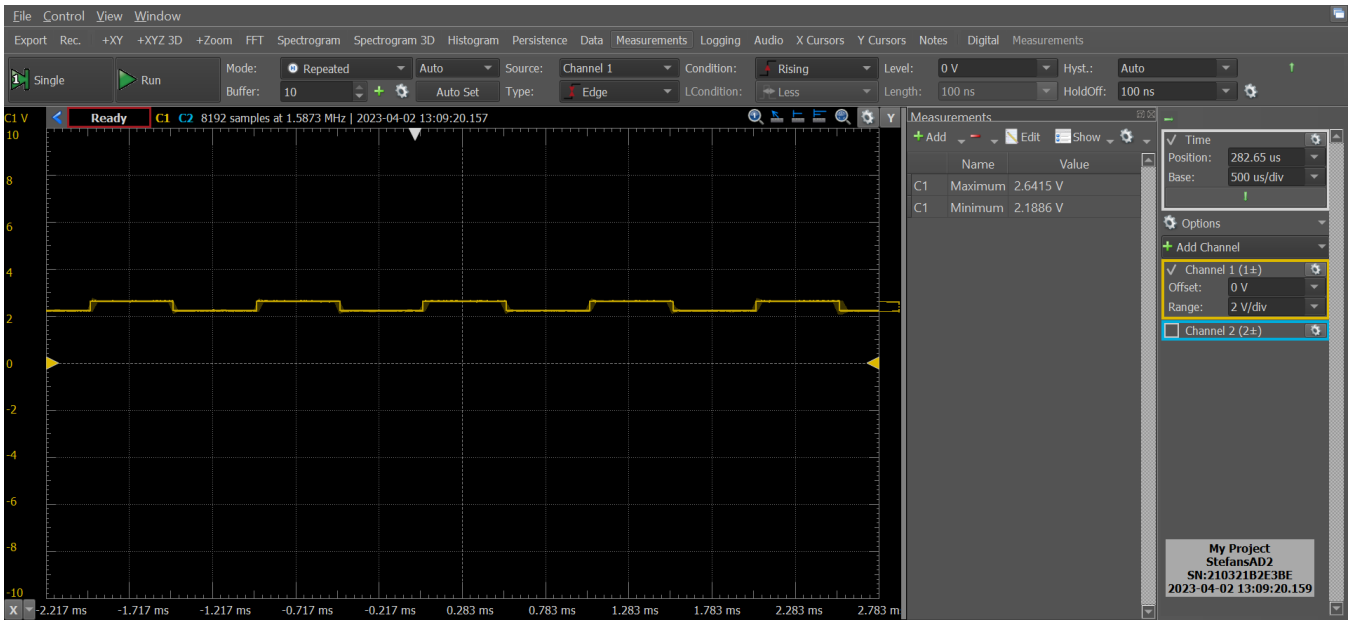
The two graphs have…

$V_L = -9.41mV$

$V_H = 4.01V$

These measurements stay relatively consistent throughout the two graphs. There is a 0.0073V difference in the values of V_H

Section 2B - Dynamic Level Testing

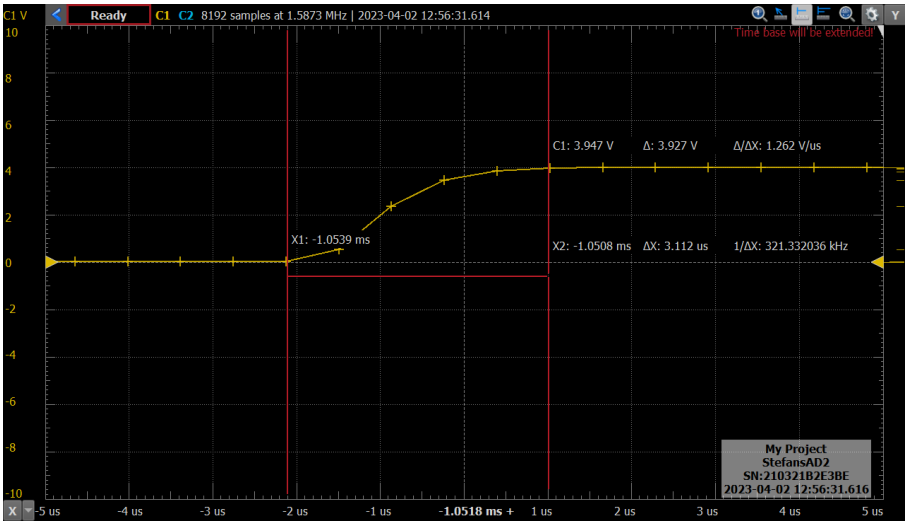


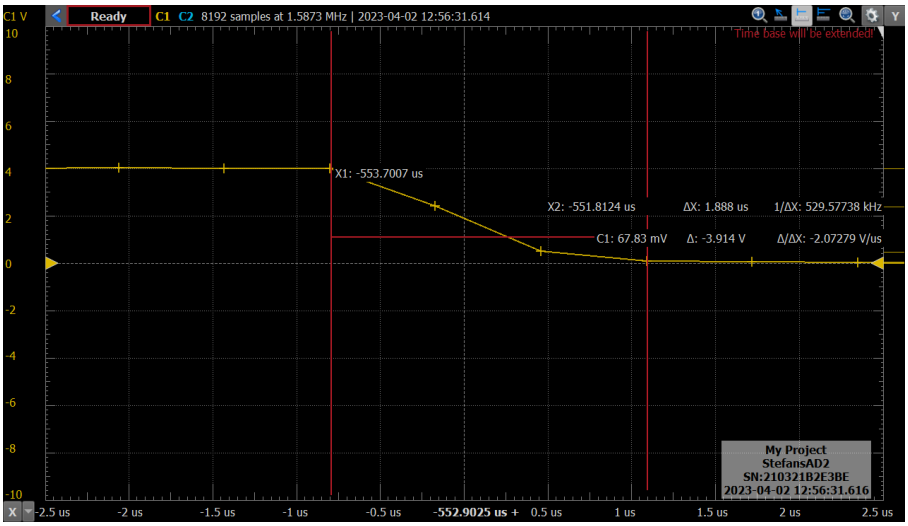
From above, it can be seen that…

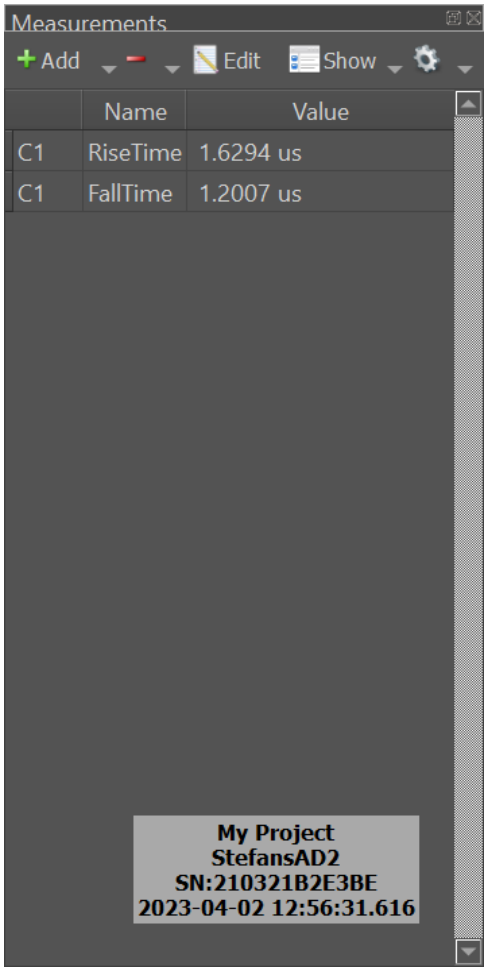
$V_{IH} = 2.6415V$

$V_{Il} = 2.1886V$

Section 3Ai - Fall time and Rise Time







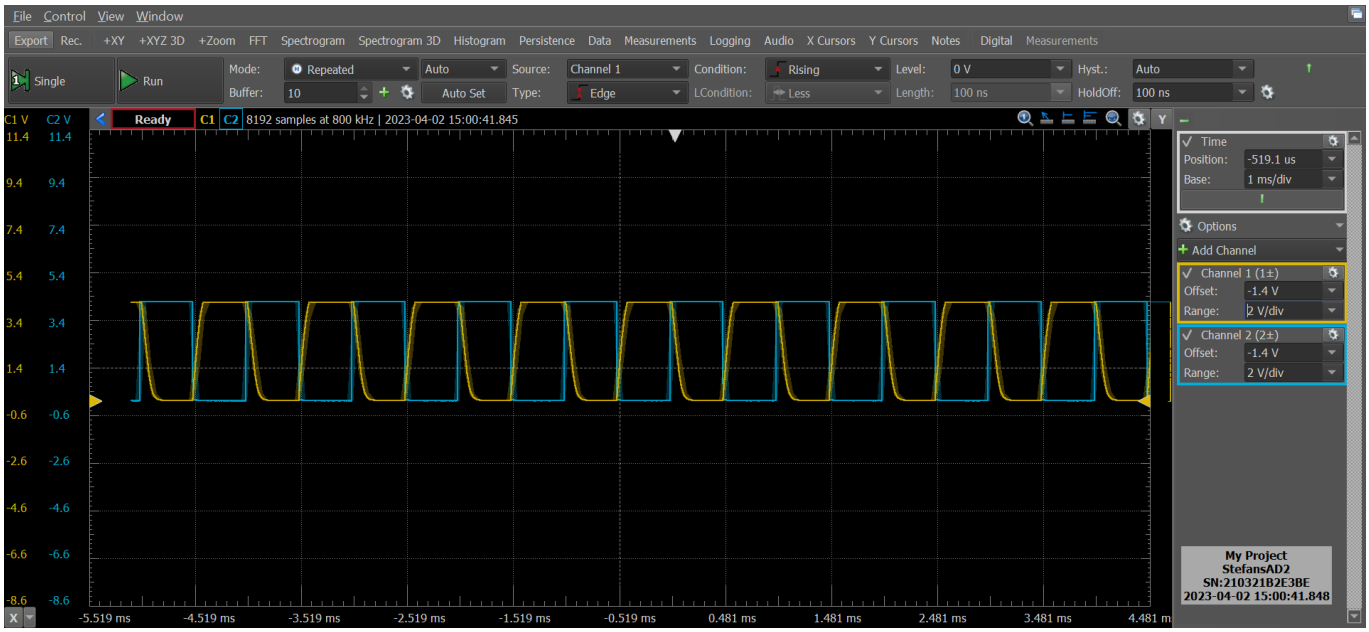
The rise and fall times were determined by using the AD2 cursors to measure the time it takes for the output of the XOR gate to get from 10% of its maximum range to 90% of its maximum range, and vice versa.

As can be seen, the determined rise and fall times were…

$Output\ Rise\ Time\ =\ 1.6294\ uS$

$Output\ Fall\ Time\ =\ 1.2007\ uS$

Section 3Aii - Time constant Parameters



To measure τ_{phl} and τ_{plh} I first graphed the input square waveform with channel 2, and then graphed the output of the XOR gate with channel 1. Then, to measure τ_{phl} I used the AD2 cursors to measure the amount of time that it took between the input waveform going high, to the output of the XOR gate getting to 50% of its total range. Similarly, in order to find τ_{plh} I measured the amount of time between the input waveform going low, and the output of the XOR gate getting to 50% of its total range.

$\tau_{phl} = 167\ nS$

$\tau_{plh} = 38\ nS$

$\tau_{p} = \frac{167 + 38}{2} = 102.5\ nS$