Electronic Devices & Circuits II - EE 3EJ4
Lab #2

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Stefan Tosti - Tostis - 400367761 - L08

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Questions for Part 1

Question 1 (10 points)

Part A

Step 1.2

$V_{o,min} = -\ 3\ V$

$I_o = 0.0001848\ mA$

Step 1.10

$V_{o,min} = -\ 3\ V$

$I_o = 0.0002022\ mA$

Part B

Step 1.2

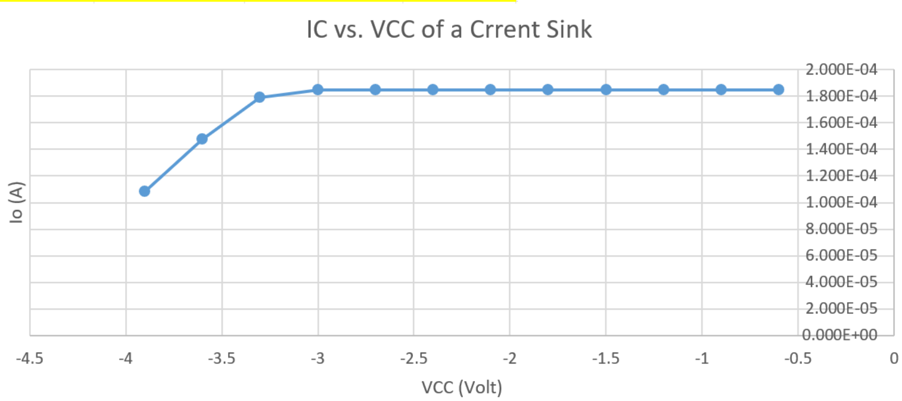
$R_o = [7.50\times10^7,\ 7.69\times10^7]$

Step 1.10

$R_o = [-\ 8.23\times10^6,\ 2.47\times10^7]$

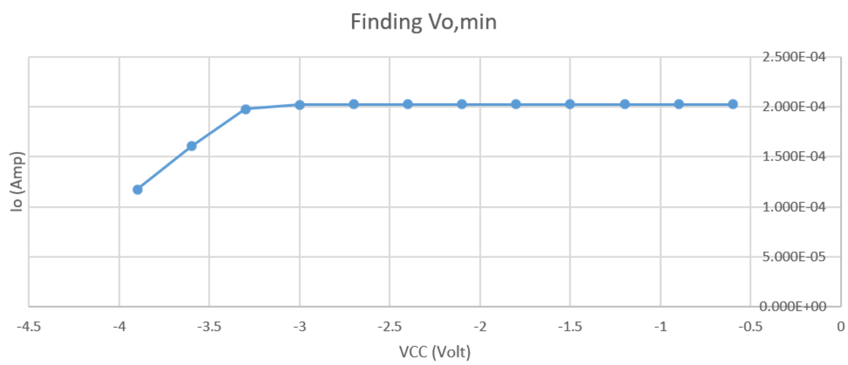
The simulated data can be found as follows…

VCC	IC	VE	Ro
Volts	Amps	Volts	Ohm
-3.9	1.083E-04	-3.98E+00	7.60E+03
-3.6	1.477E-04	-3.73E+00	9.64E+03
-3.3	1.788E-04	-3.53E+00	5.02E+04
-3	1.848E-04	-3.49E+00	7.19E+06
-2.7	1.848E-04	-3.49E+00	7.50E+07
-2.4	1.848E-04	-3.49E+00	7.50E+07
-2.1	1.849E-04	-3.49E+00	7.69E+07
-1.8	1.849E-04	-3.49E+00	7.50E+07
-1.5	1.849E-04	-3.49E+00	7.69E+07
-1.2	1.849E-04	-3.49E+00	7.69E+07
-0.9	1.849E-04	-3.49E+00	7.69E+07
-0.6	1.849E-04	-3.49E+00	-3.25E+03



The measured data can be found as follows…

VCC	VEE	CH1 (VB)	CH2 (VE)	IR1	IR2	IB = IR1 - IR2	IE	IC = IE - IB	Ro
Volts	Volts	Volts	Volts	Amps	Amps	Amps	Amps	Amps	Ohm
-3.9	-5	-3.338	-3.9366	4.35E-05	2.88542E-05	1.46094E-05	0.000131935	1.173E-04	6.92E+03
-3.6	-5	-3.0578	-3.656	3.98E-05	3.37188E-05	6.09635E-06	0.000166749	1.607E-04	8.10E+03
-3.3	-5	-2.8184	-3.416	3.67E-05	3.7875E-05	-1.17708E-06	0.000196526	1.977E-04	6.62E+04
-3	-5	-2.7884	-3.3868	3.63E-05	3.83958E-05	-2.08854E-06	0.000200149	2.022E-04	3.48E+06
-2.7	-5	-2.7872	-3.3864	3.63E-05	3.84167E-05	-0.000002125	0.000200199	2.023E-04	9.55E+06
-2.4	-5	-2.7878	-3.386	3.63E-05	3.84063E-05	-2.10677E-06	0.000200248	2.024E-04	2.47E+07
-2.1	-5	-2.7874	-3.386	3.63E-05	3.84132E-05	-2.11892E-06	0.000200248	2.024E-04	-8.23E+06
-1.8	-5	-2.7886	-3.386	3.63E-05	3.83924E-05	-2.08247E-06	0.000200248	2.023E-04	6.89E+06
-1.5	-5	-2.7888	-3.3856	3.63E-05	3.83889E-05	-2.07639E-06	0.000200298	2.024E-04	3.04E+06
-1.2	-5	-2.788	-3.385	3.63E-05	3.84028E-05	-2.10069E-06	0.000200372	2.025E-04	2.55E+06
-0.9	-5	-2.7874	-3.3842	3.63E-05	3.84132E-05	-2.11892E-06	0.000200471	2.026E-04	5.44E+06
-0.6	-5	-2.7864	-3.384	3.63E-05	3.84306E-05	-2.14931E-06	0.000200496	2.026E-04	



Question 2 (10 points)

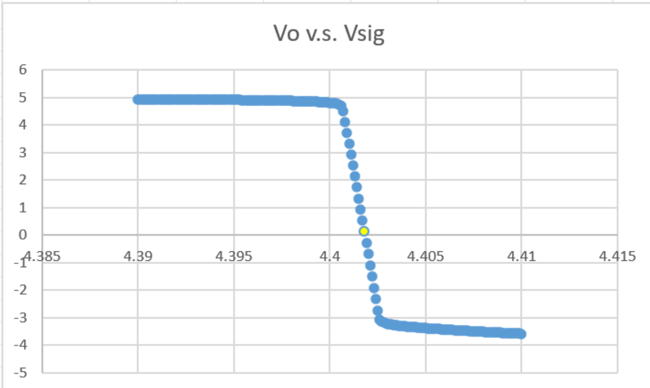
$V_{01} = 4.9403\, V$

$V_{02} =- 3.578\, V$

In the above case scenarios, the value of V_{sig} is outside of the voltage range in which our circuit functions as an amplifier - this means that the corresponding outputs, V_{01} & V_{02} are close to the maximum and minimum outputs of the circuit.

Question 3 (15 Points)

Part 1



Part 2

$Required\ Range\ for\ V_{sig} = [4.4006\ V,\ 4.4028\ V]$

$Output\ voltage\ range\ for\ V_o = [4.6895\ V,\ \ -3.175\ V]$

Part 3

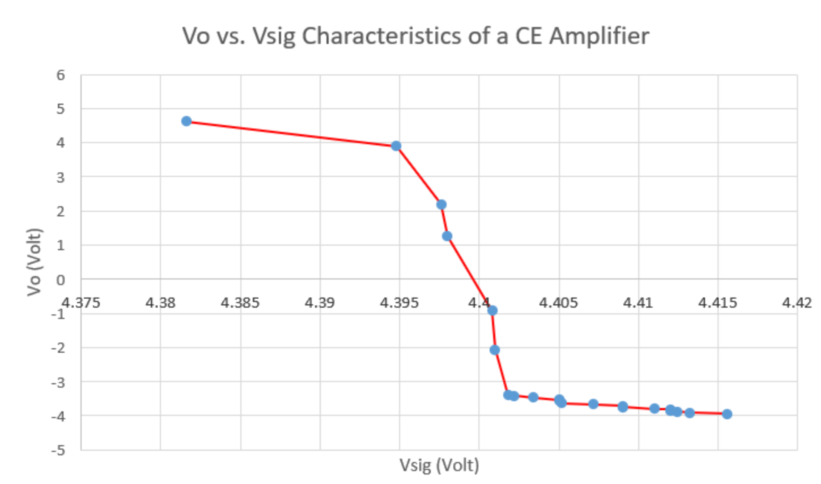
$V_{sig} = 4.4018\ V$

$V_o = 0.124312\ V$

$I_{C2} = 0.0001866\ A$

Part 4

The plot of V_o *v.s.* V_{sig} *as well as the corresponding data can be found as follows…*



W1 Setting	Channel 1 (Vsig, W1)	Channel 2 (Vo)
Volts	Volts	Volts
4.38	4.3816	4.6312
4.381	4.3948	3.8988
4.382	4.3976	2.194
4.383	4.398	1.2564
4.384	4.4008	-0.9154
4.385	4.401	-2.0598
4.386	4.4018	-3.3746
4.387	4.4022	-3.4226
4.388	4.4034	-3.4656
4.389	4.405	-3.5364
4.39	4.405	-3.5694
4.391	4.4052	-3.6314
4.392	4.4072	-3.6618
4.393	4.409	-3.7158
4.394	4.409	-3.742
4.395	4.411	-3.791
4.396	4.412	-3.8148
4.397	4.412	-3.8386
4.398	4.4124	-3.8824
4.399	4.4132	-3.9046
4.4	4.4156	-3.946

The measured value for $V_{BQ2} = 4.384\ V$

Question 4 (10 Points)

Part 1

For low frequencies…

$$A_{vo} = 20log(\frac{V_o}{V_i}) = 20log(\frac{4.047}{0.002}) = 66dB$$

$$Phase = 179.6°$$

In the upper 3-dB range…

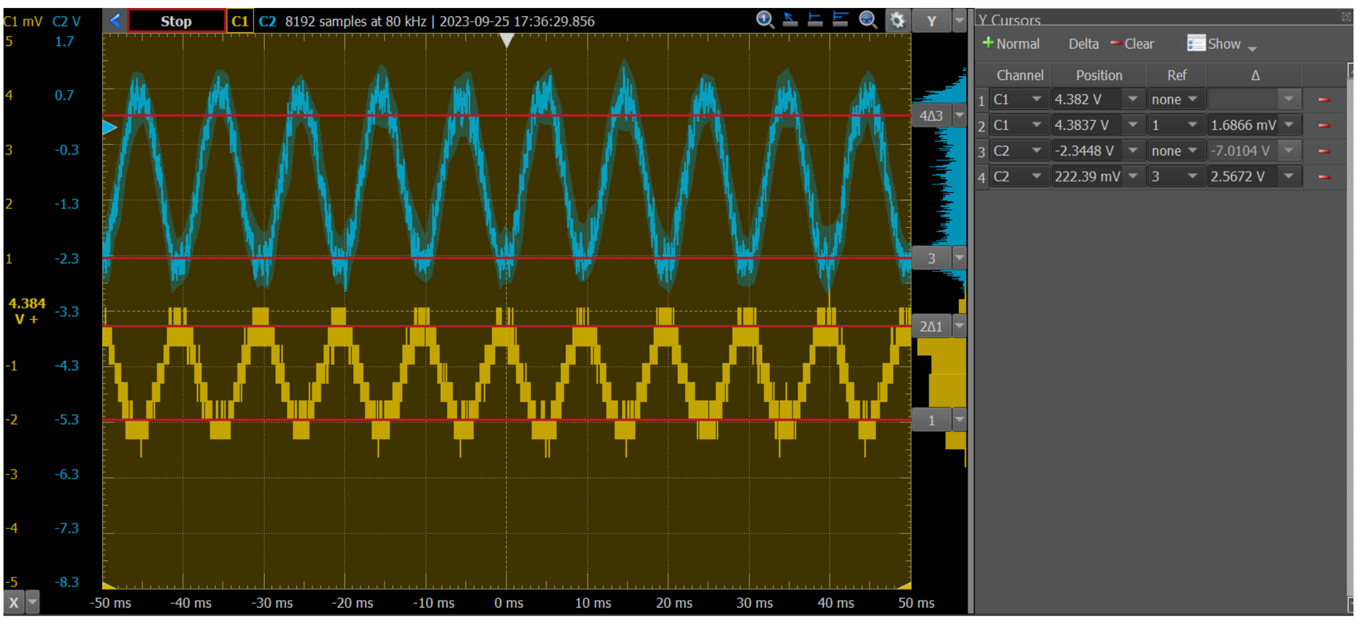
$$A_{vo} = 20log(\frac{V_o}{V_i}) = 20log(\frac{2.872}{0.002}) = 63dB$$

$$Phase = 135.5°$$

$$f_{3dB} = 14077\ Hz$$

Part 2

The measurement data can be found below as follows…

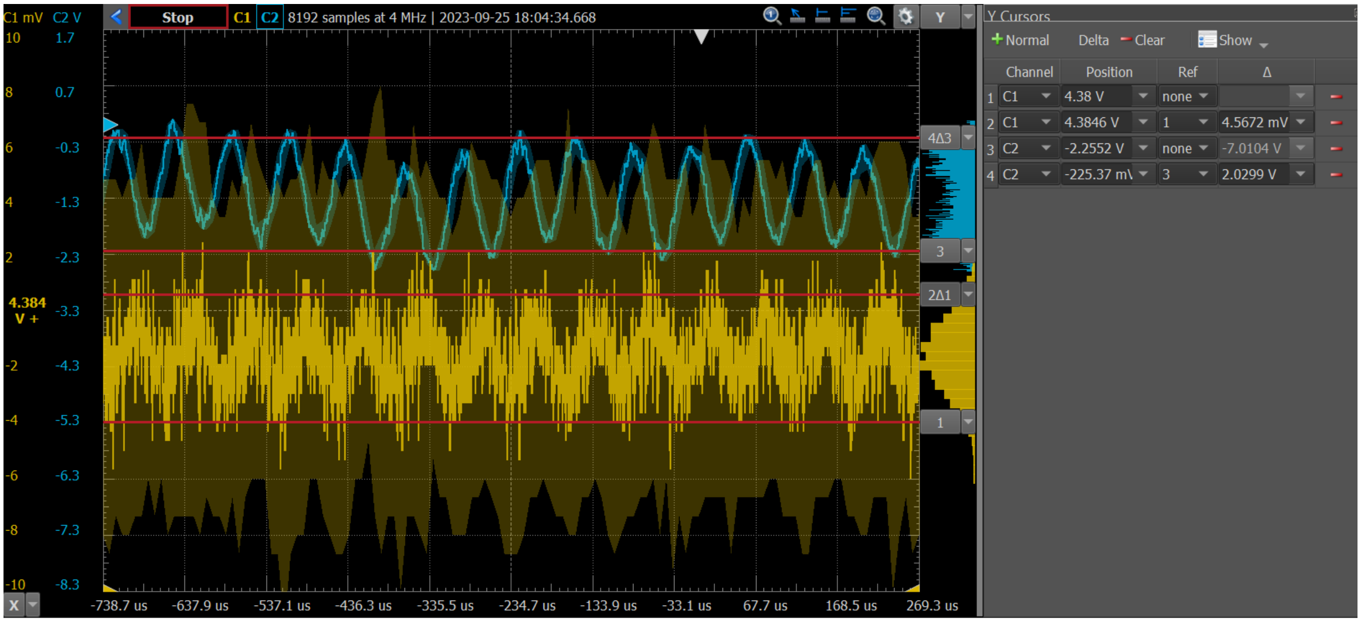


ΔC1 (V)	ΔC2 (V)	Gain Av (dB)
1.69E-03	2.5672	63.6

As can be seen, my measured values suggest that this amplifier has a low frequency gain of about 63dB. This is relatively close to our experimental values seen above.

Part 3

Adjusting the frequency of W1 to match the above, $f_{3dB} = 14077\ Hz$



In this case, our gain would be as such; $A_v = 20log\left(\frac{2.0299}{0.0042672}\right) = 53dB$

If we compare this to what we would theoretically expect, $A_v\left(f_{3dB}\right) = A_v(100Hz) \times 0.707 = 45dB$

We can see that there is definitely a slight error in our theoretical and measured, but they follow the same general trend that an increased frequency for V_{sig} results in a lower gain, A_v

Questions for Part 2

Question 5 (15 Points)

Part 1

When $V_{cm} = 0\,V$ we have the following values;

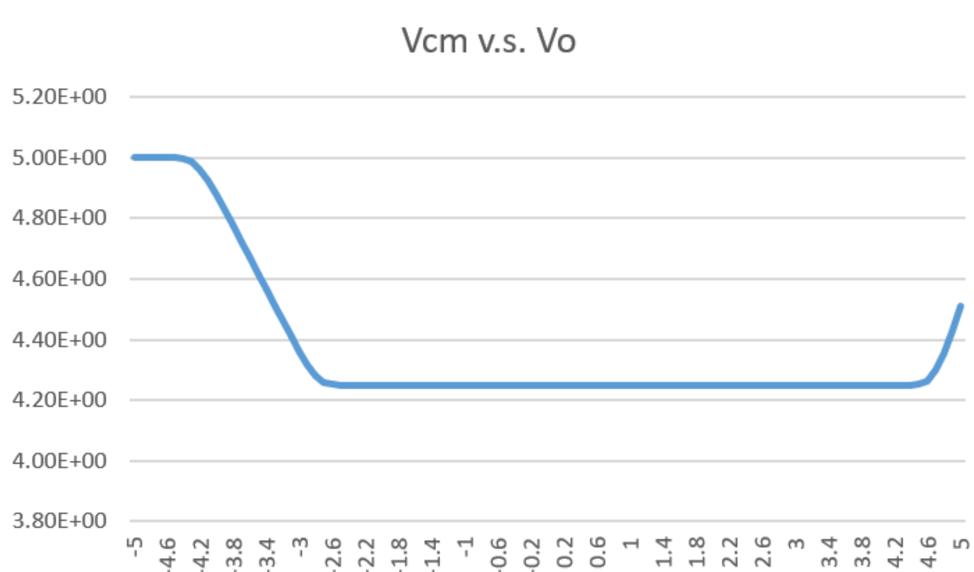
$V_o = 4.2499\,V$

$V_E = -0.525\,V$

$I_{C2} = 0.0000909\,A$

Vo (V)	VE (V)	IC2 (A)	Vcm (V)
-0.52537	4.25E+00	9.09E-05	0

Part 2



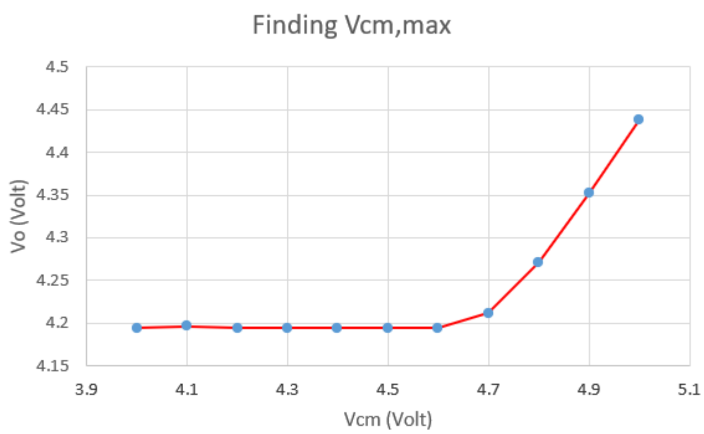
From the above generated graph, we can see that in order to keep V_o a constant, V_{cm} must remain between $-2.6V\ and\ 4.6V$

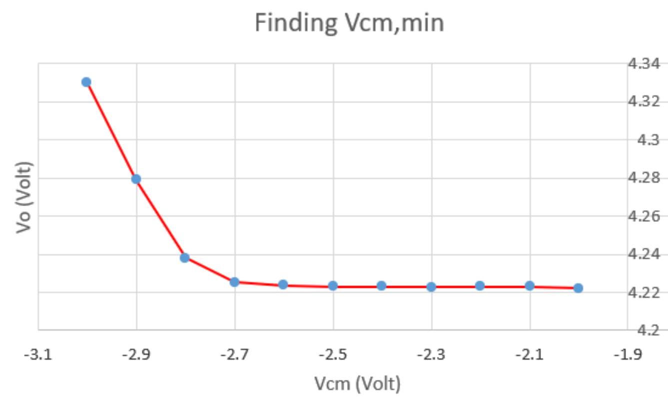
Part 3

Speaking theoretically, the upper bound of the common mode input range is limited by the need to keep the transistors within the differential pair operating in the active region. The lower limit of the common mode input is limited by the need to keep the constant current sink on. In our case scenario, the voltage needed by the constant current sink is actually just the voltage required to keep the transistor in our current sink operating in the saturation region.

Part 4

Below are the graphs from steps 2.7 and 2.8 respectively…





As can be seen, the graph on the left depicts the fact that $V_{cm,\, max}$ is somewhere between 4.5V and 4.7V, and the graph on the right depicts that $V_{cm,\, min}$ is somewhere between -2.7V and -2.5V

Question 6 (10 Points)

Frequency	M(V(Vo))	P(V(Vo))	Common-mode Gain Acm
Hz	Volts	Degrees	dB
0.1	4.52E-08	-179.9767369	-86.90

At the lowest measured frequency, $f = 0.1 Hz$, our common mode gain is, $A_{cm} =- 86.90\ dB$

Frequency	M(V(Vo))	P(V(Vo))	Common-mode Gain Acm
100	4.88E-08	-157.9043648	-86.24

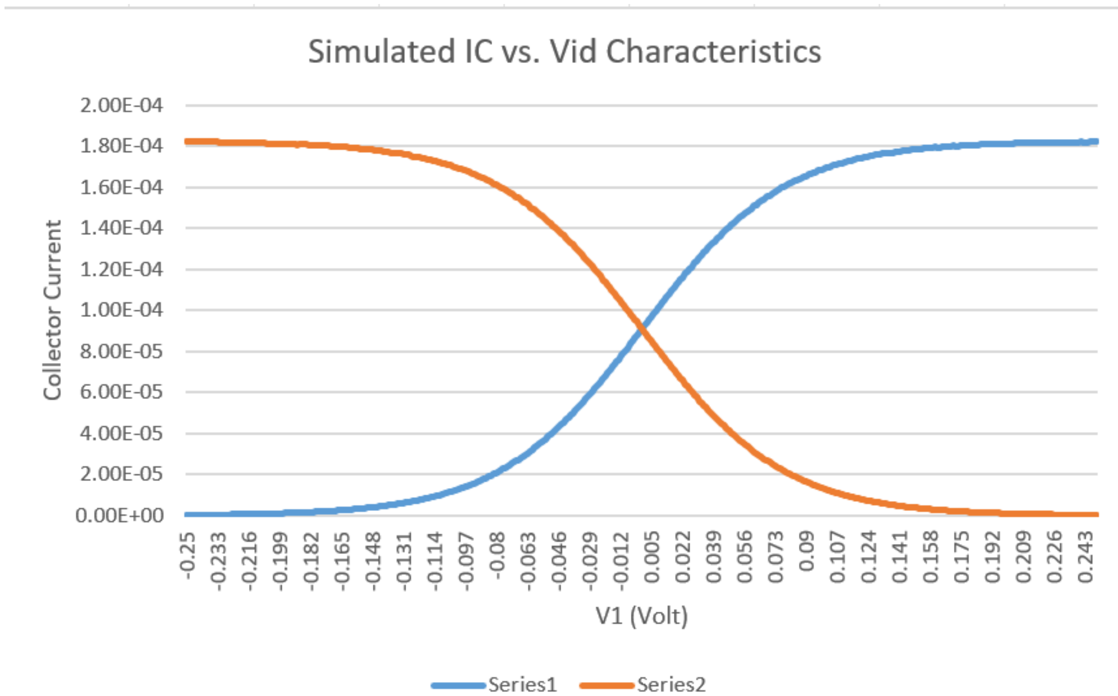
Keeping consistency with previous questions, we can also consider $f = 100Hz$, in which case the common mode gain is $A_{cm} =- 86.24\ dB$

Questions for Part 3

Question 7 (10 points)

Part 1

Below is the graph obtained in Step 3.2…



For a BJT, we know that $V_T = 0.025\ V$.

According to section 9.2.3 in the textbook and lecture notes, the limitations for the differential input are $\pm\ \frac{V_T}{2}$ about the point of intersection of Series 1 and Series 2 in the AC case, and $\pm\ 4V_T$ in the DC case. From the Excel, the intersection of the 2 series is at $V_1 = 0.004$. This means our differential mode ranges can be found as follows…

$v_{dm,\,AC} = [(0.004\ -\ 0.0125)\ V,\ (0.004\ +\ 0.0125)\ V] = [-\ 0.0085V,\ 0.0162V]$

$V_{DM,\,DC} =\ [(0.004\ -\ 0.1)\ V,\ (0.004\ +\ 0.1)\ V] = [-\ 0.096V,\ 0.104V]$

Part 2

The upper and lower bounds of the differential mode input is determined by the range in which our circuit operates as a linear amplifier. Typically, we want to operate within the middle of the graph depicted above, where the two curves intersect. This results in the differential input signal being limited to about $\frac{V_T}{2}$.

Question 8 (10 Points)

Part 1
Based on step 3.3, the differential mode gain is about $A_d \approx 19.63dB$

Part 2
$f_{3dB} = 8332821.50847752\ Hz$
At the above frequency, our phase is -45.4156507169392°
$Gain - Bandwidth\ Product = (Absolute\ Gain) \times \left(f_{3dB}\right)$
To find absolute gain…
$20log_{10}(Absolute\ Gain) = 19.63dB$
$\Rightarrow Absolute\ Gain = 10^{0.9815} = 9.58297$
Thus, we can calculate the Gain-Bandwidth Product as follows…
$Gain - bandwidth\ Product = (9.58297)(8332821.5\ Hz) = 79853178.5\ Hz$

Part 3
In question 4 we had… $f_{3dB} = 14077\ Hz$
In question 8 we had… $f_{3dB} = 8332821\ Hz$
We can see that in question 8, the 3dB frequency is substantially higher than in question 4

Part 4
According to the measured values in step 3.6, the gain of this amplifier is $A_d = 21.9dB$

Question 9 (10 points)

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| = \left|\frac{19.63}{-86.9}\right|dB = 0.22589dB$$