

A

B

C

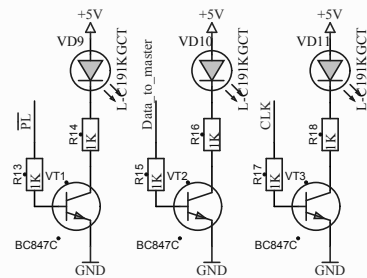
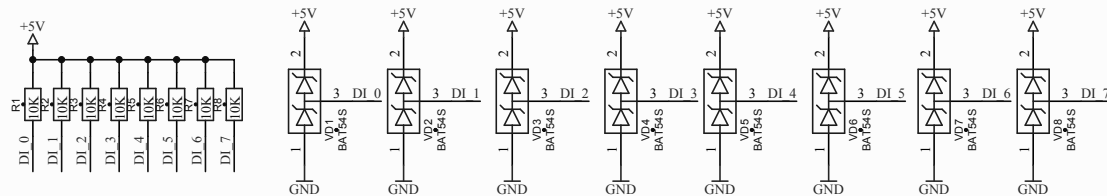
D

A

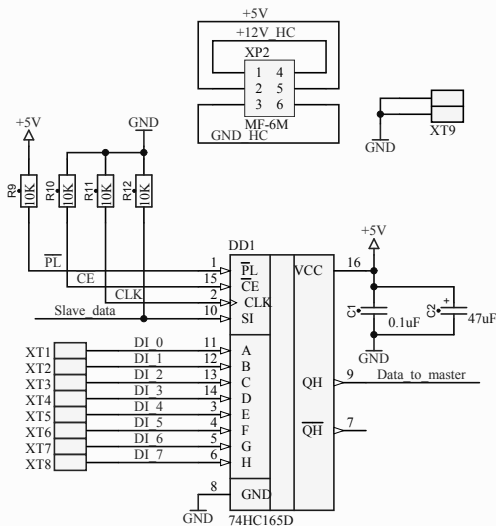
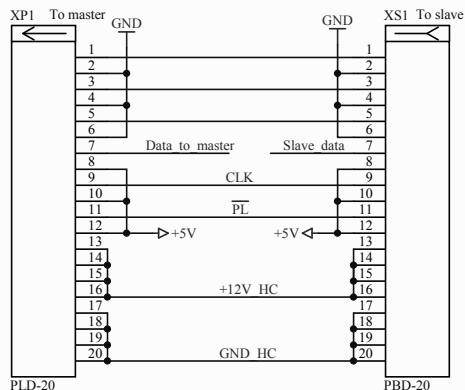
B

C

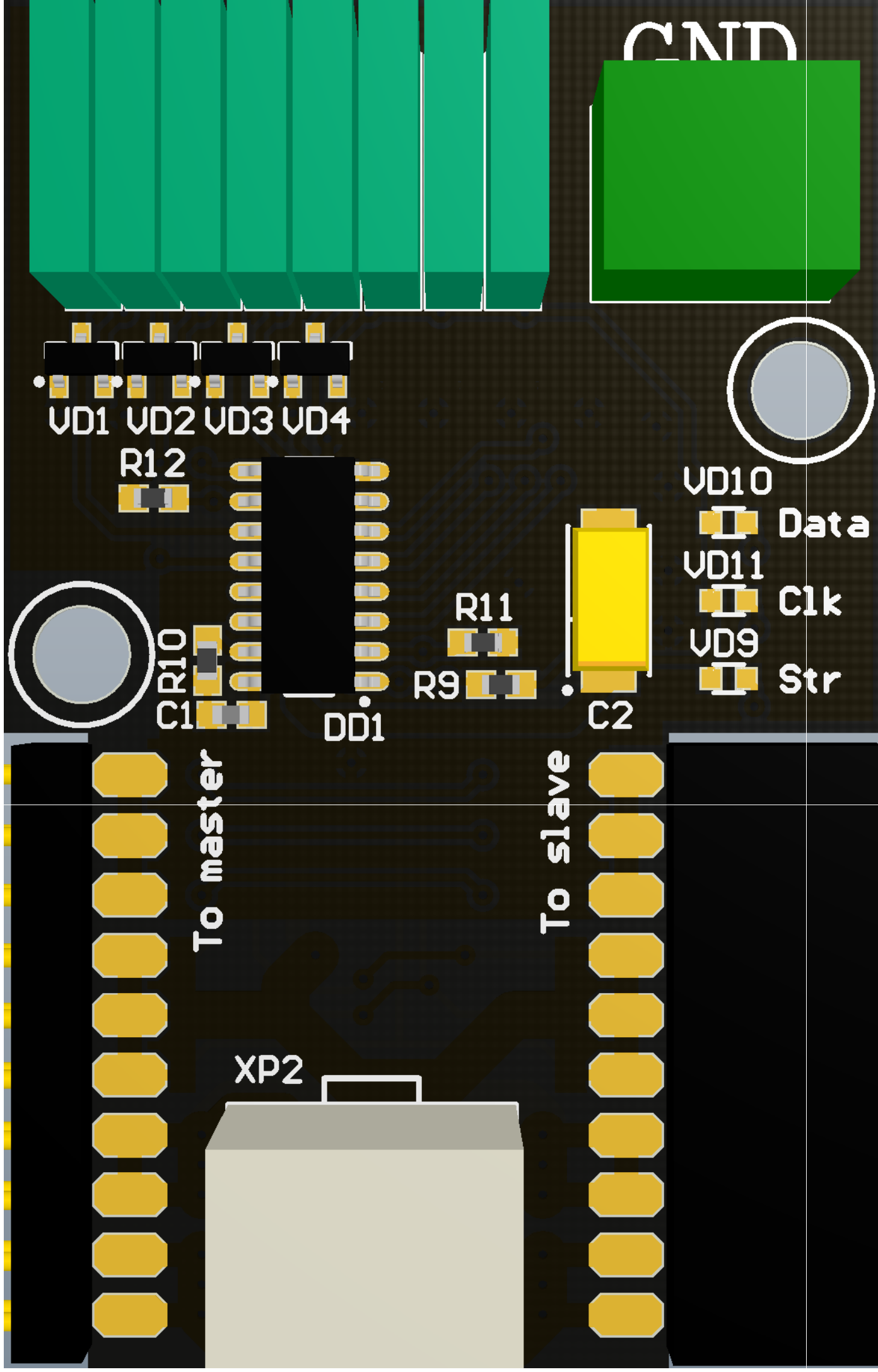
D



- 1 : data (Output module)
2 : GND (Logic)
3 : clock (Output module)
4 : GND (Logic)
5 : strobe (Output module)
6 : GND (Logic)
7 : data (Input module)
8 : +5V (Logic)
9 : clock (Input module)
10 : +5V (Logic)
11 : strobe (Input module)
12 : +5V (Logic)
13,14,15,16 : +12V
(High-Current)
17,18,19, 20 : GND
(High-Current)



Title		
Size	Number	Revision
A4		
Date:	26.10.2015	Sheet of
File:	C:\Work\kiselev\InputModule\Sch.SchDoc	Drawn By:



CND

VD1 VD2 VD3 VD4

R12

VD10

Data

VD11

Clk

VD9

Str

R11

R9

DD1

C2

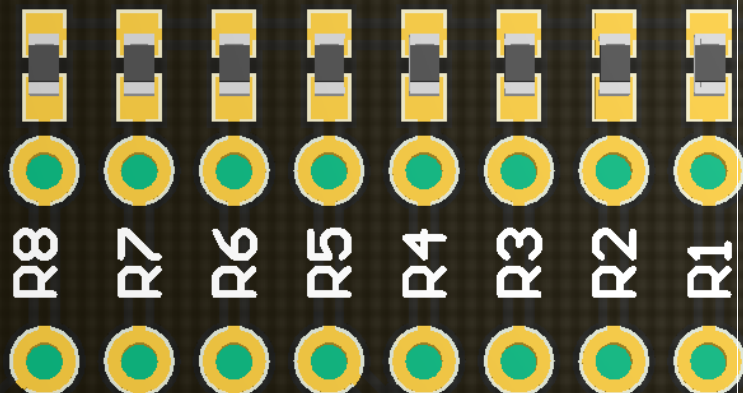
C10

C1

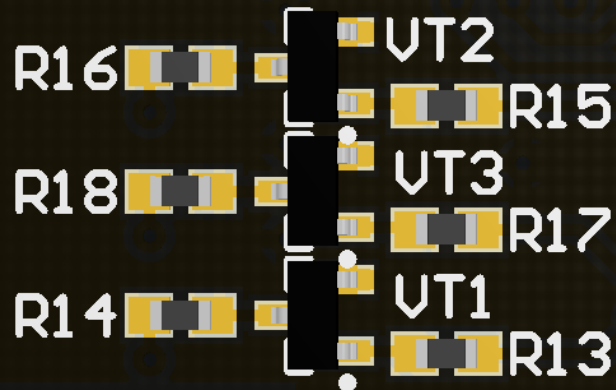
To master

To slave

XP2



VD8 VD7 VD6 VD5



UT2

R15

UT3

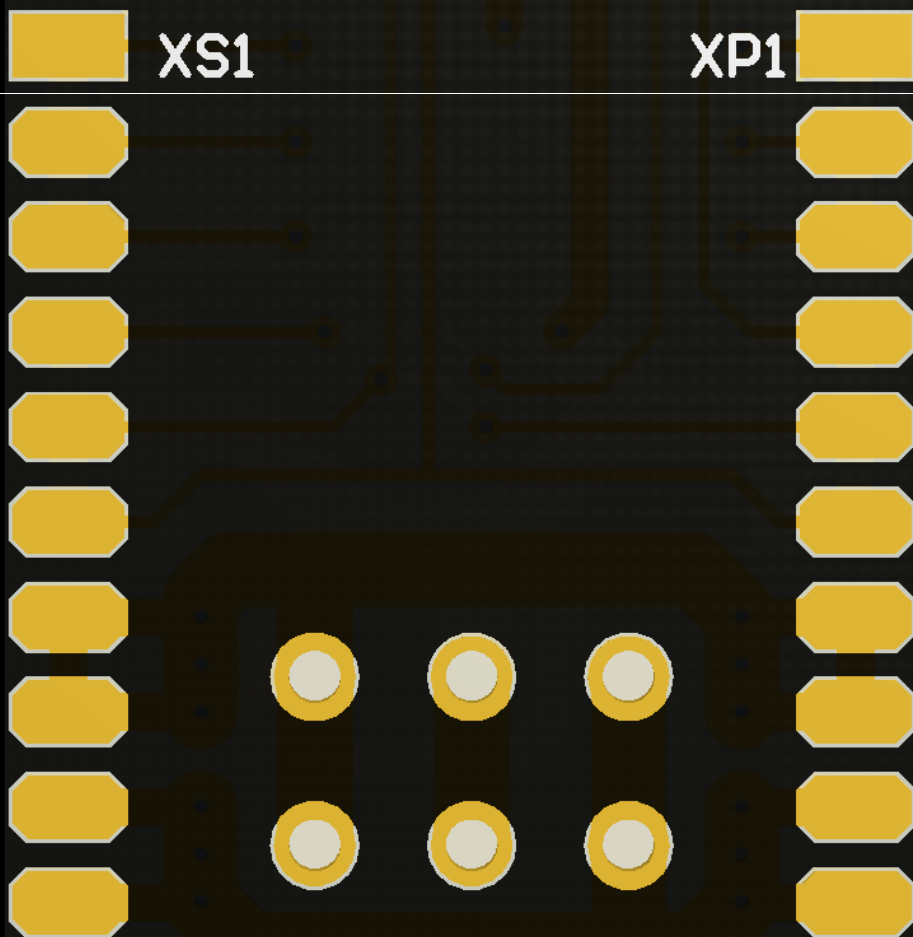
R17

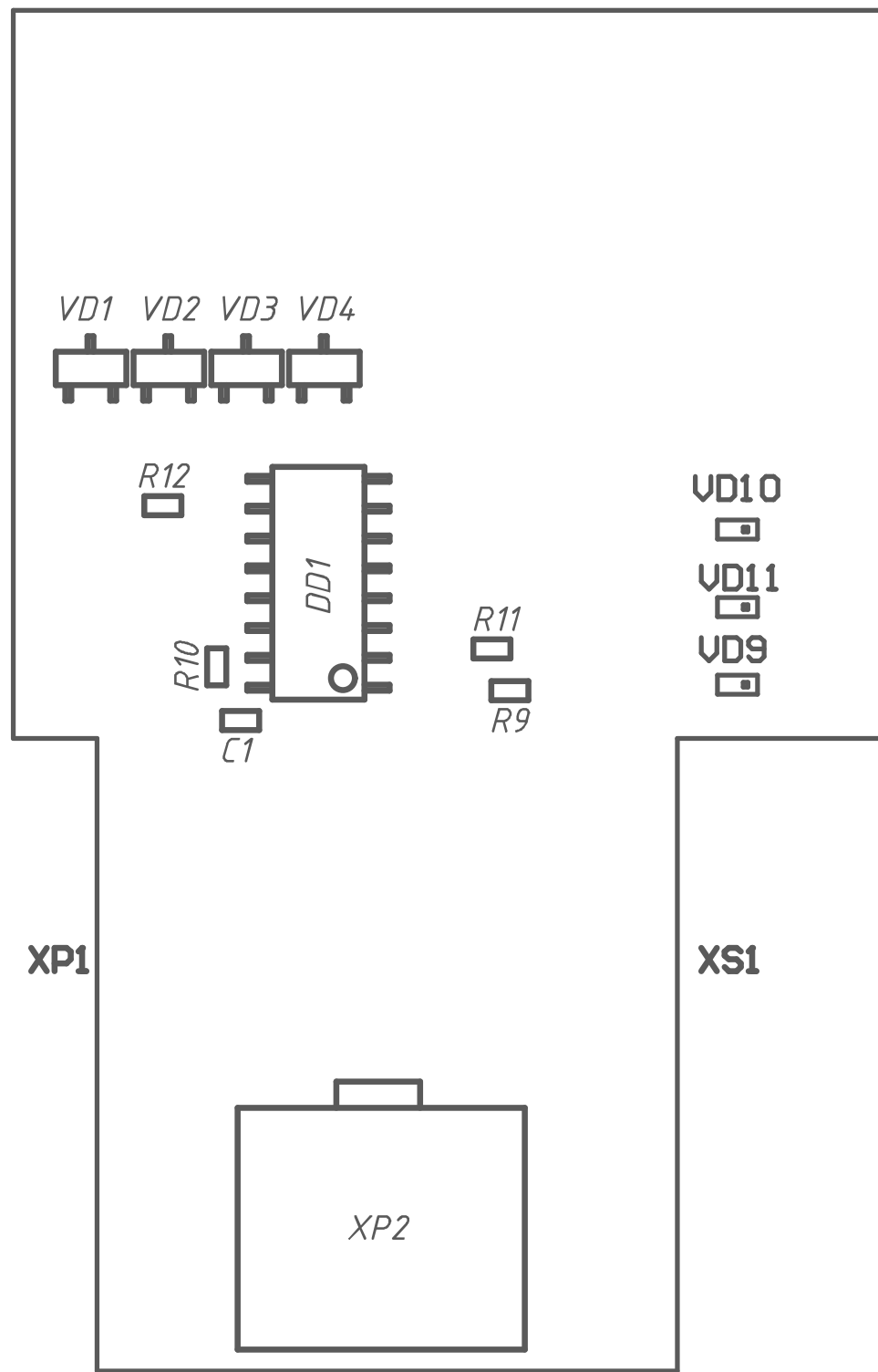
UT1

R13





XS1










XP1





       
R8 R7 R6 R5 R4 R3 R2 R1

   
VD8 VD7 VD6 VD5

R16   *VT2*  *R15*
R18   *VT3*  *R17*
R14   *VT1*  *R13*

Component list

<Parameter Title not found>

Source Data From:	Prj.PrjPCB
Project:	Prj.PrjPCB
Variant:	None

Report Date:	26.10.2015	16:47:37
Print Date:	26-Oct-15	4:47:41 PM

#	Designator	Comment	
1	C1	0.1uF	
2	C2	47uF	
3	DD1	74HC165D	
4	R1	10K	
5	R2	10K	
6	R3	10K	
7	R4	10K	
8	R5	10K	
9	R6	10K	
10	R7	10K	
11	R8	10K	
12	R9	10K	
13	R10	10K	
14	R11	10K	
15	R12	10K	
16	R13	1K	
17	R14	1K	
18	R15	1K	
19	R16	1K	
20	R17	1K	
21	R18	1K	
22	VD1	BAT54S	
23	VD2	BAT54S	
24	VD3	BAT54S	
25	VD4	BAT54S	
26	VD5	BAT54S	
27	VD6	BAT54S	
28	VD7	BAT54S	
29	VD8	BAT54S	
30	VD9	L-C191KGCT	
31	VD10	L-C191KGCT	
32	VD11	L-C191KGCT	
33	VT1	BC847C	
34	VT2	BC847C	
35	VT3	BC847C	
36	XP1	PLD-20	
37	XP2	MF-6M	
38	XS1	PBD-20	
39	XT1	DG141V-01P	
40	XT2	DG141V-01P	
41	XT3	DG141V-01P	
42	XT4	DG141V-01P	
43	XT5	DG141V-01P	
44	XT6	DG141V-01P	
45	XT7	DG141V-01P	
46	XT8	DG141V-01P	
47	XT9	1-1776244-0 (TYCO)	

Approved