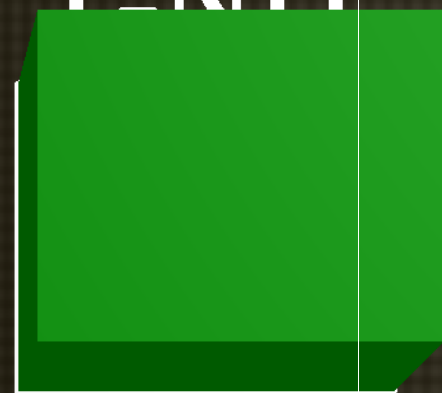


CND

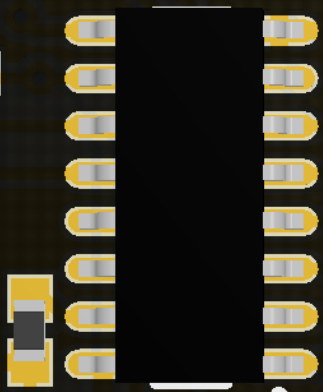


VD1 VD2 VD3 VD4

R12



CR10
C1

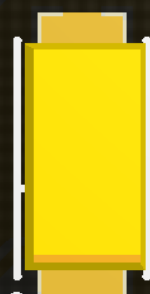


DD1

R11



R9



C2

VD10



Data

VD11



Clk

VD9

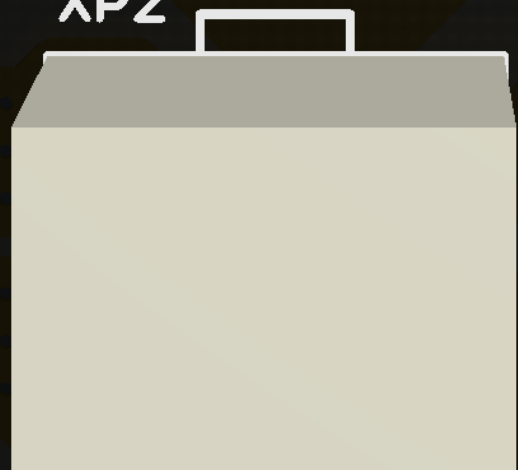


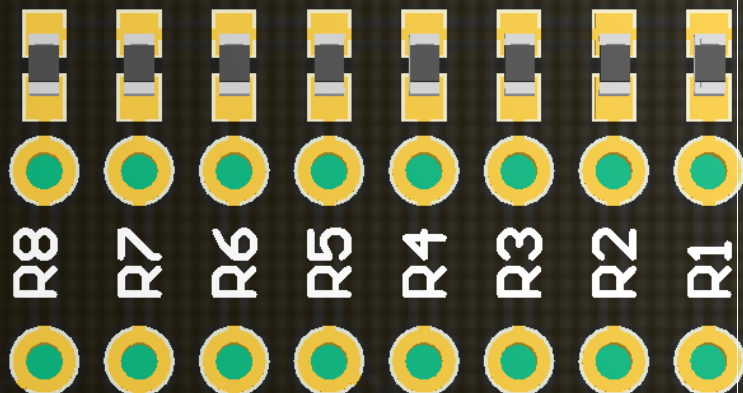
Str

To master

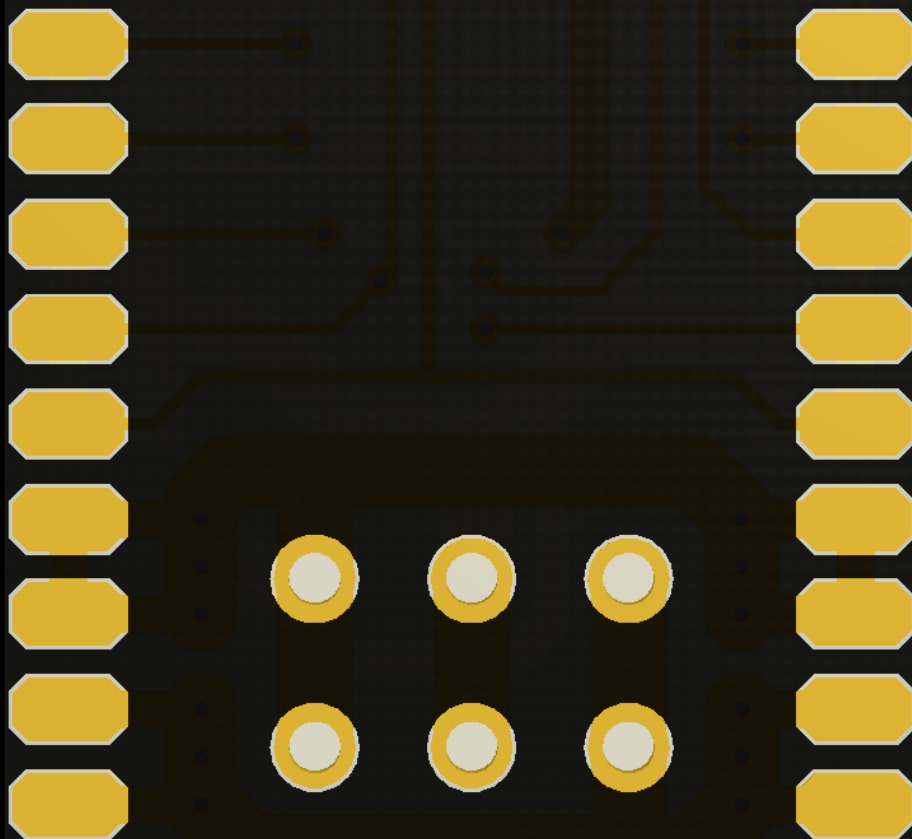
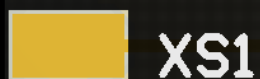
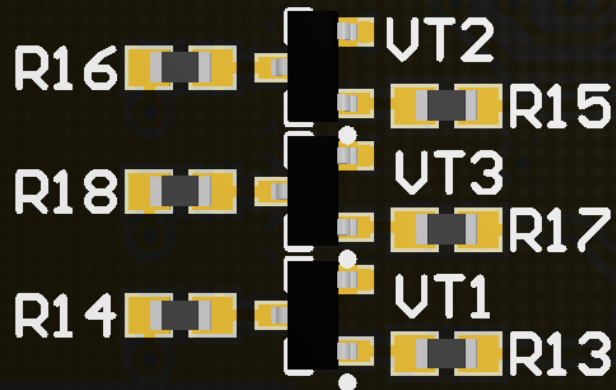
To slave

XP2


















VD8 VD7 VD6 VD5



       
R8 R7 R6 R5 R4 R3 R2 R1

   
VD8 VD7 VD6 VD5

R16   *VT2*  *R15*
R18   *VT3*  *R17*
R14   *VT1*  *R13*

