Design and analysis of First-order Sigma-Delta A-to-D Converter

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Abstract

This paper details an approach to design and analyse a First-order Sigma-Delta Analog-to-Digital Converter ($\Sigma\Delta\ ADC$) with mixed signal approach. The design produces a high-resolution data-stream output, as this consist of the Analog-block comprising of a differentiator, an integrator and a comparator and the digital-block comprising of D-latch acting as a path of negative feedback to the difference amplifier. Sigma-Delta ADC can be used effectually to digitize the diverse types of signals around which are processing numerous applications in the field of electronics and communication systems.

1. Reference circuit Details

The leftmost op-amp represents the difference amplifier to which the Analog input is fed at one terminal and another input is fed from the 1-bit DAC (Digital to Analog Converter) which follows the negative feedback path. The output from this amplifier is fed to the integrator which is going to add the obtained value from the difference amplifier with the previously present value. The integrated output is now fed to the next block that is comparator, this acts as one sort of 1-bit ADC, that producing 1-bit of output either high (‘1’) or low (‘0’) depending on whether the integrator output is positive or negative.

Next is the D-latch to which the output from the comparator is fed. It latches the comparator’s output at every clock pulse, and the final data-stream output is obtained from its end. This +V feedback signal tends to drive the integrator output in a negative direction. If that output voltage ever becomes negative, the feedback loop will send a corrective signal (-V) back around to the top input of the integrator to drive it in a positive direction. A part of it is fed back to the difference amplifier via the 1-bit DAC bridge.

Variations on this theme exist, employing multiple integrator stages and/or comparator circuits outputting more than 1 bit, but one concept common to all $\Delta\Sigma$ converters is that of oversampling. Oversampling is when multiple samples of an Analog signal are taken by an ADC (in this case, a 1-bit ADC), and those digitized samples are averaged.

2. Implemented Circuit

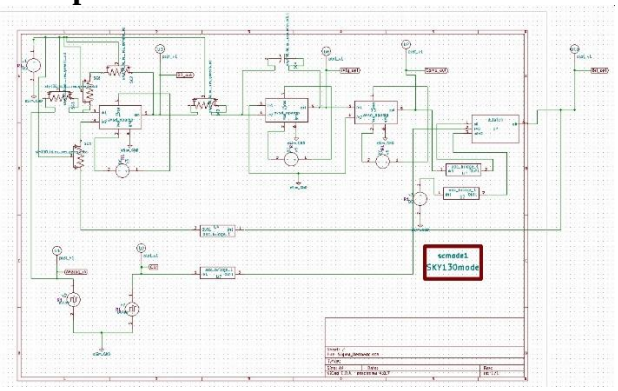

Fig 1. Sigma-Delta ADC implementation with mixed signal approach.

3. Circuit Waveforms

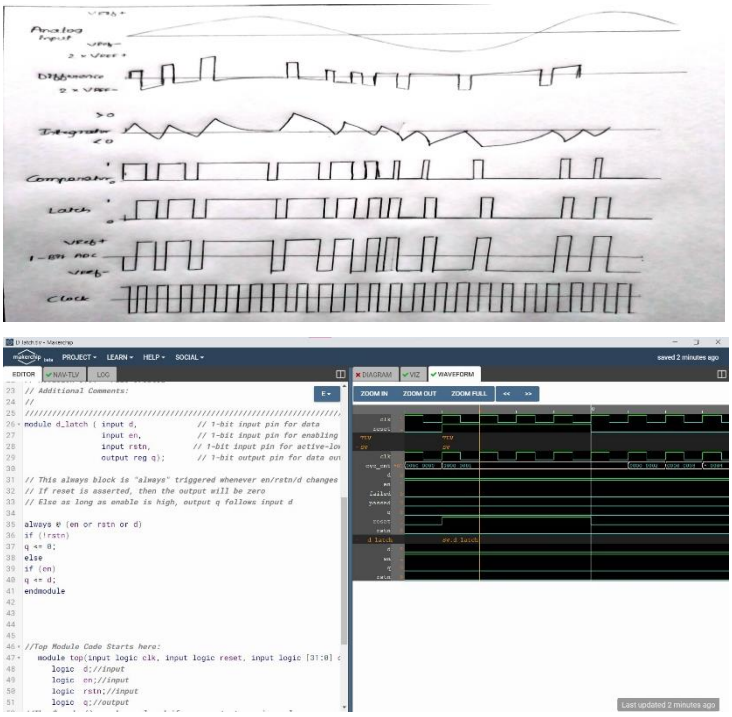

Fig 2. Reference waveforms and digital block output of $\Sigma\Delta\ ADC$.

References

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