Fall 2024 VLSI Design/CAD VLSI Design

Homework Assignment 4

Due date: Dec 8th Sunday

Problem 1 (Booth Encoding-based Multiplication)

Use Booth encoding to perform multiplication between 24 and 15

Materials to be submitted:

1. The entire computation procedure in PDF/Word format

Problem 2 (Memory modeling)

Use Verilog to design and implement a function as $c = c + \sum_{i=1}^{8} b * a_i$.

Here a_i is stored in a SRAM with width as 16 and depth as 8 (8 rows of 16-bit data), and *b* is stored in a 16-bit register. *c* is initialized as 0.

Materials to be submitted:

1. Verilog codes for design module.

2. Verilog codes for testbench.

3. Image of the screen that shows the test results.