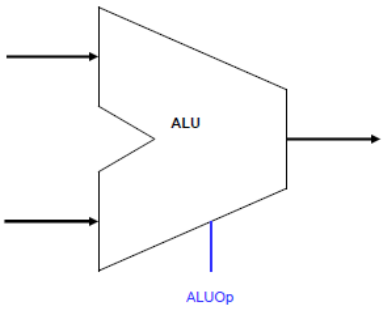
Fall 2024 VLSI Design/CAD VLSI Design

Homework Assignment 1

Due date: Oct 11 Friday

Problem 1. Using Verilog to design and test an arithmetic logic unit (ALU).

ALU Module Design: This ALU has three inputs, two 32-bit signed inputs, one 3-bit ALUop input, and one 32-bit signed output.



ALUOp	Function
000	and
001	or
010	add
110	subtract
111	slt

Testbench Design: The test results should be printed on the screen with format as below (for example):

"1st Test data: input A is 1, input B is 2, ALUOp is 010, result is 3."

"2nd Test data: input A is 3, input B is 4, ALUOp is 110, result is -1."

…

Note: All the five functions of ALU need to be tested.

Materials to be submitted:

1. Verilog codes for ALU module

2. Verilog codes for testbench

3. Image of the screen that shows the test results.