Fall 2024 VLSI Design/CAD VLSI Design

Homework Assignment 2

Due date: Oct. 27 Sunday

Problem 1 (FSM Design)

Use Verilog to design an FSM. The FSM accepts an input binary sequence such as 001010011101…. Its output is **zero** except when the number of 1's that have been input is a multiple of three. In the example below, the output that is observed after each input bit is received is shown directly below the input bit received:

```
input :    -   0 1 0 0 1 1 0 0 1 0 1 0 0 1 0 1 0 1 1 0 1 1 0 1 1 0 1 1 ...
output:    1   1 0 0 0 0 1 1 1 0 0 0 0 0 1 1 0 0 0 1 1 0 0 0 1 0 0 0 1 ...
```

Note: Before any bits have been received, the output is 1. This is because zero 1's is also a multiple of three.

Materials to be submitted:

1. Verilog codes for FSM module. You can choose either two-always or three-always blocks style.

2. Verilog codes for testbench using the above example

3. Image of the screen that shows the test results.