Fall 2024 VLSI Design/CAD VLSI Design

Homework Assignment 3

Due date: Nov 15th Friday

Problem 1 (Carry Lookahead/Selector Adder Design, Mandatory)

Use Verilog to design and implement an 8-bit Carry Lookahead Adder OR 8-bit Carry Selector Adder. You can choose to either use or not use generate statements.

Materials to be submitted:

1. Verilog codes for carry lookahead/carry selector adder module.
2. Verilog codes for testbench.
3. Image of the screen that shows the test results.

Problem 2 (Carry Skip Adder Design, Optional)

Use Verilog to design and implement a 16-bit Carry Skip Adder. You can choose to either use or not use generate statements.

Materials to be submitted:

1. Verilog codes for carry skip adder module.
2. Verilog codes for testbench.
3. Image of the screen that shows the test results.