MS Technical Paper:
Placement Algorithms for Heterogenous FPGAs

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1 Keywords

- FPGA, EDA, Placement, Simulated Annealing, Optimization, RapidWright

2 Abstract

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3 Design Flow

A typical FPGA design flow goes like the following. First, the developer writes the design entry in a high level Hardware Description Language (HDL) like Verilog or VHDL.

- Synthesis (Vivado default)
- Placement (the focus of this paper)
  - **Prepacking**:
    Traverse the raw EDIFNetlist from synthesis and identify patterns of cells that should be grouped together. This can be CARRY chains, DSP cascades, LUTFF pairs, etc.
  - **Packing**:
    Take the prepacked cell groups and pack them into SiteInsts. IntraSite routing.
  - **Placement**:
    Take the SiteInsts and optimally place them onto physical Sites.
- Routing InterSite routing