Technical Paper Proposal:
Placement Algorithms for Heterogenous FPGAs

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1   Abbreviations

– FPGA: Field Programmable Gate Array

– VLSI: Very Large Scale Integration

– EDA: Electronic Design Automation

– VHSIC: Very High Speed Integrated Circuits

– HDL: Hardware Description Language

– VHDL: VHSIC HDL

– HLS: High Level Synthesis

– PL-PS: Programmable Logic - Processing System

2   Ideas

- **FPGA**: Field Programmable Gate Array

    – FPGA Vendors:
        · AMD-Xilinx (50% FPGA vendor market share)
        · Intel-Altera (35% share)
        · Lattice
        · Microsemi

- **EDA**: Electronic Design Automation

    – Proprietary software for FPGA and VLSI development:
        · Xilinx - Vivado (Design + Simulation) + Vitis (HLS + PL-PS codesign)
        · Altera - Quartus (Design) + ModelSim (Simulation)
        · Synopsis (VLSI)

- · Cadence (VLSI)
  - – Open source software for FPGA development:
    - · VTR: a PNR tool popular amongst researchers who study placement techniques
    - · OSS-CAD: a full-flow software suite that includes ABC synthesis, Yosys synthesis, Yosys nextpnr.
    - · AMF-Placer (Analytical Placer)
    - · DREAMPlace (VLSI) + DREAMPlaceFPGA
    - · RapidLayout (Hard Block Placer)
    - · RapidStream (Systolic Array Placer)
    - · RapidWright: Semi-open source API that provides backend access to Xilinx Vivado EDA using design checkpoints.

- **Synthesis**

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