Technical Paper Proposal: Placement Algorithms for Heterogenous FPGAs

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1 Keywords

- FPGA, EDA, Synthesis, Placement, Routing, Parallel, Optimization

2 Proposal

A compiler takes a high-level program like a Java or Python file and assembles a corresponding machine code which is ready to be executed on a CPU. In similar fashion, an Electronic Design Automation tool (EDA) takes a high-level description of a digital system written in Verilog or VHDL and produces a bitstream which is ready to be deployed to an FPGA. In a superficial way, compilers and EDAs perform the same task for engineers but in different industries. One for software, the latter for hardware.

Software compilers have evolved to become highly optimized, significantly boosting the productivity of software developers. The compilers are so robust that developers rarely need to worry about the correctness or efficiency of their machine code, and are so refined that it all happens in a matter of milliseconds to minutes, even for large projects. The speed of compilation enables rapid debugging and implementation of design changes and allows developers to iterate through dozens or even hundreds of design cycles per day. Instead of tinkering around with assembly code, software engineers can comfortably focus on the high-level abstractions of their design.

The compilation stages mainly consists of lexing, parsing, and instruction optimization. While these stages can be complex from a design standpoint, they are, mathematically, trivial. The EDA stages are despairingly complex by comparison. First, the FPGA engineer creates and describes a digital design using a hardware description language (HDL) like Verilog or VHDL. Then the engineer submits the design entry to an EDA like Vivado or Quartus to perform three stages of automated design. These are: synthesis, placement, and routing. All three are NP-hard problems.

For even modest designs that utilize a small percentage of the available resources on the FPGA, the EDA will spend a minimum of a couple minutes

synthesizing and implementing the design. The EDA run time increases exponentially with the scale of the project. Projects that utilize 80% or more of the FPGA's resources may run for hours, and for the high-end devices like Xilinx's Kintex FPGAs which have millions of logical elements, can run for days. At high utilization, there is a possibility that the EDA cannot fit the design onto the device due to routing congestion even when it has enough logical elements to implement the design. The EDA might only reach this conclusion after attempting to fit the design for several hours.

One of the most common complaints from new FPGA engineers, especially those coming from software development, is that the FPGA toolchains are overall slow and heavy. This is because the problems that the EDA must solve are inherently complex. Unlike in software development where an error in the program can be patched and recompiled in a matter of minutes, EDA runtimes lasting several hours means that an engineer can only go through a couple design cycles per day. An FPGA engineer must be very precise with their coding and practice thorough verification of their design before submitting it to the EDA. This overall heightens the barrier of entry into FPGA development and contributes to a shortage of qualified FPGA engineers and a limitation of their productivity.

This paper aims to study one particular pillar of this barrier: the placement stage. First, it will review prerequisite knowledge for placement algorithms. This includes graph theory to represent logical elements of a digital design and the wired connections between them, and a corresponding optimization problem with a cost function which we seek to minimize.

In mathematics, a graph is usually modeled as $G = (V, E)$, where V represents the set of vertices and E represents the set of edges between them. A hypergraph is denoted as $G_H = (V_H, E_H)$, where V_H represents the set of vertices, and E_H represents the set of hyperedges, which are edges that can connect more than two vertices. Electronic circuits are typically represented as hypergraphs where In FPGA design, the graph is often modeled using a "netlist". A netlist is a graph $G = (V, E)$, where V represents the components (e.g., logic blocks or gates), and E represents the connections or nets between them.

The vast majority of existing placers use the Half Perimeter Wire Length (HPWL) cost function or one of its various flavors - manhattan distance, euclidian distance, beta-regularized, etc.. The basic HPWL models the problem as the summation of the manhattan lengths of all nets in the netlist.

$$\text{HPWL} = \sum_{i=1}^{n} \left(\max_{j \in \text{net}_i} (x_j) - \min_{j \in \text{net}_i} (x_j) + \max_{j \in \text{net}_i} (y_j) - \min_{j \in \text{net}_i} (y_j) \right) \tag{1}$$

Then, the paper will survey the current landscape of placement algorithms and strategies. This includes Simulated Annealing (SA), Analytical Placement (AP),

3 Abbreviations

- **FPGA**: Field Programmable Gate Array
- **VLSI**: Very Large Scale Integration
- **EDA**: Electronic Design Automation
- **VHSIC**: Very High Speed Integrated Circuits
- **HDL**: Hardware Description Language
- **VHDL**: VHSIC HDL
- **HLS**: High Level Synthesis: Generating synthesizable HDL from high-level software languages. A company might want to have a software engineer write C or C++ code and have a program translate it into synthesizable Verilog. This can can boost productivity and save the company the need to hire a hardware engineer.
- **IP**: Intellectual Property: In FPGA context, this means pre-built modules or subsystems like a hardened microprocessor or Ethernet controller. These are usually proprietary.
- **SoC**: System on Chip: An FPGA device (chip) that features hardened IP in addition to the programmable logic fabric.
- **PL-PS**: Programmable Logic - Processing System: A design that utilizes the on-chip hard microprocessor in conjunction with the programmable logic fabric.
- **EDIF**: Electronic Design Interchange Format
- **HPWL**: Half Perimeter Wire Length

4 Ideas

- **FPGA**: Field Programmable Gate Array
  - FPGA Vendors:
    - AMD-Xilinx (∼50% FPGA vendor market share)
    - Intel-Altera (∼35% share)
    - Lattice
    - Microsemi
- **EDA**: Electronic Design Automation
  - Proprietary software for FPGA and VLSI development:

    - Xilinx - Vivado (Design + Simulation) + Vitis (HLS + PL-PS codesign)
    - Altera - Quartus (Design) + ModelSim (Simulation)
    - Synopsis (VLSI)
    - Cadence (VLSI)
  - Open source software for FPGA development:
    - **VTR**: Simulated Annealing placer for FPGAs. Popular among researchers who study placement techniques. Commonly referred to as an "academic placer".
    - **OSS-CAD**: a full-flow software suite that includes ABC synthesis, Yosys synthesis, Yosys nextpnr.
    - **AMF-Placer**: Analytical Placer for FPGAs
    - **RapidWright**: Semi-open source Java API that provides backend access to Xilinx Vivado EDA using design checkpoints.
    - **RapidLayout**: Hard Block Placer for Systolic Arrays. Built with RapidWright.
    - **RapidStream**: HLS Placer. Built with RapidWright.
    - **DREAMPlace**: GPU-powered deep learning placement for VLSI.
    - **DREAMPlaceFPGA**: DREAMPlace, adapted to FPGAs via the RapidWright API.

- **Synthesis**
  - Takes a design written in a high-level HDL like VHDL or Verilog and "synthesizes" a **logical netlist** out of it.
  - The logical netlist is usually generated as an EDIF, JSON, or a low-level Verilog file.
  - The netlist describes the necessary basic elements of logic (BELs) and the wired connections between them that are necessary to implement the design.

- **Placement**
  - Takes the **logical netlist** and produces a **physical netlist**.
  - For each BEL in the netlist, assign the BEL to a Cell, Site, and Tile on the physical FPGA device.

- **Routing**
  - Takes the **physical netlist** and maps the connections between BELs onto wires, interconnects, and switchboxes on the FPGA.

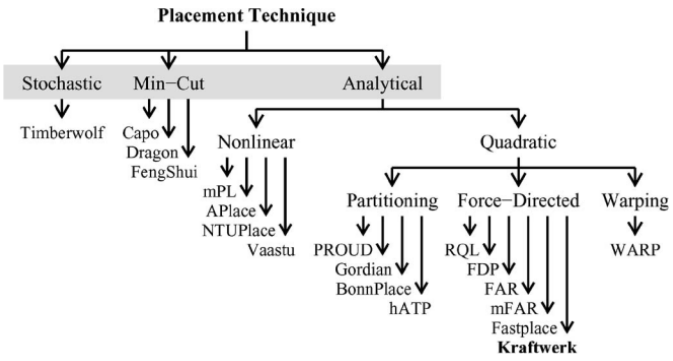

Figure 1: Landscape of VLSI placement techniques (Spindler) [1]

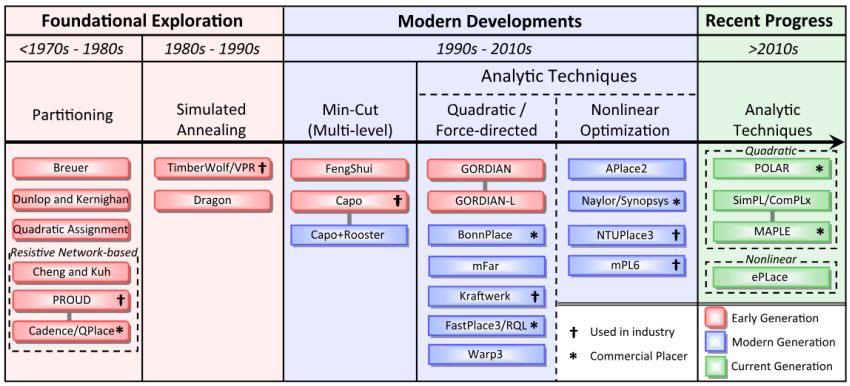

Figure 2: Historical timeline of VLSI placement techniques (Markov) [2]

This is a citation for AMFPlacer. [3]

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