Technical Paper Proposal: Placement Algorithms for Heterogenous FPGAs

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1 Abbreviations

- FPGA: Field Programmable Gate Array
- VLSI: Very Large Scale Integration
- EDA: Electronic Design Automation
- VHSIC: Very High Speed Integrated Circuits
- HDL: Hardware Description Language
- VHDL: VHSIC HDL
- HLS: High Level Synthesis
- PL-PS: Programmable Logic - Processing System
- EDIF: Electronic Design Interchange Format

2 Ideas

- **FPGA**: Field Programmable Gate Array
  - FPGA Vendors:
    - AMD-Xilinx (50% FPGA vendor market share)
    - Intel-Altera (35% share)
    - Lattice
    - Microsemi
- **EDA**: Electronic Design Automation
  - Proprietary software for FPGA and VLSI development:
    - Xilinx - Vivado (Design + Simulation) + Vitis (HLS + PL-PS codesign)
    - Altera - Quartus (Design) + ModelSim (Simulation)

    - Synopsis (VLSI)
    - Cadence (VLSI)
  - Open source software for FPGA development:
    - VTR: a PNR tool popular amongst researchers who study placement techniques
    - OSS-CAD: a full-flow software suite that includes ABC synthesis, Yosys synthesis, Yosys nextpnr.
    - AMF-Placer (Analytical Placer)
    - DREAMPlace (VLSI) + DREAMPlaceFPGA
    - RapidLayout (Hard Block Placer for Systolic Arrays)
    - RapidStream (HLS Placer)
    - RapidWright: Semi-open source API that provides backend access to Xilinx Vivado EDA using design checkpoints.

- **Synthesis**
  - Takes a design written in a high-level HDL like VHDL or Verilog and "synthesizes" a **logical netlist** out of it. This logical netlist is usually generated as an EDIF, JSON, or a low-level Verilog file. This netlist describes the necessary basic elements of logic (BELs) and the wired connections between them that are necessary to implement the design.
- **Placement**
  - Takes the **logical netlist** and produces a **physical netlist**.
- **Routing**
  - Takes the **physical netlist** and maps the connections between BELs onto physical switchboxes.

This is a citation for AMFPlacer. [1]

References

[1] T. Liang, G. Chen, J. Zhao, S. Sinha, and W. Zhang, "Amf-placer: High-performance analytical mixed-size placer for fpga," in *2021 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 1–6, 2021.