Tate Finley
ECE 3140
Testbench Design Explanation

For the testbench for hw5p2 all state transitions were tested. The testbench is reset once before assertions began to start at state A. Then with the input to the finite state machine being 0 we can go from a to b and from b to c. The input was switched to 1 to go from c to d and from d to a. Next we keep the input at 1 to go from a to c then switch the input to 0 to go from c to b. Switch the input to go from b to d and switch the input again to go from d to c. The reset state is set to reset the state back to a and the input is kept at zero resulting in an endless transition from b to c and then c to b for the rest of the simulation. Figure 1 displays the testbench waveform and Figure 2 shows the resulting assertions.

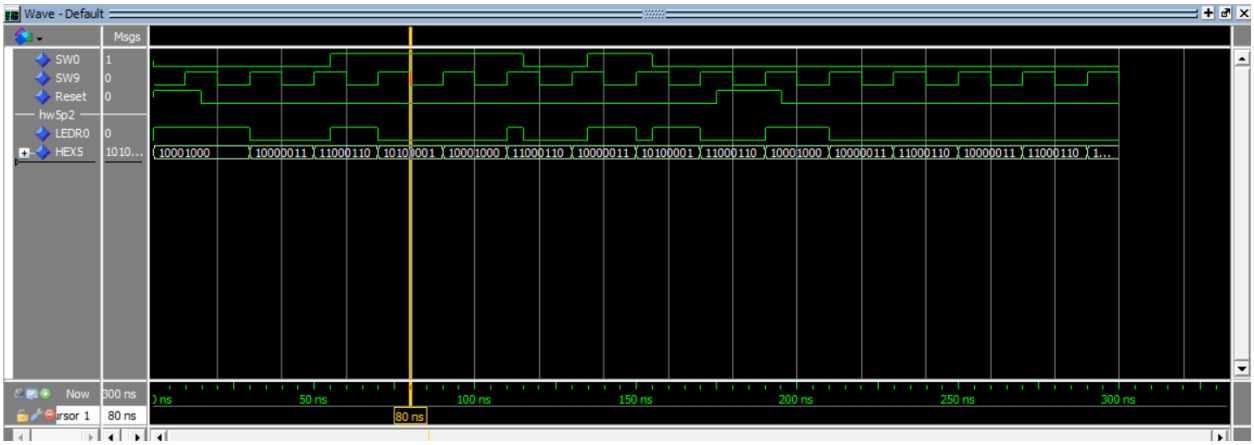

Figure 1: Resulting waveform of hw5p2 testbench

```
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.testbench(bench)
# Loading work.ttu(body)
# Loading work.hw5p2(st)
# Loading work.hw5p1(behavior)
# ** Note: Test for Homework 5 Problem 2
#    Time: 0 ps  Iteration: 0  Instance: /testbench
# ** Note: Test Success
#    Time: 195 ns  Iteration: 0  Instance: /testbench
```

Figure 2: Assert/Report results for hw5p2 testbench.

For the testbench of hw5p3 or question 3 the least significant LFSR was tested to detect a sequence repeat. The least significant LFSR has a period maximally long at 3 bits which ends up being $2^3 - 1 = 7$ which is prime and fits the specifications of the question. The rest of the LFSR's have a maximally long period that is a prime number different from each other. The other LFSR's are 5, 7, 13, and 17 bits long. Asserts are made as the LFSR starts at 000 and transitions to states 001, 011, 110, 101, 010, 100, and back to 000. The least significant LFSR has a bit that is taken from its Lsb for the random 5-bit generator which is reflected in the output for LFSR0 in Figure 3. Figure 3 is the waveform of the testbench, and Figure 4 is the assert report results.

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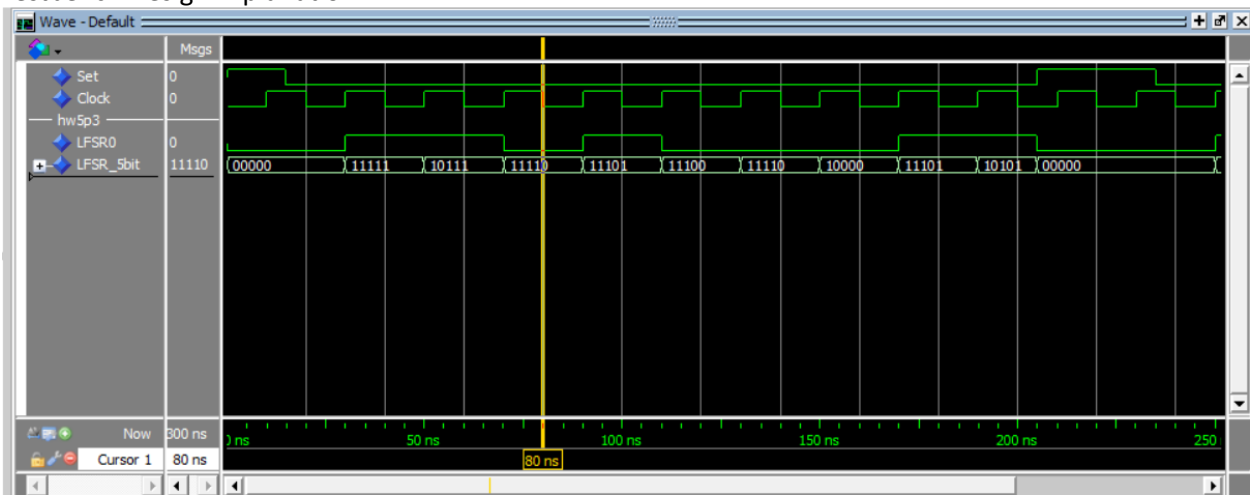

Figure 3: Resulting waveform of hw5p3 testbench. Notice that even when the sequence for LFSR0 repeats, the 5-bit LFSR has a different value. Example is taken from 50 ns and 180 ns.

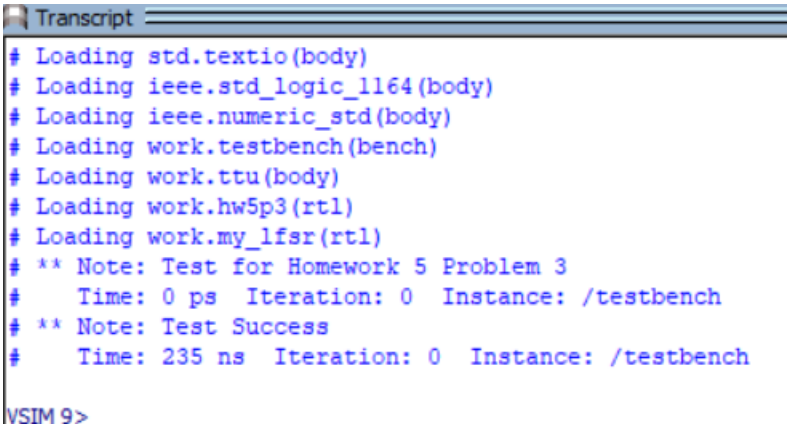

Figure 4: Assert/Report results for hw5p3 testbench.