Tate Finley
ECE 3140
HW3

Summary for each homework problem 4.2-4.10

The testbench for Problem 4.2 meets specification because the expected output for functions F and G matches the calculated output using truth tables and Karnaugh maps. The waveforms were tested both in EDAplayground and Modelsim resulting in the same waveform being depicted in Figure 1a below. The assert report was made so that if any discrepancies were to arise with conflicted logic done mathematically, it would output an error stating which function failed. Based on the report generated in Figure 1b, the design has passed all specifications.

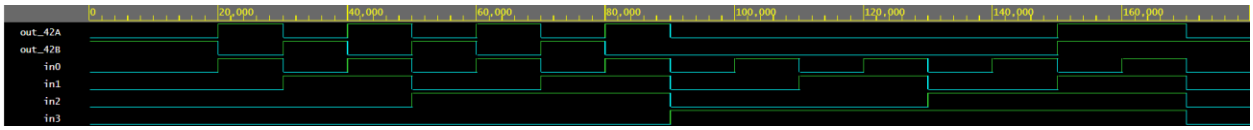

Figure 1a: Waveform for Problem 4.2 using EDAplayground.

```
# EXECUTION:: NOTE    : Test for Problem 4.2
# EXECUTION:: Time: 0 ps,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
# EXECUTION:: NOTE    : Test Success
# EXECUTION:: Time: 180 ns,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
```

Figure 1b: Assert report for Problem 4.2

The testbench for Problem 4.4 meets specification because the expected output for the combinational circuit in part a, and the combinational circuit in part b matches the calculated output of their respective logic proved using truth tables and Karnaugh maps. The waveforms were tested both in EDAplayground and Modelsim resulting in the same waveform being depicted in Figure 2a below. The assert report was made so that if any discrepancies were to arise with conflicted logic done mathematically, it would output an error stating which function failed. Based on the report generated in Figure 2b, the design has passed all specifications.

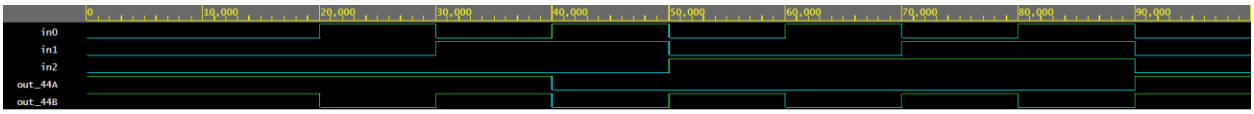

Figure 2a: Waveform for Problem 4.4 using EDAplayground

```
# EXECUTION:: NOTE    : Test for Problem 4.4
# EXECUTION:: Time: 0 ps,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
# EXECUTION:: NOTE    : Test Success
# EXECUTION:: Time: 100 ns,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
```

Figure 2b: Assert report for Problem 4.4

The testbench for Problem 4.7 meets specification because the expected output for the Gray code to a binary number matches the calculated output of their logic proved using truth tables and Karnaugh maps, and by building the circuit using only exclusive or gates. The waveforms were tested both in EDAplayground and Modelsim resulting in the same waveform being depicted in Figure 3a below.

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The assert report was made so that if any discrepancies were to arise with conflicted logic done mathematically, it would output an error stating which function failed. Based on the report generated in Figure 3b, the design has passed all specifications.

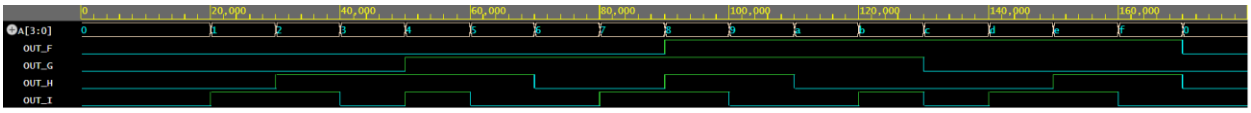

Figure 3a: Waveform for Problem 4.7 using EDAplayground. The output closest to the vector A is the Msb while Out_I is the Lsb.

```
# EXECUTION:: NOTE    : Test for Problem 4.7
# EXECUTION:: Time: 0 ps,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
# EXECUTION:: NOTE    : Test Success
# EXECUTION:: Time: 180 ns,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
```

Figure 3b: Assert report for Problem 4.7

The testbench for Problem 4.9 meets specification because the expected output for the BCD to seven segment matches the calculated output of their logic proved using truth tables and Karnaugh maps. The waveforms were tested both in EDAplayground and Modelsim resulting in the same waveform being depicted in Figure 4a below. The assert report was made so that if any discrepancies were to arise with conflicted logic done mathematically, it would output an error stating which function failed. Based on the report generated in Figure 4b, the design has passed all specifications.

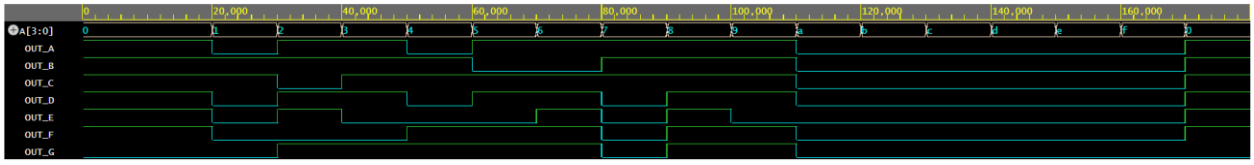

Figure 4a: Waveform for Problem 4.9 using EDAplayground. The output letters correspond to their lettering on the seven segment display.

```
# EXECUTION:: NOTE    : Test for Problem 4.9
# EXECUTION:: Time: 0 ps,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
# EXECUTION:: NOTE    : Test Success
# EXECUTION:: Time: 180 ns,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
```

Figure 4b: Assert report for Problem 4.9

The testbench for Problem 4.10 meets specification because the expected output for calculating the two's complement matches the calculated output of their logic proved using truth tables and Karnaugh maps, and by using exclusive or gates in the circuit as specified by the problem. The waveforms were tested both in EDAplayground and Modelsim resulting in the same waveform being depicted in Figure 5a below. The assert report was made so that if any discrepancies were to arise with conflicted logic done mathematically, it would output an error stating which function failed. Based on the report generated in Figure 5b, the design has passed all specifications.

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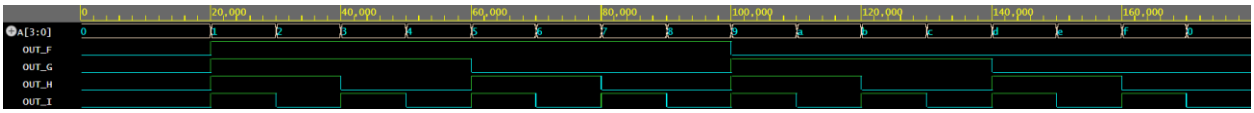

Figure 5a: Waveform for Problem 4.10 using EDAplayground. The output closest to the vector A is the Msb while Out_I is the Lsb.

```
# EXECUTION:: NOTE    : Test for Problem 4.10
# EXECUTION:: Time: 0 ps,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
# EXECUTION:: NOTE    : Test Success
# EXECUTION:: Time: 180 ns,  Iteration: 0,  Instance: /testbench,  Process: stimulus.
```

Figure 5b: Assert report for Problem 4.10