

For the testbench for the hw4p1 entity, I tested all switch outputs and tested pushbutton combinations that produced a unique result. Figure 1 displays the resulting testbench results and the first 300ns of the waveform. In Figure 2, the pushbutton combinations tested were 11, 01, and 10 as each input allowed for a unique output. The combination 00 was tested for one input because the design was made so that Key 0 for blanking the LED would override Key 1 for implementing the complement of the switch input. As outlined in HW4, this design was made from entity hw3p42 so the output for hw4p1 when both pushbuttons were released ("11" as outlined in the DE10-Lite User Manual) reflects the output expected from hw3p42's structural architecture.

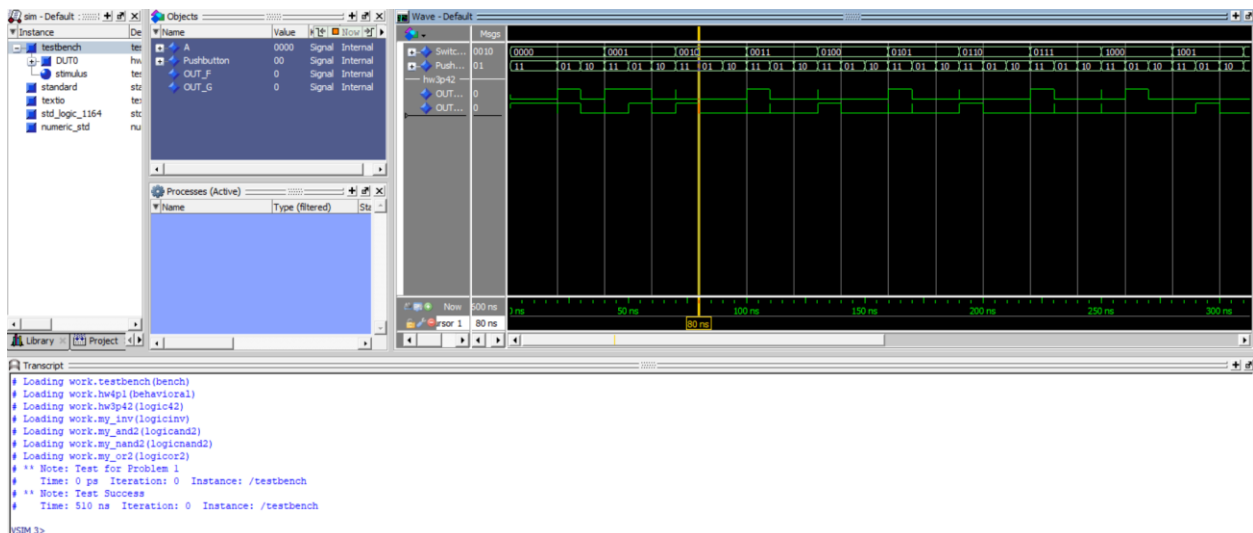


Figure 1: Resulting output waveform for the first 300ns of the testbench. Vector A was renamed to Switch, OUT_F renamed to OUT_F1, and OUT_G renamed to OUT_F2.

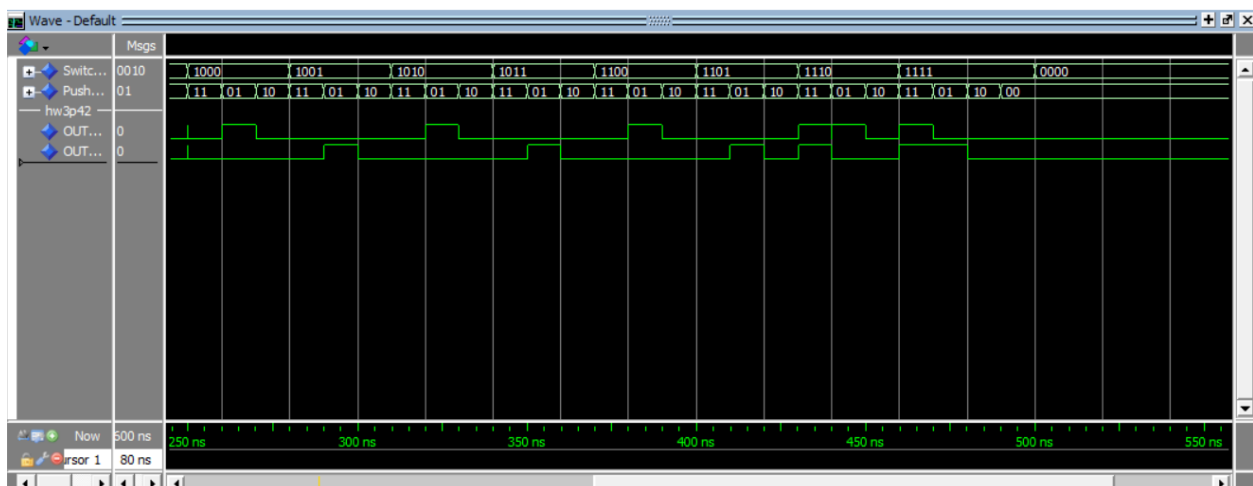


Figure 2: Second half of the testbench waveform for entity hw4p1.

For the implementation of the bin2seg7 entity all possible combinations of the inData vector were tested. All combinations between the dispHex, blanking, and dispPoint bits were tested independently for all outputs. The blanking bit was tested first and involved the use of flipping the

Testbench Explanations HW4

The screenshot shows the Vivado IDE interface during a simulation. The top panel displays the 'Objects' tree with the testbench hierarchy. The middle panel shows the 'Processes (Active)' table. The bottom panel displays the 'Wave-Default' window with a timing diagram showing signals like hexValue, point, OUT_A, OUT_B, OUT_C, OUT_D, OUT_E, OUT_F, OUT_G, OUT_Point, bin2seg7, seg_A, seg_B, seg_C, seg_D, seg_E, seg_F, seg_G, and seg_Lms. The bottom status bar shows the simulation time as 260 ns.

Figure 4: Seven Segment output reference. From Manual, logic 0 indicates high.