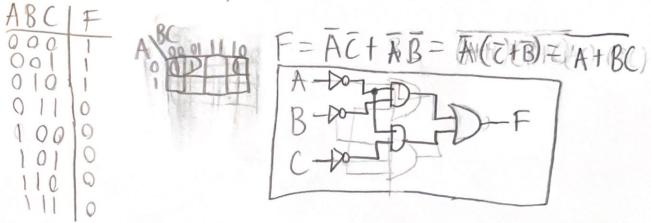
Take Finley ECE 3140 HW3 Problem 4.2 Obtain the simplified Boolean expressions for output F and G in terms of the input variables in the circuit Of Fig. P4.2 A (AID) - CHORE ANDD AIBC MELALADRAD ABCD Fis. P4.2 ADPGate)1 Gate 2 Gate 3 (A+D) ABCD BC ADD = (A+D) => ABCIAD 0000 Gate 4 Gate 5 Gate F youtput F 0001 0 ACATO) Ā+BC (A+D)(Ā+BC) OF ADABCHAD TO HABCHAD+BCD 100 A-TO = A+D ABC+AD+ABCD+ABCD Gale G 7 output G F=ABC+AD 000 001 (A+D)(A+BC) 9+ABC+AD+BCD 0 0 ABCTADTABCDTABCD G=ABC+AD

Tate Finley ECE 3140 HW 3 Problem 4.4

Design a combinational circuit with three inputs and, and

a) The output is I when the binary value of the inputs is less than 3. the output is Orother wise



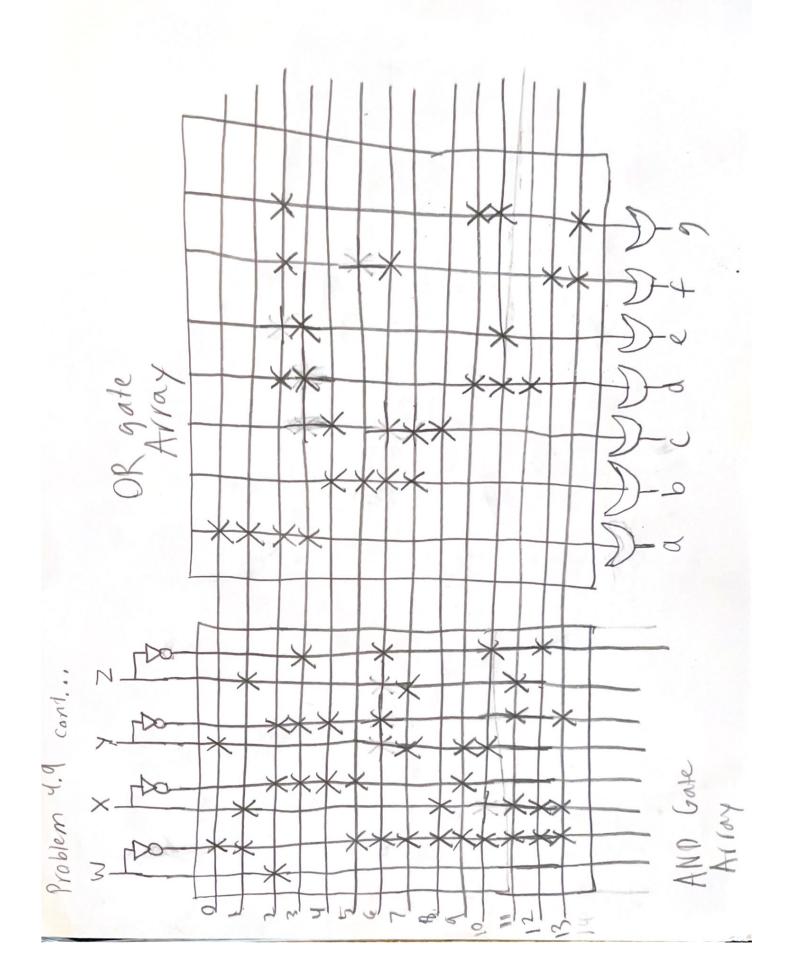
b) The output is I when the binary value of the inputs is an even number

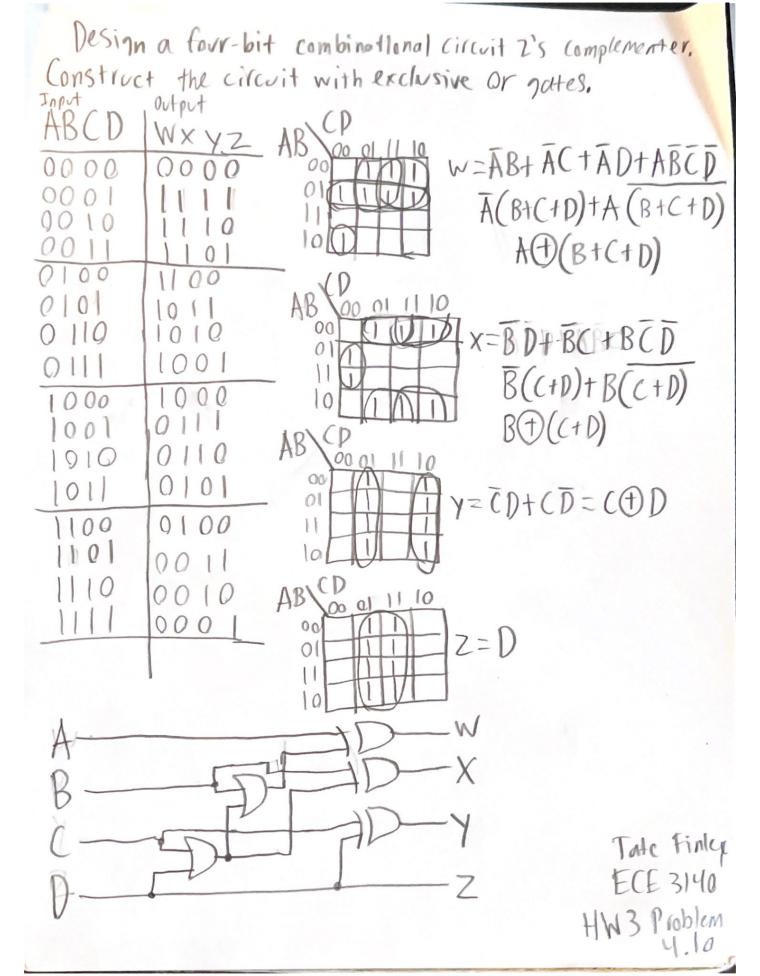
ABC 000 001 010 100	6	A BC ON 11 10	G= E	A B C-Do-	_6
110	10				

Tate Finley ECE 3140 HW3 Problem 4.7

Design a combinational circuit that converts a four bit Gray code to a four-bit binary number using exclusive OR gates

Tate Finley E(E 3140 HW3 Problem 4.9 Using a truth table and kainough maps, design the B(D-to-seven-segment decoder using a minimum number of gates. The six involid combinations should result in a blank WX YZ a= WY+WXZ+WXY+XYZ o Bplay. WXYZ abcdefg 001 0000 0001 ONNIN 6= XY+WX+WYZ+WYZ C=XY+WX+WYZ d=WXY+XYZ+WXY... WYZ+WXYZ 0000000 0000000 1100 0000000 XW 00 00 00 00 C 000 01 11 10 C= XYZ+WYZ 0000000 YZWYYXWYZ WXYYWYZ YZ 00 01 11 10 J=WXY+WXY+WXY+WYZ





Take Finley ECE 3140 HW3 Problem 8 Design the minimal SOP circuit to implement the function F(a,b,c)=SUM m(1,5,6,7) F=bc+ab