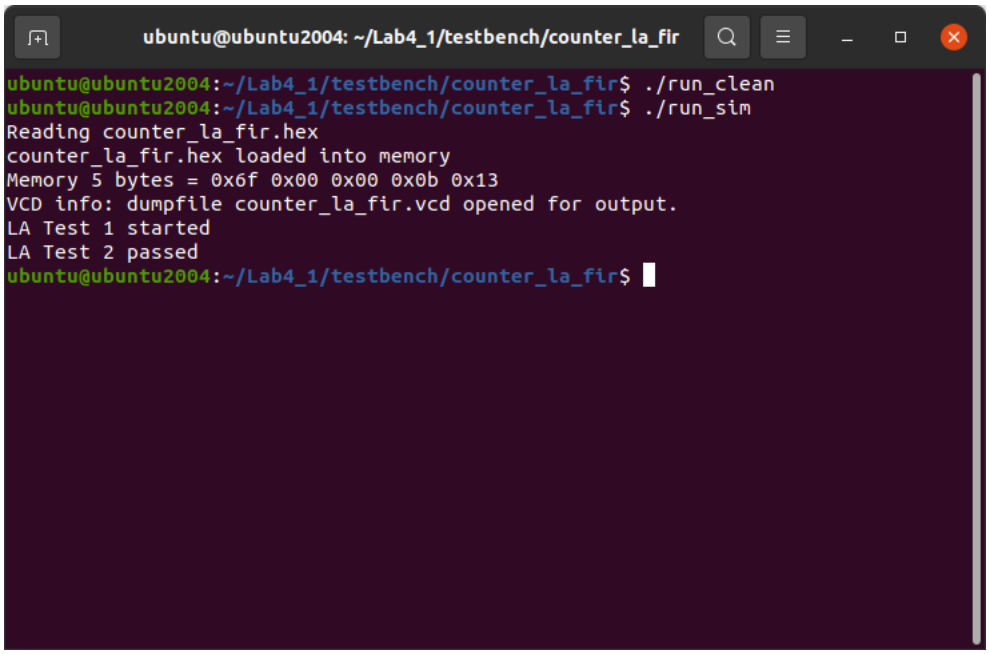
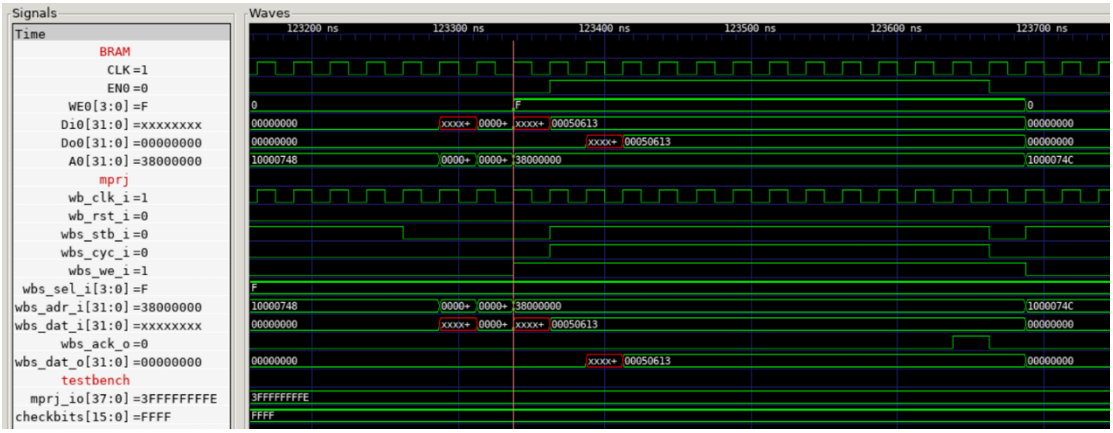
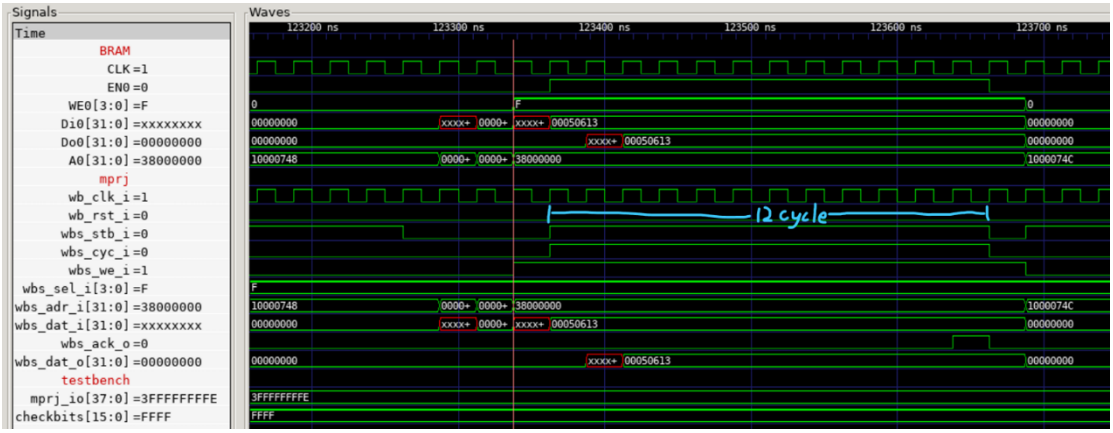
TB Pass



Interface between BRAM and wishbone





FSM

```
    always @(posedge clk) begin
        if (rst) begin
            delay_count <= 0;
            ready <= 0;
        end else begin
            ready <= 0;
            if (valid && !ready) begin
                if (delay_count == DELAYS) begin
                    ready <= 1;
                    delay_count <= 0;
                end else begin
                    delay_count <= delay_count + 1;
                end
            end
        end
    end
```