Lab 3 Verilog FIR Design Report

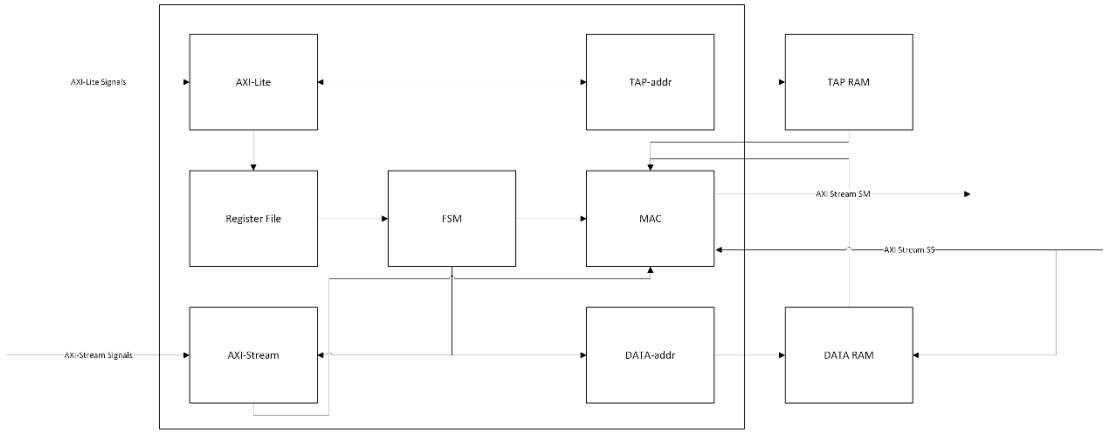
胡致远

Hu Zhiyuan

EESM6000C SoC Laboratory

March 2025

Block Diagram



Operation

In this lab, we aim to construct a Finite Impulse Response (FIR) operation module with 11 coefficients to perform filtering. The module's data must adhere to the AXI-Stream protocol.

1. AXI-Lite Interface

Configuration Management:

Handles writes for tap coefficients (awaddr ⩾ 0x20) and control signals (ap_start, data_length at awaddr=0x00 and 0x10).

Reads status signals (ap_done, ap_idle) via araddr=0x00.

2. Initialization Phase

IDLE State:

Configuration register set to 32'h04.

Host writes tap coefficients to Tap_RAM (addresses 0x20 to 0x48) and data_length to awaddr=0x10.

Tap_RAM Initialization: Coefficients stored sequentially at addresses 0, 4, 8, ..., 40.

3. Transition to CAL State

Start Signal:

Host sets ap_start=1 (awaddr=0x00), transitioning to CAL state.

Data Loading:

AXI-Stream input ss_tdata writes raw data into Data_RAM using a sliding window address pattern (e.g., 0, 40, 36, ..., 4 for the first input).

4. Address Generation Logic

Tap_RAM Access:

Coefficients read sequentially at 0, 4, 8, ..., 40 (11-tap cycle).

Data_RAM Access:

Addresses follow a sliding window:

1st iteration: 0, 40, 36, ..., 4

2nd iteration: 4, 0, 40, ..., 8

Continues until the 11th iteration.

5. Computation Phase

MAC Unit Operation:

tap_Do (coefficients) and data_Do (input data) are multiplied and accumulated into FIR_temp over 12 cycles (fir_cycle_cnt).

After 11 iterations, sm_tvalid asserts to output the result sm_tdata (Y).

6. Completion and Output

Data Length Tracking:

Internal counter fir_data_cnt tracks processed data blocks.

When fir_data_cnt == data_length, ss_tlast asserts, and the final result triggers sm_tlast and ap_done.

State Transition:

System enters DONE state after final computation, resetting to IDLE upon status read.

7. Timing Optimization

BRAM Latency Compensation:

SS_data (input) is delayed by 1 cycle via flip-flop (FF) to align with data_Do availability.

Preloading First Tap:

First coefficient is preloaded at CAL state entry to eliminate tap_Do wait cycles.

Resource Usage

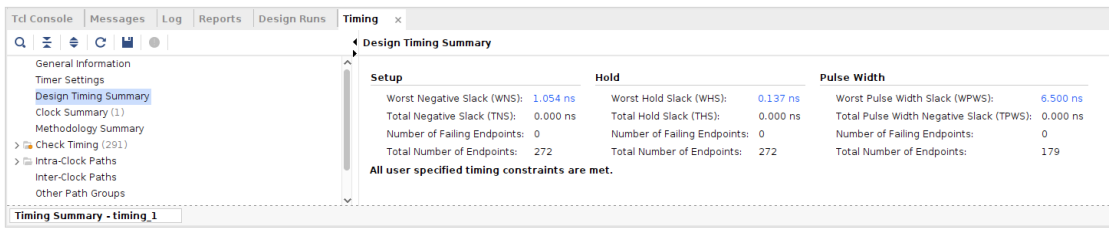
FF and LUT

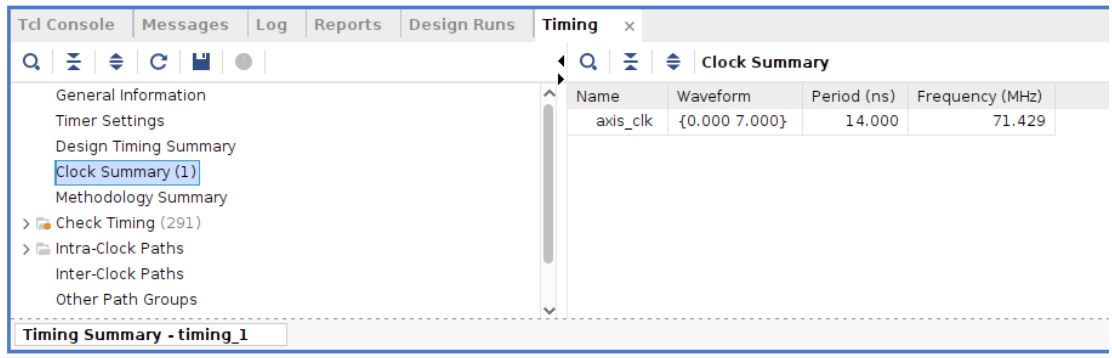
Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	277	0	0	53200	0.52
LUT as Logic	277	0	0	53200	0.52
LUT as Memory	0	0	0	17400	0.00
Slice Registers	178	0	0	106400	0.17
Register as Flip Flop	178	0	0	106400	0.17
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

BRAM

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

Timing Report



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Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             1.054ns  (required time - arrival time)
  Source:                 fir_cycle_cnt_reg[4]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.000ns period=14.000ns})
  Destination:            FIR_temp_reg[29]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.000ns period=14.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            14.000ns  (axis_clk rise@14.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        12.841ns  (logic 8.772ns (68.310%)  route 4.069ns (31.690%))
  Logic Levels:           12  (CARRY4=5 DSP48E1=2 LUT2=2 LUT3=2 LUT5=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 16.128 - 14.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock axis_clk rise edge)
                                                    0.000     0.000 r
                                                    0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                 0.000     0.000    axis_clk
                                                                       r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)       0.972     0.972 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)       0.800     1.771    axis_clk_IBUF
                                                                       r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)       0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=178, unplaced)     0.584     2.456    axis_clk_IBUF_BUFG
                         FDCE                                          r  fir_cycle_cnt_reg[4]/C
  -------------------------------------------------------------------    -------------------
                         FDCE (Prop_fdce_C_Q)       0.478     2.934 r  fir_cycle_cnt_reg[4]/Q
                         net (fo=6, unplaced)       0.773     3.707    in13[6]
                                                                       r  ss_tready_OBUF_inst_i_2/I0
                         LUT3 (Prop_lut3_I0_O)      0.319     4.026 r  ss_tready_OBUF_inst_i_2/O
                         net (fo=7, unplaced)       0.484     4.510    ss_tready_OBUF_inst_i_2_n_0
                                                                       r  mult_result_i_16/I1
                         LUT5 (Prop_lut5_I1_O)      0.124     4.634 r  mult_result_i_16/O
                         net (fo=32, unplaced)      0.520     5.154    mult_result_i_16_n_0
                                                                       r  mult_result__0_i_1/I1
                         LUT3 (Prop_lut3_I1_O)      0.124     5.278 r  mult_result__0_i_1/O
                         net (fo=1, unplaced)       0.800     6.078    mult_input[16]
                                                                       r  mult_result__0/A[16]
                         DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[47])
                                                    4.036    10.114 r  mult_result__0/PCOUT[47]
                         net (fo=1, unplaced)       0.055    10.169    mult_result__0_n_106
                                                                       r  mult_result__1/PCIN[47]
                         DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
                                                    1.518    11.687 r  mult_result__1/P[0]
                         net (fo=2, unplaced)       0.800    12.487    mult_result__1_n_105
                                                                       r  FIR_temp[16]_i_13/I0
                         LUT2 (Prop_lut2_I0_O)      0.124    12.611 r  FIR_temp[16]_i_13/O
                         net (fo=1, unplaced)       0.000    12.611    FIR_temp[16]_i_13_n_0
                                                                       r  FIR_temp_reg[16]_i_10/S[1]
                         CARRY4 (Prop_carry4_S[1]_CO[3])
                                                    0.533    13.144 r  FIR_temp_reg[16]_i_10/CO[3]
                         net (fo=1, unplaced)       0.009    13.153    FIR_temp_reg[16]_i_10_n_0
                                                                       r  FIR_temp_reg[20]_i_10/CI
                         CARRY4 (Prop_carry4_CI_CO[3])
                                                    0.117    13.270 r  FIR_temp_reg[20]_i_10/CO[3]
                         net (fo=1, unplaced)       0.000    13.270    FIR_temp_reg[20]_i_10_n_0
                                                                       r  FIR_temp_reg[24]_i_10/CI
                         CARRY4 (Prop_carry4_CI_O[3])
                                                    0.331    13.601 r  FIR_temp_reg[24]_i_10/O[3]
                         net (fo=2, unplaced)       0.620    14.220    mult_result__3[27]
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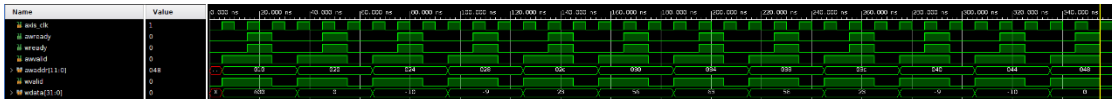
                                                0.331    13.601 r  FIR_temp_reg[24]_i_10/O[3]
                         net (fo=2, unplaced)         0.629    14.230    mult_result__3[27]
                                                                 r  FIR_temp[24]_i_2/I0
                         LUT2 (Prop_lut2_I0_O)        0.302    14.532 r  FIR_temp[24]_i_2/O
                         net (fo=1, unplaced)         0.000    14.532    FIR_temp[24]_i_2_n_0
                                                                 r  FIR_temp_reg[24]_i_1/DI[3]
                         CARRY4 (Prop_carry4_DI[3]_CO[3])
                                                      0.429    14.961 r  FIR_temp_reg[24]_i_1/CO[3]
                         net (fo=1, unplaced)         0.000    14.961    FIR_temp_reg[24]_i_1_n_0
                                                                 r  FIR_temp_reg[28]_i_1/CI
                         CARRY4 (Prop_carry4_CI_O[1])
                                                      0.337    15.298 r  FIR_temp_reg[28]_i_1/O[1]
                         net (fo=1, unplaced)         0.000    15.298    FIR_temp_reg[28]_i_1_n_6
                         FDCE                                           r  FIR_temp_reg[29]/D
    ----------------------------------------------------------------    -------------------

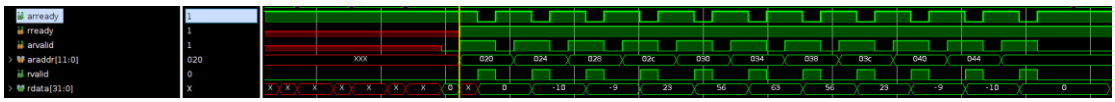
                         (clock axis_clk rise edge)
                                                     14.000    14.000 r
                                                      0.000    14.000 r  axis_clk (IN)
                         net (fo=0)                   0.000    14.000    axis_clk
                                                                 r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)         0.838    14.838 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)         0.760    15.598    axis_clk_IBUF
                                                                 r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)         0.091    15.689 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=178, unplaced)       0.439    16.128    axis_clk_IBUF_BUFG
                         FDCE                                           r  FIR_temp_reg[29]/C
                         clock pessimism              0.184    16.311
                         clock uncertainty           -0.035    16.276
                         FDCE (Setup_fdce_C_D)        0.076    16.352    FIR_temp_reg[29]
    ----------------------------------------------------------------
                         required time                         16.352
                         arrival time                         -15.298
    ----------------------------------------------------------------
                         slack                                 1.054
```

Simulation waveform

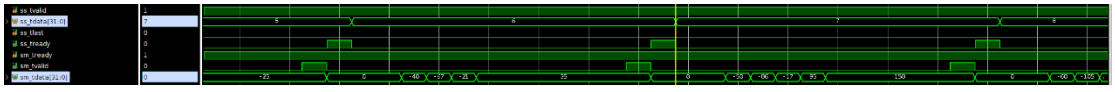
Coefficient program



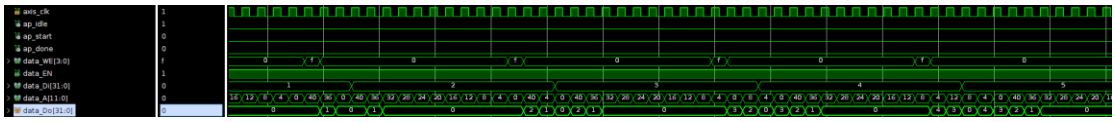
Read back



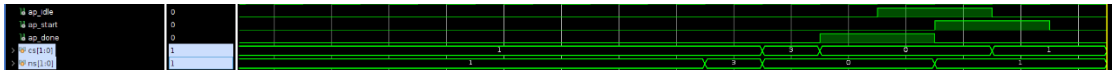
Data-in Stream-in && Data-out Stream-OUT



RAM access control



FSM



Github: https://github.com/TouHou-Yukari/EESM6000C-SoC-Laboratory