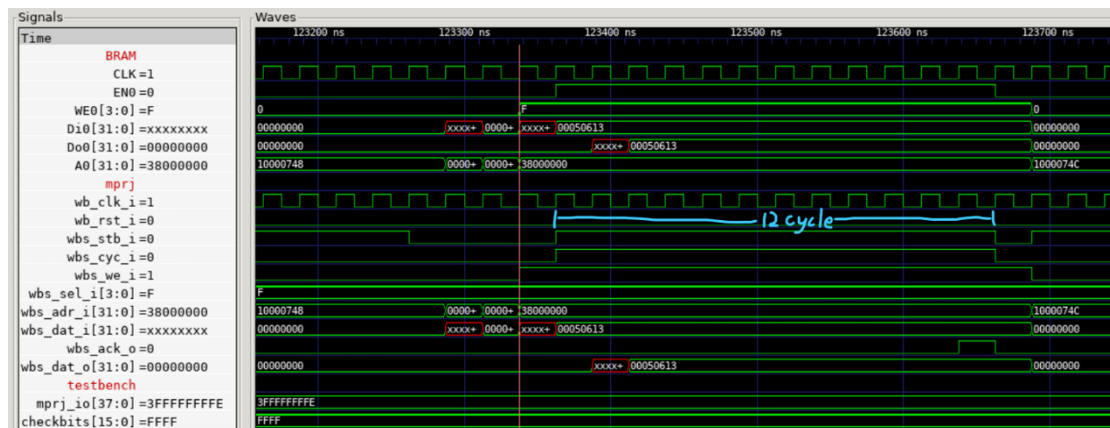
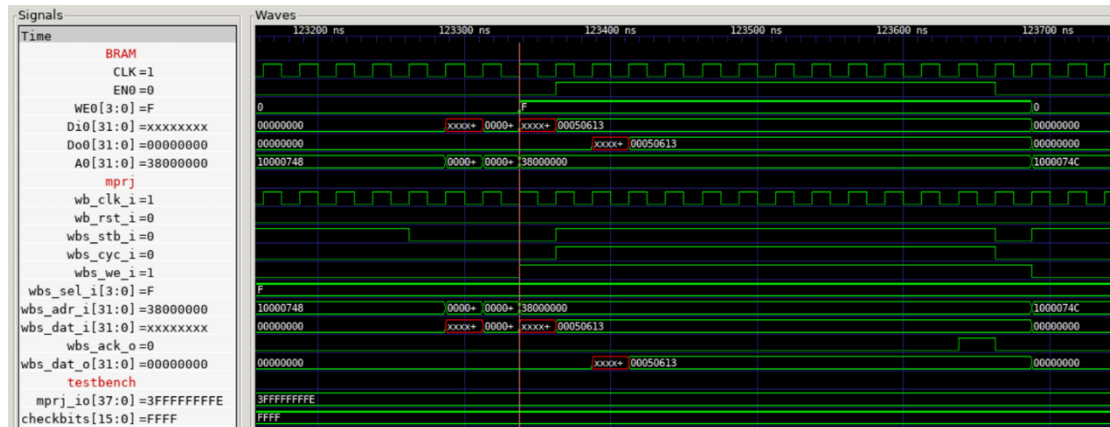
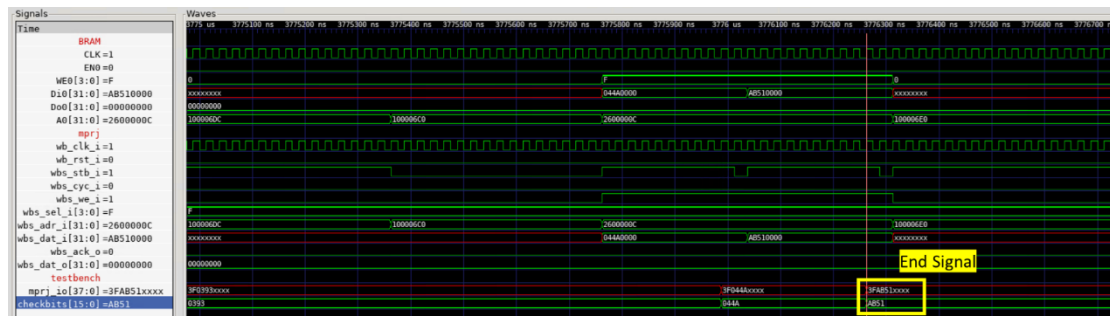


TB Pass

```
ubuntu@ubuntu2004: ~/Lab4_1/testbench/counter_la_fir
ubuntu@ubuntu2004:~/Lab4_1/testbench/counter_la_fir$ ./run_clean
ubuntu@ubuntu2004:~/Lab4_1/testbench/counter_la_fir$ ./run_sim
Reading counter_la_fir.hex
counter_la_fir.hex loaded into memory
Memory 5 bytes = 0x6f 0x00 0x00 0x0b 0x13
VCD info: dumpfile counter_la_fir.vcd opened for output.
LA Test 1 started
LA Test 2 passed
ubuntu@ubuntu2004:~/Lab4_1/testbench/counter_la_fir$
```

Interface between BRAM and wishbone





FSM

```

always @(posedge clk) begin
    if (rst) begin
        delay_count <= 0;
        ready <= 0;
    end else begin
        ready <= 0;
        if (valid && !ready) begin
            if (delay_count == DELAYS) begin
                ready <= 1;
                delay_count <= 0;
            end else begin
                delay_count <= delay_count + 1;
            end
        end
    end
end

```

