
STM32
CubeMX

1. Description

1.1. Project

Project Name	TIM_DashBoard
Board Name	custom
Generated with:	STM32CubeMX 6.4.0
Date	02/25/2022

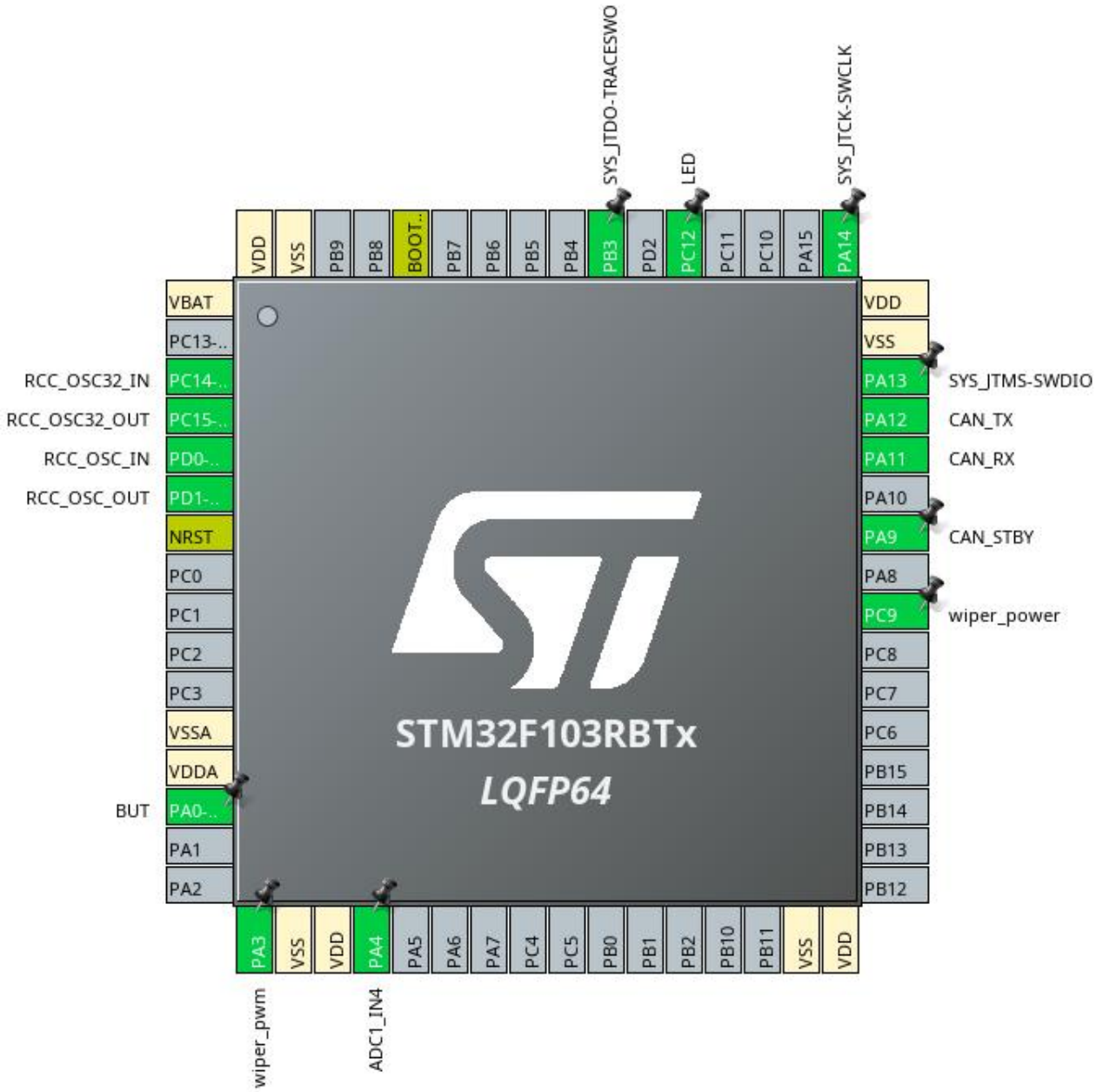
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RBTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration

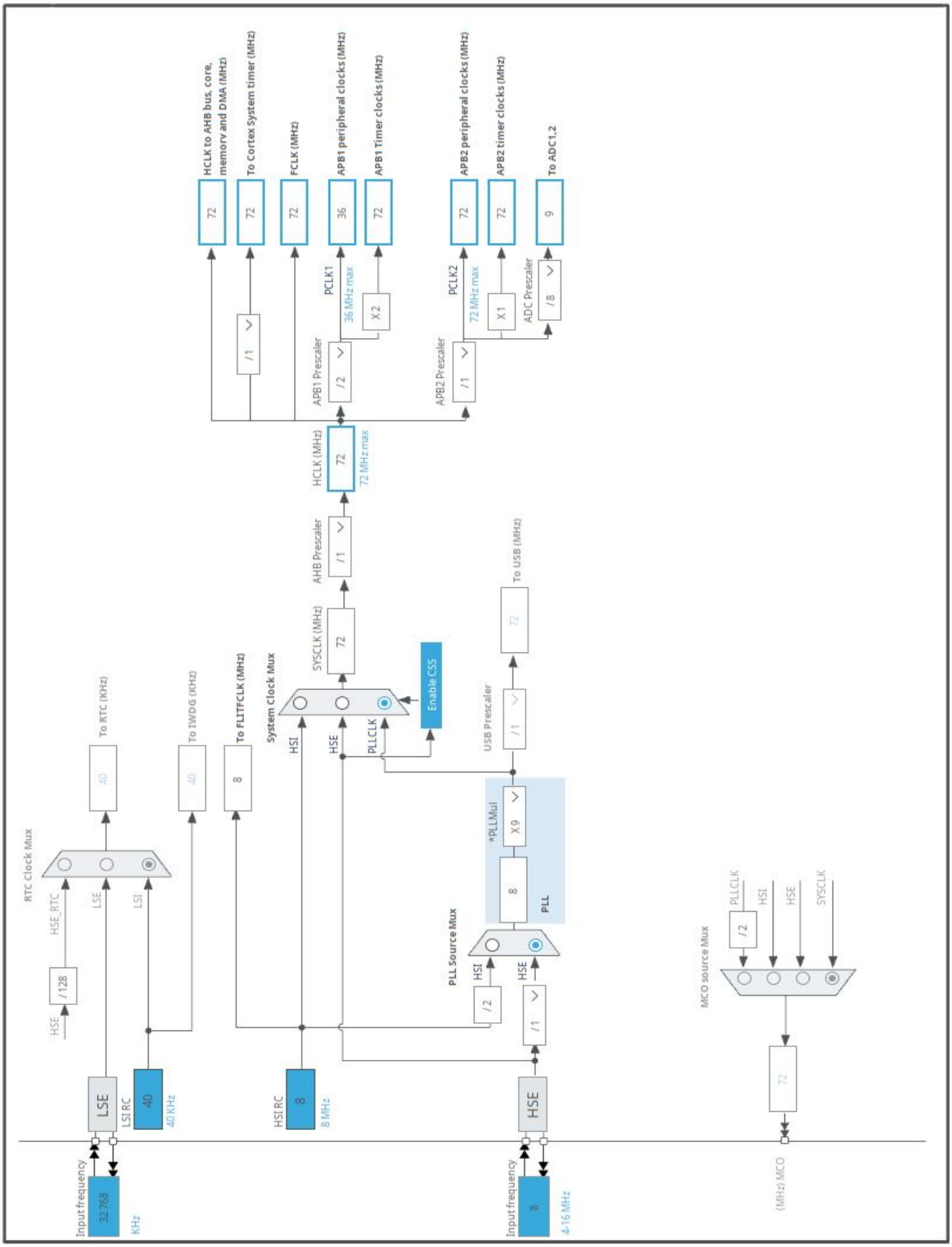


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	GPIO_EXTI0	BUT
17	PA3	I/O	TIM2_CH4	wiper_pwm
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
31	VSS	Power		
32	VDD	Power		
40	PC9 *	I/O	GPIO_Output	wiper_power
42	PA9 *	I/O	GPIO_Output	CAN_STBY
44	PA11	I/O	CAN_RX	
45	PA12	I/O	CAN_TX	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
53	PC12 *	I/O	GPIO_Output	LED
55	PB3	I/O	SYS_JTDO-TRACESWO	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	TIM_DashBoard
Project Folder	/home/prince/Seafile/Organisation/TIM/Projet
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_CAN_Init	CAN
4	MX_TIM2_Init	TIM2
5	MX_DMA_Init	DMA
6	MX_ADC1_Init	ADC1
7	MX_TIM4_Init	TIM4
8	MX_TIM1_Init	TIM1
9	MX_TIM3_Init	TIM3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RBTx
Datasheet	DS5319_Rev17

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

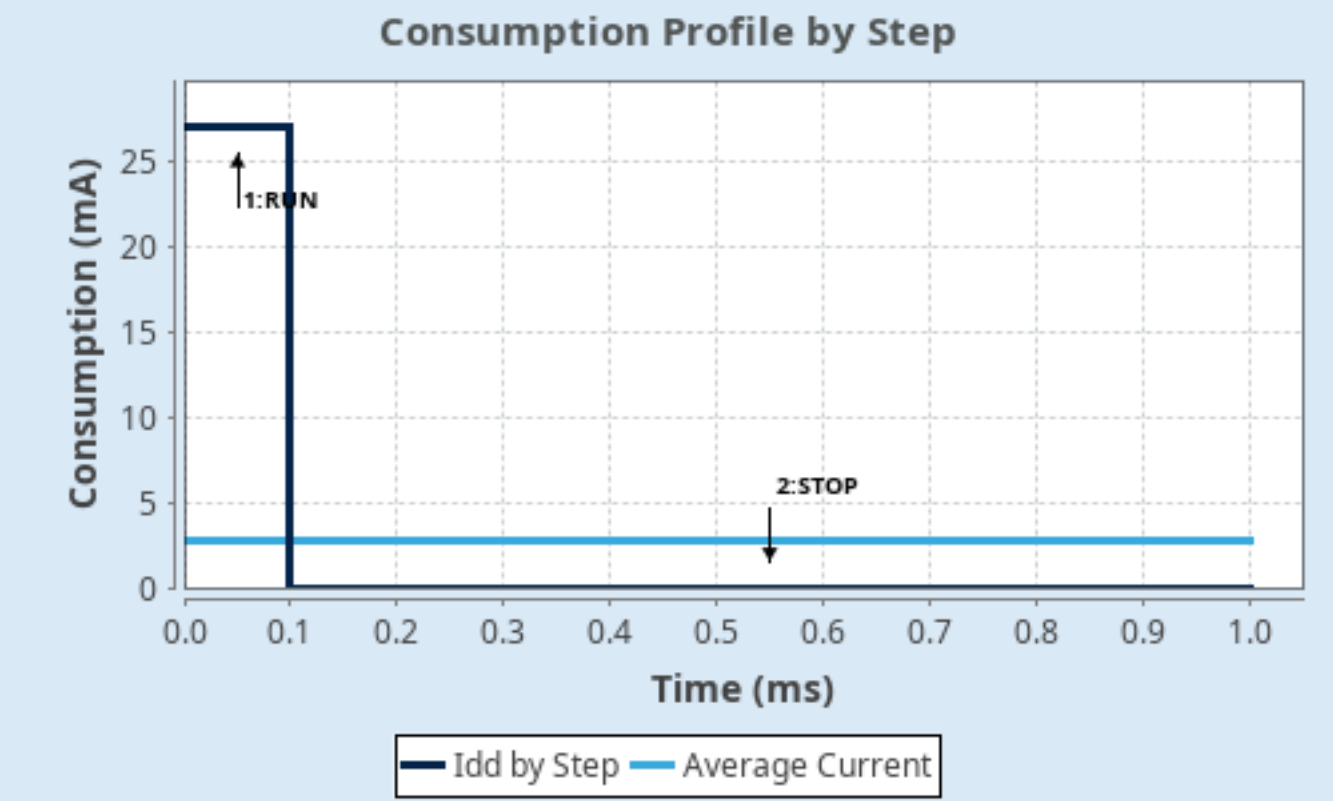
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27 mA	14 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	100.99	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.71 mA
Battery Life	1 month, 21 days, 17 hours	Average DMIPS	61.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN4

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 4
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CAN

mode: Activated

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**9 ***
Time Quantum	**250.0 ***
Time Quanta in Bit Segment 1	**13 Times ***
Time Quanta in Bit Segment 2	**2 Times ***
Time for one Bit	**4000 ***
Baud Rate	**250000 ***
ReSynchronization Jump Width	**4 Times ***

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Test Mode	Normal

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.4. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**720-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000-1 ***

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.6. TIM2

Clock Source : Internal Clock

Channel4: PWM Generation CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**720-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	**Disable ***
Fast Mode	Disable
CH Polarity	High

7.7. TIM3

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**7200-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000-1 ***

Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. TIM4

mode: Clock Source

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**7200-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	n/a	n/a	
CAN	PA11	CAN_RX	Input mode	No pull-up and no pull-down	n/a	
	PA12	CAN_TX	Alternate Function Push Pull	n/a	**High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
TIM2	PA3	TIM2_CH4	Alternate Function Push Pull	n/a	Low	wiper_pwm
GPIO	PA0-WKUP	GPIO_EXTI0	**External Interrupt Mode with Rising/Falling edge**	No pull-up and no pull-down	n/a	BUT
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	wiper_power
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CAN_STBY
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
MEMTOMEM	DMA1_Channel2	Memory To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

MEMTOMEM: DMA1_Channel2 DMA request Settings:

Mode:	Normal
Src Memory Increment:	Disable
Dst Memormy Increment:	Disable
Src Memory Data Width:	**Half Word ***
Dst Memormy Data Width:	**Half Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line0 interrupt	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	0	0
USB low priority or CAN RX0 interrupts	true	0	0
CAN RX1 interrupt	true	0	0
TIM1 break interrupt	true	0	0
TIM1 update interrupt	true	0	0
TIM1 trigger and commutation interrupts	true	0	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USB high priority or CAN TX interrupts	unused		
CAN SCE interrupt	unused		
TIM1 capture compare interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line0 interrupt	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel2 global interrupt	false	true	true
ADC1 and ADC2 global interrupts	false	true	true
USB low priority or CAN RX0 interrupts	false	true	true
CAN RX1 interrupt	false	true	true
TIM1 break interrupt	false	true	true
TIM1 update interrupt	false	true	true
TIM1 trigger and commutation interrupts	false	true	true
TIM2 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/CD00161566.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/CD00171190.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00228163.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00283419.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/CD00190234.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00164185.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167326.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00032987.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033267.pdf
Application note	http://www.st.com/resource/en/application_note/DM00033344.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00052530.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf

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Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00325582.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf