

# 四川大学期末考试试题（闭卷）

## （2019——2020 学年第 1 学期） A 卷

课程号：304131030      课序号：      课程名称：数字逻辑（双语）      任课教师：      成绩：  
 适用专业年级：2019 级      学生人数：      印题份数：      学号：      姓名：

### 考生承诺

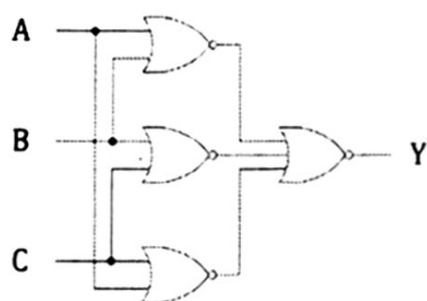
我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

- 1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；
- 2、不带手机进入考场；
- 3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

1. Choose the best answer from the four choices(20 points, 2 points per question).

- (1) The output of an AND gate is LOW when (      ).  
 A. any input is LOW    B. all inputs are LOW    C. no inputs are LOW    D. Both (A) and (B)
- (2) The two types of gates which are called universal gates are (      ).  
 A. AND/OR    B. NAND/NOR    C. AND/NAND    D. OR/NOR
- (3) The logical expression of the following logic circuit diagram is (      ).



- A.  $\overline{(A+B)(B+C)(A+C)}$

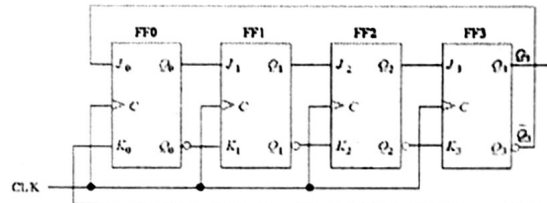
C.  $\overline{(AB)(BC)(AC)}$

B.  $\overline{(A+B)+(B+C)+(A+C)}$

D.  $\overline{(AB)+(BC)+(AC)}$
- (4) With the inputs  $A=1, B=0, C_{in}=1$ , the outputs of the Full Adder is (      ).  
 A.  $C_{out}=0, Sum=0$ ;    B.  $C_{out}=1, Sum=0$ ;    C.  $C_{out}=0, Sum=1$ ;    D.  $C_{out}=1, Sum=1$ ;
- (5)  $F = f(A,B) = \sum m(1, 2)$ , select the right answer for  $\bar{F}$ . (      )  
 A.  $\bar{F} = m_1 + m_2$     B.  $\bar{F} = A \odot B$     C.  $\bar{F} = M_1 M_2$     D.  $\bar{F} = m_1 m_2$
- (6) Which of the following combinations of logic gates can decode binary 1101 with active-HIGH? (      )  
 A. One 4-input AND gate    B. One 4-input AND gate, one inverter  
 C. One 4-input AND gate, one OR gate    D. One 4-input NAND gate, one inverter

第      页，共      页  
 试卷编号：

- (7) An example of a data storage device is ( )  
 A. the logic gate B. the comparator C. the register D. the multiplier
- (8) The reset state of a D latch occurs when ( )  
 A. D=0 B. D=1 C. D=0 or 1 D. D=0 and 1
- (9) A 4-bit binary up/down counter is in the state of 1111. The next 4th state in the UP mode is ( ) .  
 A. 0000 B. 1011 C. 1100 D. 0011
- (10) The circuit shown is a ( )



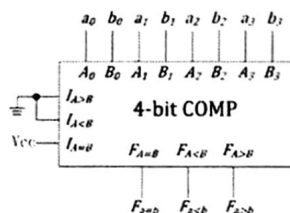
- A. serial-in/parallel-out shift register B. serial-in/serial-out shift register  
 C. ring counter D. Johnson counter

2. Fill in the blanks with the correct answer.(20 points, 2 points per blank)

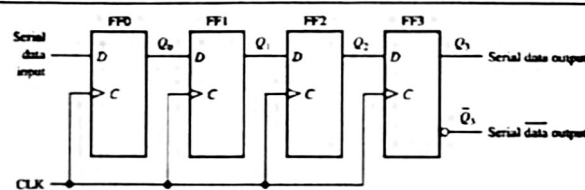
- (1) Fill in the numbers with 1 sign bit and 7 magnitude bit

Decimal numbers	1's complement form	2's complement form
-63	11000000	11000001

- (2) Convert the octal number 23 to 8421BCD \_\_\_\_\_
- (3) The standard POS form of  $f(a,b,c) = \overline{a}bc$  is 在此处键入公式。
- (4) The output of an exclusive-NOR is \_\_\_\_\_ if the inputs are same.
- (5) If  $a_3 \sim a_0 = 1101$  and  $b_3 \sim b_0 = 1011$ , the output of the 4-bit comparator is \_\_\_\_\_.



- (6) The modulus-10 Johnson counter requires \_\_\_\_\_ flip-flops.
- (7) If an octal-to-binary priority encoder has its 0, 2, 5, and 6 inputs at the active level, the active HIGH binary output is \_\_\_\_\_.
- (8) A JK flip-flop is in the toggle condition when \_\_\_\_\_.
- (9) The data 1101 is applied to the input of a 4-bit serial shift register that is initially cleared. The state of the shift register after two clock of pulses is \_\_\_\_\_



3. Answer the questions briefly(40 points, 8 points per question).

(1) It is known that the waveforms of input signals A, B and the waveforms of output  $Y_1, Y_2$  are as shown in Figure 3-1:

- Try to determine which logic gate output  $Y_1$  is, and draw standard logic symbols of this logic gate (2 points)
- Try to determine which logic gate output  $Y_2$  is, and draw standard logic symbols of this logic gate. (2 points)
- Implement  $Y_1$  and  $Y_2$  with a 3-8 decoder. (4 points)

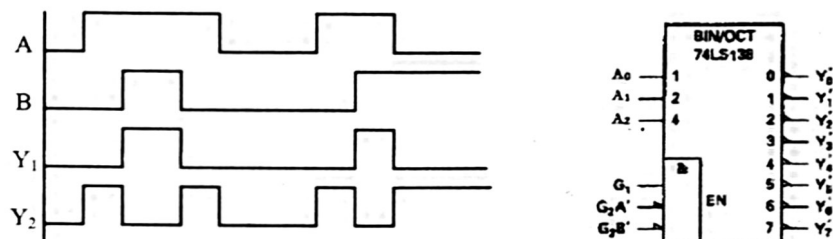


Figure 3-1

(2) A combinational logic circuit has two control signal  $C_1$  and  $C_2$ , request:

$C_2C_1$	Action
00	$F = A \oplus B$
01	$F = \overline{AB}$
10	$F = \overline{A + B}$
11	$F = AB$

Please design this circuit with logic gates.(open answer)

(3) Simplify the following logic functions using karnaugh maps

- $F(A,B,C,D) = \sum m(0,2,3,7,8,9,10,11,13,15)$  (4 points)
- $F(A,B,C,D) = \sum m(4,5,6,7,12,13) + \sum d(8,9)$  (4 points)

(4) For the circuit in Fig 3-2

- draw the state table and state diagram (5 points)
- complete the timing diagram by showing Y output. Assume the initial values are  $Q=0$ . (3 points)

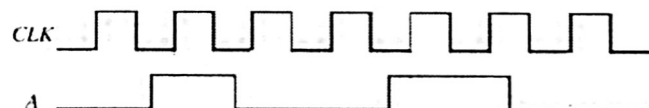
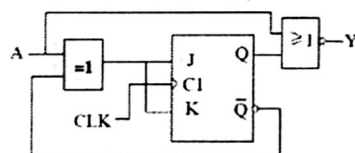


Figure 3-2

(5) A BCD decade counter is shown in Figure 3-3. The waveforms are applied to the clock and clear inputs as indicated. Determine the waveforms for each of the counter outputs ( $Q_0, Q_1, Q_2$ , and  $Q_3$ ).

The clear is synchronous, and the counter is initially in the binary 1000 state.

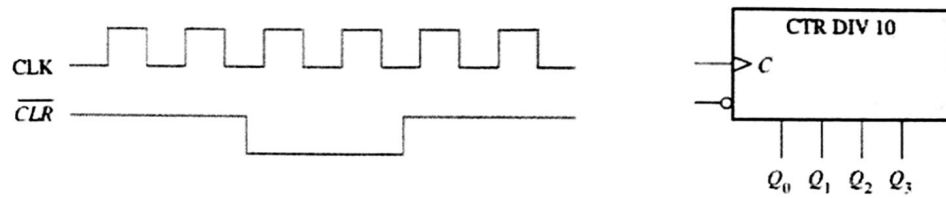
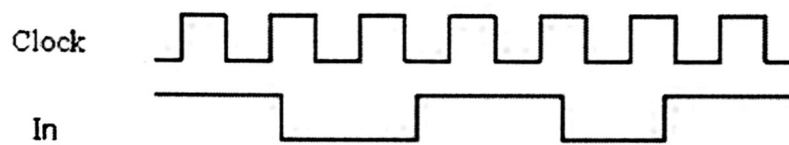


Figure 3-3

**4. Comprehensive questions (20 points, 10 points per question).**

- (1) Develop a logic circuit for detecting all positive-edges of In.(open answer)



- (2) Design a counter to produce the following sequence: 1, 4, 5, 7, 1, ... (open answer)