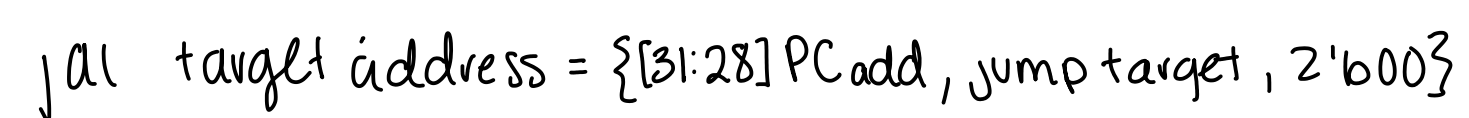


Tuesday, August 16, 2022 3:26 PM



Hand-drawn logic diagram of a 2-bit ALU. The ALU has two 2-bit inputs: 'Data' and 'ALUOut'. It has two 2-bit outputs: 'A3' and 'PC1'. The ALU is controlled by a 'Control Unit' which provides a 'JAL' signal and a 'Mem to Reg' signal. The 'JAL' signal is connected to the top input of a 2-to-1 multiplexer that selects between 'Data' and 'ALUOut' to produce the 'A3' output. The 'Mem to Reg' signal is connected to the top input of a 2-to-1 multiplexer that selects between 'Data' and 'ALUOut' to produce the 'PC1' output.

Q2

- Multiplier: $\frac{\%}{\# \text{Cycles}}$
 CPI $\left\{ \begin{array}{l} \text{load: } 0.08 (5) \\ \text{store: } 0.04 (4) \\ \text{branch: } 0.33 (3) \\ \text{jump: } 0.18 (3) \\ \text{R type: } 0.37 (4) \end{array} \right\} + \left\{ \begin{array}{l} \text{total CPI} = 3.57 \end{array} \right.$

CPI: 3.57

Execution time = 5355 ns

instructions: 100

$T_c: 45 \text{ ns}$

execution time: 4500 ns