Lab Assignment 2
4-bit Adder With Interface

Lab 2 Introduction

In this lab we will design a circuit capable of adding two 4-bit binary numbers and display the outputs using a seven-segment decoder. Students will complete this lab assignment using Quartus Schematic and upload their design to the DE1-SoC to test the functionality of our design.

Accessing Quartus

Our lab is equipped with Quartus Lite and you can also download and install Quartus Lite directly to your computer/laptop.

Make sure the name of your top module matches the name of your folder and project.

Group

This assignment is intended to be completed individually but you are allowed to form a group of two to complete this assignment.

Pre-Lab Assignment

Please submit the solution to the following pre-lab assignments in PDF format via Canvas.

a) Draw the full schematic for a 3-bit adder by chaining a group of full adders in series using Quartus Schematic. Make sure you label the inputs as A2, A1, A0, B2, B1, B0, and Cin. Label the outputs as Cout, Sum2, Sum1, Sum0. Make sure your solution is in SOP form. Place the drawing into your prelab, and make sure that your grader can see, follow, and understand your drawing.

Submit a single PDF file that contains your responses to Canvas before coming to the lab. The name of your prelab report needs to be prelab2.pdf.

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2. Lab Assignment

2.1 4-bit Adder

Design a 4-bit adder using Quartus Schematic.

Connect A3, A2, A1, A0 to SW3, SW2, SW1, SW0 respectively.

Connect B3, B2, B1, B0 to SW7, SW6, SW5, SW4 respectively.

Connect Cout, Sum3, Sum2, Sum1, Sum0 to LEDR4, LEDR3, LEDR2, LEDR1, LEDR0 respectively.

Assignment 1

Run your design to verify that you have successfully completed Lab 2.1

You are responsible to ensure that your design works.

2.2 4-bit Adder & 7-Segment Decoder

Use your 7-Segment Decoder from the previous lab assignment. Rather than using D3, D2, D1, D0 as your inputs, you will connect the inputs of the 7-Segment Decoder directly to the outputs of the 4-bit adder you have designed and they are Sum3, Sum2, Sum1 and Sum0.

Connect the outputs of the 7-Segment Decoder directly to one of the 7-Segment displays on DE1-SoC.

Assignment 2

Run your design to verify that you have successfully completed Lab 2.2

You are responsible to ensure that your design works.

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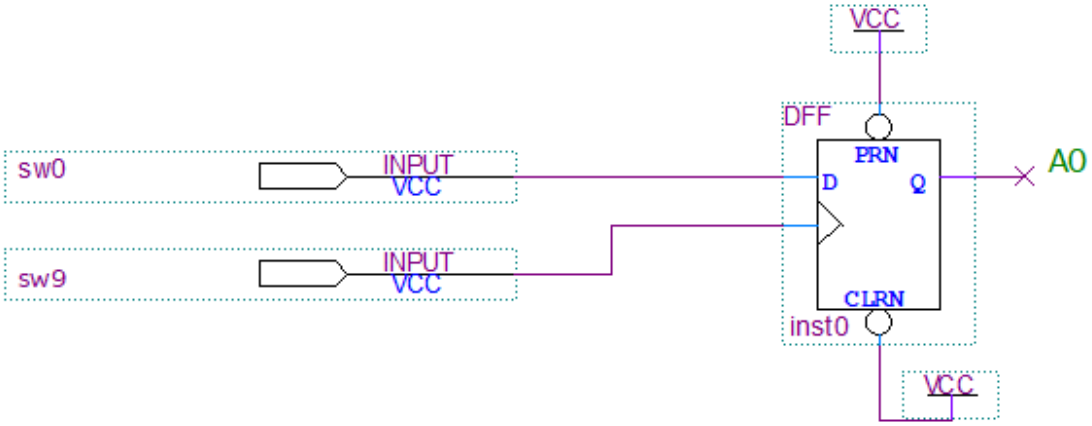
2.3 DFF & 4-bit Adder & 7-Segment Decoder

The outputs of the schematic in 2.2 change immediately as we change the inputs. In assignment 2.3, we want to introduce a basic concept of clock (clk) by inserting a DFF between each individual toggle switch (SW0 to SW7) and 4-bit adder input (A0 to A3, B0 to B3) respectively.

Insert a DFF between A3 & SW3, …, A0 & SW0, B3 & SW7, …, B0 & SW4.

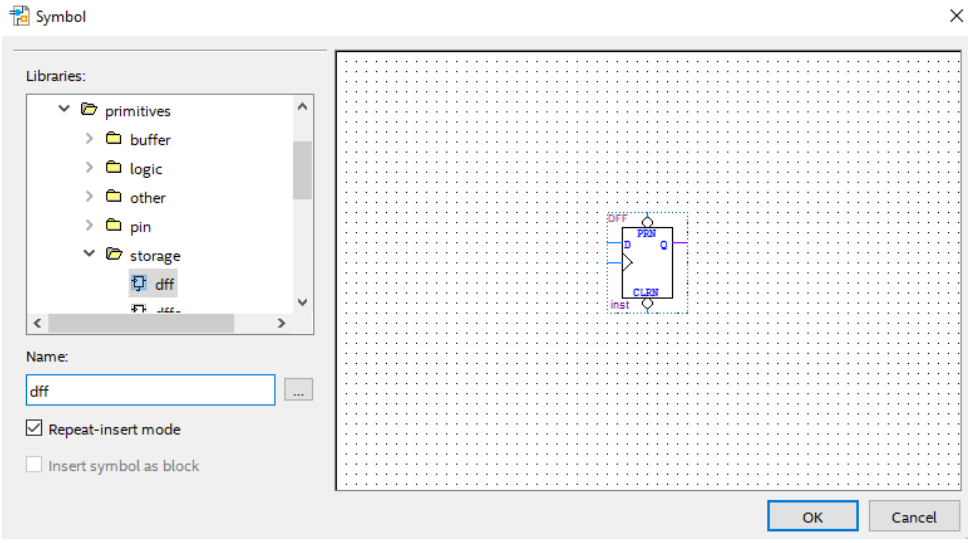
Connect the clock of each DFF to SW9 or a push-down button. **Clearly indicate this on your Lab Report.**

An illustration can be found below:



WARNING: Please make sure that the instance name for the DFF and the two VCCs are different. Double click each device to name its instance differently.

You can find DFF by typing it directly to the search box:



You can also find the logic behavior of DFF by going to:

https://www.intel.com/content/www/us/en/programmable/quartushelp/17.0/mapIdTopics/jka1465580036406.htm

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Assignment 3

Run your design to verify that you have successfully completed Lab 2.3

You are responsible to ensure that your design works.

After you have finished completing Lab 2.3, submit all the files needed to run Lab 2.3 to Canvas.

Upload all your files (.bdf, .qsf, etc etc) to Canvas as separate files.

You must include a Readme file to inform the course instructor/grader how to set-up a project to run your design.

A grade of Zero will be assigned to this Lab Assignment if the course instructor/grader is unable to run your design. This includes the failure to follow your steps, or you forgot to submit a file to Canvas.

Laboratory Report

You need to follow the lab report outline provided on Canvas.

Copy and paste all your drawings into your report.

Make sure you that your grader can see, follow, and understand your drawings.

You also need to upload all your drawings (.bdf, .bsf, etc) and .qsf as separate files to Canvas.

Your grader will run your code/drawing(s).

For individual submission:

Submit a document with the following naming convention: FirstNameLastName-Lab2.docx (for example: JohnDoe-Lab2.docx) that contains all the drawings needed to complete Assignment 1, 2 and 3. Turnitin will check the genuineness of your work.

For a group of two submission:

Submit a document with the following naming convention: YourFirstNameLastName-YourLabPartnerFirstNameLastName-Lab2.docx (for example: JohnDoe-JaneDoe-Lab2.docx) that contains all the drawings needed to complete Assignment 1, 2 and 3. Turnitin will check the genuineness of your work. Each individual is responsible to submit their own file(s)/document(s).

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