**Key Components in the Design:**

1. **Timer Increment Logic**:
   * The timer (timer\_value) increments on each clock cycle when the control signal Control\_timer is set to "10" (indicating the timer is active).
   * If the timer\_value reaches the TIMER\_LIMIT, the reset logic is triggered.
2. **Reset Logic**:
   * **Delay Counter**: When the timer exceeds TIMER\_LIMIT, a delay counter (reset\_delay\_counter) starts counting up to the value of CPU\_RESET\_DELAY (which is set to 2).
   * **Reset Signal (cpu\_restart)**: During this delay period, cpu\_restart is set to '0', signaling a reset. Once the delay period is over, cpu\_restart is set back to '1'.
3. **Reset Condition**:
   * The reset signal (cpu\_restart) is activated (set to '0') when timer\_value exceeds the limit (TIMER\_LIMIT) and remains active for the duration of the delay (CPU\_RESET\_DELAY).

**Does This Watchdog Timer Implement a Restart System?**

* **Restart Mechanism**: In typical watchdog systems, a "restart" or "reset" would involve the system being reset to a known initial state when the timer exceeds its limit, followed by restarting the operations from the beginning. However, this design **only signals a reset** through the cpu\_restart signal for a specified delay period and does not automatically restart the entire system or timer.
* **Delay Only**: The delay (CPU\_RESET\_DELAY) controls how long the cpu\_restart signal stays low, indicating that a reset should occur. After this delay, the cpu\_restart signal returns to '1', which may be interpreted as the system being ready to resume normal operation. However, there is no logic in place to automatically restart the timer or any other part of the system.

**To Implement a Full Restart System:**

* You would need to ensure that the entire system (or key components) is reset to its initial state when cpu\_restart is activated.
* You might add logic to reset all critical components and possibly re-initialize the timer or other important signals.

**Conclusion:**

the current design implements a delay before signaling a reset but does not include a full system restart. To convert this into a restart system, you would need additional logic to reset and reinitialize the system's critical components when the cpu\_restart signal is asserted.