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Memristor-Based CMOS Hybrid Circuit Design and Analysis

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Abstract

Electronic memory with ever-increasing storage capacity is always in high demand. Every year, a computer transforms into a smaller, faster, and more reliable device. Memristor is a passive aspect recently developed that is gaining popularity. The non-volatile and small area features of this element are very essential. A Memristor's ability to fabricate around CMOS architectures is a step forward in VLSI design enhancement. When developing a fast multilevel switching device, increasing information density in the same silicon area is a desirable feature. In this design and analysis, a unique memristor-based CMOS inverter is presented. A unique inverter with a nonvolatile output and good performance. This characteristic makes it useful for a substitute inverter as well as an SRAM memory cell that supports input negation for special uses. Memristor-based CMOS design is an emerging concept that targets efficient memory computing systems. Simulations were performed in cadence using a memristor model extracted to analyze and compare power consumption. The analyses of non-volatility, the voltage produced, and the read/write period were performed with cadence virtuoso 130 nm CMOS technology using a power supply voltage of 1.9 V while consuming 35.67 μW, and the delay is 9.235 ps. The comparison with a pure CMOS implementation is promising in terms of power, area, and delay significant improvement. Further, the Monte Carlo simulation results using 2000 samples confirmed the total power and delay of the proposed design.

Keywords: ReRAM, CMOS-Memristor, Cadence, Non-Volatile, VLSI Circuit Design

1. Introduction

Innovation of CMOS integrated circuits has brought about superior technology throughout the last three decades The utmost important merits of CMOS technology are less power depletion, faster access, and increased integration.

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The sustained VLSI growth technology reduces the size of transistors. Transistor miniaturization would not continue indefinitely [1], [2]. Such circuits confront major hurdles and restrictions in terms of fabrication concerns, such as process limits like lithography or area control. Thus, Novel approaches must be invented to expand Moor's Law and the size reduction guideline [3]. The advent of nanoscale devices was highly beneficial in addressing the challenges of CMOS technology [4]. Memristive devices have arisen as an effective technology for overcoming these challenges [5]. The memristor could be lowered in size while still providing faster speed, less area, and non-volatility [6]. Furthermore, a memristor is well suited for manufacturing Circuits for hybrid CMOS-memristor-based circuits [7]. Memristive techniques have progressed: multiple candidates compete to become the dominant technology in electronic memories, each based on a different physical phenomenon and material combination [8]. Memory devices such as ferroelectricRAM [9], phase-changeRAM [10], and magnetoresistiveRAM [11] have introduced new data storage paradigms. These technologies have advantages, but not many have the optimal combination of features such as miniaturization, quick access, ease of manufacture and operation, low price, and durability [12]. Memristors have grown in popularity in recent years, and they are now used in a wide range of applications, either separately or in combination with crossbar arrays [13]. Furthermore, it has uses in both analog and digital environments. Subsequently, several expected benefits of memristors over conven- tional transistor-based memories have been confirmed [14], [15]. This technique is one of the contenders for extending Moore's Law because of its potential to minimize size in 3D nanowire crossbar architectures [16], [17]. A design drawback of a CMOS inverter gate used to build NAND or NOR gates in general, is an inability to store the value of the most recent output [18].

While the concept of using an RRAM cell within a CMOS memristor-based inverter has been proposed by others [19], [26] these implementations are merely proposed as a concept, an implementation using an existing and specified CMOS-Process. Within this paper, we present an implementation, consisting of a memristor-based using an optimized inverter designed using IHP 130 nm SG13S technology, which allows for the integration of RRAM technology into CMOS designs. Here, the memristor linear boundary drift model can be used with nonlinearity injected via a window function. The present circuit, based on a memristor, has a nonvolatile output with a feedback design. This circuit can store the last output, and the memristor design performs the duties of an SRAM cell, thereby improving read/write times. As a result, improvement of the overall power is achieved.

The remaining paper is organized as follows: Section 2 describes the basic architecture of the memristor and its special features. Section 3 highlights the design of the proposed memristor-based inverter with non-volatile features. The simulation results are discussed in section 4, followed with a conclusion in section 5.

2. Memristor

This circuit component was outdoored as a late-discovered detachable unit concept by Leon Chua in 1971 [19]. According to Chua's hypotheses, two terminal elements must be related to charge and flux. These components were expected to supplement the three past circuit components L(inductor), R(resistor), and C(capacitor), as shown in Figure 1. The memristance Z, a basic characteristic of memristors, connects the flux and charge in a relationship through the following equation [19], [20]. This concept and the following equations have been proposed by others [19], [21].

$$df = ZdQ \tag{1}$$

The memristance is obtained by dividing (1) by dQ

$$Z(Q) = \frac{df}{dQ} \tag{2}$$

Where, Z the memristor's memristance value is also charge (or flux) controllable. And dt produces

$$V = Z(Q).I \tag{3}$$

Where V is the voltage across the charge carried by this device. Under certain conditions, Equation (3) behaves similarly to the memristor and its equivalent resistor. A Resistive resistance value is read at the meeting point of the voltage and current characteristic curves. The output of memristor is different from the output of a resistor. The pinched hysteresis loop is a memristor's voltage and a current representative curve in Figure 2. The hysteresis loop demonstrate the memristor's memory behavior, and that is a crucial feature. A memristor is classified as an irregular charge-dependent resistor in relation to voltage and current curves. This hysteresis loop displays the varying resistance values, with the memristance ranging between them [22].

2.1. A Memristive linear ion drift model

HP Labs developed the most fundamental pragmatic Titanium Dioxide memristor. It basically consisted of two simple layers of thin film titanium dioxide that were stacked together (Tio_2) and bounded by two platinum (Pt) electrodes. The resistance property of Titanium dioxide (Tio_2) renders it useful as a broadly used component of oxygen sensors after being modified with oxygen atoms [19], [23]. The flow of electrons in that material controls the haphazard motion of the atoms in the thin film, allowing for an alteration in the device's nuclear structure or mainly in the memristor. The core layer works as an insulator, whereas the top film layer conducts due to the additional oxygen vacancies in the Tio_2 material. The resistance or state changes when the empty spaces around the oxygen molecules slide towards the bottom layer; as a result, the top layer maintains a steady state. Crossbars consisting of nanowires were placed above and below the top and bottom layers of material to achieve memristive characteristics [23], [24].

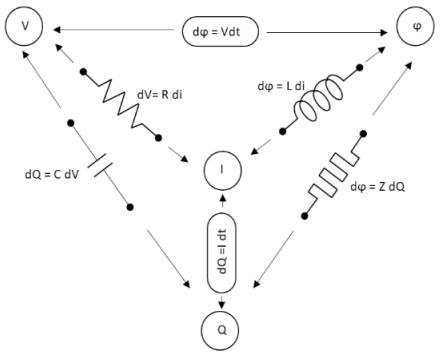

Fig. 1. R, L, and C circuit element relations with Memristance Z [19, 21].

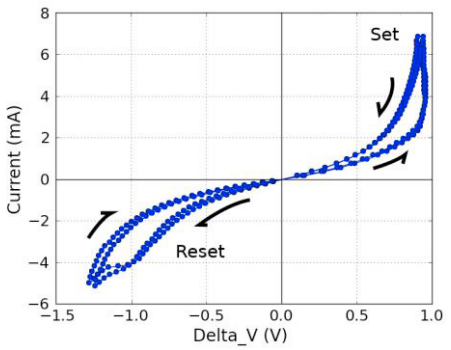

Fig. 2. Memristor's I-V cycles hysteresis loop [22].

2.2. Modeling of Memristor

The model was overly simplistic, accepting only One state variable. The oxygen atoms doping method in Tio_2 thin films provides two zones with differing resistance in relation to the film [19], [24]. The zone that was doped (Tio_2) would have lower resistance and better conductivity, while the area which is not doped has higher resistance with lower conductivity. When the bias voltage is removed, the oxygen vacancies do not shift, and the region between doped and un-doped areas of the memristor's boundary remains in place [19], [25]. This is displayed by a component consisting of two resistors arranged in series (R_{ON}, R_{OFF}). F is state variable that describes each resistor's relative doped or undoped part (see Fig. 3). Doped areas are oxygen deficit ($Tio_2 - x$) and serve as R_{ON} whereas undoped areas act as R_{OFF}.

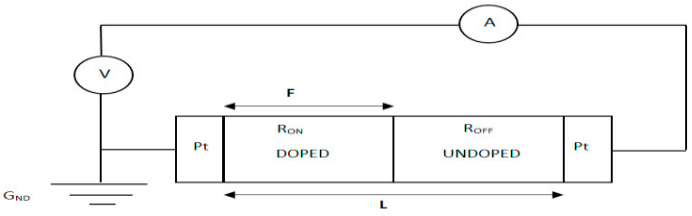

Fig. 3. Memristor Model Based on Linear Ion Drift Titanium Dioxide (HPs) [19, 24].

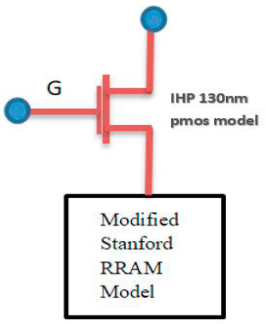

Fig. 4. Composite Memristor model [27].

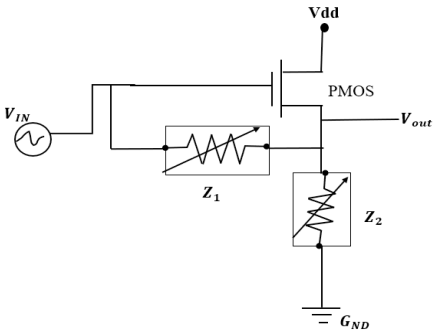

Fig. 5. Memristor based inverter circuit.

The dopant's velocity (V_L) will be used to establish the boundary location within the doped and un-doped areas [24], [26].

$$V_L = lim(\Delta \to 0)\frac{\Delta F}{\Delta t} = \frac{dF}{dt} \tag{4}$$

Where, F denotes the boundary area, which is located along the length of the film L. For the Memristor device, there have been numerous models presented. The first is the model of linear boundary drift [24], [26]. The formula is:

$$V_L = \left(\frac{\eta \cdot \mu_L \cdot R_{ON}}{L}\right) * I_{(t)} \tag{5}$$

Here, η represents the memristor's polarity, μ_L represents the dopant mobility, and L represents the film thickness. Resistance in the doping concentration region is R_{ON}, while that of the undoped part is R_{OFF}. Memristor's memristance decreasing as the boundary portion moves along the Tio_2 thin layer, with aboundary location of F less than the film thickness L, is given by [24], [26].

$$F_W = R_{ON} * (F/L) + R_{OFF} * (1 - F/L) \tag{6}$$

As a necessary consequence, a current-voltage correlation:

$$I_{(t)} = \frac{V_{(t)}}{R_{init}\left(\sqrt{1 - \frac{2 \cdot \eta \cdot \mu_L \cdot R_{ON} \cdot \Delta R \cdot \phi_t}{L^2 \cdot R^2 init}}\right)} \tag{7}$$

The R_{init} and ΔR parameters are provided by [26],

$$F_W = R_{ON} * (F_O/L) + R_{OFF} * (1 - F_O/L) \tag{8}$$

In (8) F_0, indicates the memristors boundary region's initial position. The nonlinear nature of the memristor necessitates the need for a linear model, despite the usage of equation (5) to simulate memristor behavior.

3. Proposed Memristor Based Hybrid Circuit

Figure 4 shows our modeling approach. CMOS memristor inverter can be invented with two memristors (Z_1 and Z_2) and one PMOS. As shown in Figure 5, a memristor circuit uses one PMOS and two memristors instead of an NMOS with a less threshold voltage to enhance switching speed. This Circuit consists of a PMOS transistor connected in series to an insulator metal. Memristors control the current passing through PMOS and are used for recent feedback. The supplied voltage (Vdd) links to the PMOS transistor's source terminal as indicated in the circuit. This circuit design, memristor Z_1, work as a feedback branch. As a result, an additional memristor links the output node to the

ground. The output node is connected to the positive terminals of the Z_1 and Z_2 memristors. In this circuit, a PMOS acts as a switch. The memristor inverter is designed using an IHP 130 nm technology with transistor dimensions as memristor, and memristor film length t_{ox} is 6nm, R_{th}=1500 k/w, and T_O=300 K, Wp=0.15 um, L=0.15 um.

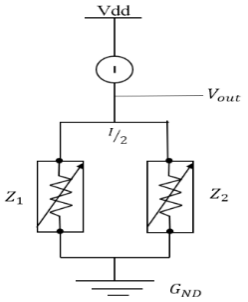

Fig. 6. analogous circuit Vin=0

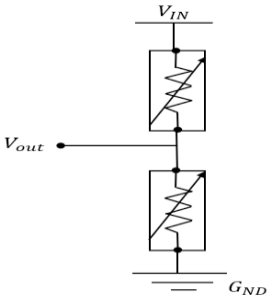

Fig. 7. analogous circuit Vin=1

Due to constant Vdd, the input Voltage Vin is used to schedule the ON and OFF states of the PMOS switch. PMOS, Z_1, and Z_2 will be ON state if the input voltage Vin is set to 0 due to current passing through the memristor with R_{ON} activation. Another scenario illustrates PMOS cutoff when the source to gate voltage drops below the PMOS threshold voltage, causing memristor Z_1 to turn off while Z_2 remains in the ON state. The transistor switches to the on-state when Vin=0, thus extracting the output voltage as follows [26]

$$V_{out} = R_{eq} * I_L \tag{9}$$

Figure 6 shows the Req, equivalent memristance of the memristors. The R_{ON} and R_{OFF} values differ based on the memristor model. The current flows to the +ve side of both memristors, causing them to remain in the ON state. An Output power could be extracted by using memristors with equal resistance and current, which expresses 1.9 volts for that output level. The condition will change if the input voltage remains at 1.9 volts. The PMOS switch is turned off if (VSG) is less than the PMOS transistor's edge voltage (VTP). Figure 7 depicts an equal circuit. The current is generated by the input voltage, causing memristor Z_1 to remain in the OFF position while memristor Z_2 remains in the ON position. Passive resistance R_{OFF} creates a condition in which no current is produced. The following voltage output [26].

$$V_{out} = \left(\frac{M_{z2}}{M_{z2}+M_{z1}}\right) * V_1 \tag{10}$$

Equation to becmoes:

$$V_{out} = \left(\frac{R_{ON}}{R_{ON}+R_{OFF}}\right) * V_1 \tag{11}$$

4. Results and Discussion

This section describes the simulations of proposed inverter circuits in 130nm CMOS technology. The power supply is 1.9 V. The delay of this structure is about 9.235 ps. Considering these conditions, the total power consumption of the CMOS memristor circuit is 35.670 µW. When the real values of R_{ON} and R_{OFF} are replaced, the output node is set to approximately 0 volts. This signifies that this circuit operates in the same way as an ideal inverter. Figure 8 represents the inverter's transient analysis. A feedback network connects the output to the input of this memristor.

The input values are defined as the status of Z_1. The different memristor values for the Vin=1 and Vin=0, memristor-based inverters are shown in Table 1.

To analyze non-volatility features of the suggested inverter circuit, some important considerations about read and write times should be born in mind. The write time is the shortest amount of time the input pulse must have persisted for the memristor status to switch from F=0 (R_{OFF}) to F=L (R_{ON}) [26].

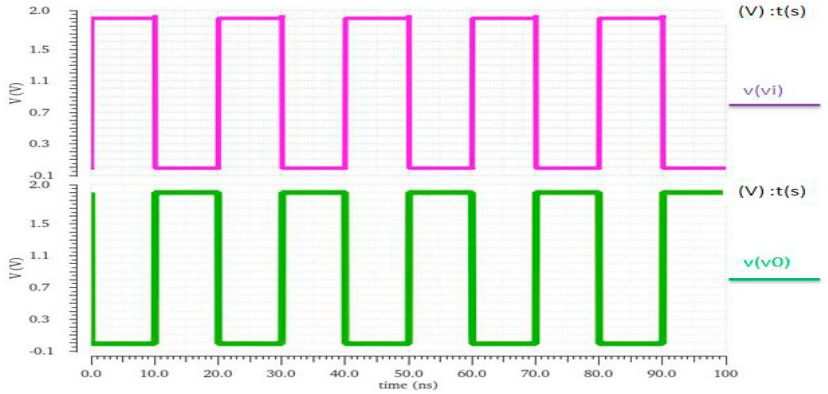

Fig. 8. PMOS-Memristor input and output waves

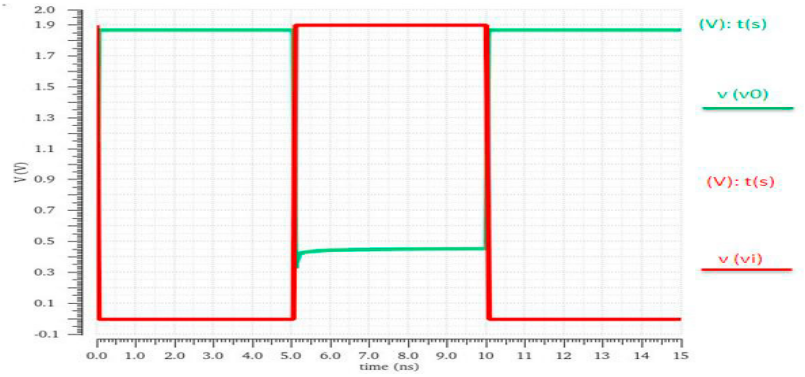

Fig. 9. Memristor Z1 based input voltage changes (Write time analysis)

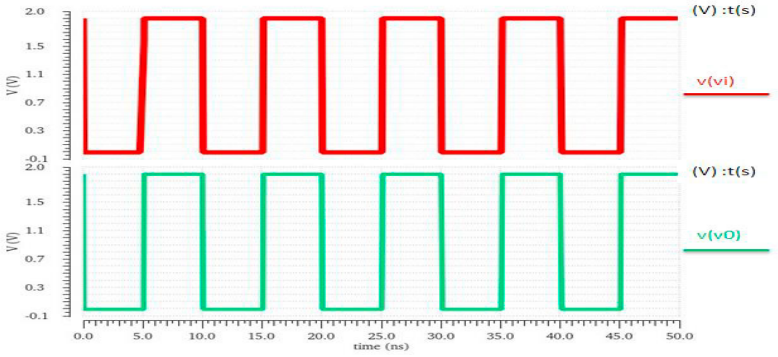

Fig. 10. Vout=1 non-volatile output

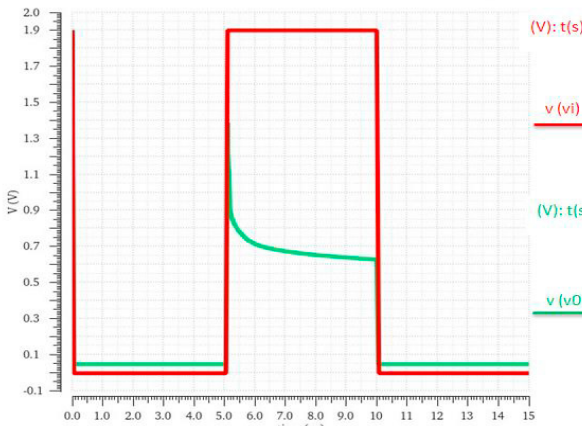

Fig. 11. non-volatile output for Vout=0

Table 1. Memristors with different voltage valves [26]

	Z_1	Z_2
Vin=0	R_{ON}	R_{ON}
Vin=1	R_{OFF}	R_{OFF}

* Z_1, Z_2= Two Memristor

write time has passed in the proposed inverter, the resistance of Z_2 will remain at R_{ON} . if the input voltage changes, the resistance of Z_1 will change after the write time . For this circuit, the write time is 5ns. The proposed circuit can be enhanced by using different models to improve the write time. The memresistance of memristor Z_1 for the applied input voltage is illustrated in Figure 9. Figure 10 shows the output response for Vout=1. In this circumstance, both memristors are switched on. After supplying the input pulse of the read operation, the output node value is expected to be similar to a pulsed input. Its amplitude equalling half of that of the input pulse. When Vout=0, the memristor status is set according to the values in Table 1. Z_1 is in the OFF state in this condition, and Z_2 is ON. The output value is generally expected to be zero. The simulation result for this condition is presented in Figure 11. It will help determine the performance of the circuit and that of memristor Z_1, acting as an SRAM cell. As a result, circuit becomes non-volatile.

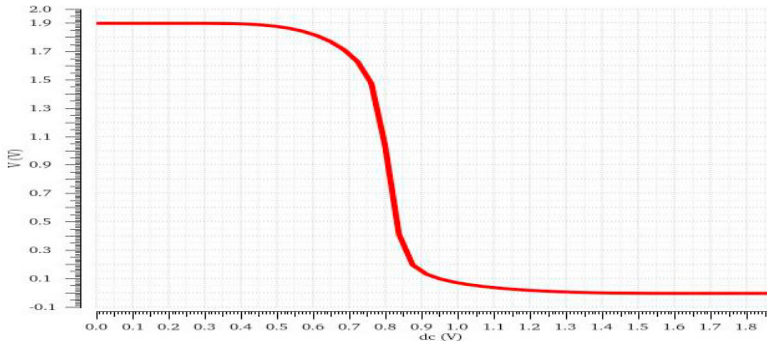

Fig. 12. DC response for 1.9 V

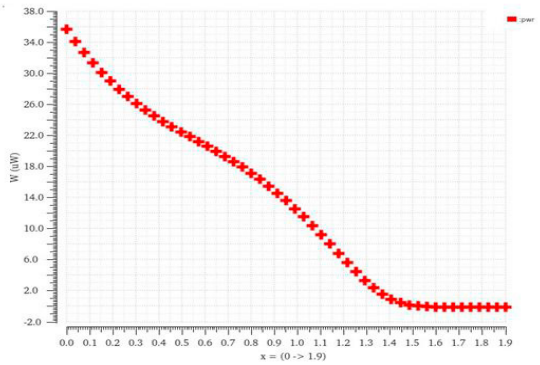

Fig. 13. Memristor inverter power consumption

For other CMOS technologies, Table 2 illustrates the results of their simulations for the lowest and highest output voltage levels and power consumption.

Table 2. Comparison of voltage and Power characteristics different technologies

Technology CMOS (nm) /	**Ref.**	**Power (µw)**	**W/L**	**Vi**	**VoMax**
32	[24]	4	8	0.9 v	≈ 0.9 V
45	[24]	8.3	8	1 v	≈ 1 V
65	[24]	15	8	1.1 v	≈ 1.1 V
180	[24]	95	8	1.8 v	≈ 1.8 V
Proposed work	**130**	**35.67**	**8**	**1.9 v**	**≈ 1.9 V**

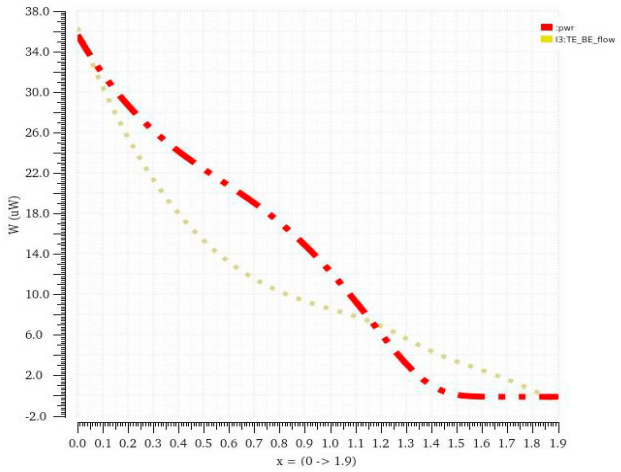

Fig. 14. Variation of power consumption based on Memristor

Figure 12 shows the DC response of the Memristor inverter, with lower thershold voltage. consumption Figure 13

shows the power consumption of the design inverter, and Figure 14 indicates the variation of power consumption on memristor device. Figures 15 and 16 show the Monte-Carlo simulations for the power expended, and delay of the proposed CMOS memristor inverter. For the tolal power consumption, the standard deviation and variation coefficient is approximately 35.67 µW. The variation coefficient of delay, on the other hand, is 9.234 ps.

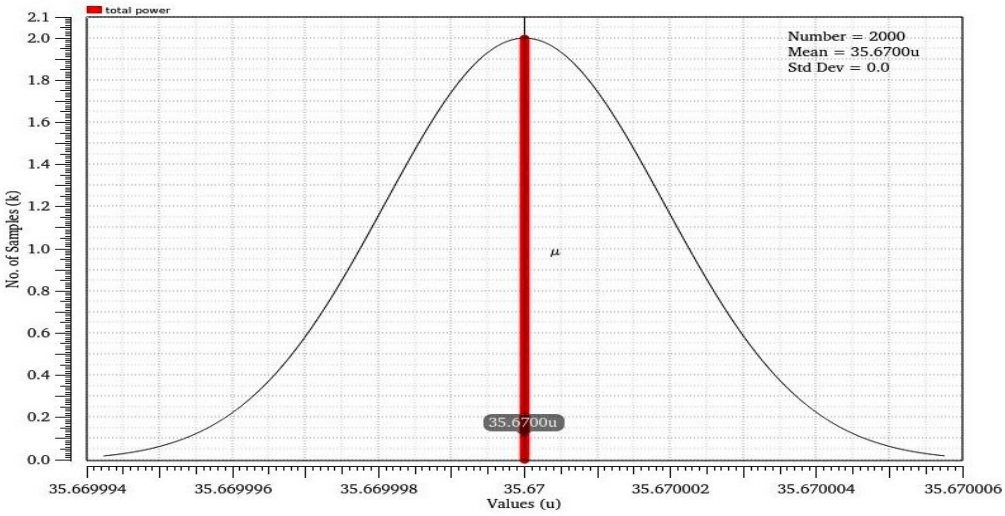

Fig. 15. Monte Carlo simulation results for power consumption

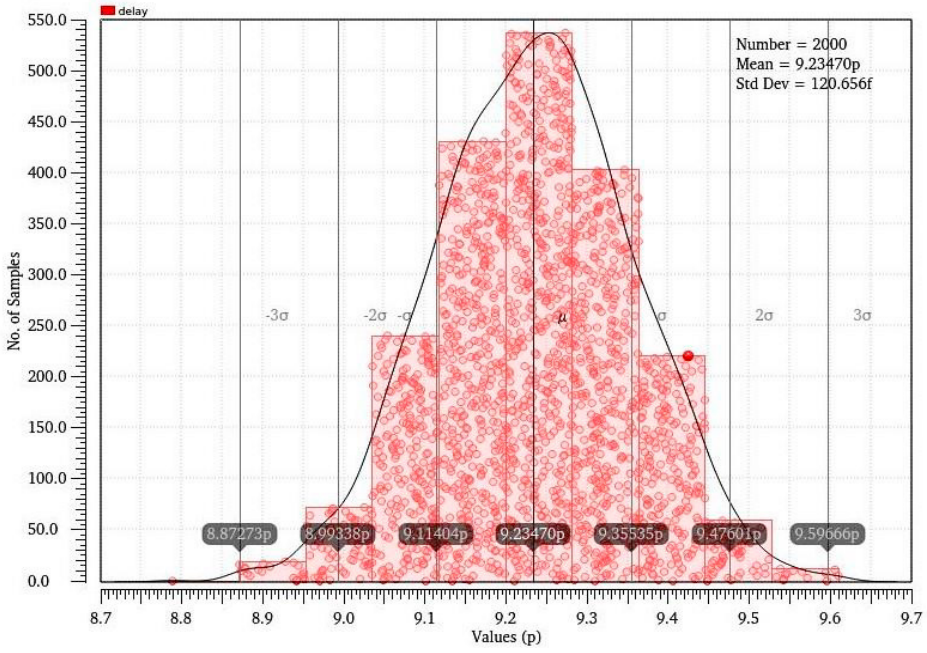

Fig. 16. Monte Carlo simulation results for delay

5. Conclusion

A new memristor-based inverter circuit is introduced and discussed in this paper. The suggested hybrid design features a non-volatile output with feedback based on a memristor. Output voltages for the novel inverter have been demonstrated to be acceptable at the minimum and maximum levels. The memristor based hybrid CMOS circuit had highlighted many favorable properties: Less area, nonvolatile features, CMOS implementation, and robust performance over device degeneration. In addition, the design flow is straightforward, with a nonlinear dopant drift memristor model. The architecture was simulated using CMOS (130nm) technologies. This memristor is indeed to fulfill SRAM cell functions. The operation supply voltage is 1.9 V, and power consumption is 35.67 μW. As a result, the delay is 9.235 ps. The Monte Carlo simulation was performed with 2000 samples. Future research will include the fabrication of an array and integration with memristors.

CRediT authorship contribution statement

Abhinav Vishwakarma: Conceptualization, Methodology, Software, Writing original draft. **Kwame Owusu Ampadu:** Visualization,, Writing original draft. **Santosh Vishvakarma**: Visualiza- tion, Writing review editing, Supervision. **Michael Huebner and Marc Reichenbach**: Project administra- tion, Resources, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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