VDIC - Testbench test specification

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28.10.2021

1 Remote github repository

https://github.com/TraitorablePL/VDIC

2 Test specification

In the current state testbench checks the following actions:

- All available ALU operations have 50% of chance to use arguments that are randomly generated 32-bit signed integers. Another 50% of chance are available for arguments that are known as special cases (max, min and zero values).
- All of 4 flags (Carry, Overflow, Negative, Zero) returned from ALU with CTL packet, are calculated as expected values and compared to the ones received from the ALU.
- When Data packets with CTL packet are returned from ALU, CRC3 is calculated locally and compared with the received one if values are not equal assertion is used.
- Errors are artificially included in sent packets based on the output of error generation function that have 1/64 chance to add single random error in transaction. That checks if the proper reaction from ALU happened.
- Error that causes CRC Error flag to appear, simply negates one of the bit from CRC field. This covers also error that could appear when some of the A or B bits are swapped. In both cases CRC is invalid for sent data.
- Operation Error flag is checked with 3 bit random operation codes that are not supported by ALU.
- Data Error flag check is done only for case when 3 data bytes are followed by CTL packet instead of 4th Data packet.