LAB 1 STRUCTURAL REPORT

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing "yes" at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? **yes**

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: ____

Student Name: **Andy Tran**
Student ID: 57422363
Date Completed: 4/15/21
Time Spent: Reviewing Digital Design Material: 30 minutes
Design/Preparation Work: 30 minutes
VHDL Coding & Debugging: 30 minutes

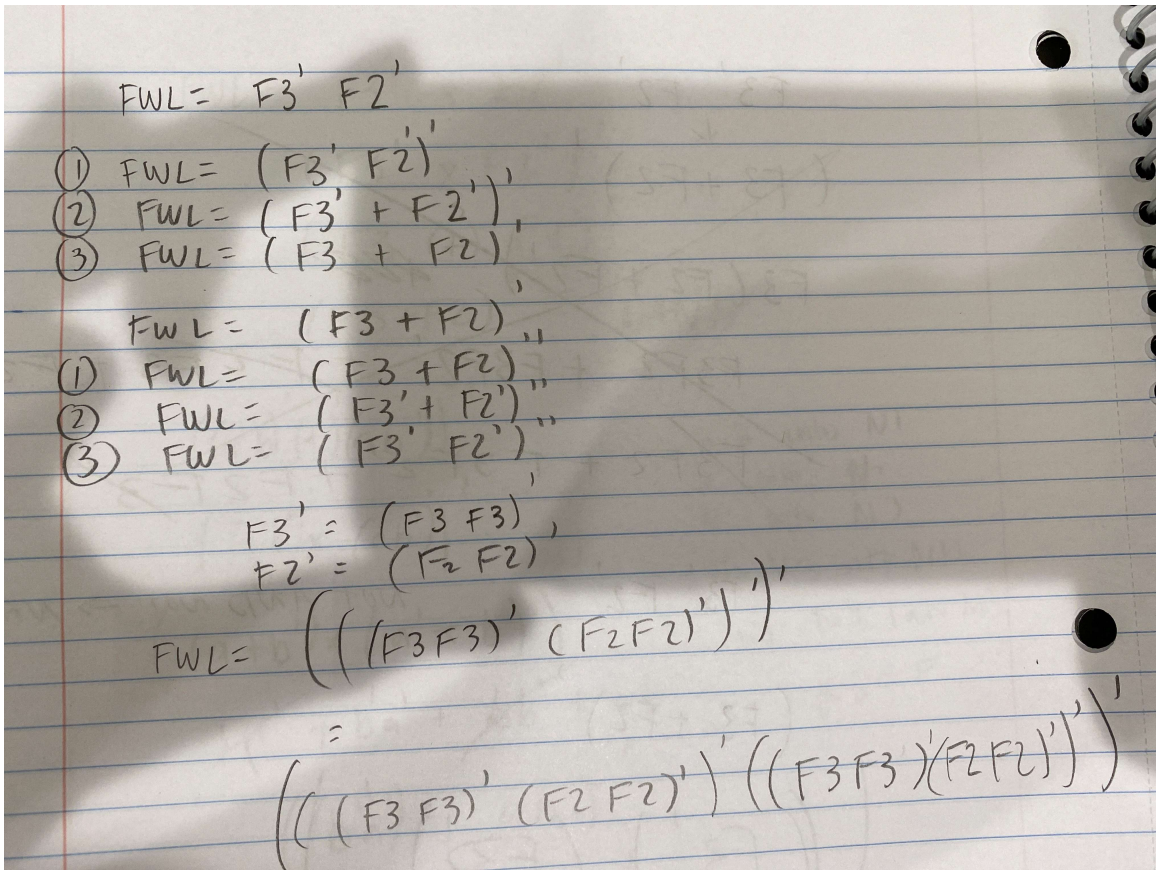
STRUCTURAL OVERVIEW

Replace this text w/ the % you feel you completed the lab. Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

I feel like I have completed 100% of this lab. I started off by rewatching the lecture to get a better understanding on how to design the lab1s file and the test bench. I then converted my orignal boolean expression from the behavioral lab using demorgans law to get the boolean expression to only have nands. Then I filled in the lab1s to have the signal and the gates and inputs and outputs for each gate. Then switched all the behavioral items from the testbench to structural. Then ran the simulation to see if the results are the same.

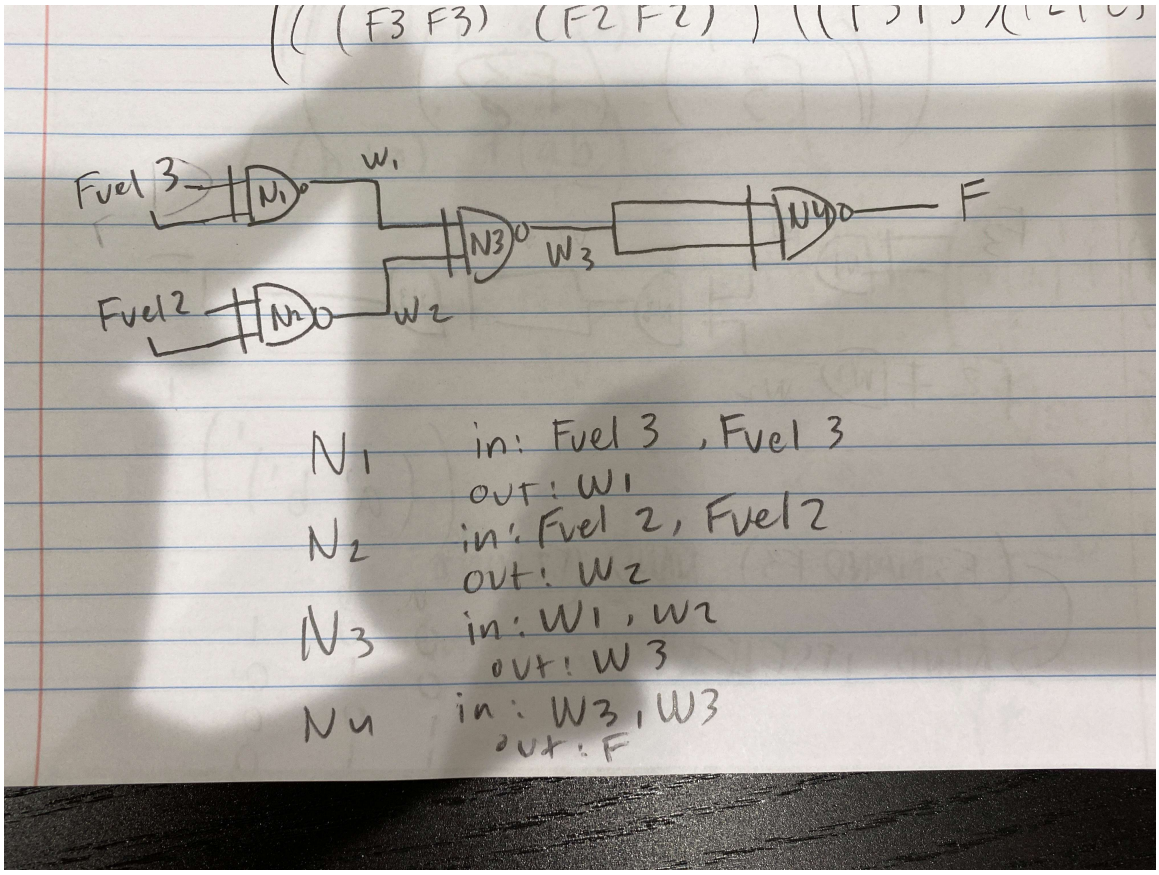
LAB 1 NAND EQUATION

Show the work you did to go from your minimized equation to final structural equation here.



LAB 1 CIRCUIT AND INPUT-TO-OUTPUT DELAY

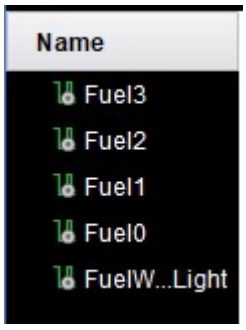
Provide a drawing/figure/circuit of your final structural equation in terms of gates here. You can use Visio or other gate drawing software here or attach a picture of your circuit as long as it is legible.

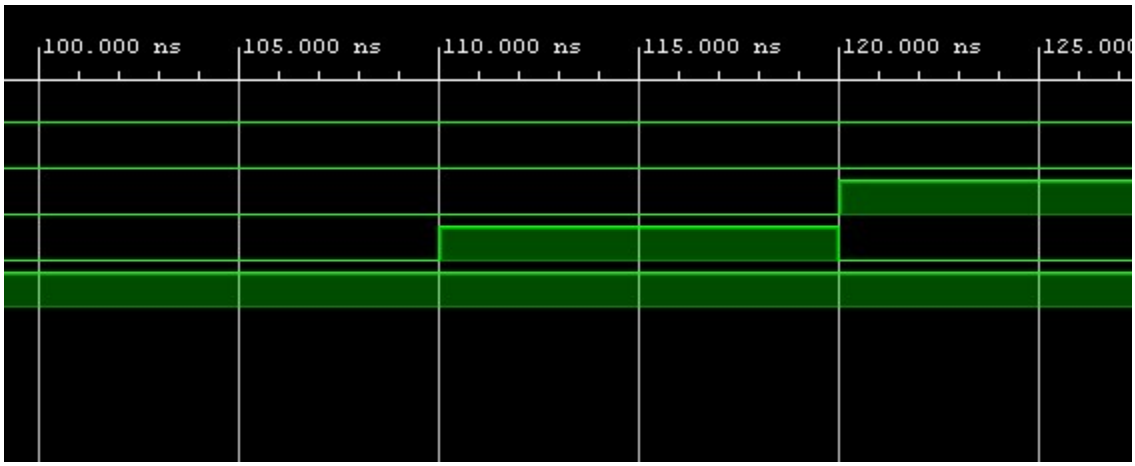


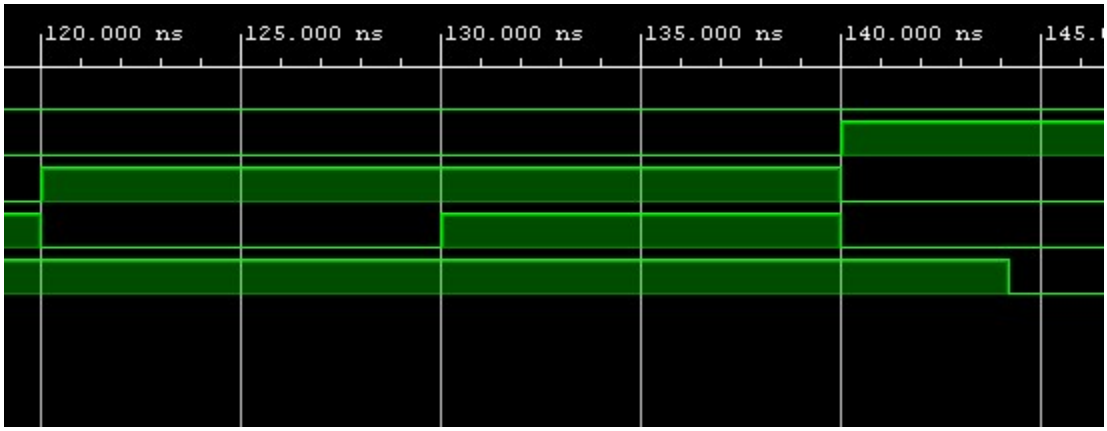
Delay of circuit: _4.2_ ns

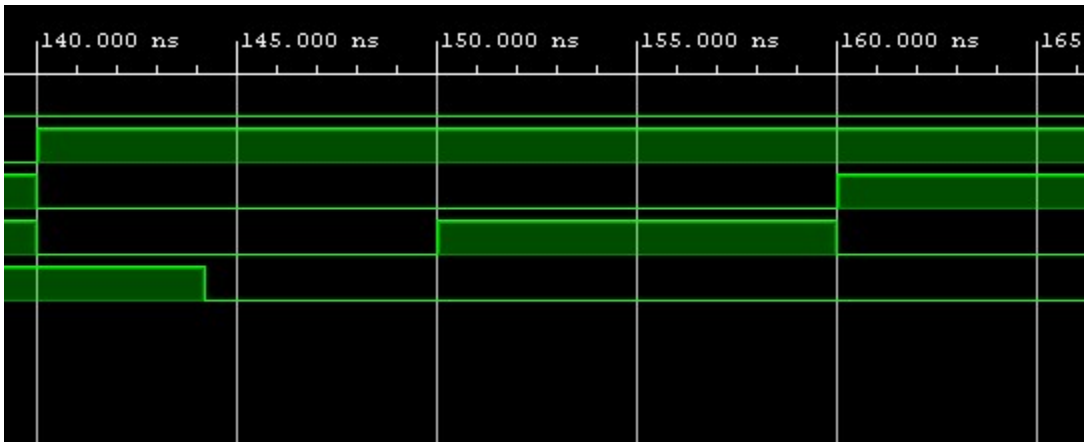
LAB 1 STRUCTURAL SIMULATION GRAPH

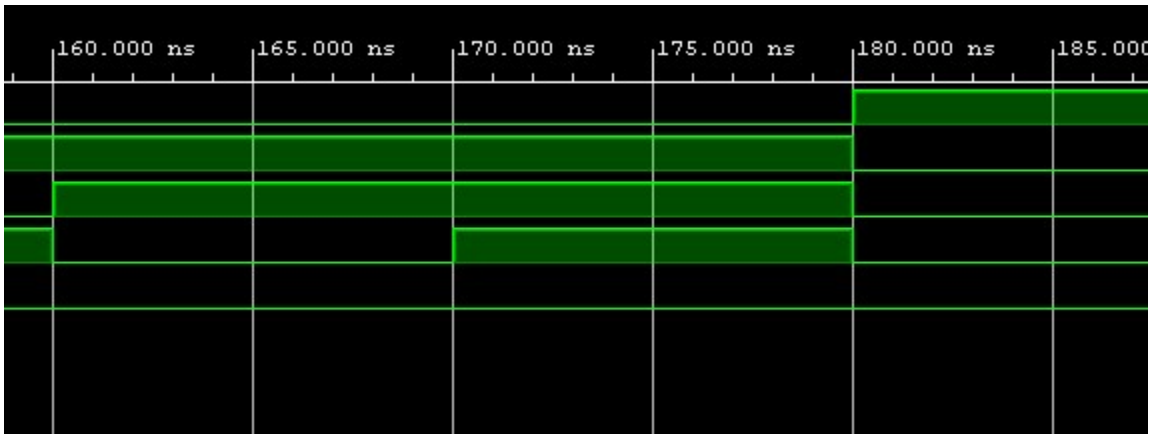
Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

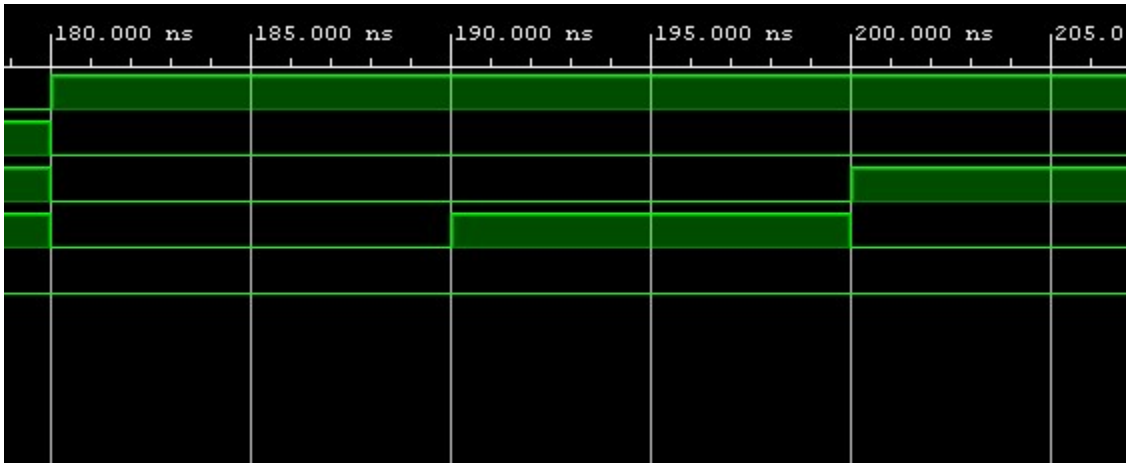


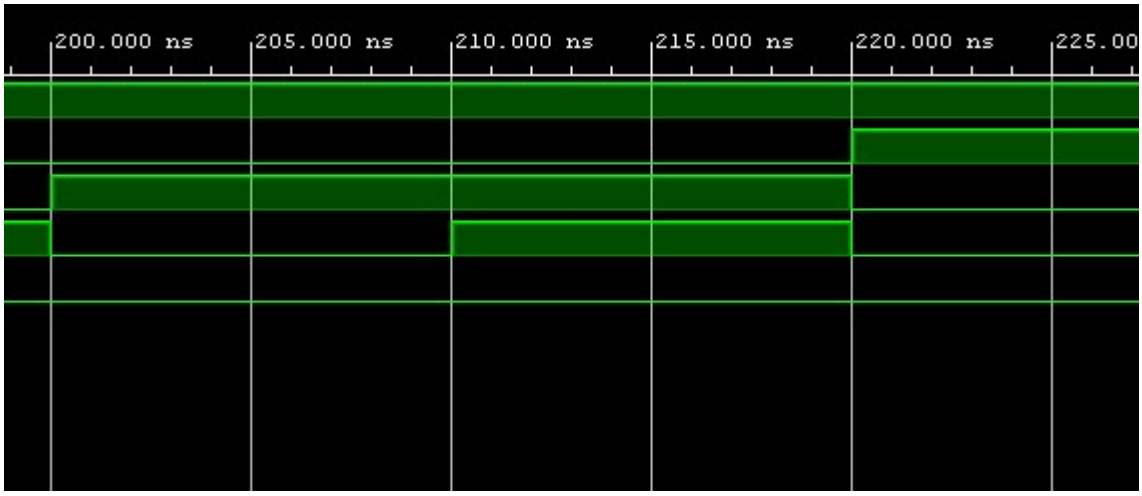

100.000 ns
105.000 ns
110.000 ns
115.000 ns
120.000 ns

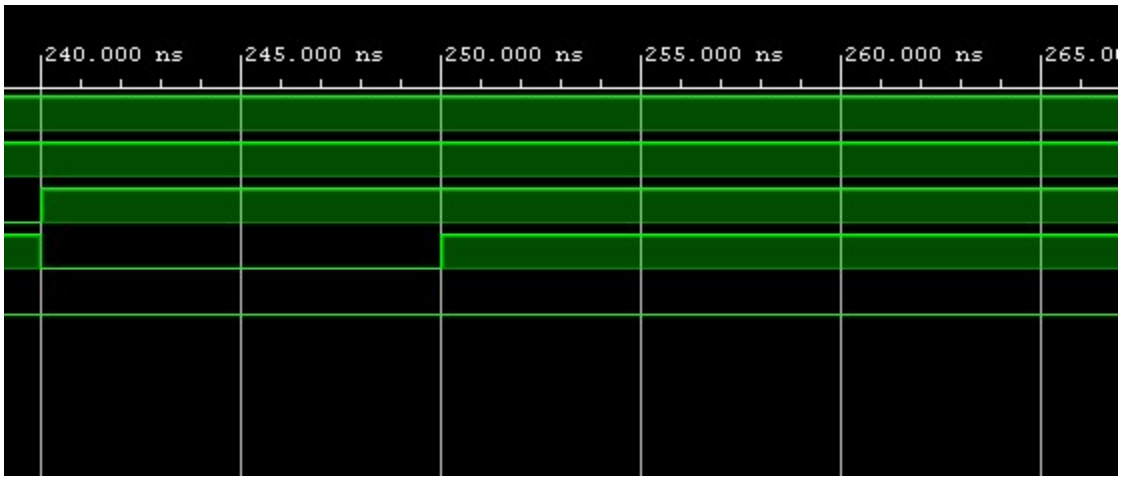

120.000 ns
125.000 ns
130.000 ns
135.000 ns
140.000 ns


140.000 ns
145.000 ns
150.000 ns
155.000 ns
160.000 ns


160.000 ns
165.000 ns
170.000 ns
175.000 ns
180.000 ns
185.000


180.000 ns
185.000 ns
190.000 ns
195.000 ns
200.000 ns
205.0


200.000 ns
205.000 ns
210.000 ns
215.000 ns
220.000 ns
225.00



LAB 1 STRUCTURAL AND BEHAVIORAL SIMULATION GRAPH COMPARISONS

Compare your behavioral & structural graphs here. If there are any differences (delays, outputs, etc.), be sure to explain them here.

The only diffrence is the delay becasue before the critical delay was 3.4 becasue one inverter and one and gate, whereas now it must go through 3 nand gates, so that is 4.2.