LAB 3 STRUCTURAL REPORT

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing "yes" at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? yes

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: ____

Student Name: Andy Tran
Student ID: 57422363
Date Completed: 5/16/2021
Time Spent: Reviewing Digital Design Material: 1 Hour
Design/Preparation Work: 2 Hours
VHDL Coding & Debugging: 3 Hours

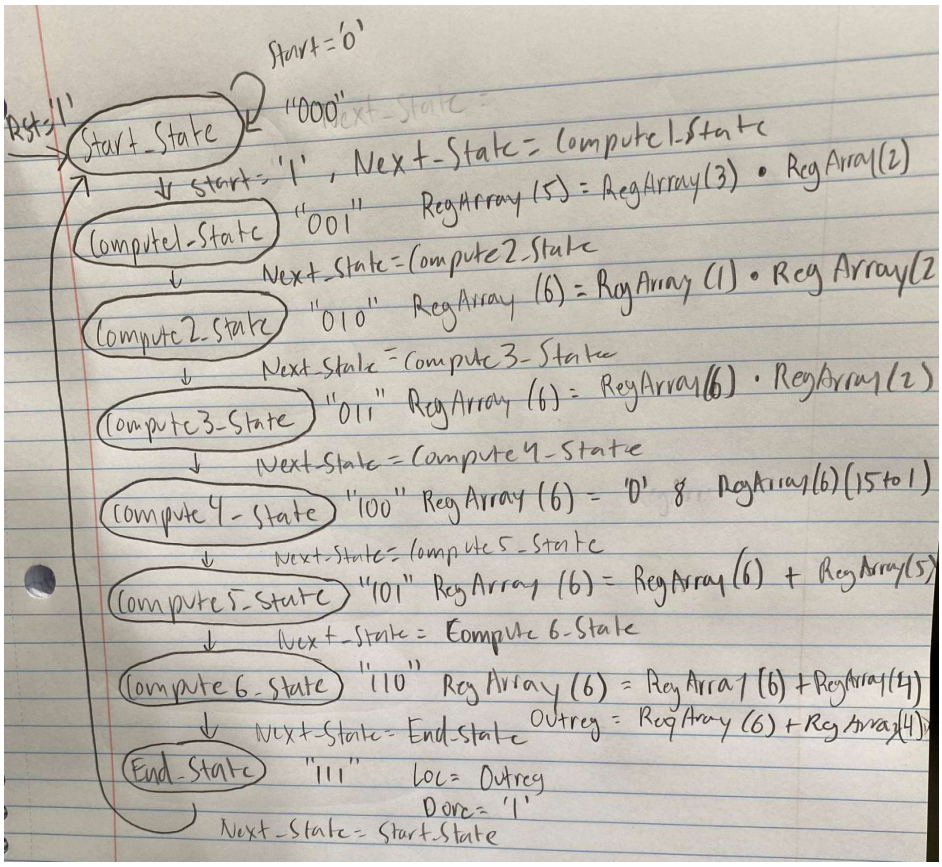
STRUCTURAL OVERVIEW

Replace this text w/ the % you feel you completed the lab. Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

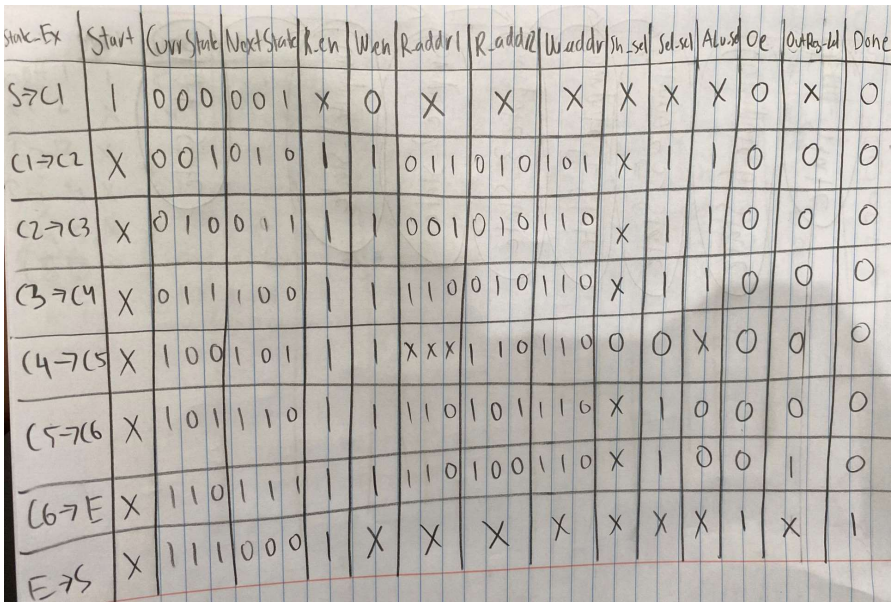
I think I did 100% of the lab, I filled in the Comblogic and StateRegister for the controller, then created signals and mapped them to the components so the signal went to the right places. I rewatched the Integrator Example and read through chapter 4 and 5 of the VHDL Desgin Book. Then created the fsm and chart and then implemented into code.

LAB 3 FSMD & CONTROL WORD TABLE

Show your final FSMD here (even if nothing's changed). Explain why anything has changed or hasn't changed.



Show your control word table for your design here.



State_Ex	Start	Curr State	Next State	R_en	W_en	Raddr1	Raddr2	Waddr	Sh_sel	Sel_sel	ALU_sel	Oe	OutReg_ld	Done
S→C1	1	000	001	X	0	X	X	X	X	X	X	0	X	0
C1→C2	X	001	010	1	1	011	010	101	X	1	1	0	0	0
C2→C3	X	010	011	1	1	001	010	110	X	1	1	0	0	0
C3→C4	X	011	100	1	1	110	010	110	X	1	1	0	0	0
C4→C5	X	100	101	1	1	XXX	110	110	0	0	X	0	0	0
C5→C6	X	101	110	1	1	110	101	116	X	1	0	0	0	0
C6→E	X	110	111	1	1	110	100	110	X	1	0	0	1	0
E→S	X	111	000	1	X	X	X	X	X	X	X	1	X	1

LAB 3 MINIMUM CLOCK CYCLE

Minimum clock cyle: 37

Explain how you derived your minimum clock cycle (as discussed in class) here.

I derived the minimum clock cycle from watching the video and laso reading the minimum clock delay in teh book. It is the longest path from a clock to a clock, the register fiel does have one but when we are reading it is not neccesary. So we start with 4 ns for the state register, then 11 ns for the comblogic, then 6 ns for the register file, then 12 ns for the ALU, then 3 ns for the selector, and finally 1 ns for setup time.

4 + 11 + 6 + 12 + 3 + 1 = 37 ns

LAB 3 STRUCTURAL SIMULATION GRAPH

Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

LAB 3 STRUCTURAL AND BEHAVIORAL SIMULATION GRAPH COMPARISONS

Compare your behavioral & structural graphs here. If there are any differences (delays, outputs, etc.), be sure to explain them here.

The diffrences between the graphs are that in the structural the output comes out much later because they are more states that compute the final location and also the clock cycle is much greater due to the delays of the components.