LAB 1 BEHAVIORAL REPORT

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing "yes" at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? **yes**

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: ____

Student Name: **Andy Tran**
Student ID: 57422363
Date Completed: 4/8/21
Time Spent: Reviewing Digital Design Material: 2 hours
Design/Preparation Work: 1 hour
VHDL Coding & Debugging: 30 minutes

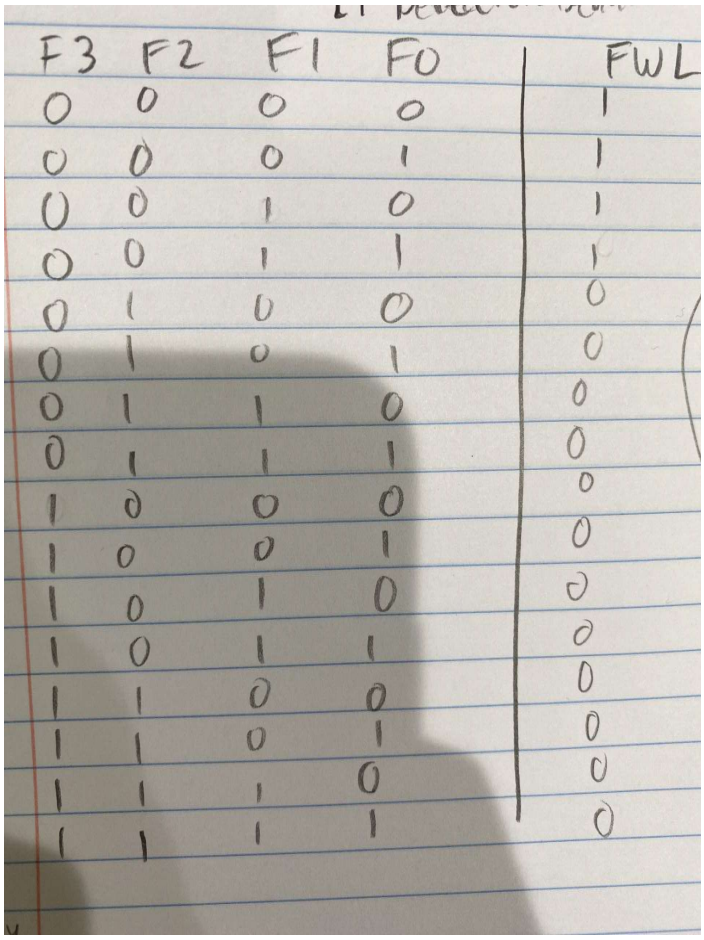
BEHAVIORAL OVERVIEW

What % do you feel you completed on the lab? Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

I feel like I have completed 100% of this lab. I watched the first lectures to see how to get started as this is our first lab. Then I read the prompt, then created a truth table, k map, boolean expression, and delay. Then I reread the drivelock exmaple to see how to build the process for the boolean expression to be put in. I did not really have difficulties.

LAB 1 TRUTH TABLE

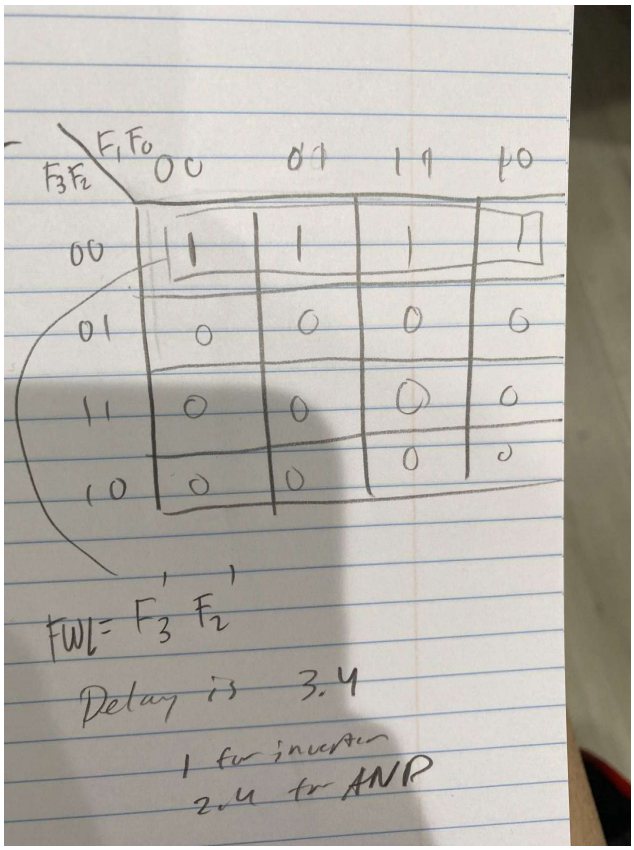
Provide your truth table for Lab 1 here. You can create a table in Word, Excel, or attach a picture of your truth table as long as it is legible and in the correct orientation.



F3	F2	F1	F0	FWL
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

LAB 1 MINIMIZED EQUATION

Show the work you did to go from the truth table to your minimized equation here. Don't show your NAND/NOR/etc. conversions here, just the minimized Boolean equation that satisfies the requirements of the lab.



FWL = (F3)' (F2)'

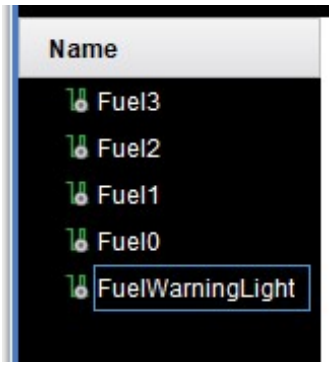
LAB 1 ESTIMATED DELAY

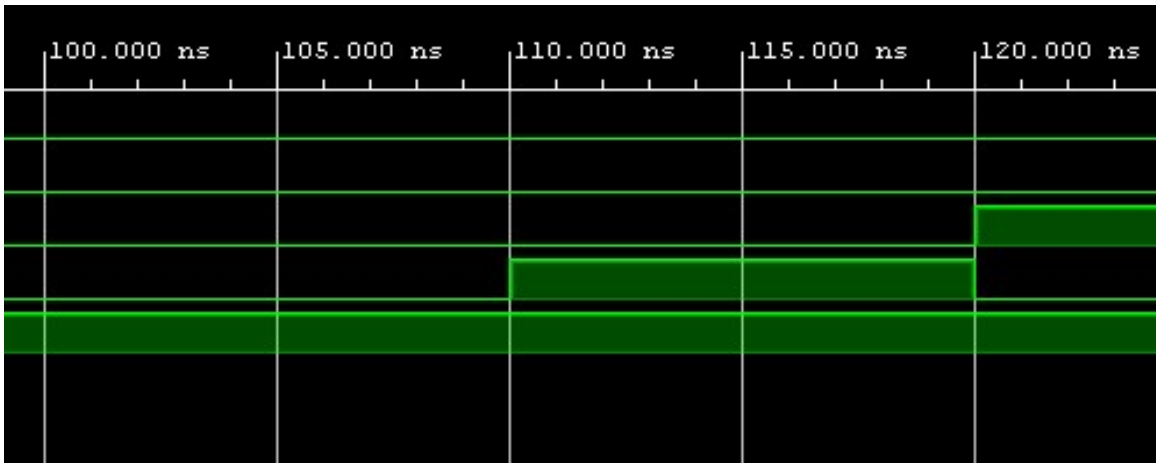
List your estimated delay here (you are not required to add the delay to the actual vhdl code for behavioral): 3.4 ns

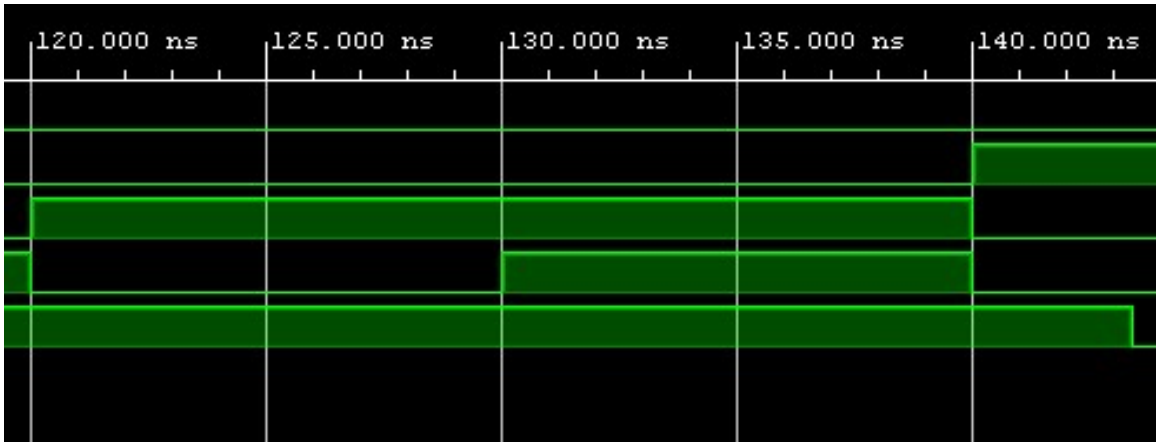
LAB 1 BEHAVIORAL SIMULATION GRAPH

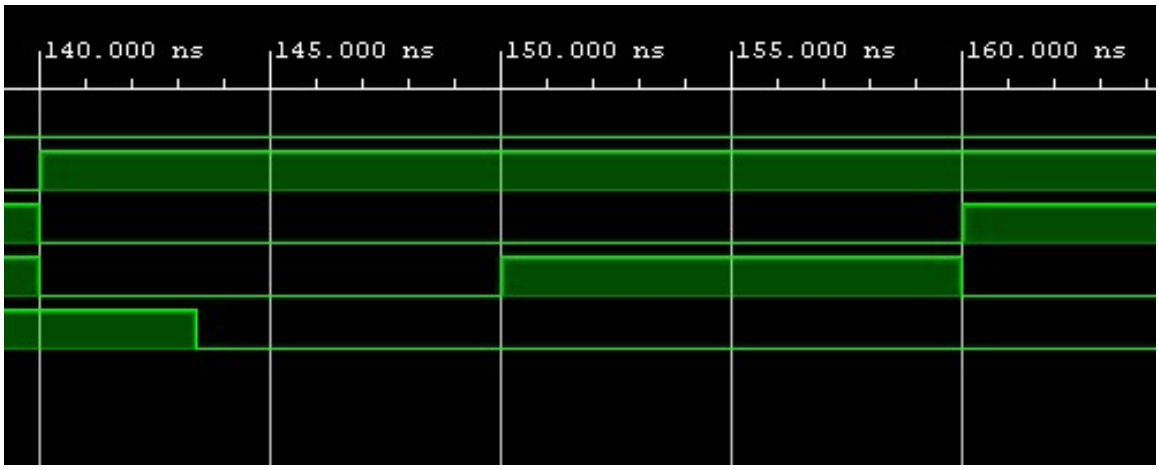
Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

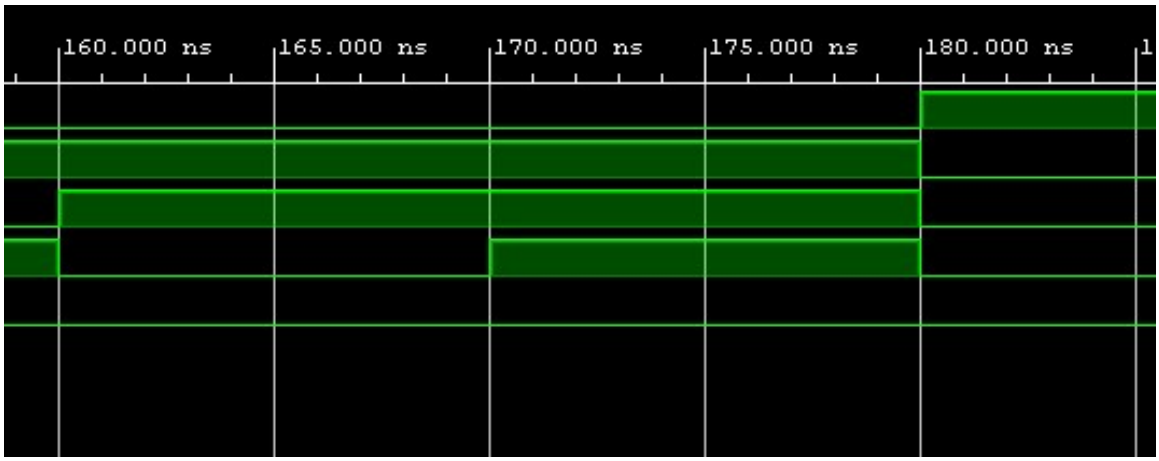
Apologies for not being able to get the final graph into less screenshots, the black backgrounds makes the lines blend with less pixel. Every 10ns is the next step.

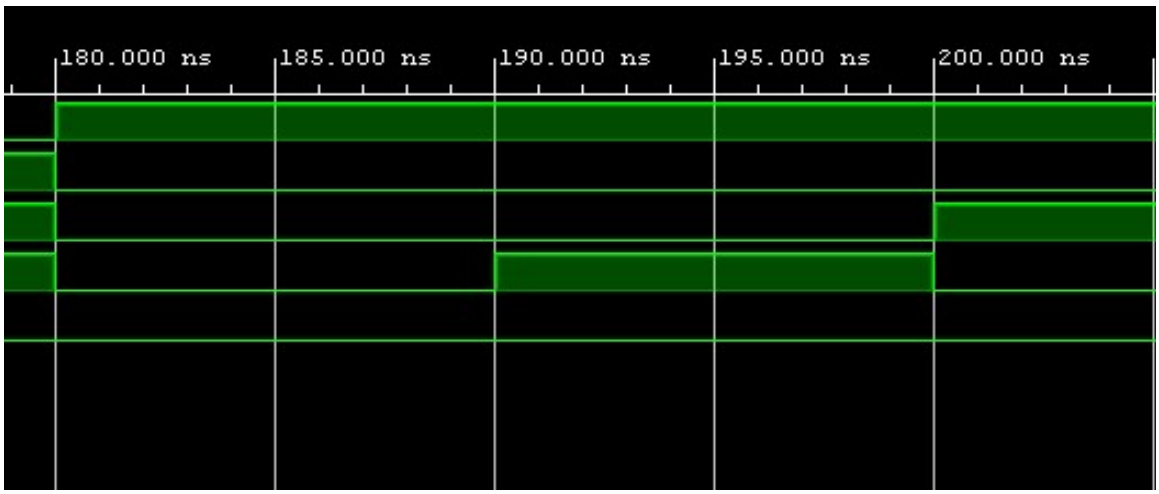

Name
Fuel3
Fuel2
Fuel1
Fuel0
FuelWarningLight

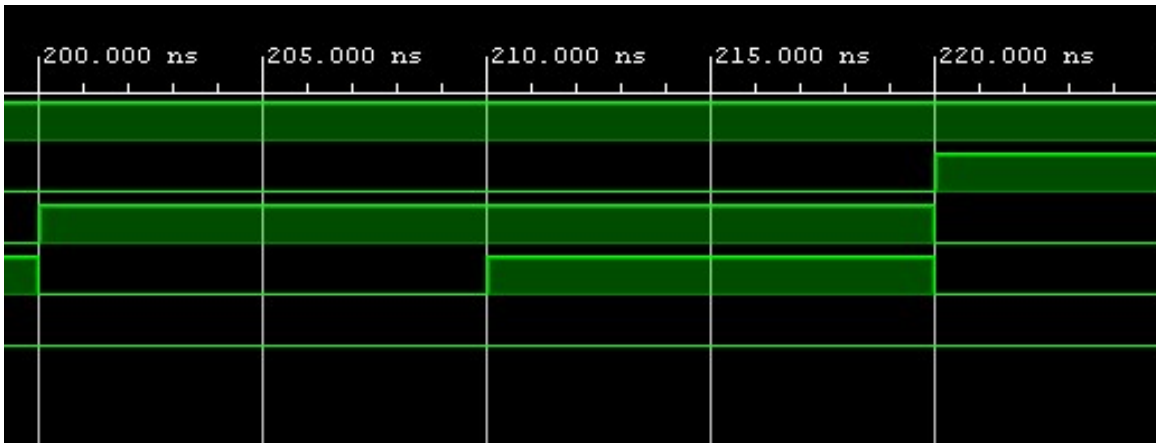

100.000 ns
105.000 ns
110.000 ns
115.000 ns
120.000 ns


120.000 ns
125.000 ns
130.000 ns
135.000 ns
140.000 ns

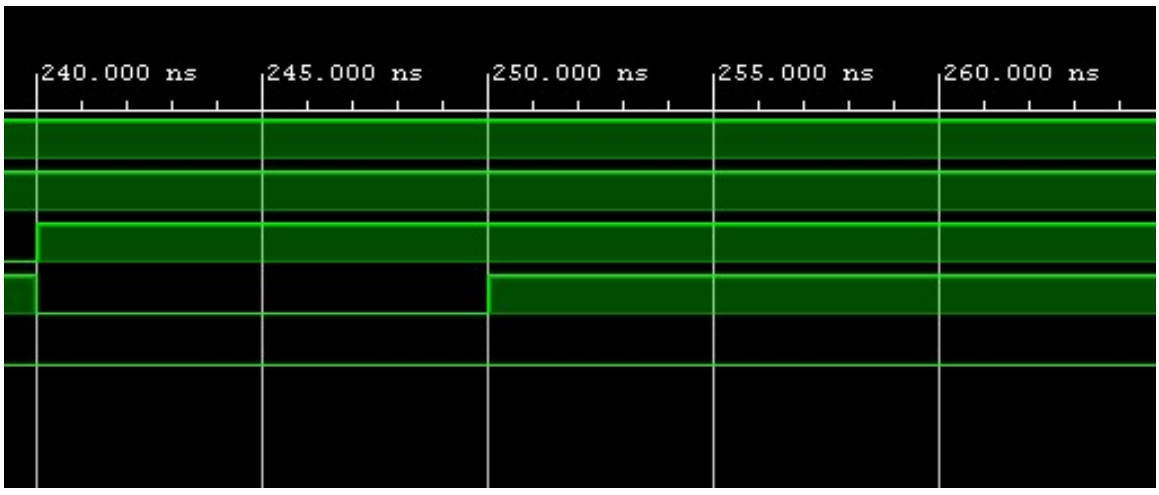

140.000 ns
145.000 ns
150.000 ns
155.000 ns
160.000 ns


160.000 ns
165.000 ns
170.000 ns
175.000 ns
180.000 ns


180.000 ns
185.000 ns
190.000 ns
195.000 ns
200.000 ns


200.000 ns
205.000 ns
210.000 ns
215.000 ns
220.000 ns


220.000 ns
225.000 ns
230.000 ns
235.000 ns
240.000 ns


240.000 ns
245.000 ns
250.000 ns
255.000 ns
260.000 ns