LAB 4 STRUCTURAL REPORT

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing "yes" at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? yes

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: ____

Student Name: Andy Tran
Student ID: 57422363
Date Completed: 6/1/2021
Time Spent: Reviewing Digital Design Material: 30 minutes
Design/Preparation Work: 1 hour
VHDL Coding & Debugging: 1 hour

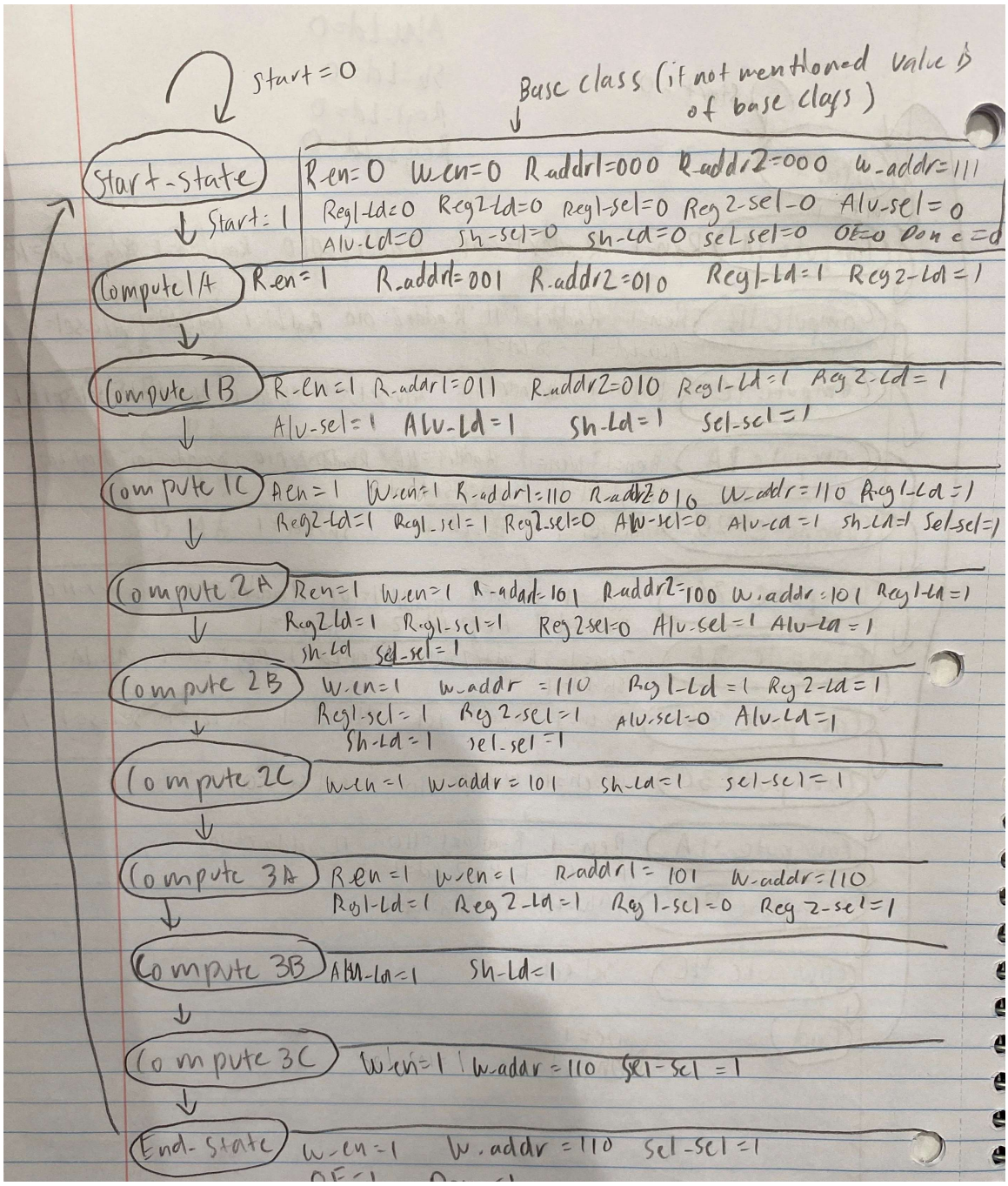
STRUCTURAL OVERVIEW

Replace this text w/ the % you feel you completed the lab. Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

I think I have completed this lab 100%. I started off by watchignt he overview video and anazling the new paths. Then I fixed my data control table to take advantage of the new path then implemented it with the existing code for lab 4s part 1 with slight changes for the selectors.

LAB 4 – PART 2 - FSMD & CONTROL WORD TABLE

Show your final FSMD here.



Show your control word table for your design here.

Start	Cur_State	Next_State	R_en	W_en	R_addr1	R_addr2	W_addr	Reg1_Ld	Reg2_Ld	Reg1_sel	Reg2_sel	Alu_Sel	Alu_Ld	Sh_sel	Sh_Ld	Sel_sel	Oe	Done
0	Start	Start	0	0	XXX	XXX	XXX	0	0	0	0	X	0	X	0	X	0	0
1	Start	Compute1A	0	0	XXX	XXX	XXX	0	0	0	0	X	0	X	0	X	0	0
X	Compute1A	Compute1B	1	0	001	010	XXX	1	1	0	0	X	0	X	0	X	0	0
X	Compute1B	Compute1C	1	0	011	010	XXX	1	1	0	0	1	1	X	1	X	0	0
X	Compute1C	Compute2A	1	1	110	010	110	1	1	1	0	1	1	X	1	1	0	0
X	Compute2A	Compute2B	1	1	101	100	101	1	1	1	0	1	1	X	1	1	0	0
X	Compute2B	Compute2C	0	1	XXX	XXX	110	1	1	1	1	0	1	X	1	1	0	0
X	Compute2C	Compute3A	0	1	XXX	XXX	101	0	0	0	0	X	0	X	1	1	0	0
X	Compute3A	Compute3B	1	1	101	XXX	110	1	1	0	1	X	0	X	0	0	0	0
X	Compute3B	Compute3C	0	0	XXX	XXX	XXX	0	0	0	0	0	1	X	1	X	0	0
X	Compute3C	End	0	1	XXX	XXX	110	0	0	0	0	X	0	X	0	1	0	0
X	End	Start	0	1	XXX	XXX	110	0	0	0	0	X	0	X	0	1	1	1

LAB 4 – PART 2 - MINIMUM CLOCK CYCLE

Minimum clock cycle: 25

Explain how you derived your minimum clock cycle (as discussed in class) here.

So the minimum clock cycle would be the longest path from a clock to clock which is from the

State Register to either of the Reg_Data Registers. The State Register is 4 ns, then the

CombLogic is 11 ns, the Register File is 6 ns, the Selector is 3 ns, and then 1 ns for setup time.

4 + 6 + 11 + 3 + 1 = 22

LAB 4 STRUCTURAL SIMULATION GRAPH

Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.

LAB 4 STRUCTURAL PART 1 AND PART 2 SIMULATION GRAPH COMPARISONS

Compare your structural graphs between the Lab 4s Part 2 and Lab 4s Part 1 implementations here. If there are any differences (delays, outputs, etc.), be sure to explain them here.

The structural graph got Lab 4s Part 2 had a slightly longer clock cycle but there were less states, so in the end it took less amount of time to calculate the results. The delays were almost the same but witht he added selectors the clock cycle increased by 3 ns but there were 3 less states, so before in total we needed 286 ns, but this time we needed 250 ns.