LAB 4 STRUCTURAL REPORT

Academic Integrity (more info @ https://aisc.uci.edu/): You are encouraged to discuss the labs at a high level, but the code/equations/simulations you come up with should be your own. By typing "yes" at the end of this question and filling in your name, you certify that the work you are turning in is your own work. Is the work you are turning in your own? yes

If you worked on any portion of your report or vhdl code with other students (discussion at high level & debugging; if more, please describe), please list their names here: ____

Student Name: Andy Tran
Student ID: 57422363
Date Completed: 5/26/2021
Time Spent: Reviewing Digital Design Material: 2 hours
Design/Preparation Work: 2 hours
VHDL Coding & Debugging: 3 hours

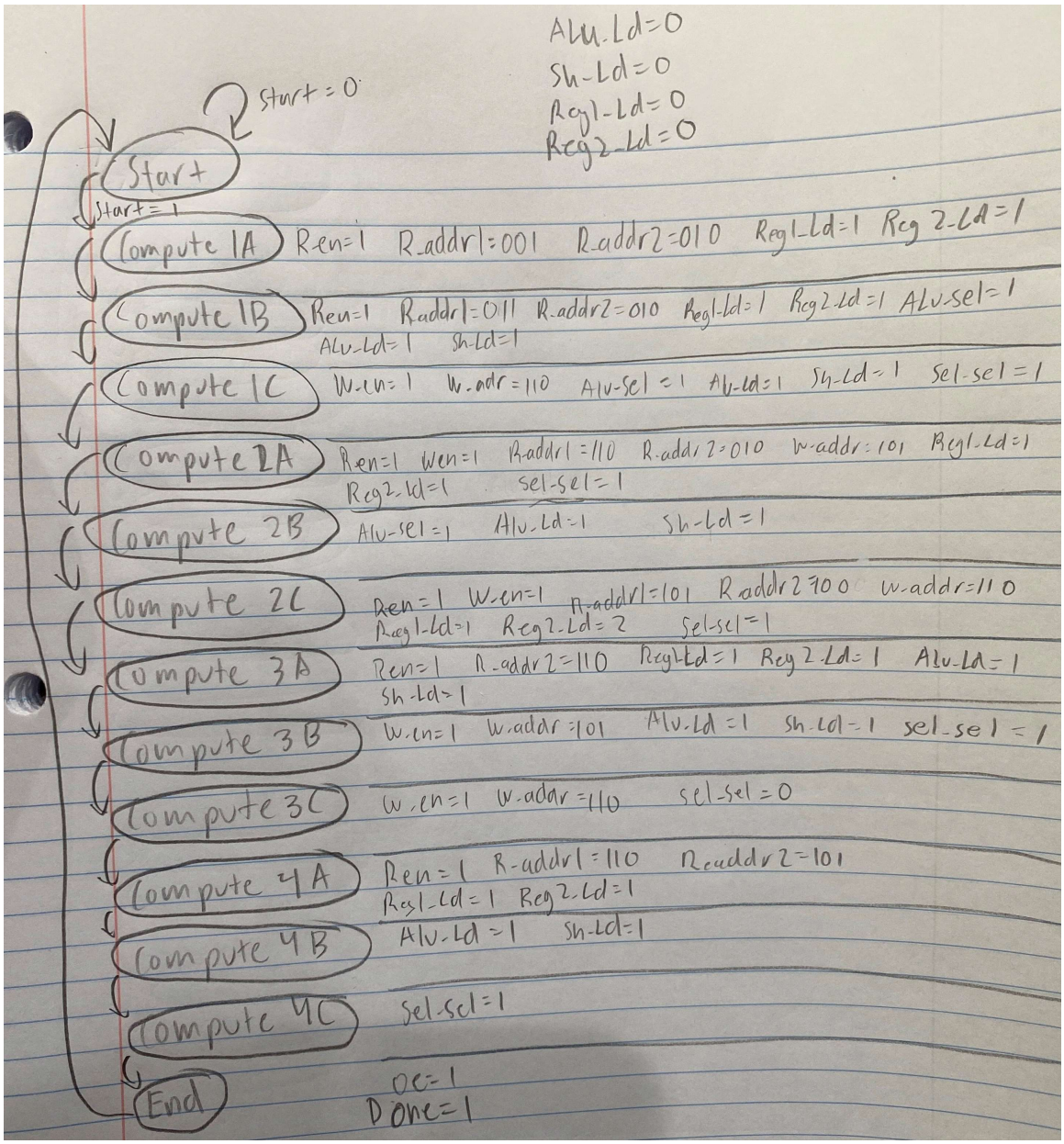
STRUCTURAL OVERVIEW

Replace this text w/ the % you feel you completed the lab. Be sure to list your general procedure of how you completed this lab & material (if any) you reviewed to help you complete this lab. Regardless of % stated, provide any details of difficulties (if any) you encountered during this lab. A few sentences are sufficient.

I think I did 100% of the lab. I review the 31 RTL components to make sure I knew which is did. I then used my basic comblogic from 3S and built upon becasue the new registers change the clock cycle and the path for each process. So each original state became 3 states to handle the new registers. Then I added more ports to the controller and remapped the port maps to have the registers connected and have new signals to handle the new wiring. Then I took those states and combined some to get from 6 original states to 18 smaller states into 12 smaller states using the pipeline design and doing certian operation after on another. The only operations, I had to wait for a cycle to complete were those that invovled using one value over and over again.

LAB 4 – PART 1 - FSMD & CONTROL WORD TABLE

Show your final FSMD here.



Show your control word table for your design here.

Start	Cur_State	Next_State	R_en	W_en	R_addr1	R_addr2	W_addr	Reg1_Ld	Reg2_Ld	Alu_Sel	Alu_Ld	Sh_sel	Sh_Ld	Sel_sel	Oe	Done
0	Start	Start	0	0	XXX	XXX	XXX	0	0	X	0	X	0	X	0	0
1	Start	Compute1A	0	0	XXX	XXX	XXX	0	0	X	0	X	0	X	0	0
X	Compute1A	Compute1B	1	0	001	010	XXX	1	1	X	0	X	0	X	0	0
X	Compute1B	Compute1C	1	0	011	010	XXX	1	1	1	1	X	1	X	0	0
X	Compute1C	Compute2A	0	1	XXX	XXX	110	0	0	1	1	X	1	1	0	0
X	Compute2A	Compute2B	1	1	110	010	101	1	1	X	0	X	0	1	0	0
X	Compute2B	Compute2C	0	0	XXX	XXX	XXX	0	0	1	1	X	1	X	0	0
X	Compute2C	Compute3A	1	1	101	100	110	1	1	X	0	X	0	1	0	0
X	Compute3A	Compute3B	1	0	XXX	110	XXX	1	1	0	1	X	1	X	0	0
X	Compute3B	Compute3C	0	1	XXX	XXX	101	0	0	X	1	0	1	1	0	0
X	Compute3C	Compute4A	0	1	XXX	XXX	110	0	0	X	0	X	0	0	0	0
X	Compute4A	Compute4B	1	0	110	101	XXX	1	1	X	0	X	0	X	0	0
X	Compute4B	Compute4C	0	0	XXX	XXX	XXX	0	0	0	1	X	1	X	0	0
X	Compute4C	End	0	1	XXX	XXX	110	0	0	X	0	X	0	1	0	0
X	End	Start	0	1	XXX	XXX	110	0	0	X	0	X	0	1	1	1

LAB 4 – PART 1 - MINIMUM CLOCK CYCLE

Minimum clock cycle: 22

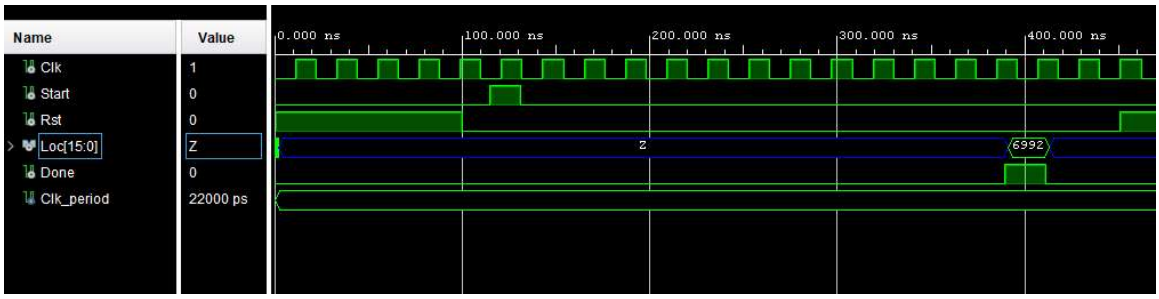
Explain how you derived your minimum clock cycle (as discussed in class) here.

So the minimum clock cycle would be the longest path from a clock to clock which is from the State Register to either of the Reg_Data Registers. The State Register is 4 ns, then the CombLogic is 11 ns, the Register File is 6 ns, and then 1 ns for setup time.

4 + 6 + 11 + 1 = 22

LAB 4 STRUCTURAL SIMULATION GRAPH

Show a screenshot of your final graph here. You should crop it to the appropriate size so that it is legible.



LAB 4 STRUCTURAL AND LAB 3 STRUCTURAL SIMULATION GRAPH COMPARISONS

Compare your structural graphs between the Lab 4s and Lab 3s implementations here. If there are any differences (delays, outputs, etc.), be sure to explain them here.

There are diffrences becasue with the new registers, it created more states and each register had its own delay, the clock cycle might be shorter but there are almost two times as many states this time compared to 3S, so the increase is not too large.