KIỂM TRA CUỐI KỲ

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Môn: Tổ chức máy tính

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Phần 1

Addressing Modes

✓ The instruction, Add #45,R1 does _____ * 1/1

- Adds the value of 45 to the address of R1 and stores 45 in that address
- (•) Adds 45 to the value of R1 and stores it in R1
- Finds the memory location 45 and adds that content to that of R1
- None of the mentioned

✗ In the case of, Zero-address instruction method the operands are stored in _____ 0/1

- a) Registers
- b) Accumulators
- (•) c) Push down stack
- d) Cache

Correct answer

- (•) a) Registers

✓ Add #45, when this instruction is executed the following happen/s _____ /1

- a) The processor raises an error and requests for one more operand
- b) The value stored in memory location 45 is retrieved and one more operand is requested
- c) The value 45 gets added to the value on the stack and is pushed onto the stac
- d) None of the mentioned

✓ The addressing mode which makes use of in-direction pointers is _____ * /1

- a) Indirect addressing mode
- b) Index addressing mode
- c) Relative addressing mode
- d) Offset addressing mode

Feedback

Explanation: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.

✓ The addressing mode/s, which uses the PC instead of a general purpose register is _____ 1/1

- a) Indexed with offset
- b) Relative
- c) Direct
- d) Both Indexed with offset and direct

Feedback

Explanation: In this, the contents of the PC are directly incremented.

✓ The addressing mode, where you directly specify the operand value is _____ 1/1

- a) Immediate
- b) Direct
- c) Definite
- d) Relative

✓ The effective address of the following instruction is mul $v0, $t1, $t2 * 1/1

- v0=t1+t2
- v0=t1-t2
- v0=t1*t2
- v0=t1/t2

✓ _____ addressing mode is most suitable to change the normal sequence of execution of instructions. 1/1

- a) Relative
- b) Indirect
- c) Index with Offset
- d) Immediate

Feedback

Explanation: The relative addressing mode is used for this since it directly updates the PC

✓ Result of the instruction add $v0, $t1, $t2 with $t1 and $t2 have value 2 an… /1
3.

- ○ 6
- ○ -1
- ○ 2/3
- ◉ 5

✓ The type of memory assignment used in Intel processors is _____ /1

- ◉ a) Little Endian
- ○ b) Big Endian
- ○ c) Medium Endian
- ○ d) None of the mentioned

Feedback

Explanation: The method of address allocation to data to be stored is called as memory assignment.

✓ When using the Big Endian assignment to store a number, the sign bit of the number is stored in _____ /1

- (●) a) The higher order byte of the word
- ( ) b) The lower order byte of the word
- ( ) c) Can't say
- ( ) d) None of the mentioned

✓ 9. During the transfer of data between the processor and memory we use _____ /1

- ( ) a) Cache
- ( ) b) TLB
- ( ) c) Buffers
- (●) d) Registers

✓ Physical memory is divided into sets of finite size called as _____ * /1

- (●) a) Frames
- ( ) b) Pages
- ( ) c) Blocks
- ( ) d) Vectors

✓ RTN stands for _____ * 1/1

- (●) a) Register Transfer Notation
- ( ) b) Register Transmission Notation
- ( ) c) Regular Transmission Notation
- ( ) d) Regular Transfer Notation

✓ The instruction, Add R1,R2,R3 in RTN is _____ *

- ( ) a) R3=R1+R2+R3
- ( ) b) R3<-[R1]+[R2]+[R3]
- ( ) c) R3=[R1]+[R2]
- (●) d) R3<-[R1]+[R2]

Feedback

Explanation: In RTN the first operand is the destination and the second operand is the source.

✓ In a system, which has 32 registers the register id is _____ long. * 1

- a) 16 bit
- b) 8 bits
- c) 5 bits
- d) 6 bits

Feedback

Explanation: The ID is the name tag given to each of the registers and used to identify them.

✓ The two phases of executing an instruction are _____ * 1

- a) Instruction decoding and storage
- b) Instruction fetch and instruction execution
- c) Instruction execution and storage
- d) Instruction fetch and Instruction processing

Feedback

Explanation: First, the instructions are fetched and decoded and then they're executed and stored.

✓ The Instruction fetch phase ends with _____ * 1/1

- a) Placing the data from the address in MAR into MDR
- b) Placing the address of the data into MAR
- c) Completing the execution of the data and placing its storage address into MA
- d) Decoding the data in MDR and placing it in IR

Feedback

Explanation: The fetch ends with the instruction getting decoded and being placed in the IR and the PC getting incremented.

✓ While using the iterative construct (Branching) in execution _____ instruction is used to check the condition. 1/1

- a) TestAndSet
- b) Branch
- c) TestCondn
- d) None of the mentioned

Feedback

Explanation: Branch instruction is used to check the test condition and to perform the memory jump with the help of offset.

✓ When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded which is called as _____ /1

- (●) a) Branch target
- ( ) b) Loop target
- ( ) c) Forward target
- ( ) d) Jump instruction

✓ _____ converts the programs written in assembly language into machine instructions. /1

- ( ) a) Machine compiler
- ( ) b) Interpreter
- (●) c) Assembler
- ( ) d) Converter

Feedback

Explanation: An assembler is a software used to convert the programs into machine instructions.

✓ The program is divided into operable parts called as _____ /1

- a) Frames
- (•) b) Segments
- c) Pages
- d) Sheets

Feedback

Explanation: The program is divided into parts called as segments for ease of execution.

✓ The techniques which move the program blocks to or from the physical memory is called as _____ /1

- a) Paging
- (•) b) Virtual memory organisation
- c) Overlays
- d) Framing

Feedback

Explanation: By using this technique the program execution is accomplished with a usage of less space.

✓ The binary address issued to data or instructions are called as _____ * 1/1

- a) Physical address
- b) Location
- c) Relocatable address
- d) Logical address

Feedback

Explanation: The logical address is the random address generated by the processor.

✓ _____ is used to implement virtual memory organisation. * 1/1

- a) Page table
- b) Frame table
- c) MMU
- d) None of the mentioned

Feedback

Explanation: The MMU stands for Memory Management Unit.

✓ _____ translates the logical address into a physical address. * /1

- (●) a) MMU
- ( ) b) Translator
- ( ) c) Compiler
- ( ) d) Linker

Feedback

Explanation: The MMU translates the logical address into a physical address by adding an offset.

✓ The main aim of virtual memory organisation is _____ * /1

- ( ) a) To provide effective memory access
- ( ) b) To provide better memory transfer
- ( ) c) To improve the execution of the program
- (●) d) All of the mentioned

✓ The DMA doesn’t make use of the MMU for bulk data transfers. * 1/1

- a) True
- (•) b) False

Feedback

Explanation: The DMA stands for Direct Memory Access, in which a block of data gets directly transferred from the memory.

✓ The virtual memory basically stores the next segment of data to be executed on the _____ 1/1

- (•) a) Secondary storage
- b) Disks
- c) RAM
- d) ROM

✓ The associatively mapped virtual memory makes use of _____ * 1

- (●) a) TLB
- ( ) b) Page table
- ( ) c) Frame table
- ( ) d) None of the mentioned

Feedback

Explanation: TLB stands for Translation Look-aside Buffer.

✓ The reason for the implementation of the cache memory is _____ * 1

- ( ) a) To increase the internal memory of the system
- (●) b) The difference in speeds of operation of the processor and memory
- ( ) c) To reduce the memory access and cycle time
- ( ) d) All of the mentioned

Feedback

Explanation: This difference in the speeds of operation of the system caused it to be inefficient.

✓ The effectiveness of the cache memory is based on the property of _____ 1

- (●) a) Locality of reference
- ( ) b) Memory localisation
- ( ) c) Memory size
- ( ) d) None of the mentioned

Feedback

Explanation: This means that the cache depends on the location in the memory that is referenced often.

✓ The temporal aspect of the locality of reference means _____ * 1

- ( ) a) That the recently executed instruction won't be executed soon
- ( ) b) That the recently executed instruction is temporarily not referenced
- (●) c) That the recently executed instruction will be executed soon again
- ( ) d) None of the mentioned

✓ The spatial aspect of the locality of reference means _____ * 1/1

- a) That the recently executed instruction is executed again next
- b) That the recently executed won't be executed again
- c) That the instruction executed will be executed at a later time
- d) That the instruction in close proximity of the instruction executed will be executed in future

Feedback

Explanation: The spatial aspect of locality of reference tells that the nearby instruction is more likely to be executed in future.

✓ The correspondence between the main memory blocks and those in the cache is given by _____ 1/1

- a) Hash function
- b) Mapping function
- c) Locale function
- d) Assign function

Feedback

Explanation: The mapping function is used to map the contents of the memory to the cache.

✓ The algorithm to remove and place new contents into the cache is called _____ 1/1

- (●) a) Replacement algorithm
- ( ) b) Renewal algorithm
- ( ) c) Updation
- ( ) d) None of the mentioned

Feedback

Explanation: As the cache gets full, older contents of the cache are swapped out with newer contents. This decision is taken by the algorithm.

✓ The write-through procedure is used _____ *

- ( ) a) To write onto the memory directly
- ( ) b) To write and read from memory simultaneously
- (●) c) To write directly on the memory and the cache simultaneously
- ( ) d) None of the mentioned

Feedback

Explanation: When write operation is issued then the corresponding operation is performed.

✓ The bit used to signify that the cache location is updated is _____ * /1

- (●) a) Dirty bit
- ( ) b) Update bit
- ( ) c) Reference bit
- ( ) d) Flag bit

Feedback

Explanation: When the cache location is updated in order to signal to the processor this b is used.

✓ The copy-back protocol is used _____ * /1

- ( ) a) To copy the contents of the memory onto the cache
- (●) b) To update the contents of the memory from the cache
- ( ) c) To remove the contents of the cache and push it on to the memory
- ( ) d) None of the mentioned

Feedback

Explanation: This is another way of performing the write operation, wherein the cache is updated first and then the memory.

✓ The approach where the memory contents are transferred directly to the processor from the memory is called _____ 1

- a) Read-later
- b) Read-through
- c) Early-start
- d) None of the mentioned

✓ The main memory is structured into modules each with its own address register called _____ *

- a) ABR
- b) TLB
- c) PC
- d) IR

Feedback

Explanation: ABR stands for Address Buffer Register.

✓ When consecutive memory locations are accessed only one module is accessed at a time. 1/1

- (●) a) True
- ( ) b) False

Feedback

Explanation: In a modular approach to memory structuring only one module can be accessed at a time.

✓ In memory interleaving, the lower order bits of the address is used to _____ 1/1

- ( ) a) Get the data
- (●) b) Get the address of the module
- ( ) c) Get the address of the data within the module
- ( ) d) None of the mentioned

Feedback

Explanation: To implement parallelism in data access we use interleaving.

✓ The number successful accesses to memory stated as a fraction is called as _____ 1

- (●) a) Hit rate
- ( ) b) Miss rate
- ( ) c) Success rate
- ( ) d) Access rate

Feedback

Explanation: The hit rate is an important factor in performance measurement.

✓ The number failed attempts to access memory, stated in the form of a fraction is called as _____ 1

- ( ) a) Hit rate
- (●) b) Miss rate
- ( ) c) Failure rate
- ( ) d) Delay rate

Feedback

Explanation: The miss rate is a key factor in deciding the type of replacement algorithm.

✓ In associative mapping during LRU, the counter of the new block is set to ‘0’ and all the others are incremented by one, when _____ occurs. 1/1

- a) Delay
- b) Miss
- c) Hit
- d) Delayed hit

Feedback

Explanation: Miss usually occurs when the memory block required is not present in the cache.

✓ In LRU, the referenced blocks counter is set to’0' and that of the previous blocks are incremented by one and others remain same, in the case of _____ 1/1

- a) Hit
- b) Miss
- c) Delay
- d) None of the mentioned

Feedback

Explanation: If the referenced block is present in the memory it is called as hit.

✓ If hit rates are well below 0.9, then they’re called as speedy computers. * 1/1

- a) True
- (●) b) False

Feedback

Explanation: It has to be above 0.9 for speedy computers.

✓ The miss penalty can be reduced by improving the mechanisms for data transfer between the different levels of hierarchy. 1/1

- (●) a) True
- b) False

Feedback

Explanation: The extra time needed to bring the data into memory in case of a miss is called as miss penalty.

✓ The key factor/s in commercial success of a computer is/are _____ * 1/1

- a) Performance
- b) Cost
- c) Speed
- d) Both Performance and Cost

Feedback

Explanation: The performance and cost of the computer system is a key decider in the commercial success of the system.

✓ The extra time needed to bring the data into memory in case of a miss is called as _____ 1/1

- a) Delay
- b) Propagation time
- c) Miss penalty
- d) None of the mentioned

✓ The main objective of the computer system is _____ * 1

- a) To provide optimal power operation
- b) To provide the best performance at low cost
- c) To provide speedy operation at low power consumption
- d) All of the mentioned

Feedback

Explanation: An optimal system provides the best performance at low costs.

✓ A common measure of performance is _____ * 1

- a) Price/performance ratio
- b) Performance/price ratio
- c) Operation/price ratio
- d) None of the mentioned

Feedback

Explanation: If this measure is less than one then the system is optimal.

✓ The performance depends on _____ * 1/1

- a) The speed of execution only
- b) The speed of fetch and execution
- c) The speed of fetch only
- d) The hardware of the system only

Feedback

Explanation: The performance of a system is decided by how quick an instruction is brought into the system and executed.

✗ The main purpose of having memory hierarchy is to _____ * 0/1

- a) Reduce access time
- b) Provide large capacity
- c) Reduce propagation time
- d) Reduce access time & Provide large capacity

Correct answer

- d) Reduce access time & Provide large capacity

✗ The memory transfers between two variable speed devices are always done at the speed of the faster device. 0/1

- ○ a) True
- ◉ b) False

Correct answer

- ◉ a) True

✓ An effective to introduce parallelism in memory access is by _____ *

- ◉ a) Memory interleaving
- ○ b) TLB
- ○ c) Pages
- ○ d) Frames

Feedback

Explanation: Interleaving divides the memory into modules.

✓ The performance of the system is greatly influenced by increasing the level 1 cache. /1

- (●) a) True
- ( ) b) False

Feedback

Explanation: This is so because the L1 cache is onboard the processor.

✓ Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster. /1

- (●) a) A
- ( ) b) B
- ( ) c) Both take the same time
- ( ) d) Insufficient information